High Voltage, Latch-Up Proof, 8-/16-Channel Multiplexers

Data Sheet

ADG5206/ADG5207

FEATURES

- Latch-up proof
- 3.5 pF off source capacitance
- Off drain capacitance
  - ADG5206: 64 pF
  - ADG5207: 33 pF
- 0.35 pC typical charge injection
- ±0.02 nA on channel leakage
- Low on resistance: 155 Ω typical
- ±9 V to ±22 V dual-supply operation
- 9 V to 40 V single-supply operation
- V_{SS} to V_{DD} analog signal range
- Human body model (HBM) ESD rating
  - ADG5206: 8 kV all pins
  - ADG5207: 8 kV I/O port to supplies

APPLICATIONS

- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Battery monitoring
- Communication systems

FUNCTIONAL BLOCK DIAGRAMS

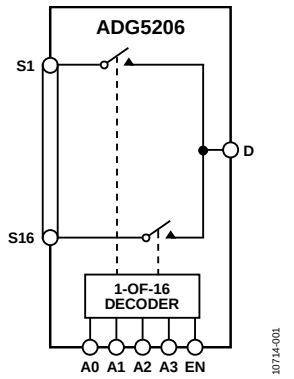


Figure 1.

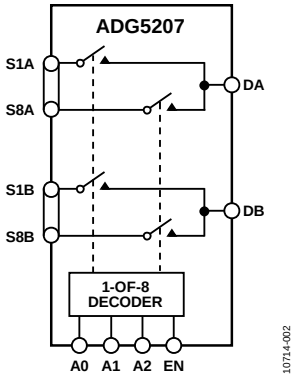


Figure 2.

GENERAL DESCRIPTION

The ADG5206 and ADG5207 are monolithic CMOS analog multiplexers comprising 16 single channels and 8 differential channels, respectively. The ADG5206 switches one of sixteen inputs to a common output, as determined by the 4-bit binary address lines, A0, A1, A2, and A3. The ADG5207 switches one of eight differential inputs to a common differential output, as determined by the 3-bit binary address lines, A0, A1, and A2.

An EN input on both devices enables or disables the device. When EN is low, the device is disabled and all channels switch off. The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed coupled with high signal bandwidth make these devices suitable for video signal switching.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG5206/ADG5207 do not have V_L pins; instead, an on-chip voltage generator generates the logic power supply internally.

PRODUCT HIGHLIGHTS

1. Trench Isolation Guards Against Latch-Up. A dielectric trench separates the P and N channel transistors to prevent latch-up even under severe overvoltage conditions.
2. Optimal switch design for low charge injection, low switch capacitance, and low leakage currents.
3. The ADG5206 achieves 8 kV HBM ESD specification on all external pins, while the ADG5207 achieves 8 kV on the I/O port to supply pins, 2 kV on the I/O port to I/O port pins, and 8 kV on all other pins.
4. Dual-Supply Operation. For applications where the analog signal is bipolar, the ADG5206/ADG5207 can be operated from dual supplies of up to ±22 V.
5. Single-Supply Operation. For applications where the analog signal is unipolar, the ADG5206/ADG5207 can be operated from a single rail power supply of up to 40 V.

Rev. A
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

5/13—Rev. 0 to Rev. A

Added 32-Lead LFCSP ... Universal
Changes to Features Section and Product Highlights Section ... 1
Moved Continuous Current per Channel, Sx, D, or Dx Section, Table 5, and Table 6 ... 10
Changes to Table 7 ... 11
Changes to Figure 3 ... 12
Changes to Figure 5 ... 13
Changes to Figure 30, Figure 32, and Figure 33 ... 22

7/12—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	155				Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 32
	200	225	250	285	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels, ΔR_{ON}	4				Ω typ	V_S = ±10 V, I_S = −1 mA
	12	13	14	15	Ω max	
On Resistance Flatness, $R_{FLAT (ON)}$	48				Ω typ	V_S = ±10 V, I_S = −1 mA
	65	73	80	90	Ω max	
LEAKAGE CURRENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.005				nA typ	V_S = ±10 V, V_D = ∓10 V; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, ΔLeakage, I_S (Off)[1]	0.01			0.015	nA typ	V_S = ±10 V, V_D = ∓10 V
Drain Off Leakage, I_D (Off)						V_S = ±10 V, V_D = ∓10 V; see Figure 33
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (Off), ADG5207 Only	0.015			0.015	nA typ	V_S = ±10 V, V_D = ∓10 V
Channel On Leakage, I_D (On), I_S (On)						V_S = V_D = ±10 V; see Figure 34
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (On), I_S (On)[2]	0.01			0.03	nA typ	V_S = V_D = ±10 V
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002				μA typ	V_{IN} = V_{GND} or V_{DD}
				±0.1	μA max	
Digital Input Capacitance, C_{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS[3]						
Transition Time, $t_{TRANSITION}$	200				ns typ	R_L = 300 Ω, C_L = 35 pF
	260	300	320	360	ns max	V_S = 10 V; see Figure 35
t_{ON} (EN)	180				ns typ	R_L = 300 Ω, C_L = 35 pF
	245	260	270	285	ns max	V_S = 10 V; see Figure 36
t_{OFF} (EN)	140				ns typ	R_L = 300 Ω, C_L = 35 pF
	200	220	240	270	ns max	V_S = 10 V; see Figure 36
Break-Before-Make Time Delay, t_D	85				ns typ	R_L = 300 Ω, C_L = 35 pF
				27	ns min	V_{S1} = V_{S2} = 10 V; see Figure 37

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Charge Injection, Q_{INJ}	0.35				pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 38
	±1.8			±2	pC typ	V_S = ±10 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−90				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 39
Channel-to-Channel Crosstalk	−76				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
−3 dB Bandwidth						R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5206	60				MHz typ	
ADG5207	140				MHz typ	
Insertion Loss	6.4				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	3.5				pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)						
ADG5206	64				pF typ	V_S = 0 V, f = 1 MHz
ADG5207	33				pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)						
ADG5206	68				pF typ	V_S = 0 V, f = 1 MHz
ADG5207	36				pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45				µA typ	Digital inputs = 0 V or V_{DD}
	55			70	µA max	
I_{SS}	0.001				µA typ	Digital inputs = 0 V or V_{DD}
				1	µA max	
V_{DD}/V_{SS}				±9/±22	V min/V max	GND = 0 V

[1] The off channel leakage delta is calculated using the maximum of V_S = +10 V and V_D = −10 V, or V_S = −10 V and V_D = +10 V.
[2] The on channel leakage delta is calculated using the maximum of V_S = V_D = +10 V, or V_S = V_D = −10 V.
[3] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	130				Ω typ	V_S = ±15 V, I_S = −1 mA; see Figure 32
	160	180	200	230	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	4				Ω typ	V_S = ±15 V, I_S = −1 mA
	12	13	14	15	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	35				Ω typ	V_S = ±15 V, I_S = −1 mA
	50	58	65	75	Ω max	

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
LEAKAGE CURRENTS						V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.005				nA typ	V_S = ±15 V, V_D = ∓15 V; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, ΔLeakage, I_S (Off)[1]	0.01			0.015	nA typ	
Drain Off Leakage, I_D (Off)						V_S = ±15 V, V_D = ∓15 V; see Figure 33
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (Off), ADG5207 Only	0.015			0.015	nA typ	
Channel On Leakage, I_D (On), I_S (On)						V_S = V_D = ±15 V; see Figure 34
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (On), I_S (On)[2]	0.01			0.03	nA typ	
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.002				μA typ	V_{IN} = V_{GND} or V_{DD}
				±0.1	μA max	
Digital Input Capacitance, C_{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS[3]						
Transition Time, $t_{TRANSITION}$	185				ns typ	R_L = 300 Ω, C_L = 35 pF
	240	270	290	320	ns max	V_S = 10 V; see Figure 35
t_{ON} (EN)	175				ns typ	R_L = 300 Ω, C_L = 35 pF
	230	245	255	270	ns max	V_S = 10 V; see Figure 36
t_{OFF} (EN)	135				ns typ	R_L = 300 Ω, C_L = 35 pF
	185	205	220	245	ns max	V_S = 10 V; see Figure 36
Break-Before-Make Time Delay, t_D	75				ns typ	R_L = 300 Ω, C_L = 35 pF
				27	ns min	V_{S1} = V_{S2} = 10 V; see Figure 37
Charge Injection, Q_{INJ}	0.45				pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 38
	±4			±4	pC typ	V_S = ±10 V, R_S = 0 Ω, C_L = 1 nF
Off Isolation	−90				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 39
Channel-to-Channel Crosstalk	−76				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
−3 dB Bandwidth						R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5206	65				MHz typ	
ADG5207	145				MHz typ	
Insertion Loss	5.6				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	3.3				pF typ	V_S = 0 V, f = 1 MHz

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
C_D (Off)						
ADG5206	62				pF typ	V_S = 0 V, f = 1 MHz
ADG5207	32				pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)						
ADG5206	67				pF typ	V_S = 0 V, f = 1 MHz
ADG5207	35				pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS						V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50				µA typ	Digital inputs = 0 V or V_{DD}
	70			110	µA max	
I_{SS}	0.001				µA typ	Digital inputs = 0 V or V_{DD}
				1	µA max	
V_{DD}/V_{SS}				±9/±22	V min/V max	GND = 0 V

[1] The off channel leakage delta is calculated using the maximum of V_S = +15 V and V_D = −15 V, or V_S = −15 V and V_D = +15 V.
[2] The on channel leakage delta is calculated using the maximum of V_S = V_D = +15 V, or V_S = V_D = −15 V.
[3] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				0 V to V_{DD}	V	
On Resistance, R_{ON}	350				Ω typ	V_S = 0 V to 10 V, I_S = −1 mA; see Figure 32
	500	560	610	700	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	5				Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	20	21	22	24	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	170				Ω typ	V_S = 0 V to 10 V, I_S = −1 mA
	280	310	335	370	Ω max	
LEAKAGE CURRENTS						V_{DD} = +13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.005				nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, ΔLeakage, I_S (Off)[1]	0.01			0.015	nA typ	
Drain Off Leakage, I_D (Off)						V_S = 1 V/10 V, V_D = 1 V/10 V; see Figure 33
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (Off), ADG5207 Only	0.015			0.015	nA typ	
Channel On Leakage, I_D (On), I_S (On)						V_S = V_D = 1 V/10 V; see Figure 34
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (On), I_S (On)[2]	0.01			0.03	nA typ	

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002				μA typ	$V_{IN} = V_{GND}$ or V_{DD}
				±0.1	μA max	
Digital Input Capacitance, C_{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS[3]						
Transition Time, $t_{TRANSITION}$	290				ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	290	440	480	550	ns max	$V_S = 8$ V; see Figure 35
t_{ON} (EN)	230				ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	290	320	340	370	ns max	$V_S = 8$ V; see Figure 36
t_{OFF} (EN)	230				ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
	315	360	390	450	ns max	$V_S = 8$ V; see Figure 36
Break-Before-Make Time Delay, t_D	170				ns typ	$R_L = 300\ \Omega$, $C_L = 35$ pF
				45	ns min	$V_{S1} = V_{S2} = 8$ V; see Figure 37
Charge Injection, Q_{INJ}	0.25				pC typ	$V_S = 6$ V, $R_S = 0\ \Omega$, $C_L = 1$ nF; see Figure 38
	±0.6			±0.7	pC typ	$V_S = 0$ V to 10 V, $R_S = 0\ \Omega$, $C_L = 1$ nF
Off Isolation	−90				dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 39
Channel-to-Channel Crosstalk	−76				dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 40
−3 dB Bandwidth						$R_L = 50\ \Omega$, $C_L = 5$ pF; see Figure 41
ADG5206	50				MHz typ	
ADG5207	105				MHz typ	
Insertion Loss	8.55				dB typ	$R_L = 50\ \Omega$, $C_L = 5$ pF, f = 1 MHz; see Figure 41
C_S (Off)	3.6				pF typ	$V_S = 6$ V, f = 1 MHz
C_D (Off)						
ADG5206	71				pF typ	$V_S = 6$ V, f = 1 MHz
ADG5207	36				pF typ	$V_S = 6$ V, f = 1 MHz
C_D (On), C_S (On)						
ADG5206	75				pF typ	$V_S = 6$ V, f = 1 MHz
ADG5207	40				pF typ	$V_S = 6$ V, f = 1 MHz
POWER REQUIREMENTS						$V_{DD} = 13.2$ V
I_{DD}	40				μA typ	Digital inputs = 0 V or V_{DD}
	50			65	μA max	
V_{DD}				9/40	V min/V max	GND = 0 V, $V_{SS} = 0$ V

[1] The off channel leakage delta is calculated using the maximum of $V_S = 1$ V and $V_D = 10$ V, or $V_S = 10$ V and $V_D = 1$ V.
[2] The on channel leakage delta is calculated using the maximum of $V_S = V_D = 1$ V, or $V_S = V_D = 10$ V.
[3] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH						
Analog Signal Range				0 V to V_{DD}	V	
On Resistance, R_{ON}	140				Ω typ	V_S = 0 V to 30 V, I_S = −1 mA; see Figure 32
	170	195	215	245	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	4				Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	12	13	14	15	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	40				Ω typ	V_S = 0 V to 30 V, I_S = −1 mA
	55	63	70	80	Ω max	
LEAKAGE CURRENTS						V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.005				nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 33
	±0.1	±0.15	±0.2	±0.4	nA max	
Match Between Channels, ΔLeakage, I_S (Off)[1]	0.01			0.015	nA typ	
Drain Off Leakage, I_D (Off)						V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 33
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.25	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (Off), ADG5207 Only	0.015			0.015	nA typ	
Channel On Leakage, I_D (On), I_S (On)						V_S = V_D = 1 V/30 V; see Figure 34
ADG5206	±0.02				nA typ	
	±0.1	±0.25	±0.6	±3.3	nA max	
ADG5207	±0.02				nA typ	
	±0.1	±0.2	±0.4	±1.7	nA max	
Match Between Channels, ΔLeakage, I_D (On), I_S (On)[2]	0.01			0.03	nA typ	
DIGITAL INPUTS						
Input High Voltage, V_{INH}				2.0	V min	
Input Low Voltage, V_{INL}				0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002				μA typ	V_{IN} = V_{GND} or V_{DD}
				±0.1	μA max	
Digital Input Capacitance, C_{IN}	3				pF typ	
DYNAMIC CHARACTERISTICS[3]						
Transition Time, $t_{TRANSITION}$	225				ns typ	R_L = 300 Ω, C_L = 35 pF
	290	310	320	350	ns max	V_S = 18 V; see Figure 35
t_{ON} (EN)	215				ns typ	R_L = 300 Ω, C_L = 35 pF
	265	285	285	295	ns max	V_S = 18 V; see Figure 36
t_{OFF} (EN)	170				ns typ	R_L = 300 Ω, C_L = 35 pF
	215	230	245	270	ns max	V_S = 18 V; see Figure 36
Break-Before-Make Time Delay, t_D	90				ns typ	R_L = 300 Ω, C_L = 35 pF
				28	ns min	V_{S1} = V_{S2} = 18 V; see Figure 37
Charge Injection, Q_{INJ}	0.7				pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 38
	±3			±3	pC typ	V_S = 0 V to 30 V, R_S = 0 Ω, C_L = 1 nF

Parameter	25°C	−40°C to +60°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	−90				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 39
Channel-to-Channel Crosstalk	−76				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 40
−3 dB Bandwidth						R_L = 50 Ω, C_L = 5 pF; see Figure 41
ADG5206	55				MHz typ	
ADG5207	115				MHz typ	
Insertion Loss	5.65				dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 41
C_S (Off)	3.4				pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)						
ADG5206	62				pF typ	V_S = 18 V, f = 1 MHz
ADG5207	32				pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)						
ADG5206	66				pF typ	V_S = 18 V, f = 1 MHz
ADG5207	35				pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS						V_{DD} = 39.6 V
I_{DD}	80				µA typ	Digital inputs = 0 V or V_{DD}
	100			130	µA max	
V_{DD}				9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] The off channel leakage delta is calculated using the maximum of V_S = 1 V and V_D = 30 V, or V_S = 30 V and V_D = 1 V.
[2] The on channel leakage delta is calculated using the maximum of V_S = V_D = 1 V, or V_S = V_D = 30 V.
[3] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx, D, OR Dx

Table 5. ADG5206

Parameter	25°C	60°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR D					
V_{DD} = +15 V, V_{SS} = −15 V					
TSSOP (θ_{JA} = 67.7°C/W)	44	32	23	12	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	62	42	28	13	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V					
TSSOP (θ_{JA} = 67.7°C/W)	47	33	24	12	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	66	44	29	13	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V					
TSSOP (θ_{JA} = 67.7°C/W)	31	24	19	11	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	45	33	24	12	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V					
TSSOP (θ_{JA} = 67.7°C/W)	46	33	24	12	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	65	43	28	13	mA maximum

Table 6. ADG5207

Parameter	25°C	60°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx					
V_{DD} = +15 V, V_{SS} = −15 V					
TSSOP (θ_{JA} = 67.7°C/W)	33	25	19	11	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	48	34	24	12	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V					
TSSOP (θ_{JA} = 67.7°C/W)	35	27	20	11	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	51	36	25	12	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V					
TSSOP (θ_{JA} = 67.7°C/W)	23	19	15	12	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	34	26	20	12	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V					
TSSOP (θ_{JA} = 67.7°C/W)	34	26	20	11	mA maximum
LFCSP (θ_{JA} = 27.27°C/W)	50	35	25	12	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, Sx, D, or Dx Pins	
ADG5206	140 mA (pulsed at 1 ms, 10% duty cycle maximum)
ADG5207	105 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx, D, or Dx Pins[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
28-Lead TSSOP (4-Layer Board)	67.7°C/W
32-Lead LFCSP (4-Layer Board)	27.27°C/W
Reflow Soldering Peak Temperature, Pb Free	As per JEDEC J-STD-020
HBM ESD (ESDA/JEDEC JS-001-2011)	
ADG5206	
All Pins	8 kV
ADG5207	
I/O Port to Supplies	8 kV
I/O Port to I/O Port	2 kV
All Other Pins	8 kV

[1] Overvoltages at the Ax, EN, Sx, D, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5 and Table 6.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

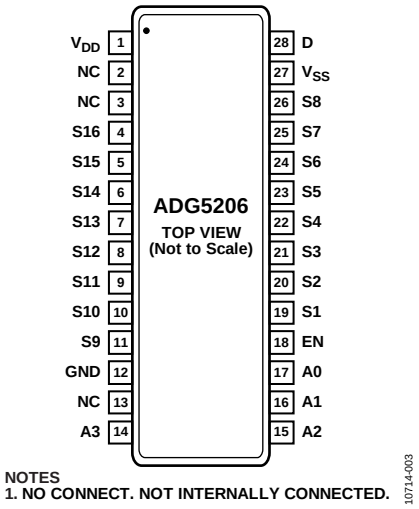


Figure 3. ADG5206 Pin Configuration (TSSOP)

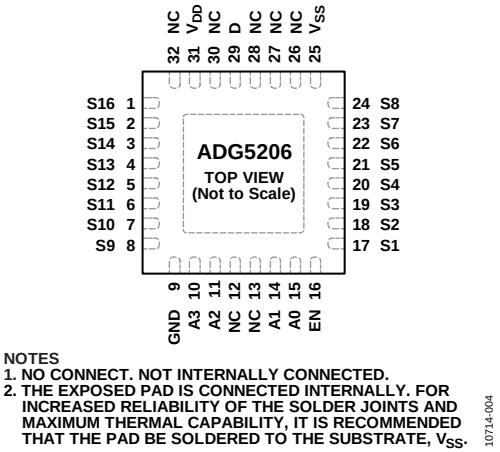


Figure 4. ADG5206 Pin Configuration (LFCSP)

Table 8. ADG5206 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	31	V_{DD}	Most Positive Power Supply Potential.
2, 3, 13	12, 13, 26, 27, 28, 30, 32	NC	No Connect. Not internally connected.
4	1	S16	Source Terminal 16. This pin can be an input or an output.
5	2	S15	Source Terminal 15. This pin can be an input or an output.
6	3	S14	Source Terminal 14. This pin can be an input or an output.
7	4	S13	Source Terminal 13. This pin can be an input or an output.
8	5	S12	Source Terminal 12. This pin can be an input or an output.
9	6	S11	Source Terminal 11. This pin can be an input or an output.
10	7	S10	Source Terminal 10. This pin can be an input or an output.
11	8	S9	Source Terminal 9. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
14	10	A3	Logic Control Input.
15	11	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1	Source Terminal 1. This pin can be an input or an output.
20	18	S2	Source Terminal 2. This pin can be an input or an output.
21	19	S3	Source Terminal 3. This pin can be an input or an output.
22	20	S4	Source Terminal 4. This pin can be an input or an output.
23	21	S5	Source Terminal 5. This pin can be an input or an output.
24	22	S6	Source Terminal 6. This pin can be an input or an output.
25	23	S7	Source Terminal 7. This pin can be an input or an output.
26	24	S8	Source Terminal 8. This pin can be an input or an output.
27	25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	29	D	Drain Terminal. This pin can be an input or an output.
NA	Exposed Pad		The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 9. ADG5206 Truth Table

A3	A2	A1	A0	EN	On Switch
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

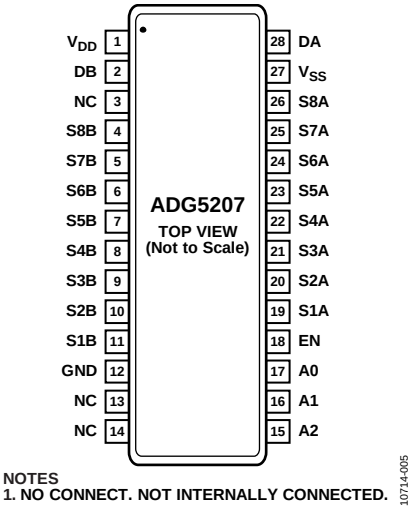


Figure 5. ADG5207 Pin Configuration (TSSOP)

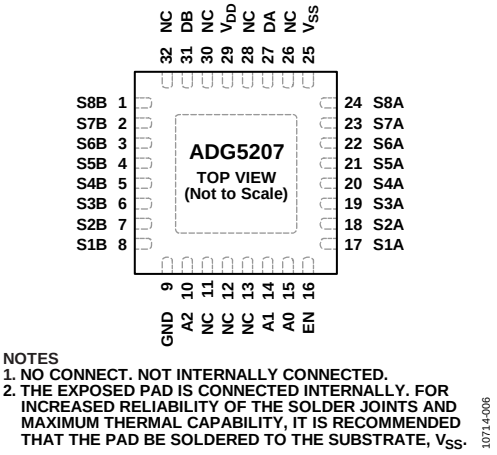


Figure 6. ADG5207 Pin Configuration (LFCSP)

Table 10. ADG5207 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	29	V_{DD}	Most Positive Power Supply Potential.
2	31	DB	Drain Terminal B. This pin can be an input or an output.
3, 13, 14	11, 12, 12, 26, 28, 30, 32	NC	No Connect. Not internally connected.
4	1	S8B	Source Terminal 8B. This pin can be an input or an output.
5	2	S7B	Source Terminal 7B. This pin can be an input or an output.
6	3	S6B	Source Terminal 6B. This pin can be an input or an output.
7	4	S5B	Source Terminal 5B. This pin can be an input or an output.
8	5	S4B	Source Terminal 4B. This pin can be an input or an output.
9	6	S3B	Source Terminal 3B. This pin can be an input or an output.
10	7	S2B	Source Terminal 2B. This pin can be an input or an output.
11	8	S1B	Source Terminal 1B. This pin can be an input or an output.
12	9	GND	Ground (0 V) Reference.
15	10	A2	Logic Control Input.
16	14	A1	Logic Control Input.
17	15	A0	Logic Control Input.
18	16	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are turned off. When this pin is high, the Ax logic inputs determine which switch is turned on.
19	17	S1A	Source Terminal 1A. This pin can be an input or an output.
20	18	S2A	Source Terminal 2A. This pin can be an input or an output.
21	19	S3A	Source Terminal 3A. This pin can be an input or an output.
22	20	S4A	Source Terminal 4A. This pin can be an input or an output.
23	21	S5A	Source Terminal 5A. This pin can be an input or an output.
24	22	S6A	Source Terminal 6A. This pin can be an input or an output.
25	23	S7A	Source Terminal 7A. This pin can be an input or an output.
26	24	S8A	Source Terminal 8A. This pin can be an input or an output.
27	25	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, this pin can be connected to ground.
28	27	DA	Drain Terminal A. This pin can be an input or an output.
NA	Exposed Pad		The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

Table 11. ADG5207 Truth Table

A2	A1	A0	EN	On Switch Pair
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TYPICAL PERFORMANCE CHARACTERISTICS

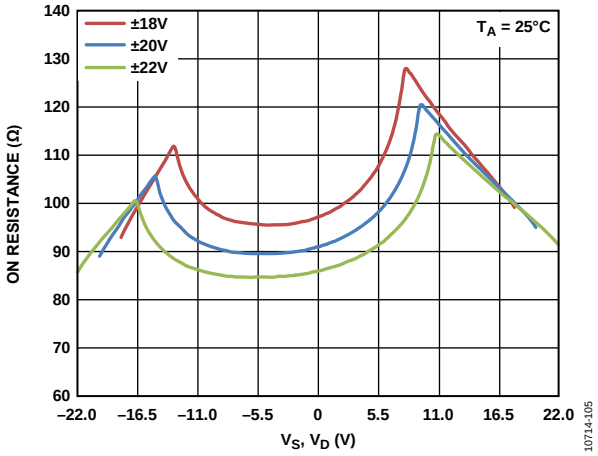


Figure 7. R_{ON} as a Function of V_S, V_D (±20 V Dual Supply)

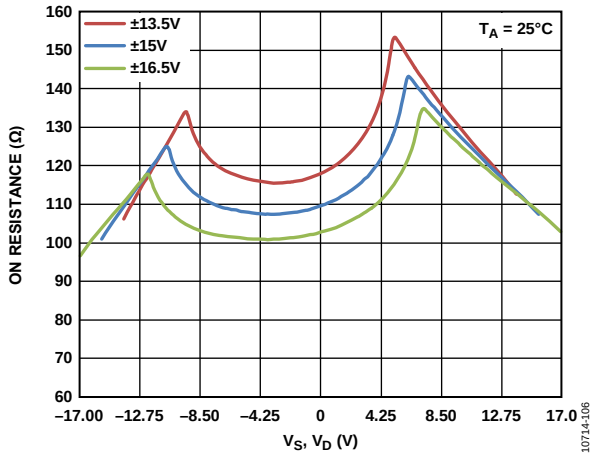


Figure 8. R_{ON} as a Function of V_S, V_D (±15 V Dual Supply)

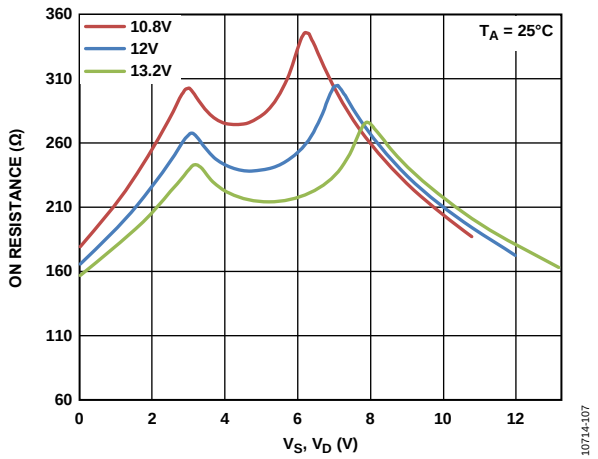


Figure 9. R_{ON} as a Function of V_S, V_D (12 V Single Supply)

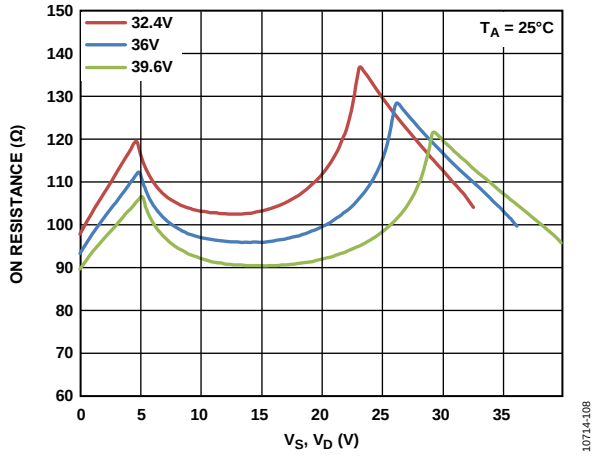


Figure 10. R_{ON} as a Function of V_S, V_D (36 V Single Supply)

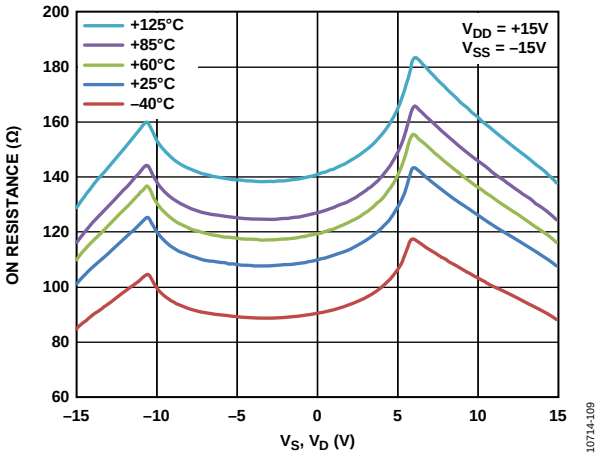


Figure 11. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±15 V Dual Supply

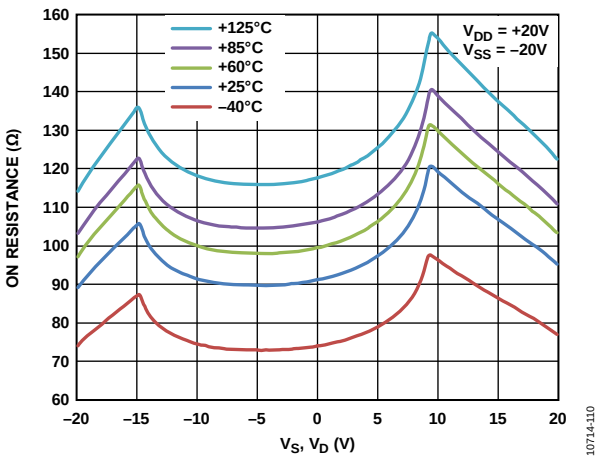


Figure 12. R_{ON} as a Function of V_S, V_D for Different Temperatures, ±20 V Dual Supply

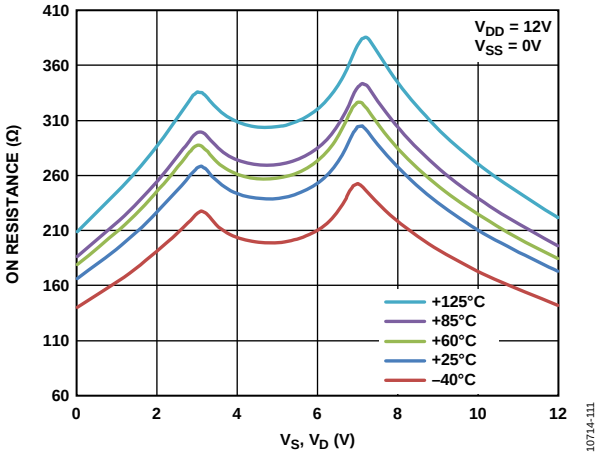


Figure 13. R_{ON} as a Function of V_S, V_D for Different Temperatures, 12 V Single Supply

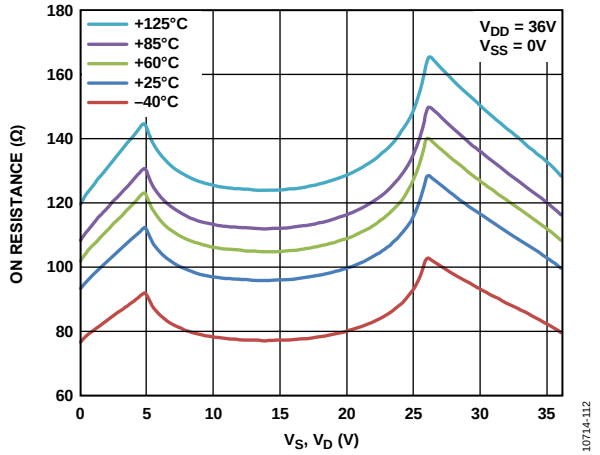


Figure 14. R_{ON} as a Function of V_S, V_D for Different Temperatures, 36 V Single Supply

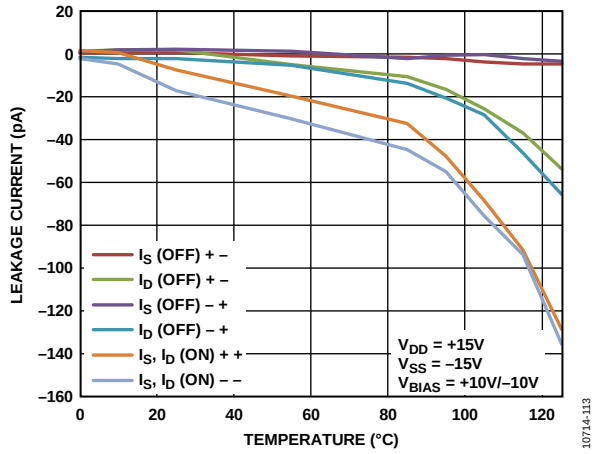


Figure 15. Leakage Currents vs. Temperature, ±15 V Dual Supply

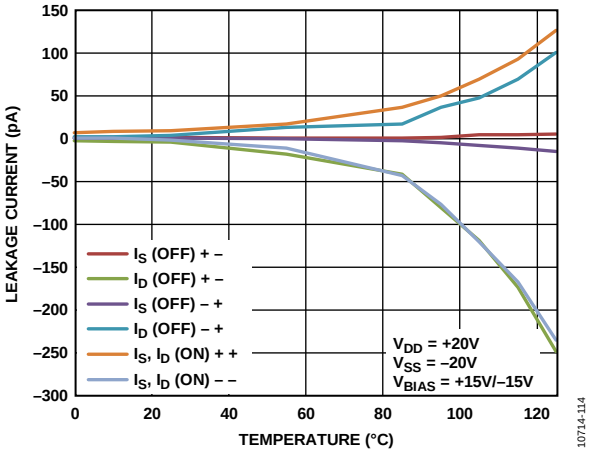


Figure 16. Leakage Currents vs. Temperature, ±20 V Dual Supply

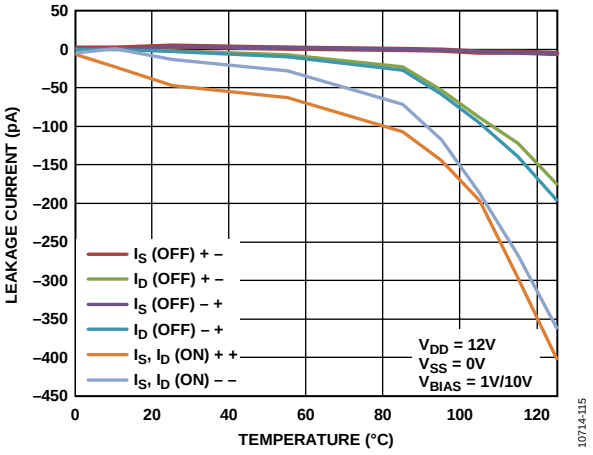


Figure 17. Leakage Currents vs. Temperature, 12 V Single Supply

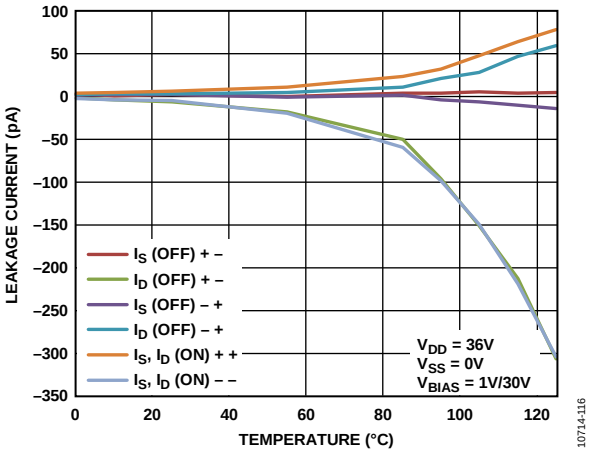


Figure 18. Leakage Currents vs. Temperature, 36 V Single Supply

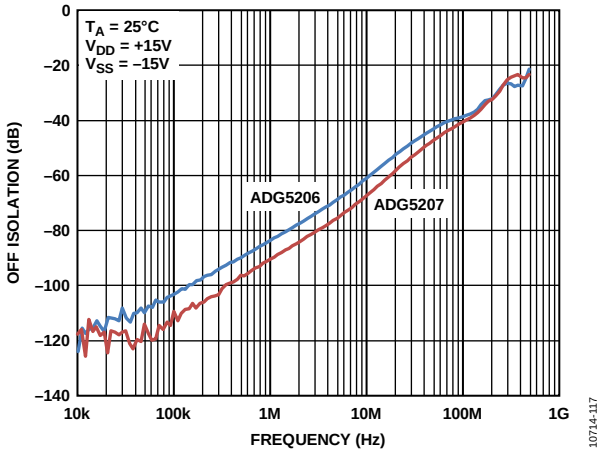


Figure 19. Off Isolation vs. Frequency, ±15 V Dual Supply

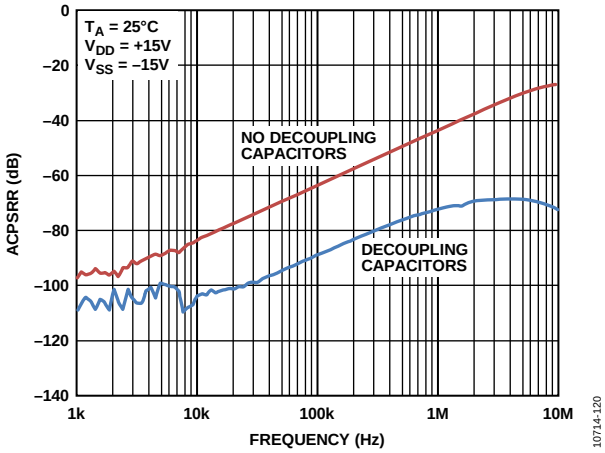


Figure 22. ACPSRR vs. Frequency, ±15 V Dual Supply

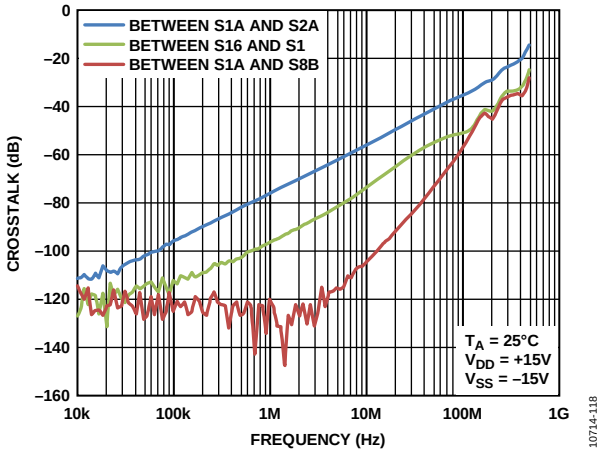


Figure 20. Crosstalk vs. Frequency, ±15 V Dual Supply

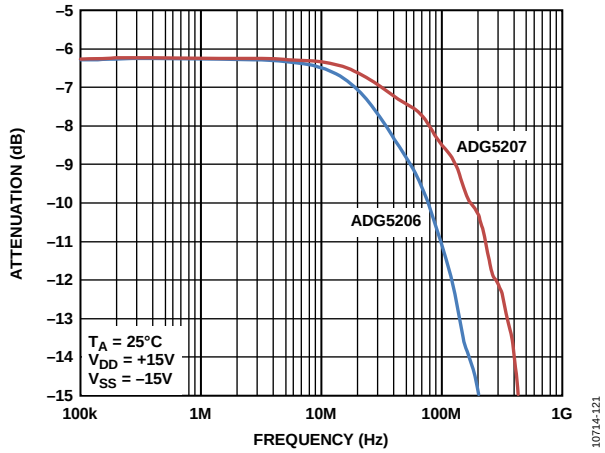


Figure 23. Bandwidth

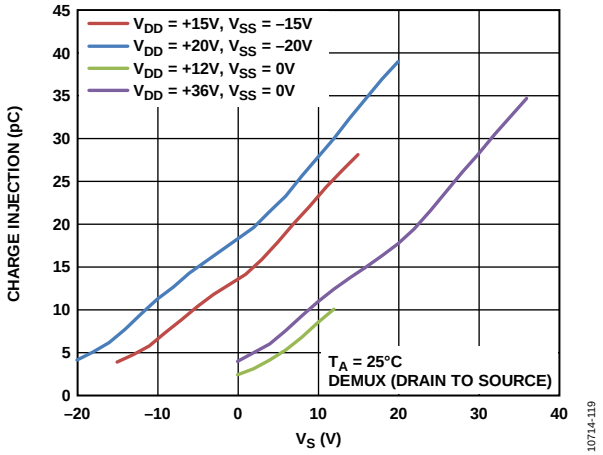


Figure 21. Charge Injection vs. Source Voltage, Drain to Source

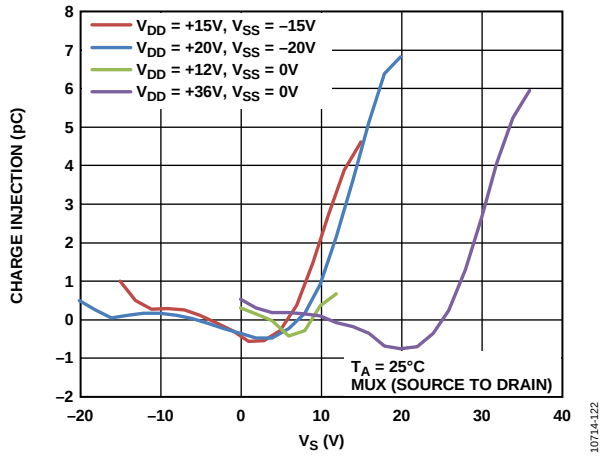


Figure 24. Charge Injection vs. Source Voltage, Source to Drain

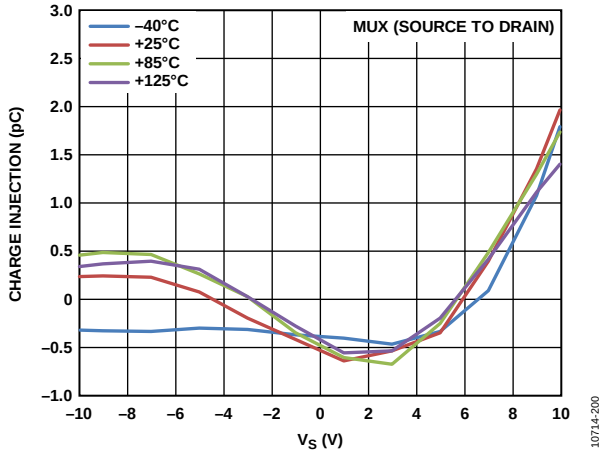


Figure 25. Q_{INJ} as a Function of V_S for Different Temperatures, ±15 V Dual Supply

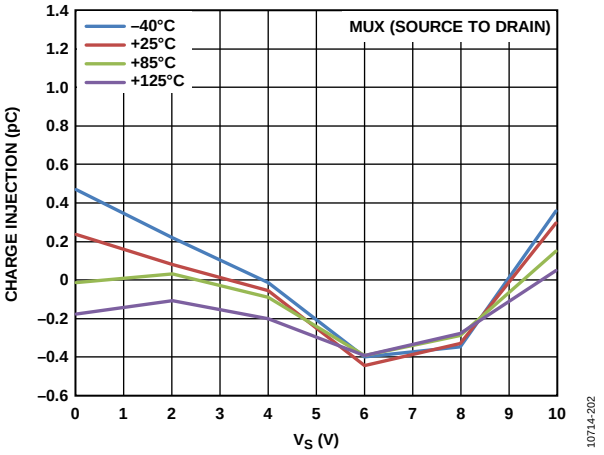


Figure 28. Q_{INJ} as a Function of V_S for Different Temperatures, 12 V Single Supply

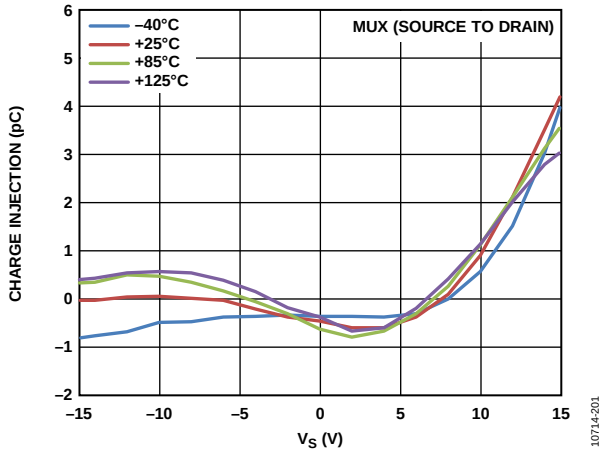


Figure 26. Q_{INJ} as a Function of V_S for Different Temperatures, ±20 V Dual Supply

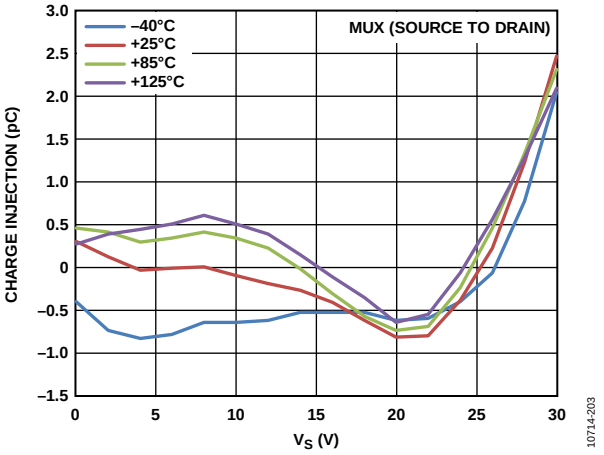


Figure 29. Q_{INJ} as a Function of V_S for Different Temperatures, 36 V Single Supply

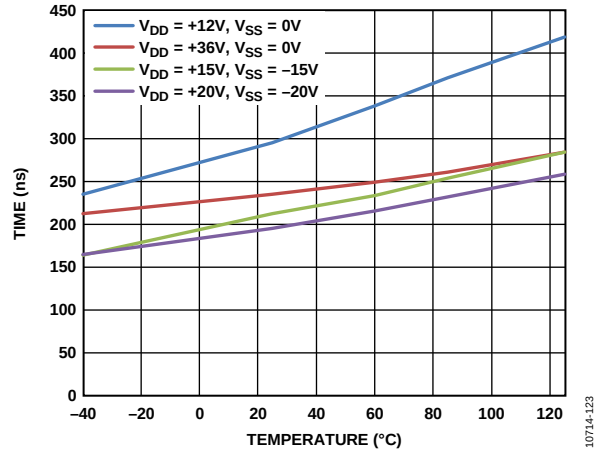


Figure 27. $t_{TRANSITION}$ Time vs. Temperature

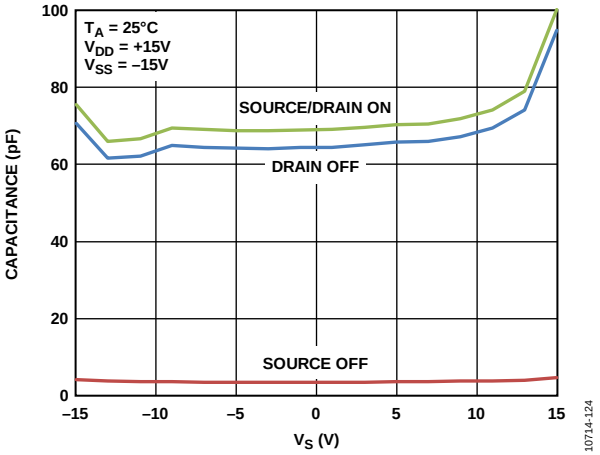


Figure 30. ADG5206 Capacitance vs. Source Voltage, ±15 V Dual Supply

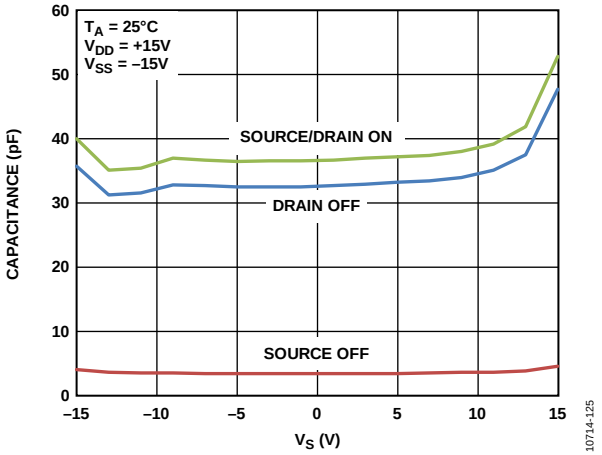


Figure 31. ADG5207 Capacitance vs. Source Voltage, ±15 V Dual Supply

TEST CIRCUITS

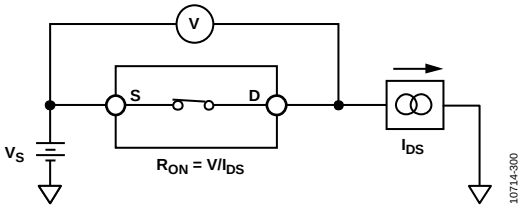


Figure 32. On Resistance

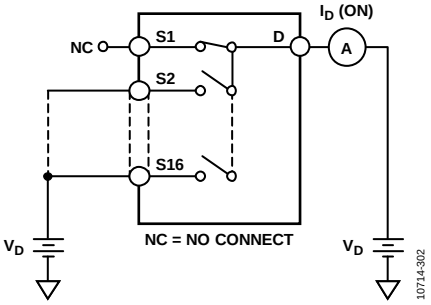


Figure 34. On Leakage

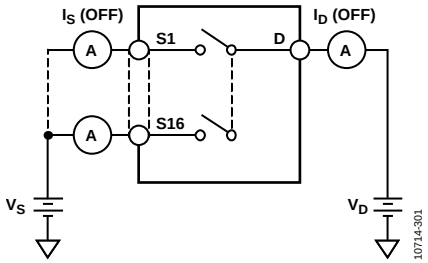


Figure 33. Off Leakage

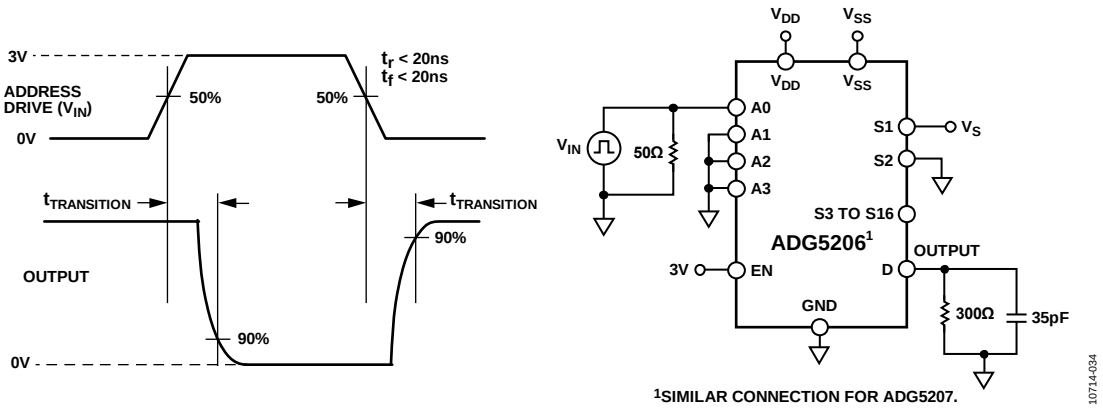


Figure 35. Address to Output Switching Times, $t_{TRANSITION}$

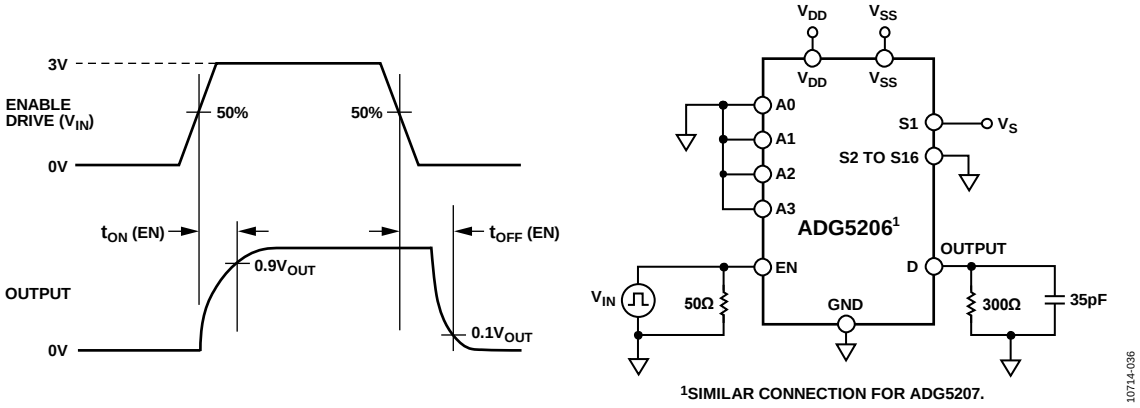


Figure 36. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

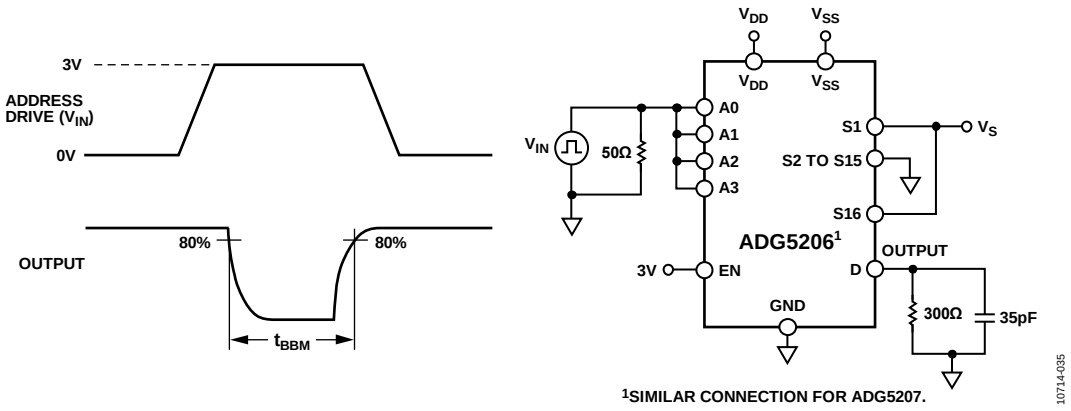


Figure 37. Break-Before-Make Time Delay, t_D

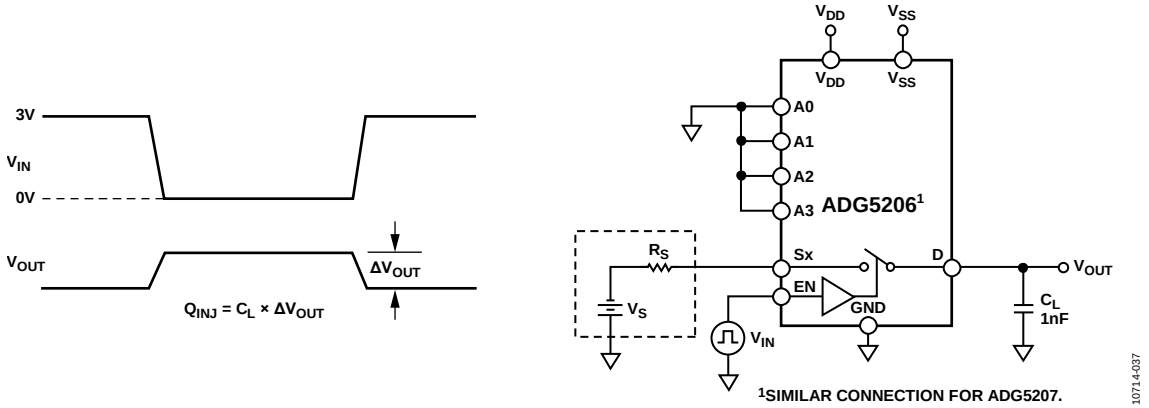


Figure 38. Charge Injection

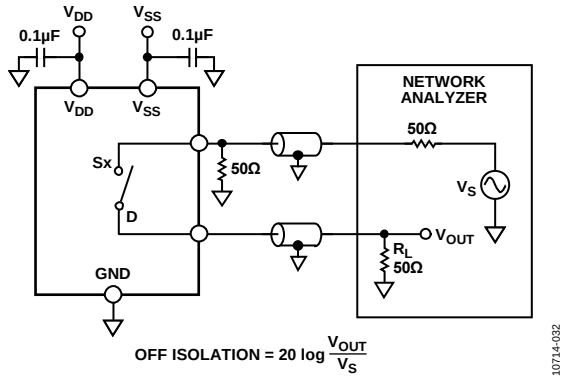


Figure 39. Off Isolation

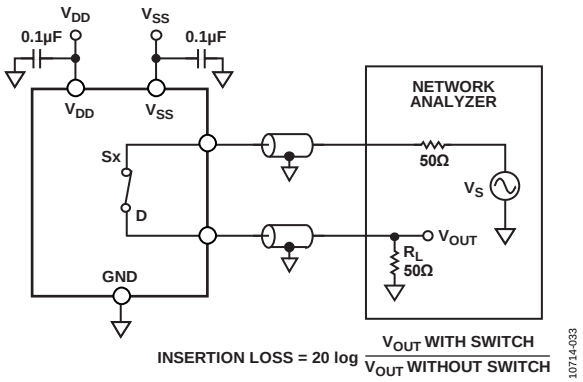


Figure 41. Bandwidth

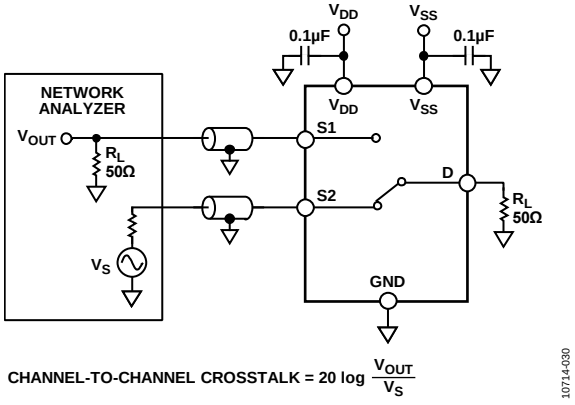


Figure 40. Channel-to-Channel Crosstalk

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} is the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
$R_{FLAT (ON)}$ is the flatness defined as the difference between the maximum and the minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} represents digital input capacitance.

t_{ON} (EN)
t_{ON} (EN) represents the delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} (EN)
t_{OFF} (EN) represents the delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
$t_{TRANSITION}$ represents the delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

Break-Before-Make Time Delay (t_D)
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off channel.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is a measure of the ability of a device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

APPLICATIONS INFORMATION

The ADG52xx family of switches and multiplexers provides a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persist until the power supply is turned off. The ADG5206/ADG5207 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V.

TRENCH ISOLATION

In the ADG5206/ADG5207, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors, causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed and the result is a latch-up proof switch.

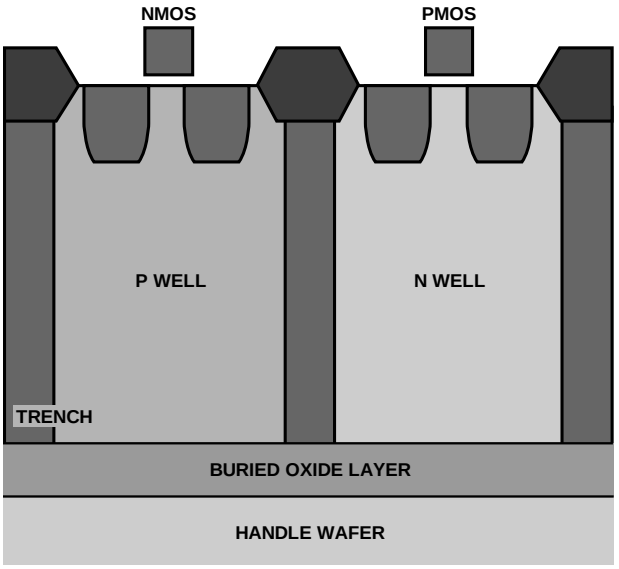
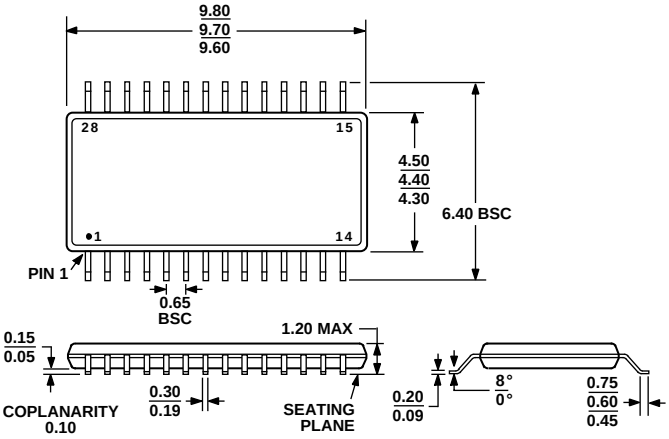


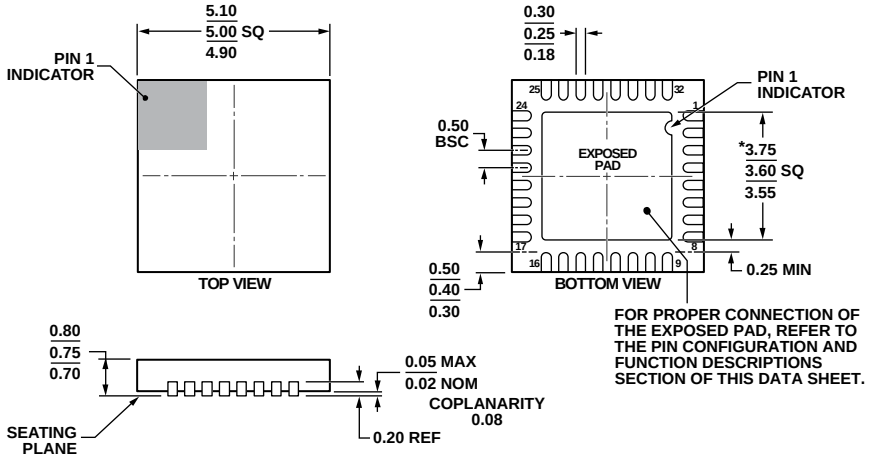
Figure 42. Trench Isolation

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 43. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5
WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 44. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 × 5 mm Body, Very Very Thin Quad (CP-32-12)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG5206BRUZ	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5206BRUZ-RL7	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5206BCPZ-RL7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADG5207BRUZ	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5207BRUZ-RL7	−40°C to +125°C	28-Lead Thin Shrink Small Outline Package [TSSOP]	RU-28
ADG5207BCPZ-RL7	−40°C to +125°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES

D10714-0-5/13(A)