

FEATURES

Latch-up immune under all circumstances
2.5 pF off source capacitance
12 pF off drain capacitance
-0.6 pC charge injection
Low leakage: 0.4 nA maximum at 85°C
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
48 V supply maximum ratings
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
V_{SS} to V_{DD} analog signal range

APPLICATIONS

High voltage signal routing
Automatic test equipment
Analog front-end circuits
Precision data acquisition
Industrial instrumentation
Amplifier gain select
Relay replacement

GENERAL DESCRIPTION

The **ADG5236** is a monolithic CMOS device containing two independently selectable single-pole/double throw (SPDT) switches. An EN input on the LFCSP package enables or disables the device. When disabled, all channels switch off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

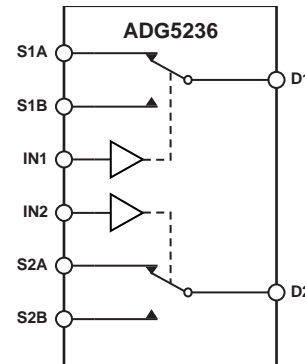
The ultralow capacitance and charge injection of these switches make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required. Fast switching speed together with high signal bandwidth make the device suitable for video signal switching.

Rev. B

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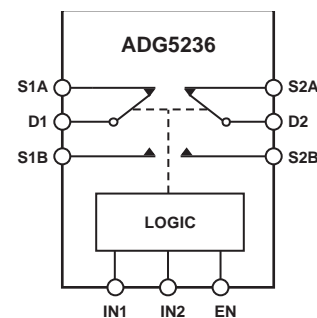
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FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC 1 INPUT. 09769-001

Figure 1. TSSOP Package



SWITCHES SHOWN FOR A LOGIC 1 INPUT. 09769-002

Figure 2. LFCSP Package

PRODUCT HIGHLIGHTS

- Trench Isolation Guards Against Latch-Up.**
 A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.
- Ultralow Capacitance and <1 pC Charge Injection.**
- Dual-Supply Operation.**
 For applications where the analog signal is bipolar, the **ADG5236** can be operated from dual supplies up to ±22 V.
- Single-Supply Operation.**
 For applications where the analog signal is unipolar, the **ADG5236** can be operated from a single rail power supply up to 40 V.
- 3 V Logic-Compatible Digital Inputs.**
 $V_{INH} = 2.0 \text{ V}$, $V_{INL} = 0.8 \text{ V}$.
- No V_L Logic Power Supply Required.**

ADG5236* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADG5236: High Voltage Latch-Up Proof, Dual SPDT Switches Data Sheet

REFERENCE DESIGNS

- CN0269

REFERENCE MATERIALS

Product Selection Guide

- Switches and Multiplexers Product Selection Guide

DESIGN RESOURCES

- ADG5236 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADG5236 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

Features	1	Absolute Maximum Ratings	8
Applications.....	1	ESD Caution.....	8
Functional Block Diagrams.....	1	Pin Configurations and Function Descriptions	9
General Description	1	Truth Tables for Switches	9
Product Highlights	1	Typical Performance Characteristics	10
Revision History	2	Test Circuits.....	14
Specifications.....	3	Terminology	16
±15 V Dual Supply	3	Trench Isolation	17
±20 V Dual Supply	4	Applications Information	18
12 V Single Supply.....	5	Outline Dimensions	19
36 V Single Supply.....	6	Ordering Guide	19
Continuous Current per Channel, Sx or Dx.....	7		

REVISION HISTORY

11/13—Rev. A to Rev. B

Changes to Features and Applications Sections	1
Changes to Figure 23.....	13

4/12—Rev. 0 to Rev. A

Updated Outline Dimensions	19
Changes to Ordering Guide	19

7/11—Revision 0: Initial Version

SPECIFICATIONS

±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V max	
On Resistance, R_{ON}	160 200	250	280	Ω typ Ω max	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$, see Figure 25 $V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$ $V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
On-Resistance Match Between Channels, ΔR_{ON}	1.4			Ω typ	
On-Resistance Flatness, $R_{FLAT(ON)}$	8 38 50	9 65	10 70	Ω max Ω typ Ω max	$V_S = \pm 10\text{ V}$, $I_S = -1\text{ mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01 0.1	0.2	0.4	nA typ nA max	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ $V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 27
Drain Off Leakage, I_D (Off)	0.01 0.1	0.4	1.2	nA typ nA max	$V_S = \pm 10\text{ V}$, $V_D = \mp 10\text{ V}$, see Figure 27
Channel On Leakage, I_D (On), I_S (On)	0.02 0.2	0.4	1.2	nA typ nA max	$V_S = V_D = \pm 10\text{ V}$, see Figure 24
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	150 230	280	315	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 30
t_{ON}	170 215	265	300	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 32
t_{OFF}	160 185	205	225	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 10\text{ V}$, see Figure 32
Break-Before-Make Time Delay, t_D	75		30	ns typ ns min	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 10\text{ V}$, see Figure 31
Charge Injection, Q_{INJ}	-0.6			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 33
Off Isolation	-85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 28
Channel-to-Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 26
-3 dB Bandwidth	266			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 29
Insertion Loss	-7			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 29
C_S (Off)	2.5			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (Off)	12			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$
C_D (On), C_S (On)	15			pF typ	$V_S = 0\text{ V}$, $f = 1\text{ MHz}$

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
I_{DD}	45			$\mu\text{A typ}$	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$ Digital inputs = 0 V or V_{DD}
	55		70	$\mu\text{A max}$	
I_{SS}	0.001			$\mu\text{A typ}$	Digital inputs = 0 V or V_{DD}
			1	$\mu\text{A max}$	
V_{DD}/V_{SS}			$\pm 9/\pm 22$	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

$V_{DD} = +20\text{ V} \pm 10\%$, $V_{SS} = -20\text{ V} \pm 10\%$, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V max	
On Resistance, R_{ON}	140			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$, see Figure 25
	160	200	230	Ω max	$V_{DD} = +18\text{ V}$, $V_{SS} = -18\text{ V}$
On-Resistance Match Between Channels, ΔR_{ON}	1.3			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$
	8	9	10	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	33			Ω typ	$V_S = \pm 15\text{ V}$, $I_S = -1\text{ mA}$
	45	55	60	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01			nA typ	$V_{DD} = +22\text{ V}$, $V_{SS} = -22\text{ V}$ $V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 27
	0.1	0.2	0.4	nA max	
Drain Off Leakage, I_D (Off)	0.01			nA typ	$V_S = \pm 15\text{ V}$, $V_D = \mp 15\text{ V}$, see Figure 27
	0.1	0.4	1.2	nA max	
Channel On Leakage, I_D (On), I_S (On)	0.02			nA typ	$V_S = V_D = \pm 15\text{ V}$, see Figure 24
	0.2	0.4	1.2	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002			$\mu\text{A typ}$	$V_{IN} = V_{GND}$ or V_{DD}
			± 0.1	$\mu\text{A max}$	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	150			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	210	260	290	ns max	$V_S = 10\text{ V}$, see Figure 30
t_{ON}	150			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	190	235	267	ns max	$V_S = 10\text{ V}$, see Figure 32
t_{OFF}	155			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
	180	200	215	ns max	$V_S = 10\text{ V}$, see Figure 32
Break-Before-Make Time Delay, t_D	60			ns typ	$R_L = 300\ \Omega$, $C_L = 35\text{ pF}$
			30	ns min	$V_{S1} = V_{S2} = 10\text{ V}$, see Figure 31
Charge Injection, Q_{INJ}	-0.6			pC typ	$V_S = 0\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$, see Figure 33
Off Isolation	-85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 28
Channel-to-Channel Crosstalk	-85			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 26
-3 dB Bandwidth	266			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, see Figure 29
Insertion Loss	-7			dB typ	$R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$, see Figure 29

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
C _S (Off)	2.5			pF typ	V _S = 0 V, f = 1 MHz
C _D (Off)	12			pF typ	V _S = 0 V, f = 1 MHz
C _D (On), C _S (On)	15			pF typ	V _S = 0 V, f = 1 MHz
POWER REQUIREMENTS					
I _{DD}	50 70		110	μA typ μA max	V _{DD} = +22 V, V _{SS} = -22 V Digital inputs = 0 V or V _{DD}
I _{SS}	0.001		1	μA typ μA max	Digital inputs = 0 V or V _{DD}
V _{DD} /V _{SS}			±9/±22	V min/V max	GND = 0 V

¹ Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V _{DD}	V max	
On Resistance, R _{ON}	350			Ω typ	V _S = 0 V to 10 V, I _S = -1 mA, see Figure 25
On-Resistance Match Between Channels, ΔR _{ON}	500 3	610	700	Ω max Ω typ	V _{DD} = 10.8 V, V _{SS} = 0 V V _S = 0 V to 10 V, I _S = -1 mA
On-Resistance Flatness, R _{FLAT (ON)}	20 145 280	21 335	22 370	Ω max Ω typ Ω max	V _S = 0 V to 10 V, I _S = -1 mA
LEAKAGE CURRENTS					
Source Off Leakage, I _S (Off)	0.01			nA typ	V _{DD} = 13.2 V, V _{SS} = 0 V V _S = 1 V/10 V, V _D = 10 V/1 V, see Figure 27
Drain Off Leakage, I _D (Off)	0.1 0.01	0.2	0.4	nA max nA typ	V _S = 1 V/10 V, V _D = 10 V/1 V, see Figure 27
Channel On Leakage, I _D (On), I _S (On)	0.1 0.02 0.2	0.4	1.2 1.2	nA max nA typ nA max	V _S = V _D = 1 V/10 V, see Figure 24
DIGITAL INPUTS					
Input High Voltage, V _{INH}			2.0	V min	
Input Low Voltage, V _{INL}			0.8	V max	
Input Current, I _{INL} or I _{INH}	0.002		±0.1	μA typ μA max	V _{IN} = V _{GND} or V _{DD}
Digital Input Capacitance, C _{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, t _{TRANSITION}	220 390	430	490	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V, see Figure 30
t _{ON}	275 380	440	510	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V, see Figure 32
t _{OFF}	160 195	225	245	ns typ ns max	R _L = 300 Ω, C _L = 35 pF V _S = 8 V, see Figure 32
Break-Before-Make Time Delay, t _D	145		65	ns typ ns min	R _L = 300 Ω, C _L = 35 pF V _{S1} = V _{S2} = 8 V, see Figure 31
Charge Injection, Q _{INJ}	-0.6			pC typ	V _S = 6 V, R _S = 0 Ω, C _L = 1 nF, see Figure 33

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$, see Figure 28
Channel-to-Channel Crosstalk	−90			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$, see Figure 26
−3 dB Bandwidth	185			MHz typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, see Figure 29
Insertion Loss	−11			dB typ	$R_L = 50\ \Omega$, $C_L = 5\ \text{pF}$, $f = 1\ \text{MHz}$, see Figure 29
C_S (Off)	3			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (Off)	16			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
C_D (On), C_S (On)	16			pF typ	$V_S = 6\ \text{V}$, $f = 1\ \text{MHz}$
POWER REQUIREMENTS					
I_{DD}	40		65	μA typ μA max	$V_{DD} = 13.2\ \text{V}$ Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	GND = 0 V, $V_{SS} = 0\ \text{V}$

¹ Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

$V_{DD} = 36\ \text{V} \pm 10\%$, $V_{SS} = 0\ \text{V}$, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analogue Signal Range			0 V to V_{DD}	V max	
On Resistance, R_{ON}	150			Ω typ	$V_S = 0\ \text{V}$ to 30 V, $I_S = -1\ \text{mA}$, see Figure 25
On-Resistance Match Between Channels, ΔR_{ON}	170 1.4	215	245	Ω max Ω typ	$V_{DD} = 32.4\ \text{V}$, $V_{SS} = 0\ \text{V}$ $V_S = 0\ \text{V}$ to 30 V, $I_S = -1\ \text{mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	8 35 50	9 60	10 65	Ω max Ω typ Ω max	$V_S = 0\ \text{V}$ to 30 V, $I_S = -1\ \text{mA}$
LEAKAGE CURRENTS					
Source Off Leakage, I_S (Off)	0.01			nA typ	$V_{DD} = 39.6\ \text{V}$, $V_{SS} = 0\ \text{V}$ $V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$, see Figure 27
Drain Off Leakage, I_D (Off)	0.1 0.01	0.2	0.4	nA max nA typ	$V_S = 1\ \text{V}/30\ \text{V}$, $V_D = 30\ \text{V}/1\ \text{V}$, see Figure 27
Channel On Leakage, I_D (On), I_S (On)	0.1 0.02 0.2	0.4 0.4	1.2 1.2	nA max nA typ nA max	$V_S = V_D = 1\ \text{V}/30\ \text{V}$, see Figure 24
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.002		± 0.1	μA typ μA max	$V_{IN} = V_{GND}$ or V_{DD}
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS¹					
Transition Time, $t_{TRANSITION}$	180 250	275	305	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ $V_S = 18\ \text{V}$, see Figure 30
t_{ON}	170 225	265	295	ns typ ns max	$R_L = 300\ \Omega$, $C_L = 35\ \text{pF}$ $V_S = 18\ \text{V}$, see Figure 32

Parameter	25°C	-40°C to +85°C	-40°C to +125°C	Unit	Test Conditions/Comments
t_{OFF}	170			ns typ	$R_L = 300 \Omega$, $C_L = 35$ pF
	215	215	225	ns max	$V_S = 18$ V, see Figure 32
Break-Before-Make Time Delay, t_D	75			ns typ	$R_L = 300 \Omega$, $C_L = 35$ pF
			35	ns min	$V_{S1} = V_{S2} = 18$ V, see Figure 31
Charge Injection, Q_{INJ}	-0.6			pC typ	$V_S = 18$ V, $R_S = 0 \Omega$, $C_L = 1$ nF, see Figure 33
Off Isolation	-85			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz, see Figure 28
Channel-to-Channel Crosstalk	-85			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz, see Figure 26
-3 dB Bandwidth	266			MHz typ	$R_L = 50 \Omega$, $C_L = 5$ pF, see Figure 29
Insertion Loss	-7			dB typ	$R_L = 50 \Omega$, $C_L = 5$ pF, $f = 1$ MHz, see Figure 29
C_S (Off)	2.5			pF typ	$V_S = 18$ V, $f = 1$ MHz
C_D (Off)	12			pF typ	$V_S = 18$ V, $f = 1$ MHz
C_D (On), C_S (On)	15			pF typ	$V_S = 18$ V, $f = 1$ MHz
POWER REQUIREMENTS					
I_{DD}	85			μ A typ	$V_{DD} = 39.6$ V
	100		130	μ A max	Digital inputs = 0 V or V_{DD}
V_{DD}			9/40	V min/V max	GND = 0 V, $V_{SS} = 0$ V

¹ Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, SxA, SxB, OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, SxA, SxB, or Dx				
$V_{DD} = +15$ V, $V_{SS} = -15$ V				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	19	7	2.8	mA max
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	30	7.7	2.8	mA max
$V_{DD} = +20$ V, $V_{SS} = -20$ V				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	21	7	2.8	mA max
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	31	7.7	2.8	mA max
$V_{DD} = 12$ V, $V_{SS} = 0$ V				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	14	6.3	2.7	mA max
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	22.5	7.3	2.8	mA max
$V_{DD} = 36$ V, $V_{SS} = 0$ V				
TSSOP ($\theta_{JA} = 112.6^\circ\text{C/W}$)	24	7.4	2.8	mA max
LFCSP ($\theta_{JA} = 30.4^\circ\text{C/W}$)	35	7.8	2.8	mA max

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	-0.3 V to +48 V
V_{SS} to GND	+0.3 V to -48 V
Analog Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Digital Inputs ¹	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$ or 30 mA, whichever occurs first
Peak Current, SxA, SxB, or Dx Pin	63 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, SxA, SxB, or Dx ²	Data + 15%
Temperature Range	
Operating	-40°C to +125°C
Storage	-65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112°C/W
16-Lead LFCSP	30.4°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/-5)°C

¹ Overvoltages at the INx, SxA, SxB, and Dx pins are clamped by internal diodes. Limit the current to the maximum ratings given.

² See Table 5.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

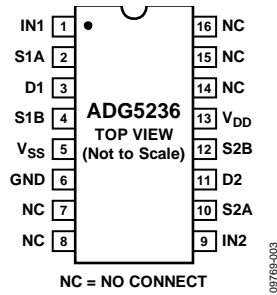
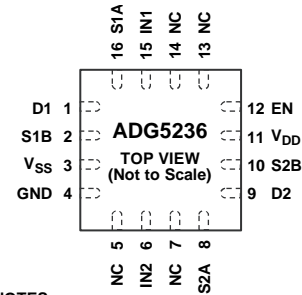


Figure 3. TSSOP Pin Configuration



NOTES
 1. EXPOSED PAD TIED TO SUBSTRATE, V_{SS}.
 2. NC = NO CONNECT.

Figure 4. LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.		Mnemonic	Description
TSSOP	LFCSP		
1	15	IN1	Logic Control Input 1.
2	16	S1A	Source Terminal 1A. This pin can be an input or output.
3	1	D1	Drain Terminal 1. This pin can be an input or output.
4	2	S1B	Source Terminal 1B. This pin can be an input or output.
5	3	V _{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 14 to 16	5, 7, 13, 14	NC	No Connect. These pins are open.
9	6	IN2	Logic Control Input 2.
10	8	S2A	Source Terminal 2A. This pin can be an input or output.
11	9	D2	Drain Terminal 2. This pin can be an input or output.
12	10	S2B	Source Terminal 2B. This pin can be an input or output.
13	11	V _{DD}	Most Positive Power Supply Potential.
N/A ¹	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the IN _x logic inputs determine the on switches.
N/A ¹	EP	Exposed Pad	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V _{SS} .

¹ N/A means not applicable.

TRUTH TABLES FOR SWITCHES

Table 8. TSSOP Truth Table

IN _x	S _x A	S _x B
0	Off	On
1	On	Off

Table 9. LFCSP Truth Table

EN	IN _x	S _x A	S _x B
0	X ¹	Off	Off
1	0	Off	On
1	1	On	Off

¹ X means don't care.

TYPICAL PERFORMANCE CHARACTERISTICS

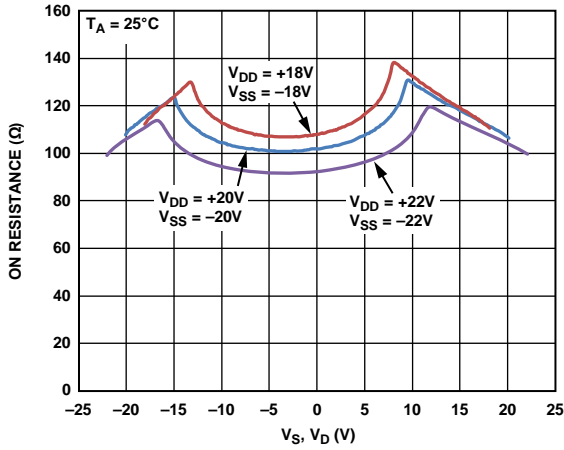


Figure 5. On Resistance vs. V_S , V_D (Dual Supply)

09769-105

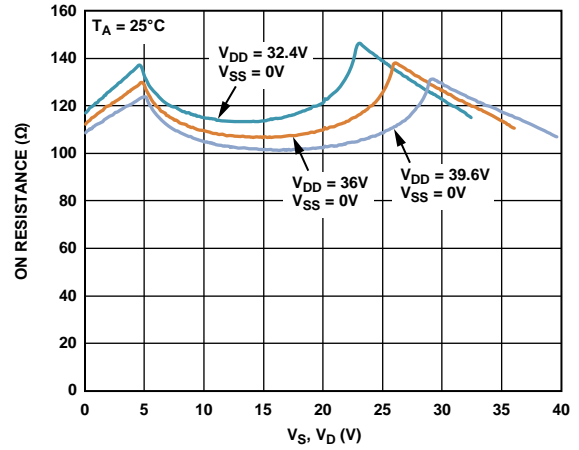


Figure 8. On Resistance vs. V_S , V_D (Single Supply)

09769-108

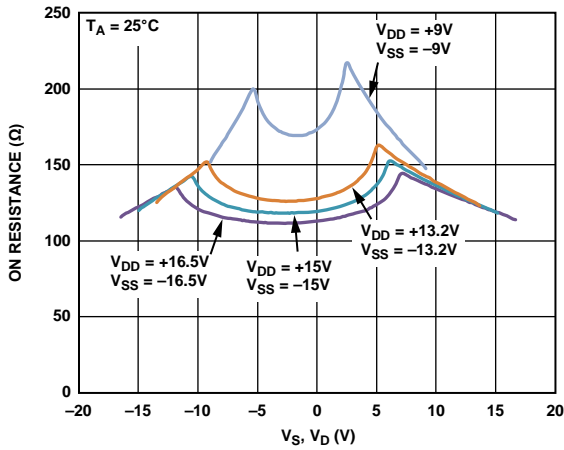


Figure 6. On Resistance vs. V_S , V_D (Dual Supply)

09769-106

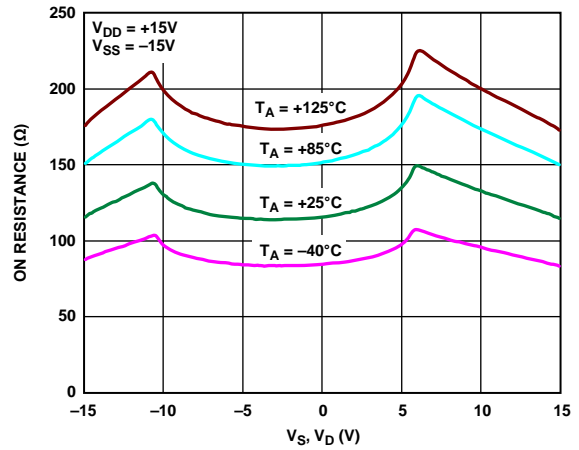


Figure 9. On Resistance vs. V_D or V_S for Different Temperatures, ± 15 V Dual Supply

09769-109

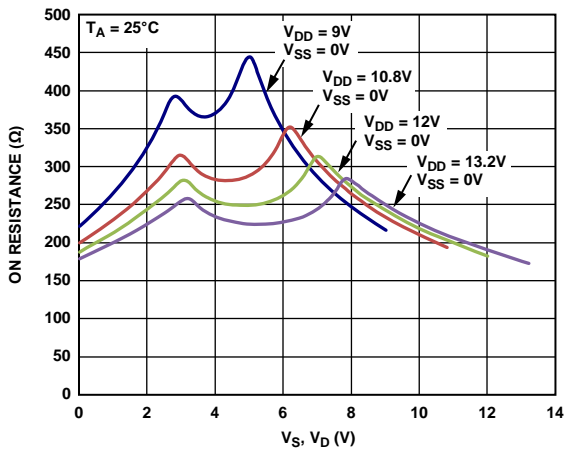


Figure 7. On Resistance vs. V_S , V_D (Single Supply)

09769-107

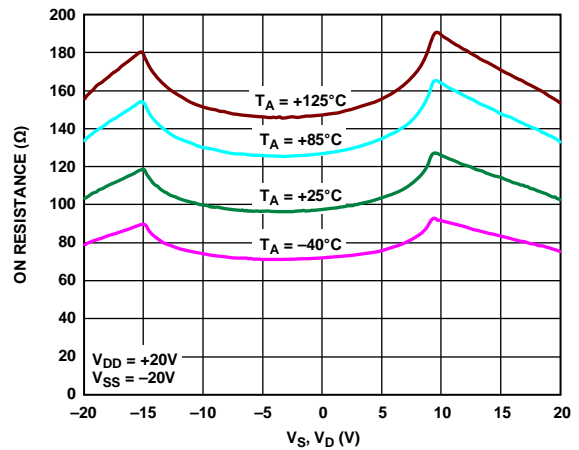


Figure 10. On Resistance vs. V_D or V_S for Different Temperatures, ± 20 V Dual Supply

09769-110

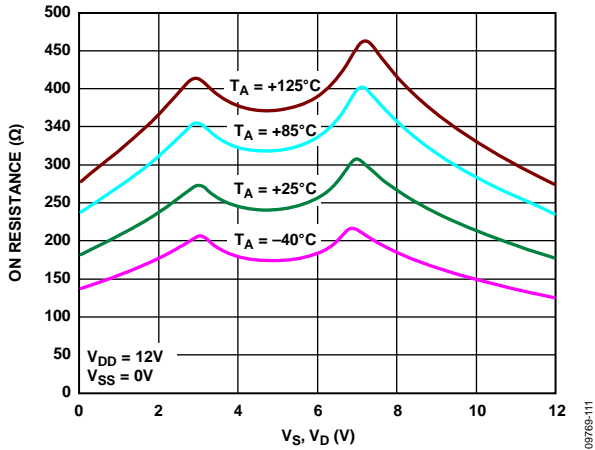


Figure 11. On Resistance vs. V_D or V_S for Different Temperatures, 12 V Single Supply

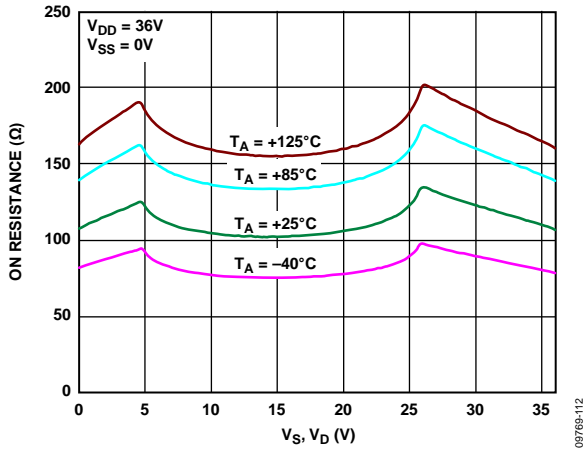


Figure 12. On Resistance vs. V_S or V_D for Different Temperatures, 36 V Single Supply

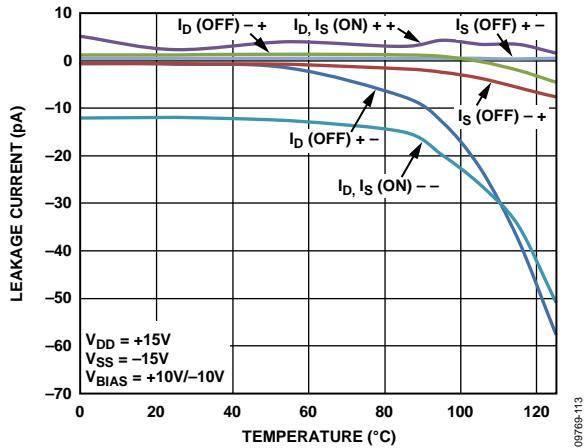


Figure 13. Leakage Current vs. Temperature, ± 15 V Dual Supply

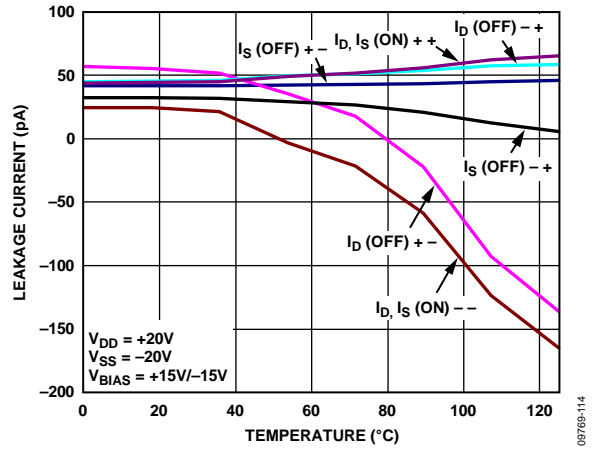


Figure 14. Leakage Current vs. Temperature, ± 20 V Single Supply

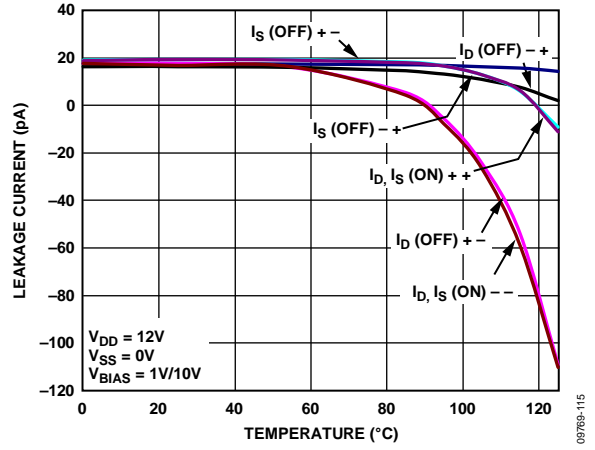


Figure 15. Leakage Current vs. Temperature, 12 V Single Supply

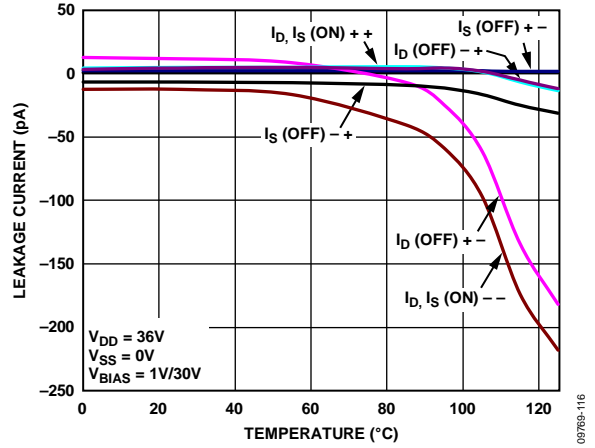


Figure 16. Leakage Current vs. Temperature, 36 V Single Supply

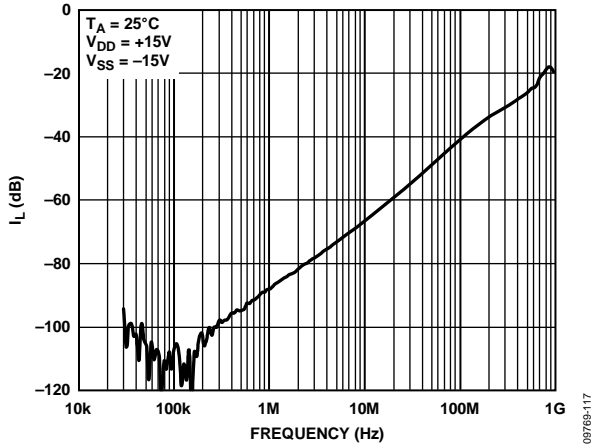


Figure 17. Off Isolation vs. Frequency

09769-117

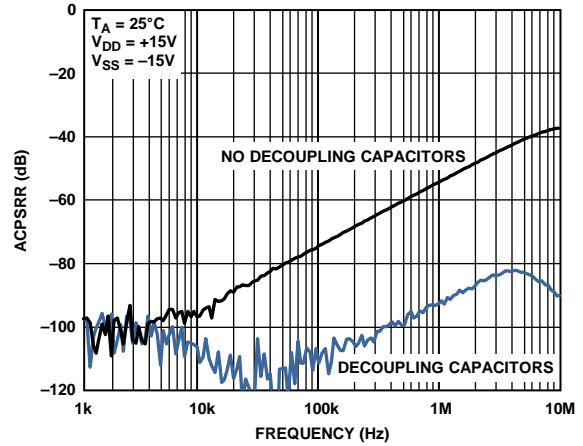


Figure 20. ACPSRR vs. Frequency

09769-120

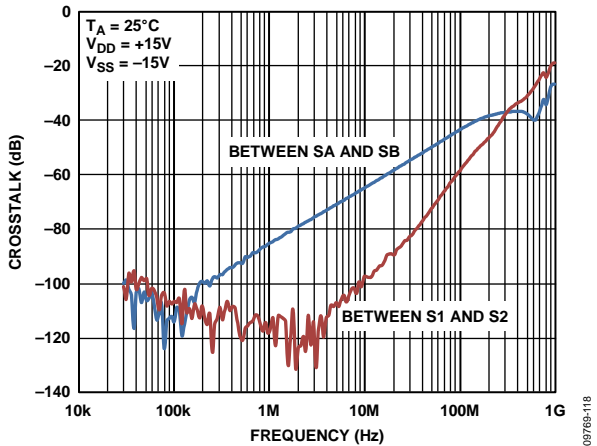


Figure 18. Crosstalk vs. Frequency

09769-118

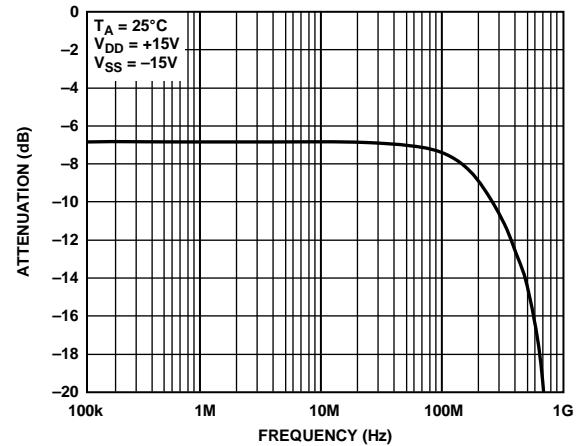


Figure 21. Bandwidth

09769-122

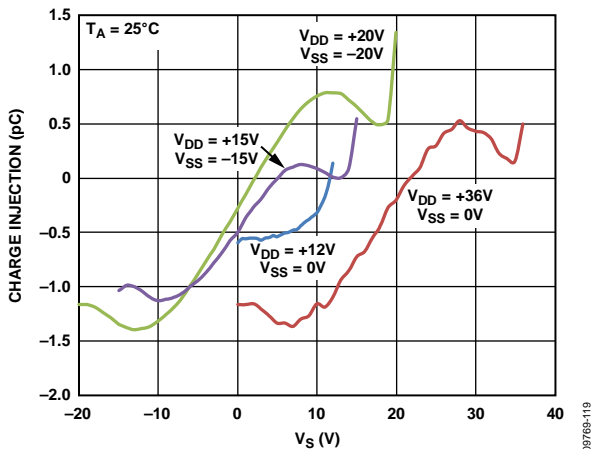


Figure 19. Charge Injection vs. Source Voltage

09769-119

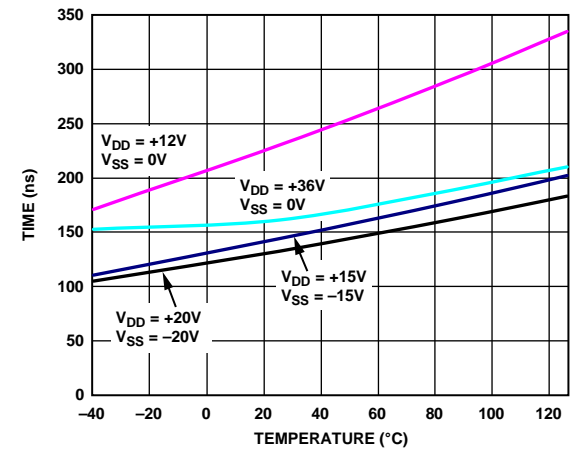


Figure 22. $t_{\text{TRANSITION}}$ Time vs. Temperature

09769-123

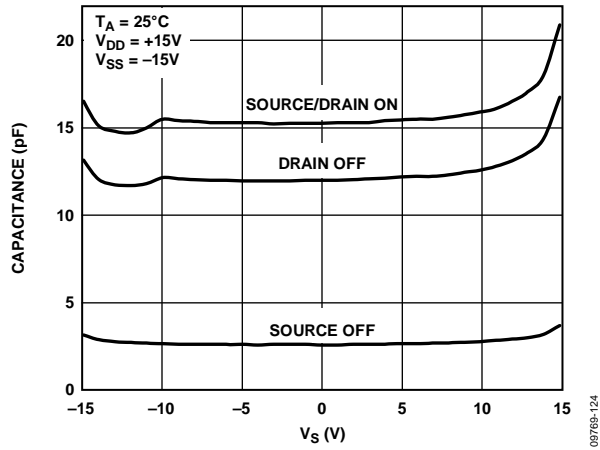


Figure 23. Capacitance vs. Source Voltage, Dual Supply

TEST CIRCUITS

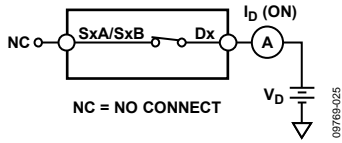


Figure 24. On Leakage



Figure 27. Off Leakage

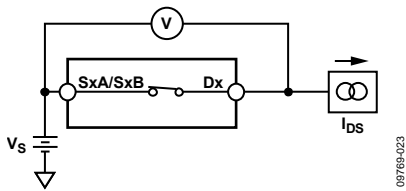


Figure 25. On Resistance

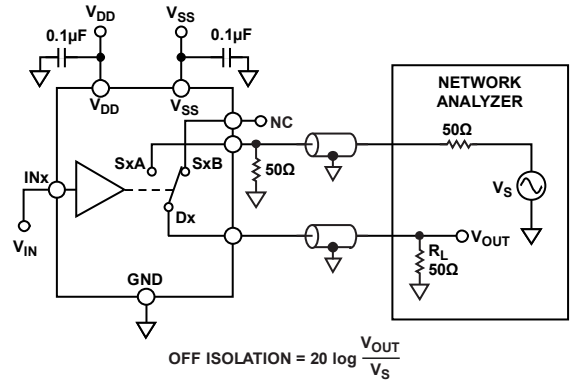


Figure 28. Off Isolation

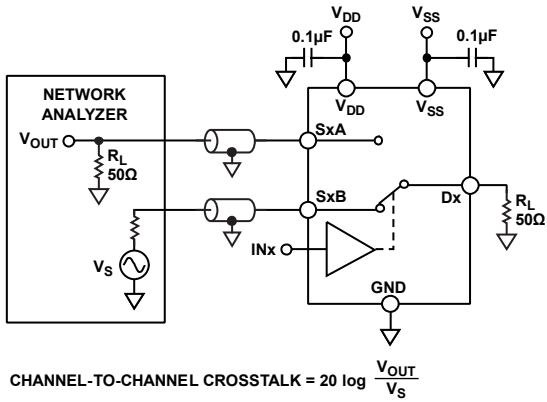


Figure 26. Channel-to-Channel Crosstalk

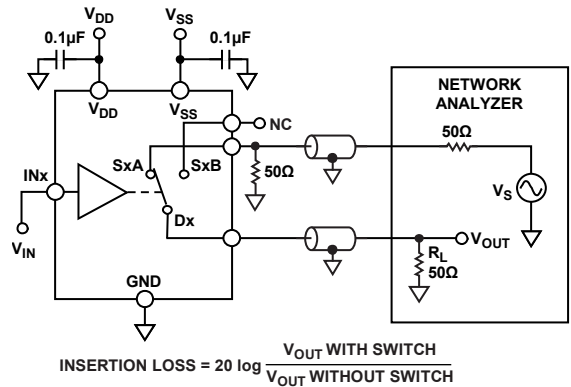


Figure 29. Bandwidth

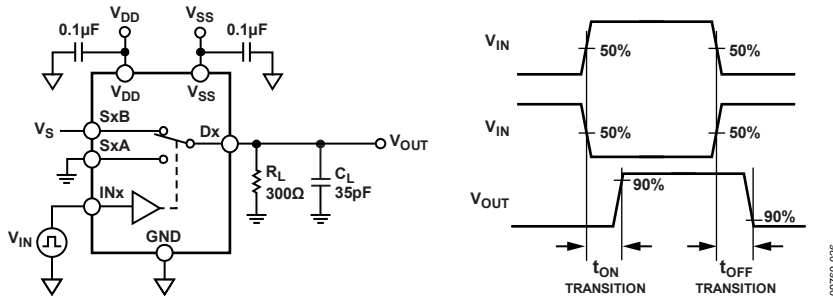


Figure 30. Switching Times

09769-026

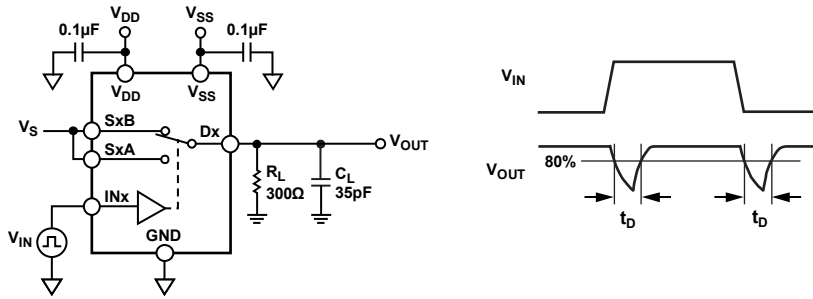


Figure 31. Break-Before-Make Time Delay t_d

09769-027

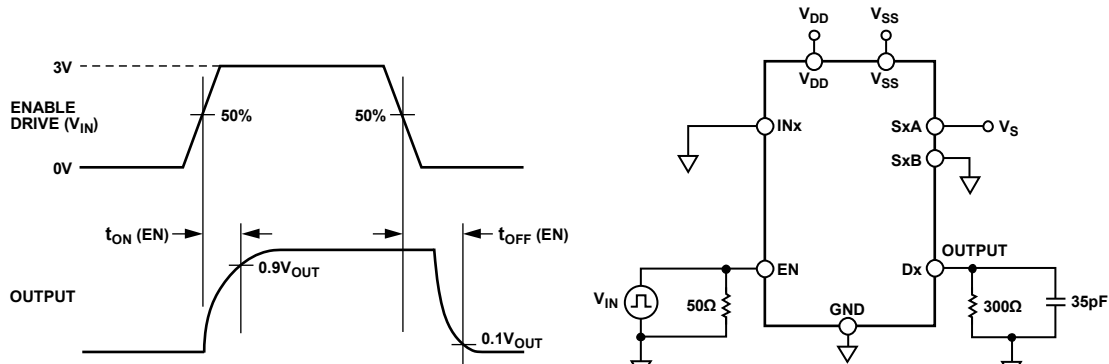


Figure 32. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$

09769-028

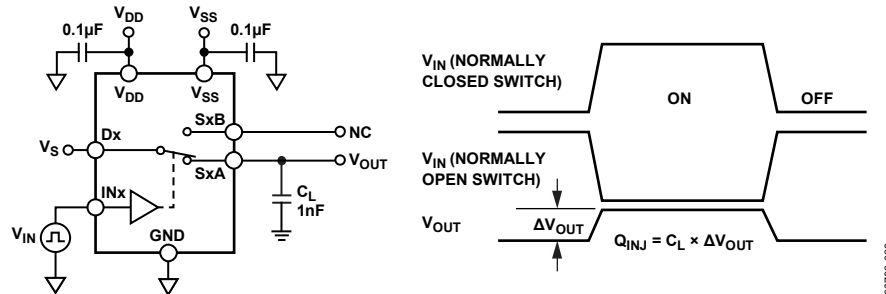


Figure 33. Charge Injection

09769-029

TERMINOLOGY

I_{DD}

I_{DD} represents the positive supply current.

I_{SS}

I_{SS} represents the negative supply current.

V_D, V_S

V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}

R_{ON} represents the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}

ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT(ON)}$.

I_S (Off)

I_S (Off) is the source leakage current with the switch off.

I_D (Off)

I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)

I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}

V_{INL} is the maximum input voltage for Logic 0.

V_{INH}

V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}

I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)

C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)

C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)

C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}

C_{IN} is the digital input capacitance.

t_{ON}

t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}

t_{OFF} represents the delay between applying the digital control input and the output switching off.

t_D

t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation

Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth

Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response

On response is the frequency response of the on switch.

Insertion Loss

Insertion loss is the loss due to the on resistance of the switch.

AC Power Supply Rejection Ratio (ACPSRR)

ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

TRENCH ISOLATION

In the [ADG5236](#), an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

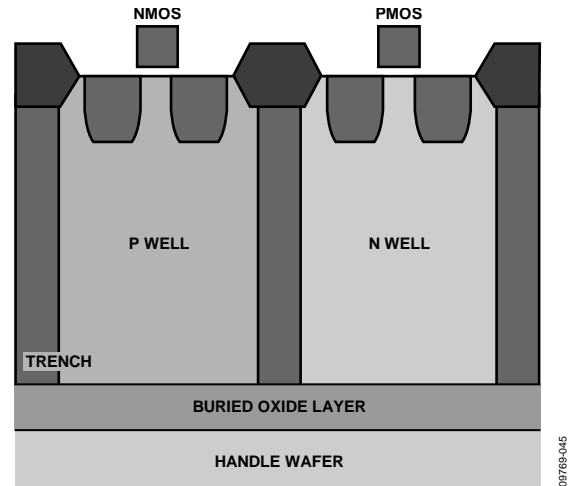
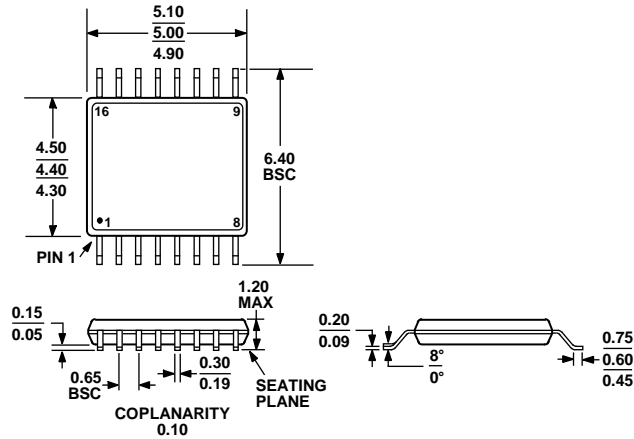


Figure 34. Trench Isolation

APPLICATIONS INFORMATION

The ADG52xx family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The [ADG5236](#) high voltage switches allow single-supply operation from 9 V to 40 V and dual supply operation from ± 9 V to ± 22 V.

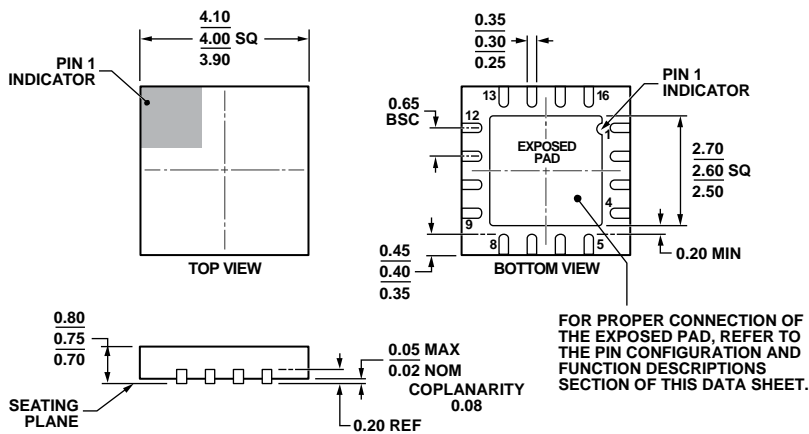
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ] 4 mm x 4 mm Body, Very Very Thin Quad (CP-16-17)

Dimensions shown in millimeters

08-16-2010-C

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
ADG5236BRUZ	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5236BRUZ-RL7	-40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG5236BCPZ-RL7	-40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-16-17

¹ Z = RoHS Compliant Part.

NOTES