# 0.5 Ω $R_{ON}$, ±20 V, +36 V, Dual SPDT Switch

## FEATURES

- Low $R_{ON}$: 0.5 Ω
- High continuous current of up to 847 mA
- Flat $R_{ON}$ across signal range: 0.003 Ω
- THD of −109 dB at 1 kHz
- Improved balance between on resistance and on capacitance
  - Low $R_{ON}$ (0.5 Ω) and $C_{ON}$ (95 pF)
- 1.8 V, 3.3 V, and 5 V logic compatibility
- 16-lead, 4 mm × 4 mm LFCSP
  - Pin to pin compatible with the ADG5436 and ADG5436F
- Fully specified at ±20 V and +36 V
- Operational with asymmetric power supplies
- $V_{SS}$ to $V_{DD}$ − 2 V analog signal range

## APPLICATIONS

- Automatic test equipment
- Data acquisition
- Instrumentation
- Avionics
- Audio and video switching
- Communication systems
- Relay replacement

## GENERAL DESCRIPTION

The ADG6436 is an analog multiplexer containing two independently selectable single-pole, double throw (SPDT) switches. An EN input is used to disable all of the switches. For use in multiplexer applications, both switches exhibit break-before-make switching action.

Each channel conducts equally well in both directions when on, and each switch has an input signal range that extends from $V_{SS}$ to $V_{DD}$ − 2 V. When switches are disabled, the signal levels up to the supplies are blocked.

The digital inputs are compatible with 5 V, 3.3 V, and 1.8 V logic inputs without the requirement for a separate digital logic supply pin.

The on-resistance profile is exceptionally flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals.

## FUNCTIONAL BLOCK DIAGRAM

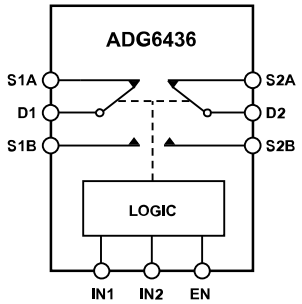


*Figure 1. Functional Block Diagram*

## PRODUCT HIGHLIGHTS

1. Low $R_{ON}$ of 0.5 Ω.
2. High continuous current carrying capability, see Table 4 to Table 5.
3. Dual-supply operation. For applications where the analog signal is bipolar, the ADG6436 can be operated from dual supplies up to ±22 V.
4. Single-supply operation. For applications where the analog signal is unipolar, the ADG6436 can be operated from a single rail power supply up to 40 V.
5. 1.8 V logic compatible digital inputs: $V_{INH}$ = 1.3 V, $V_{INL}$ = 0.8 V.
6. No $V_L$ logic power supply required.

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## REVISION HISTORY

**7/2024—Revision 0: Initial Version**

# SPECIFICATIONS

## OPERATING SUPPLY VOLTAGES

*Table 1. Operating Supply Voltages*

| Supply Voltage | Min | Max | Unit |
|---|---|---|---|
| Dual Supply | ±4.5 | ±22 | V |
| Single Supply | +5 | +40 | V |

## ±20 V DUAL SUPPLY

$V_{DD}$ = +20 V ± 10%, $V_{SS}$ = −20 V ± 10%, and GND = 0 V, unless otherwise noted.

*Table 2. ±20 V Dual-Supply Specifications*

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | $V_{DD}$ = +18 V and $V_{SS}$ = −18 V |
| Analog Signal Range | | | $V_{DD}$ − 2 V to $V_{SS}$ | V | |
| On Resistance ($R_{ON}$) | 0.50 | | | Ω typ | Source voltage ($V_S$) = −18 V to +14.5 V and source current ($I_S$) = −100 mA (see Figure 25) |
| | 0.65 | 0.8 | 0.95 | Ω max | |
| | 0.54 | | | Ω typ | $V_S$ = −18 V to +15.5 V and $I_S$ = −100 mA |
| | 0.7 | 0.85 | 1.0 | Ω max | |
| On-Resistance Match Between Channels ($\Delta R_{ON}$) | 0.003 | | | Ω typ | $V_S$ = −18 V to +15.5 V and $I_S$ = −100 mA |
| | 0.085 | 0.1 | 0.1 | Ω max | |
| On-Resistance Flatness ($R_{FLAT (ON)}$) | 0.003 | | | Ω typ | $V_S$ = −18 V to +14.5 V and $I_S$ = −100 mA |
| | 0.035 | 0.035 | 0.035 | Ω max | |
| | 0.04 | | | Ω typ | $V_S$ = −18 V to +15.5 V and $I_S$ = −100 mA |
| | 0.08 | 0.1 | 0.1 | Ω max | |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = +22 V and $V_{SS}$ = −22 V |
| Source Off Leakage ($I_S$ (Off)) | ±5 | | | nA typ | $V_S$ = ±15 V and drain current ($V_D$) = ±15 V (see Figure 28) |
| | ±12.5 | +90/−14 | +400/−14 | nA max | |
| Drain Off Leakage ($I_D$ (Off)) | ±10 | | | nA typ | $V_S$ = ±15 V and $V_D$ = ±15 V (see Figure 28) |
| | ±25 | +175/−28 | +792/−28 | nA max | |
| Channel On Leakage ($I_D$ (On)) and ($I_S$ (On)) | ±4.7 | | | nA typ | $V_S$ = $V_D$ = ±15 V (see Figure 24) |
| | ±13.8 | +91/−17.0 | +428/−17 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage ($V_{INH}$) | | | 1.3 | V min | |
| Input Low Voltage ($V_{INL}$) | | | 0.8 | V max | |
| Input Current ($I_{INL}$) or ($I_{INH}$) | 0.01 | | | μA typ | Input voltage ($V_{IN}$) = GND voltage ($V_{GND}$) or 5 V |
| | | | ±0.15 | μA max | |
| Digital Input Capacitance ($C_{IN}$) | 4.6 | | | pF typ | |
| DYNAMIC CHARACTERISTICS | | | | | |
| Transition Time ($t_{TRANSITION}$) | 343 | | | ns typ | Load resistance ($R_L$) = 300 Ω, load capacitance ($C_L$) = 35 pF |
| | 415 | 455 | 499 | ns max | $V_S$ = 10 V (see Figure 34) |
| On Time ($t_{ON(EN)}$) | 333 | | | ns typ | Load resistance ($R_L$) = 300 Ω, load capacitance ($C_L$) = 35 pF |
| | 397 | 438 | 484 | ns max | $V_S$ = 10 V (see Figure 22) |
| Off Time ($t_{OFF(EN)}$) | 193 | | | ns typ | $R_L$ = 300 Ω and $C_L$ = 35 pF |

## SPECIFICATIONS

*Table 2. ±20 V Dual-Supply Specifications (Continued)*

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| | 224 | 228 | 229 | ns max | $V_S$ = 10 V (see Figure 22) |
| Break-Before-Make Time Delay ($t_D$) | 219 | | | ns typ | $R_L$ = 300 Ω and $C_L$ = 35 pF |
| | 170 | 202 | 243 | ns min | $V_S$ = 10 V (see Figure 32) |
| Charge Injection ($Q_{INJ}$) | −2.1 | | | nC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, and $C_L$ = 1 nF (see Figure 35) |
| Off Isolation | −77.9 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and frequency = 100 kHz (see Figure 27) |
| Channel-to-Channel Crosstalk | −84 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and frequency = 100 kHz (see Figure 26) |
| Total Harmonic Distortion + Noise (THD + N) | 0.007 | | | % typ | $R_L$ = 1 kΩ, 20 V p-p, and frequency = 20 Hz to 20 kHz (see Figure 30) |
| Total Harmonic Distortion (THD) | −109 | | | dB typ | $R_L$ = 1 kΩ, 20 V p-p, and frequency = 1 kHz |
| | −83 | | | dB typ | $R_L$ = 1 kΩ, 20 V p-p, and frequency = 20 kHz |
| | −69 | | | dB typ | $R_L$ = 1 kΩ, 20 V p-p, and frequency = 100 kHz |
| −3 dB Bandwidth | 84 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and signal = 0 dBm (see Figure 31) |
| Insertion Loss | −0.06 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and frequency= 1 MHz (see Figure 31) |
| Source Off Capacitance ($C_S$ (Off)) | 67 | | | pF typ | $V_S$ = 0 V and frequency = 1 MHz |
| Drain Off Capacitance ($C_D$ (Off)) | 134 | | | pF typ | $V_S$ = 0 V and frequency = 1 MHz |
| Drain On Capacitance ($C_D$ (On)) and Source On Capacitance ($C_S$ (On)) | 91 | | | pF typ | $V_S$ = 0 V and frequency = 1 MHz |
| Match On Capacitance ($C_{MATCH}$(On)) | 0.39 | | | pF typ | $V_S$ = 0 V and frequency = 1 MHz |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = +22 V and $V_{SS}$ = −22 V |
| Power Supply Current ($I_{DD}$) | 170 | | | µA typ | Digital inputs = 0 V or 5 V |
| | 260 | | 260 | µA max | |
| | 225 | | | µA typ | Digital inputs = 1.3 V |
| | 330 | | 330 | µA max | |
| Negative Supply Current ($I_{SS}$) | 85 | | | µA typ | Digital inputs = 0 V or 5 V |
| | 140 | | 140 | µA max | |

## 36 V SINGLE SUPPLY

$V_{DD}$ = 36 V ± 10%, $V_{SS}$ = 0 V, and GND = 0 V, unless otherwise noted.

*Table 3. 36 V Single-Supply Specifications*

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | $V_{DD}$ = 32.4 V and $V_{SS}$ = 0 V |
| Analog Signal Range | | | 0 V to $V_{DD}$ − 2 V | V | |
| On Resistance ($R_{ON}$) | 0.50 | | | Ω typ | Source voltage ($V_S$) = 0 V to 28.9 V and source current ($I_S$) = −100 mA (see Figure 25) |
| | 0.65 | 0.8 | 0.95 | Ω max | |
| | 0.54 | | | Ω typ | $V_S$ = 0 V to 29.9 V and $I_S$ = −100 mA |
| | 0.7 | 0.85 | 1.0 | Ω max | |
| On-Resistance Match Between Channels ($\Delta R_{ON}$) | 0.003 | | | Ω typ | $V_S$ = 0 V to 29.9 V and $I_S$ = −100 mA |

## SPECIFICATIONS

*Table 3. 36 V Single-Supply Specifications (Continued)*

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| | 0.085 | 0.1 | 0.1 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.003 | | | Ω typ | $V_S$ = 0 V to 28.9 V and $I_S$ = −100 mA |
| | 0.035 | 0.035 | 0.035 | Ω max | |
| | 0.04 | | | Ω typ | $V_S$ = 0 V to 29.9 V and $I_S$ = −100 mA |
| | 0.08 | 0.1 | 0.1 | Ω max | |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 39.6 V and $V_{SS}$ = 0 V |
| Source Off Leakage ($I_S$ (Off)) | ±5 | | | nA typ | $V_S$ = 1 V/30 V and drain voltage ($V_D$) = 30 V/1 V (see Figure 28) |
| | ±12.5 | +90/−14 | +400/−14 | nA max | |
| Drain Off Leakage ($I_D$ (Off)) | ±10 | | | nA typ | $V_S$ = 1 V/30 V and $V_D$ = 30 V/1 V (see Figure 28) |
| | ±25 | +175/−28 | +792/−28 | nA max | |
| Channel On Leakage ($I_D$ (On)) and ($I_S$ (On)) | ±4.7 | | | nA typ | $V_S$ = $V_D$ = 1 V/30 V (see Figure 24) |
| | ±13.8 | +91/−17 | +428/−17 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage ($V_{INH}$) | | | 1.3 | V min | |
| Input Low Voltage ($V_{INL}$) | | | 0.8 | V max | |
| Input Current ($I_{INL}$) or ($I_{INH}$) | 0.01 | | | μA typ | Input voltage ($V_{IN}$) = GND voltage ($V_{GND}$) or 5 V |
| | | | ±0.15 | μA max | |
| Digital Input Capacitance ($C_{IN}$) | 4.6 | | | pF typ | |
| DYNAMIC CHARACTERISTICS | | | | | |
| Transition Time ($t_{TRANSITION}$) | 356 | | | | Load resistance ($R_L$) = 300 Ω and loa)d capacitance ($C_L$) = 35 pF |
| | 431 | 442 | 460 | | $V_S$ = 18 V (see Figure 34) |
| On Time ($t_{ON(EN)}$) | 202 | | | ns typ | Load resistance ($R_L$) = 300 Ω and loa)d capacitance ($C_L$) = 35 pF |
| | 240 | 261 | 288 | ns max | $V_S$ = 18 V (see Figure 22 |
| Off Time ($t_{OFF(EN)}$) | 309 | | | ns typ | $R_L$ = 300 Ω and $C_L$ = 35 pF |
| | 359 | 367 | 374 | ns max | $V_S$ = 18 V (see Figure 22) |
| Break-Before-Make Time Delay ($t_D$) | 88 | | | ns typ | $R_L$ = 300 Ω and $C_L$ = 35 pF |
| | 92.5 | 109.2 | 130.2 | ns min | $V_S$ = 18 V (see Figure 32) |
| Charge Injection ($Q_{INJ}$ ) | −1.79 | | | nC typ | $V_S$ = 18 V, $R_S$ = 0 Ω, and $C_L$ = 1 nF (see Figure 35) |
| Off Isolation | −64 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and frequency = 100 kHz (see Figure 27) |
| Channel-to-Channel Crosstalk | −70 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and frequency = 100 kHz (see Figure 26) |
| Total Harmonic Distortion + Noise (THD + N) | 0.006 | | | % typ | $R_L$ = 1 kΩ, 18 V p-p, and frequency = 20 Hz to 20 kHz (see Figure 30) |
| Total Harmonic Distortion (THD) | −107 | | | dB typ | $R_L$ = 1 kΩ, 18 V p-p, and frequency = 1 kHz |
| | −84 | | | dB typ | $R_L$ = 1 kΩ, 18 V p-p, and frequency = 20 kHz |
| | −70 | | | dB typ | $R_L$ = 1 kΩ, 18 V p-p, and frequency = 100 kHz |

## SPECIFICATIONS

*Table 3. 36 V Single-Supply Specifications (Continued)*

| Parameter | +25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| −3 dB Bandwidth | 81 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and signal = 0 dBm (see Figure 31) |
| Insertion Loss | −0.06 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, and frequency = 1 MHz (see Figure 31) |
| Source Off Capacitance ($C_S$ (Off)) | 69 | | | pF typ | $V_S$ = 18 V and frequency = 1 MHz |
| Drain Off Capacitance ($C_D$ (Off)) | 139 | | | pF typ | $V_S$ = 18 V and frequency = 1 MHz |
| Drain On Capacitance ($C_D$ (On)) and Source On Capacitance ($C_S$ (On)) | 95 | | | pF typ | $V_S$ = 18 V and frequency = 1 MHz |
| Match On Capacitance ($C_{MATCH}$(On)) | 0.24 | | | pF typ | $V_S$ = 18 V and frequency = 1 MHz |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 39.6 V |
| Power Supply Current ($I_{DD}$) | 170 | | | µA typ | Digital inputs = 0 V or 5 V |
| | 260 | | 260 | µA max | |
| | 225 | | | µA typ | Digital inputs = 1.3 V |
| | 330 | | 330 | µA max | |
| Negative Supply Current ($I_{SS}$) | 85 | | | µA typ | Digital inputs = 0 V or 5 V |
| | 140 | | 140 | µA max | |

## SPECIFICATIONS

### CONTINUOUS CURRENT PER CHANNEL, SX OR DX

*Table 4. One Channel On, Per Channel Specifications*

| Parameter | 25°C | 85°C | 125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| CONTINUOUS CURRENT, Sx OR Dx | | | | | |
| $V_{DD}$ = +20 V and $V_{SS}$ = −20 V | | | | | |
| LFCSP ($\theta_{JA}$ = 44°C/W) | 847 | 325 | 123 | mA maximum | $V_S$ = $V_{SS}$ to $V_{DD}$ − 3.5 V |
| $V_{DD}$ = 36 V and $V_{SS}$ = 0 V | | | | | |
| LFCSP ($\theta_{JA}$ = 44°C/W) | 847 | 325 | 123 | mA maximum | $V_S$ = $V_{SS}$ to $V_{DD}$ − 3.5 V |

*Table 5. Two Channels On, Per Channel Specifications*

| Parameter | 25°C | 85°C | 125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| CONTINUOUS CURRENT, Sx OR Dx | | | | | |
| $V_{DD}$ = +20 V and $V_{SS}$ = −20 V | | | | | |
| LFCSP ($\theta_{JA}$ = 44°C/W) | 646 | 289 | 120 | mA maximum | $V_S$ = $V_{SS}$ to $V_{DD}$ − 3.5 V |
| $V_{DD}$ = 36 V and $V_{SS}$ = 0 V | | | | | |
| LFCSP ($\theta_{JA}$ = 44°C/W) | 646 | 289 | 120 | mA maximum | $V_S$ = $V_{SS}$ to $V_{DD}$ − 3.5 V |

## ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

*Table 6. Absolute Maximum Ratings*

| Parameter | Rating |
|---|---|
| $V_{DD}$ to $V_{SS}$ | 46 V |
| $V_{DD}$ to GND | −0.3 V to +46 V |
| $V_{SS}$ to GND | +0.3 V to −46 V |
| Analog Inputs[1] | $V_{SS}$ − 0.3 V to $V_{DD}$ + 0.3 V or 30 mA, whichever occurs first |
| Digital Inputs[1] | GND − 0.3 V to +6 V or 30 mA, whichever occurs first |
| Peak Current, Sx or Dx Pins[2] | 2.6 A (pulsed at 1 ms and 10% duty cycle maximum) |
| Continuous Current, Sx or Dx[2] | Data (see Table 4 to Table 5) + 15% |
| Temperature | |
| Operating Range | −40°C to +125°C |
| Storage Range | −65°C to +150°C |
| Junction | 150°C |
| Reflow Soldering Peak, Pb-Free | As per JEDEC J-STD-020 |

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

[2] Sx refers to the S1A, S1B, S2A, and S2B pins, and Dx refers to the D1 and D2 pins.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

## THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

$\theta_{JA}$ is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and $\theta_{JCB}$ is the junction to the bottom of the case value.

*Table 7. Thermal Resistance*

| Package Type | $\theta_{JA}$ | $\theta_{JCB}$ | Unit |
|---|---|---|---|
| CP-16-17[1] | 44 | 17.4 | °C/W |

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board without thermal vias. See JEDEC JESD-51.

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

### ESD Ratings for the ADG6436

*Table 8. ADG6436, 16-Lead LFCSP*

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | ±4000 | 3A |
| FICDM | ±1250 | C3 |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

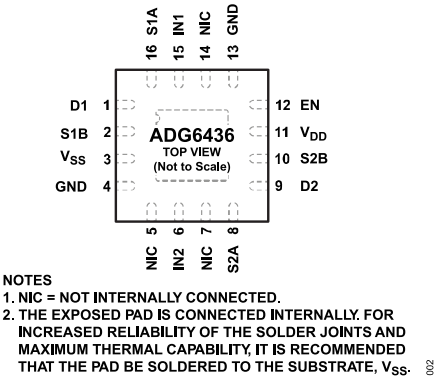


*Figure 2. Pin Configuration*

*Table 9. Pin Function Descriptions*

| Pin Number | Mnemonic | Description |
|---|---|---|
| 1 | D1 | Drain Terminal 1. The D1 pin can be an input or output. |
| 2 | S1B | Source Terminal 1B. The S1B pin can be an input or output. |
| 3 | $V_{SS}$ | Most Negative Power Supply Voltage. |
| 4, 13 | GND | Ground (0 V) Reference. |
| 5, 7, 14 | NIC | Not Internally Connected. |
| 6 | IN2 | Logic Control Input 2. |
| 8 | S2A | Source Terminal 2A. The S2A pin can be an input or output. |
| 9 | D2 | Drain Terminal 2. The D2 pin can be an input or output. |
| 10 | S2B | Source Terminal 2B. The S2B pin can be an input or output. |
| 11 | $V_{DD}$ | Most Positive Power Supply. |
| 12 | EN | Active High Digital Input. When the EN pin is low, the device is disabled, and all switches are off. When the EN pin is high, INx logic inputs determine the on switches. |
| 15 | IN1 | Logic Control Input 1. |
| 16 | S1A | Source Terminal 1A. The S1A pin can be an input or output. |
| | EP | Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, $V_{SS}$. |

*Table 10. ADG6436 Truth Table*

| EN | INx | SxA | SxB |
|---|---|---|---|
| 0 | X[1] | Off | Off |
| 1 | 0 | Off | On |
| 1 | 1 | On | Off |

[1] X is don't care.

## TYPICAL PERFORMANCE CHARACTERISTICS

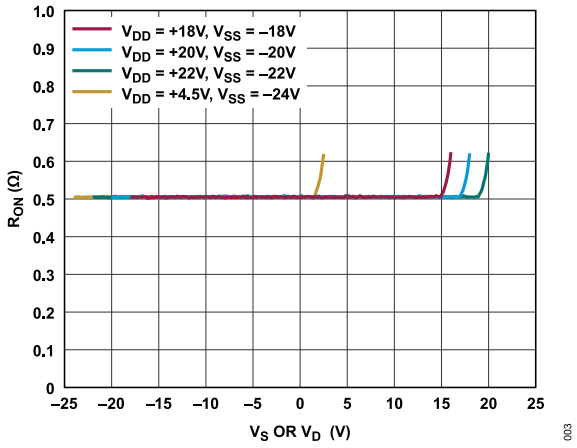


*Figure 3. $R_{ON}$ as a Function of $V_S$, $V_D$ (Dual Supply)*

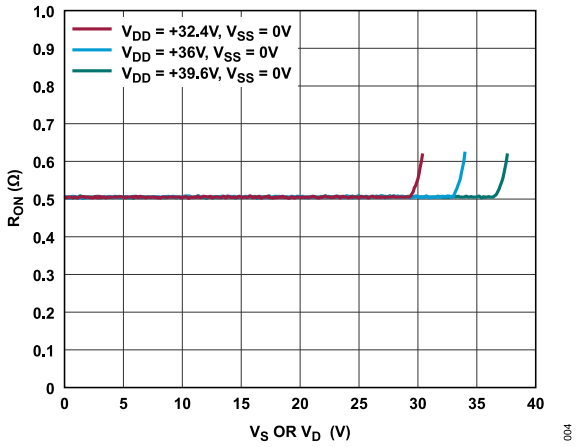


*Figure 4. $R_{ON}$ as a Function of $V_S$, $V_D$ (Single Supply)*

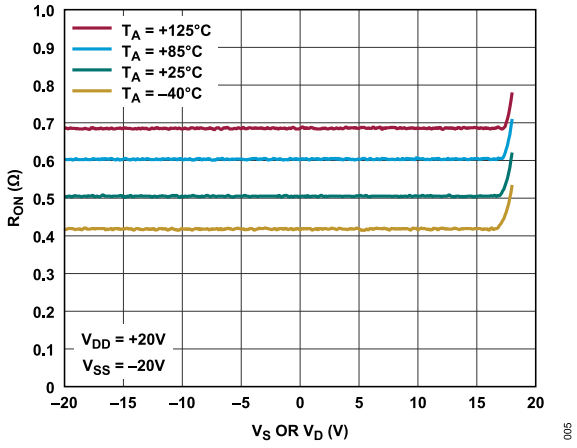


*Figure 5. $R_{ON}$ as a Function of $V_S$ ($V_D$) for Different Temperatures, ±20 V Dual Supply*

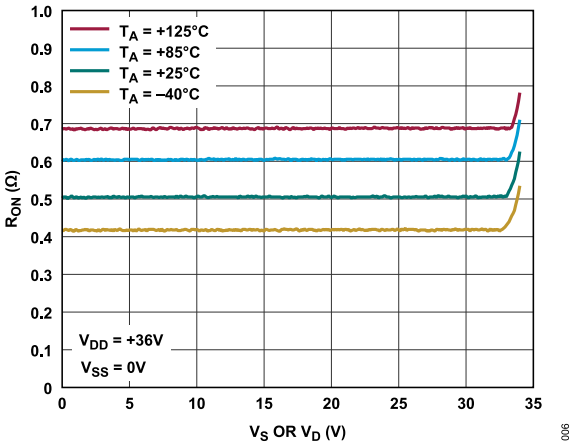


*Figure 6. $R_{ON}$ as a Function of $V_S$ ($V_D$) for Different Temperatures, 36 V Single Supply*

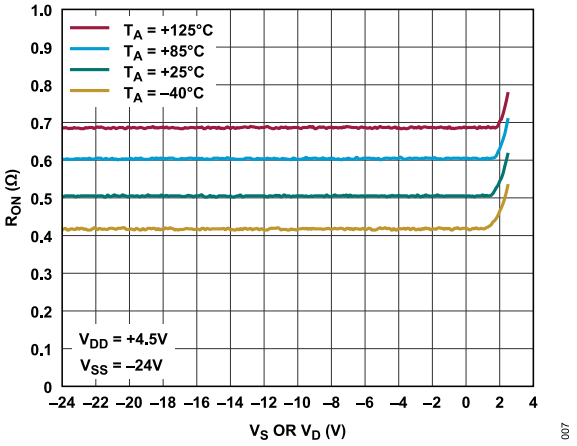


*Figure 7. $R_{ON}$ as a Function of $V_S$ ($V_D$) for Different Temperatures, Asymmetric Single Supply*

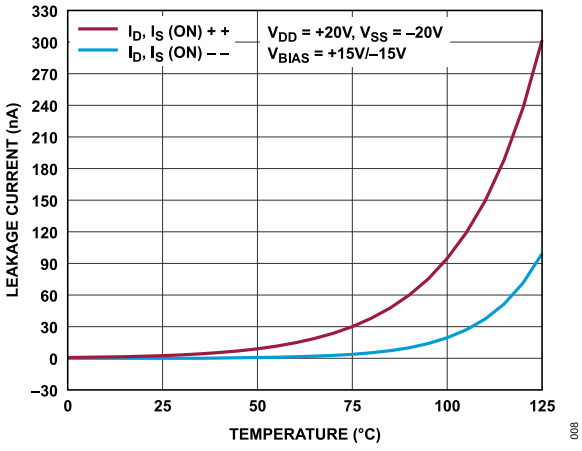


*Figure 8. On Leakage Currents vs. Temperature, ±20 V Dual Supply*

## TYPICAL PERFORMANCE CHARACTERISTICS

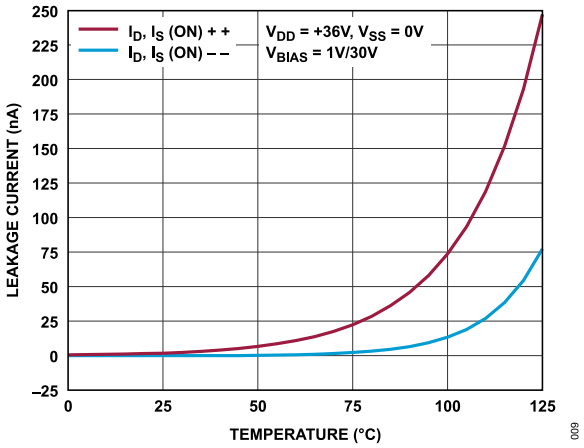


Figure 9. On Leakage Currents vs. Temperature, +36 V Single Supply

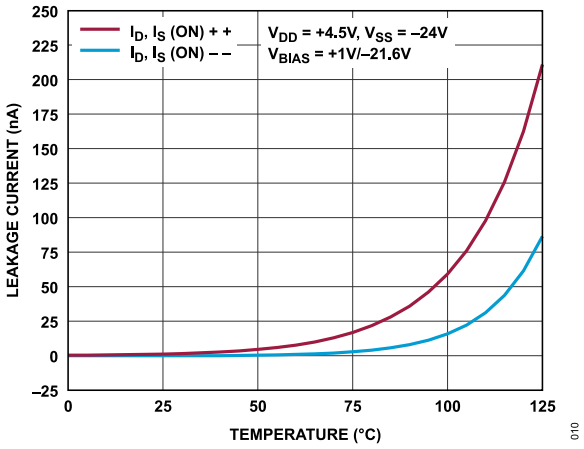


Figure 10. On Leakage Currents vs. Temperature, +4.5 V, −24 V Dual Supply

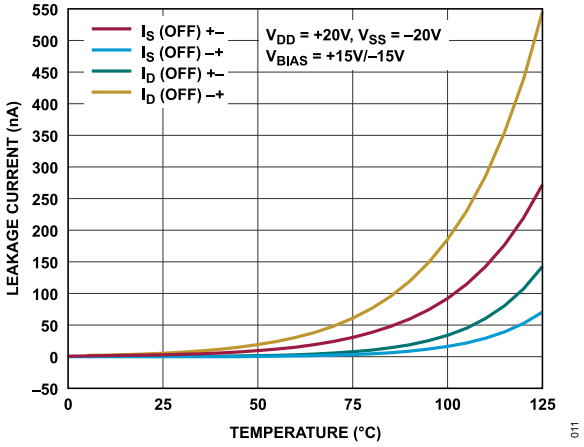


Figure 11. Off Leakage Currents vs. Temperature, ±20 V Dual Supply

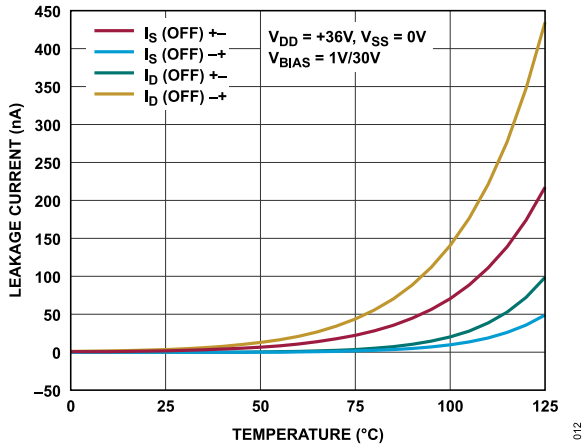


Figure 12. Off Leakage Currents vs. Temperature, +36 V Single Supply

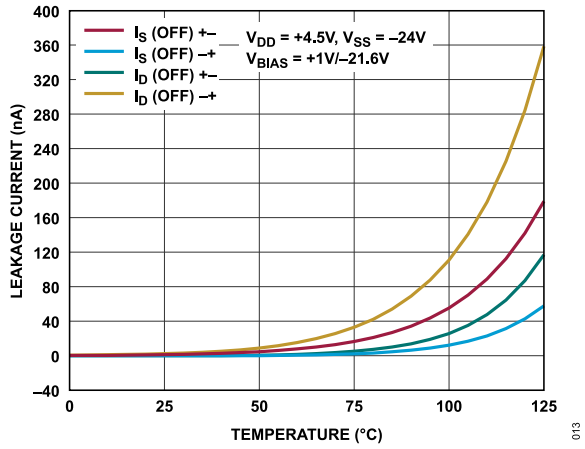


Figure 13. Off Leakage Currents vs. Temperature, +4.5 V, −24 V Dual Supply

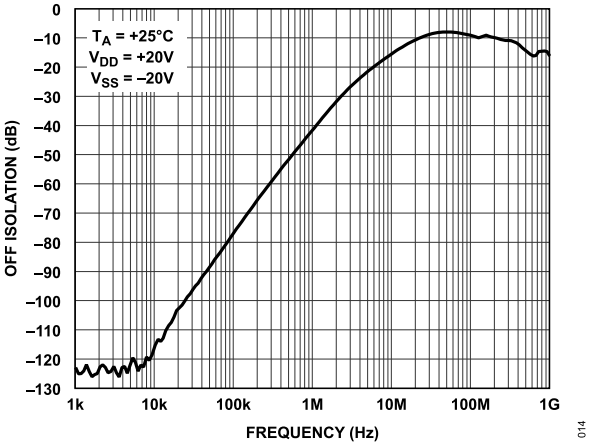


Figure 14. Off Isolation vs. Frequency, ±20 V Dual Supply

## TYPICAL PERFORMANCE CHARACTERISTICS

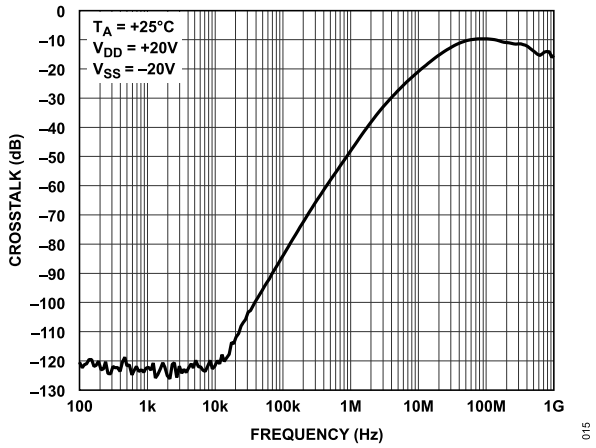


*Figure 15. Crosstalk vs. Frequency, ±20 V Dual Supply*

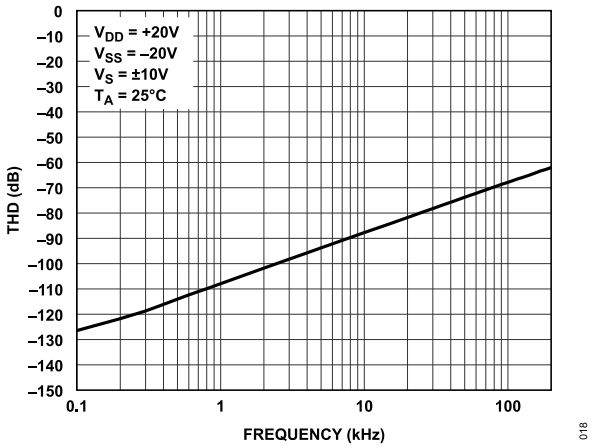


*Figure 18. THD vs. Frequency, ±20 V Dual Supply*

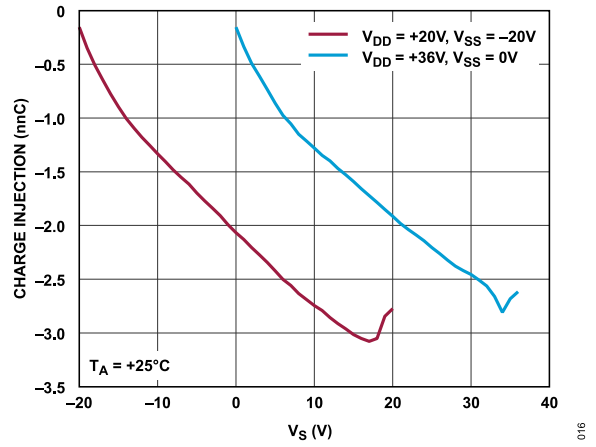


*Figure 16. Charge Injection vs. $V_S$*

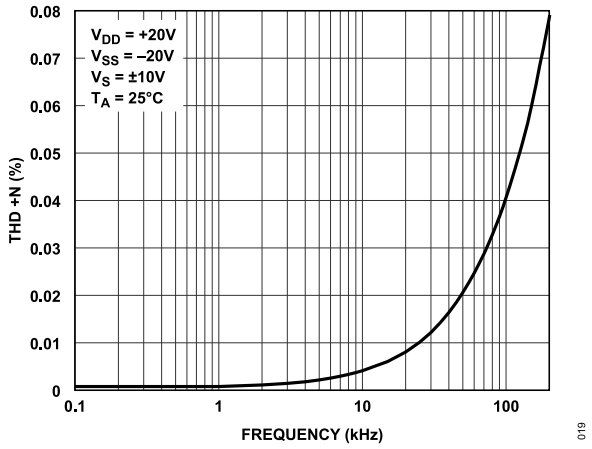


*Figure 19. THD + N vs. Frequency, ±20 V Dual Supply*

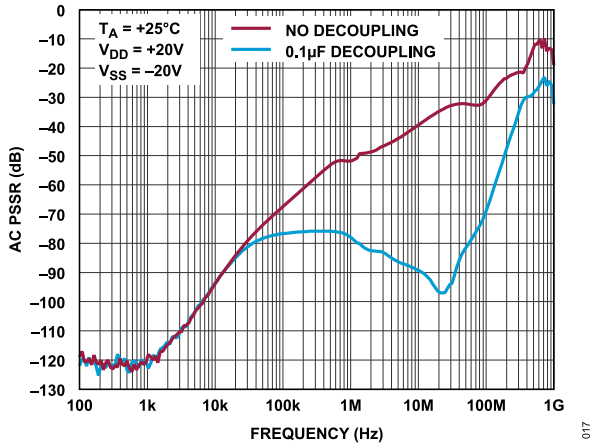


*Figure 17. AC Power Supply Rejection Ratio (PSRR) vs. Frequency, ±20 V Dual Supply*

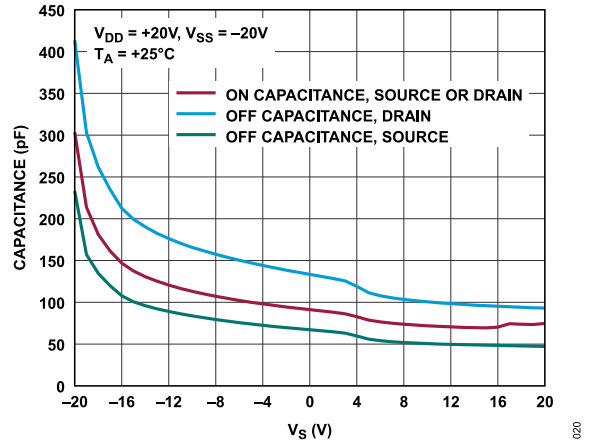


*Figure 20. Capacitance vs. $V_S$, ±20 V Dual Supply*

## TYPICAL PERFORMANCE CHARACTERISTICS

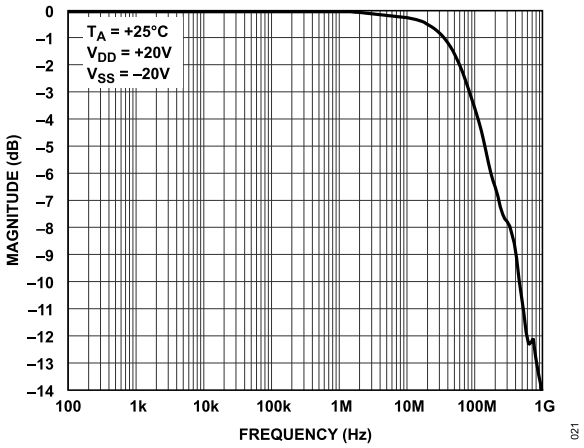


*Figure 21. Insertion Loss vs. Frequency*

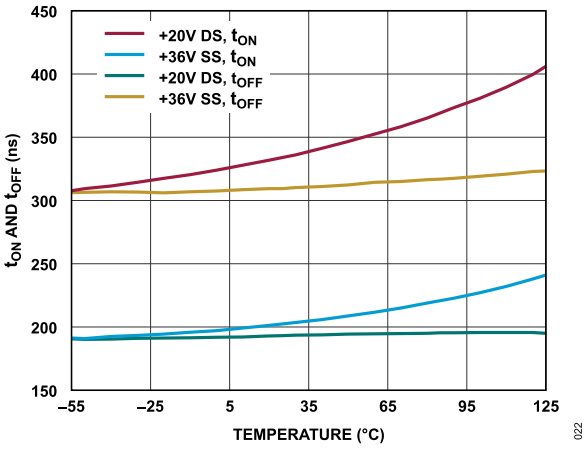


*Figure 22. $t_{ON}$, $t_{OFF}$ Times vs. Temperature*

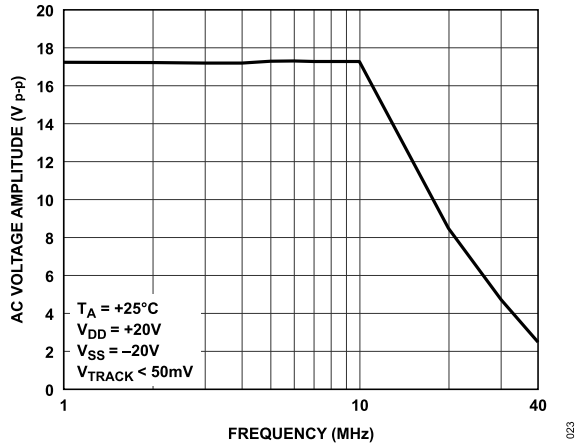


*Figure 23. Large AC Signal Voltage vs. Frequency*

## TEST CIRCUITS

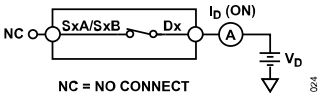


*Figure 24. On Leakage*

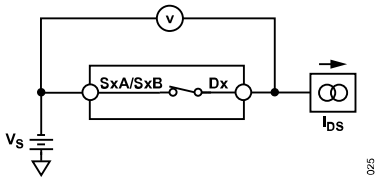


*Figure 25. On Resistance*

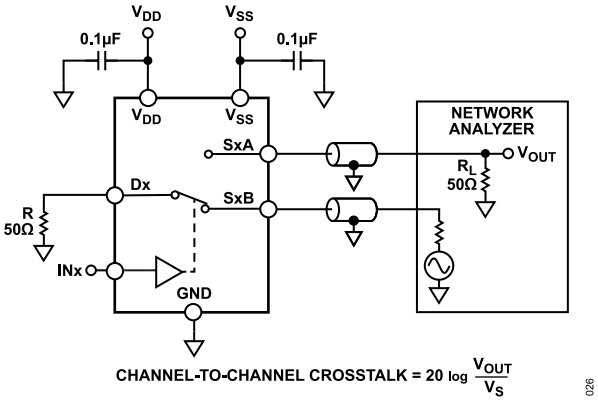


*Figure 26. Channel-to-Channel Crosstalk*

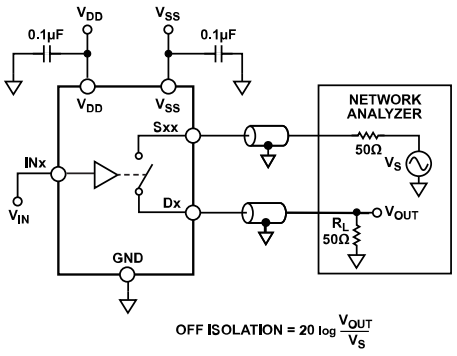


*Figure 27. Off Isolation*

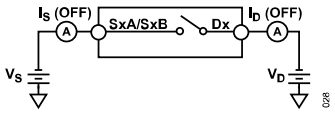


*Figure 28. Off Leakage*

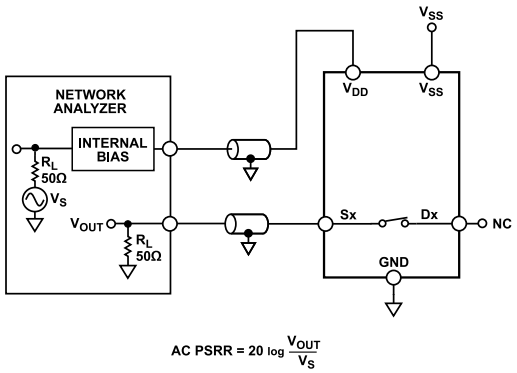


*Figure 29. AC PSRR*

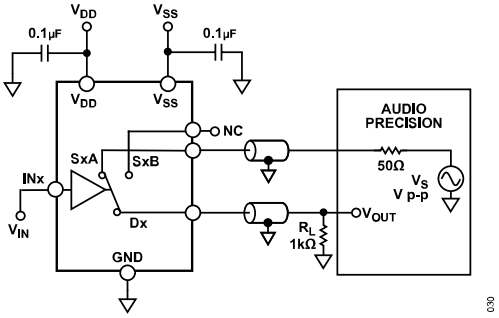


*Figure 30. THD + Noise*

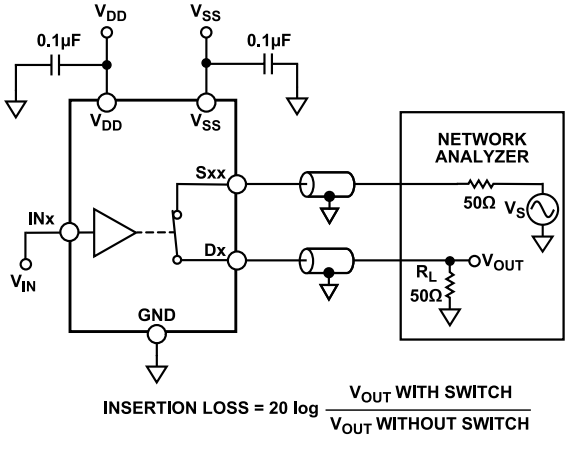


*Figure 31. Bandwidth*

## TEST CIRCUITS

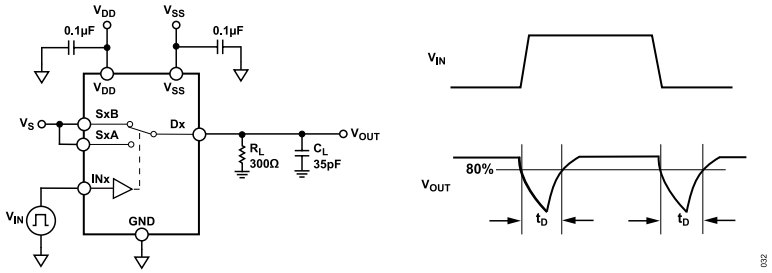


*Figure 32. Break-Before-Make Time Delay, $t_D$*

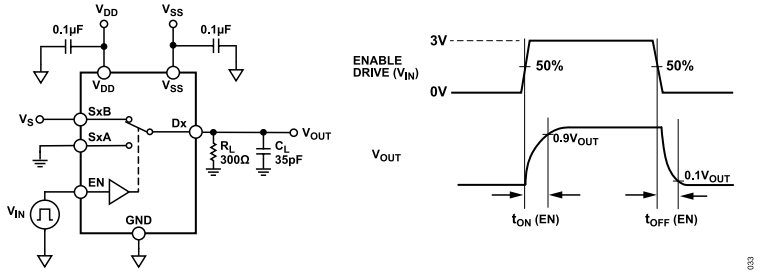


*Figure 33. Enable Delay, $t_{ON}(EN)$, $t_{OFF}(EN)$*

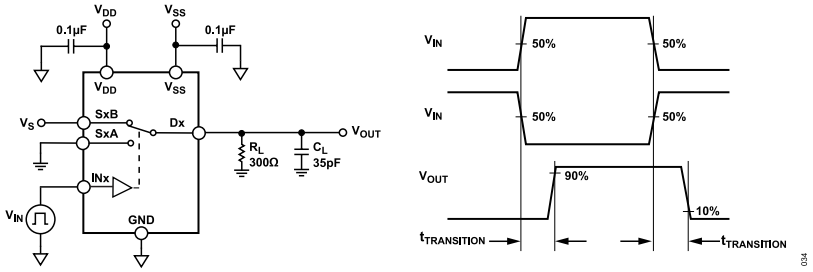


*Figure 34. Switching Times*

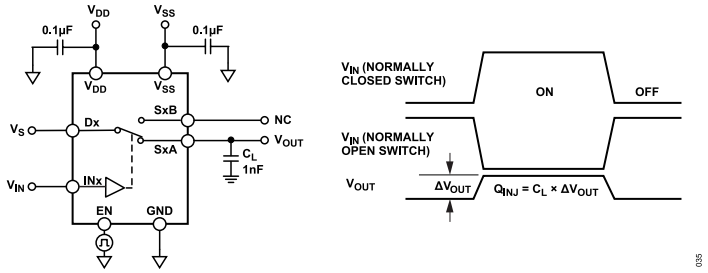


*Figure 35. Charge Injection*

## TERMINOLOGY

### $I_{DD}$

The positive supply current.

### $I_{SS}$

The negative supply current.

### $V_D$ and $V_S$

The analog voltage on Terminal D and Terminal S, respectively.

### $V_{TRACK}$

The difference between $V_S$ and $V_D$.

### $R_{ON}$

The ohmic resistance between Terminal D and Terminal S.

### $\Delta R_{ON}$

The difference between the $R_{ON}$ of any two channels.

### $R_{FLAT(ON)}$

The difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

### $I_S$ (Off)

The source leakage current with the switch off.

### $I_D$ (Off)

The drain leakage current with the switch off.

### $I_D$ (On) and $I_S$ (On)

The channel leakage current with the switch on.

### $V_{INL}$

The maximum input voltage for Logic 0.

### $V_{INH}$

The minimum input voltage for Logic 1.

### $I_{INL}$ and $I_{INH}$

The input current of the digital input when high or when low.

### $C_S$ (Off) and $C_D$ (Off)

The off switch source and drain capacitance for the off condition, which is measured with reference to ground.

### $C_D$ (On) and $C_S$ (On)

The on switch drain and source capacitance for the on condition, which is measured with reference to ground.

### $C_{IN}$

The digital input capacitance.

### $t_{ON}$

The delay between applying the digital control input and the output switching on.

### $t_{OFF}$

The delay between applying the digital control input and the output switching off.

### $t_D$

The off-time measured between the 80% point of both switches when switching from one address state to another.

### Off Isolation

A measure of unwanted signal coupling through an off switch.

### Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

### Channel-to-Channel Crosstalk

A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### Bandwidth

The frequency at which the output is attenuated by 3 dB.

### On Response

The frequency response of the on switch.

### Insertion Loss

The loss due to the on resistance of the switch.

### Total Harmonic Distortion + Noise (THD + N)

The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

### AC Power Supply Rejection Ratio (AC PSRR)

The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The DC voltage on the device is modulated by a sine wave of 0.62 V p-p.

## THEORY OF OPERATIONS

### SWITCH ARCHITECTURE

The ADG6436 contains two independently selectable SPDT, N-channel diffused metal-oxide semiconductor (NDMOS) switches that allow for excellent $R_{ON}$ performance. Using an NDMOS only architecture results in a reduction of signal headroom, meaning signals are limited to $V_{DD}$ − 2 V. To achieve the lowest on resistance, on-resistance flatness, and total harmonic distortion, it is recommended the signal stays below $V_{DD}$ − 3.5 V.

To guarantee correct operation of the ADG6436, a minimum of 0.1 µF decoupling capacitors are required on both the $V_{DD}$ and $V_{SS}$ supply pins.

The ADG6436 is compatible with single-supply systems that have a $V_{DD}$ of up to 40 V, dual-supply systems of up to ± 22 V, as well as asymmetric power supplies.

### 1.8 V LOGIC COMPATIBILITY

For ease of use, the ADG6436 does not have a logic reference voltage ($V_L$). The digital inputs are compatible with 1.8 V logic levels over the full operating supply range. The limits for 1.8 V logic are as follows: $V_{INH}$ = 1.3 V and $V_{INL}$ = 0.8 V. The 1.8 V logic level inputs enable the ADG6436 to be compatible with processors that have lower supply rails, eliminating the need for an external voltage translator.

If full 1.8 V and 1.2 V JEDEC compliance is required, refer to the Analog Devices, Inc., L-range part numbers, such as the ADG1412L.

## APPLICATIONS INFORMATION

### LARGE VOLTAGE, HIGH FREQUENCY SIGNAL TRACKING

Figure 23 shows the voltage range and corresponding frequencies that the ADG6436 can reliably convey. The tracking voltage ($V_{TRACK}$) in the figure shows the source voltage and the drain voltage difference, which is less than 50 mV for a given amplitude and frequency. For large voltage, high frequency signals, the frequency must be kept below 10 MHz. If the required frequency is greater than 10 MHz, decrease the signal range appropriately to ensure signal integrity.

### POWER SUPPLY RECOMMENDATIONS

Analog Devices has a wide range of power management products to meet the requirements of high performance signal chains.

An example of a bipolar power solution is shown in Figure 36. The LT3463 (a dual switching regulator) generates a positive and negative supply rail for the ADG6436, an amplifier, and/or a precision converter in a typical signal chain. Also, two optional low-dropout regulators (LDOs), the ADP7142 and ADP7182 (positive and negative LDOs, respectively) are shown in Figure 36, which can reduce the output ripple of the LT3463 in ultra-low noise sensitive applications.

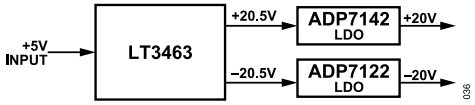


*Figure 36. Bipolar Power Solution*

*Table 11. Recommended Power Management Devices*

| Product | Description |
|---|---|
| LT3463 | Dual micropower, DC to DC converter with Schottky diodes |
| ADP7142 | 40 V, 200 mA, low noise, CMOS, LDO linear regulator |
| ADP7182 | −28 V, −200 mA, low noise, LDO linear regulator |

### DATA ACQUISITION CALIBRATION

Figure 37 shows an example application for the ADG6436. In automated test equipment (ATE) and instrumentation applications, when using data acquisition (DAQ) systems, there is a requirement for precision and accuracy. Many factors, such as drift over time and temperature, may cause the system to lose this accuracy. The low on resistance and charge injection of the ADG6436 is ideally suited to calibrate this system in real time before taking a measurement, thus, reducing error. The break-before-make feature of the ADG6436 allows the system to switch the calibration path without shorting the inputs together.

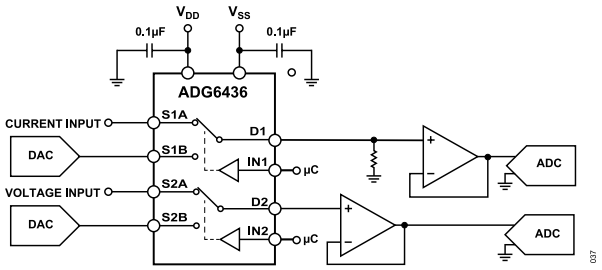


*Figure 37. DAQ Calibration Application*

## OUTLINE DIMENSIONS

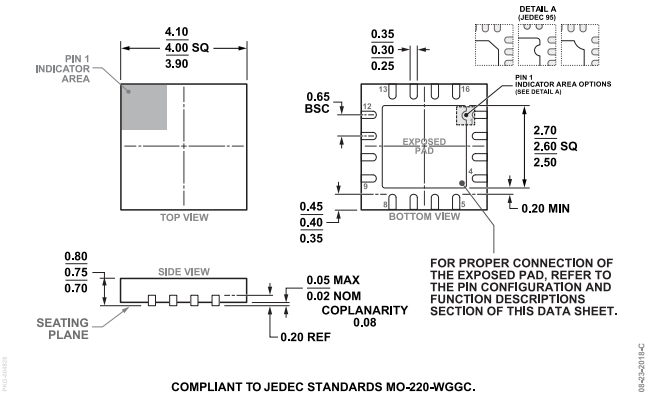


*Figure 38. 16-Lead Lead Frame Chip Scale Package [LFCSP]*
*4 mm × 4 mm Body and 0.75 mm Package Height*
*(CP-16-17)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| ADG6436BCPZ-REEL7 | −40°C to +125°C | 16-Lead LFCSP | Reel, 1500 | CP-16-17 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

*Table 12. Evaluation Boards*

| Model[1] | Description |
|---|---|
| EVAL-ADG6436EBZ | Evaluation Board |

[1] Z = RoHS Compliant Part.