



CMOS Low Power Dual 2:1 Mux/Demux USB 2.0 (480 Mbps)/USB 1.1 (12 Mbps)

ADG772

FEATURES

USB 2.0 (480 Mbps) and USB 1.1 (12 Mbps) signal switching compliant
Tiny 10-lead 1.6 mm × 1.3 mm mini LFCSP package and 12-lead 3 mm × 3 mm LFCSP package
2.7 V to 3.6 V single-supply operation
Typical power consumption: <0.1 μW
RoHS compliant

APPLICATIONS

USB 2.0 signal switching circuits
Cellular phones
PDA's
MP3 players
Battery-powered systems
Headphone switching
Audio and video signal routing
Communications systems

GENERAL DESCRIPTION

The ADG772 is a low voltage, CMOS device that contains two independently selectable single-pole, double throw (SPDT) switches. It is designed as a general-purpose switch and can be used for routing both USB 1.1 and USB 2.0 signals.

This device offers a data rate of 1260 Mbps, making the part suitable for high frequency data switching. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. The ADG772 exhibits break-before-make switching action.

The ADG772 comes in a 12-lead LFCSP, and a 10-lead mini LFCSP. These packages make the ADG772 the ideal solution for space-constrained applications.

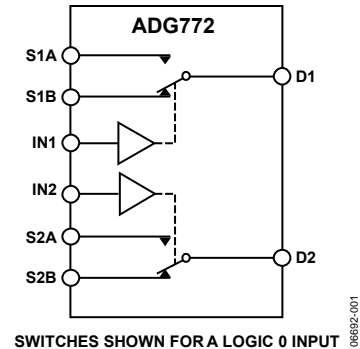


Figure 1.

PRODUCT HIGHLIGHTS

1. 1.6 mm × 1.3 mm mini LFCSP package.
2. USB 1.1 (12 Mbps) and USB 2.0 (480 Mbps) compliant.
3. Single 2.7 V to 3.6 V operation.
4. RoHS compliant.

Rev. 0

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ADG772

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REVISION HISTORY

8/07—Revision 0: Initial Version

SPECIFICATIONS

$V_{DD} = 2.7\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.

Table 1.

| Parameter | +25°C | -40°C to +85°C | Unit | Test Conditions/Comments |
|---|-----------|-----------------|--|--|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to V_{DD} | V | |
| On Resistance (R_{ON}) | 6.7 | 8.8 | Ω typ Ω max | $V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_S = 10\text{ mA}$; see Figure 21 |
| On Resistance Match Between Channels (ΔR_{ON}) | 0.04 | 0.2 | Ω typ Ω max | $V_{DD} = 2.7\text{ V}$, $V_S = 1.5\text{ V}$, $I_S = 10\text{ mA}$ |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 3.3 | 3.6 | Ω typ Ω max | $V_{DD} = 2.7\text{ V}$, $V_S = 0\text{ V to }V_{DD}$, $I_S = 10\text{ mA}$ |
| LEAKAGE CURRENTS | | | | |
| Source Off Leakage I_S (Off) | ± 0.2 | | nA typ | $V_{DD} = 3.6\text{ V}$ $V_S = 0.6\text{ V}/3.3\text{ V}$, $V_D = 3.3\text{ V}/0.6\text{ V}$; see Figure 22 |
| Channel On Leakage I_D , I_S (On) | ± 0.2 | | nA typ | $V_S = V_D = 0.6\text{ V or }3.3\text{ V}$; see Figure 23 |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V_{INH} | | 2 | V min | |
| Input Low Voltage, V_{INL} | | 0.8 | V max | |
| Input Current I_{INL} or I_{INH} | 0.005 | ± 0.1 | $\mu\text{A typ}$ $\mu\text{A max}$ | $V_{IN} = V_{INL}$ or V_{INH} $V_{IN} = V_{INL}$ or V_{INH} |
| C_{IN} , Digital Input Capacitance | 2 | | pF typ | |
| DYNAMIC CHARACTERISTICS¹ | | | | |
| t_{ON} | 9 12.5 | 13.5 | ns typ ns max | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$; see Figure 24 |
| t_{OFF} | 6 9.5 | 10 | ns typ ns max | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ $V_S = 2\text{ V}$; see Figure 24 |
| Propagation Delay | 250 | | ps typ | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ |
| Propagation Delay Skew, t_{SKEW} | 20 | | ps typ | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ |
| Break-Before-Make Time Delay (t_{BBM}) | 5 | | ns typ | $R_L = 50\ \Omega$, $C_L = 35\text{ pF}$ |
| Charge Injection | 3.4 | 2.9 | ns min | $V_{S1} = V_{S2} = 2\text{ V}$; see Figure 25 |
| Off Isolation | 0.5 | | pC typ | $V_D = 1.25\text{ V}$, $R_S = 0\ \Omega$, $C_L = 1\text{ nF}$; see Figure 26 |
| Channel-to-Channel Crosstalk | 73 | | dB typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 27 |
| | -90 | | dB typ | S1A to S2A/S1B to S2B; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 28 |
| | -80 | | dB typ | S1A to S1B/S2A to S2B; $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$; see Figure 29 |
| -3 dB Bandwidth | 630 | | MHz typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30 |
| Data Rate | 1260 | | Mbps typ | $R_L = 50\ \Omega$, $C_L = 5\text{ pF}$; see Figure 30 |
| C_S (Off) | 2.4 | | pF typ | |
| C_D , C_S (On) | 6.9 | | pF typ | |
| POWER REQUIREMENTS | | | | |
| I_{DD} | 0.006 | 1 | $\mu\text{A typ}$ $\mu\text{A max}$ | $V_{DD} = 3.6\text{ V}$ Digital inputs = 0 V or 3.6 V |

¹ Guaranteed by design, not subject to production test.

ADG772**ABSOLUTE MAXIMUM RATINGS**

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Rating |
|---|---|
| V_{DD} to GND | -0.3 V to +4.6 V |
| Analog Inputs ¹ , Digital Inputs | -0.3 V to $V_{DD} + 0.3$ V or 10 mA, whichever occurs first |
| Peak Current, Pin S1A, Pin S2A, Pin D1, or Pin D2 | 100 mA (pulsed at 1 ms, 10% duty cycle max) |
| Continuous Current, Pin S1A, Pin S2A, Pin D1, or Pin D2 | 30 mA |
| Operating Temperature Industrial Range (B version) | -40°C to $+85^\circ\text{C}$ |
| Storage Temperature Range | -65°C to $+150^\circ\text{C}$ |
| Junction Temperature | 150°C |
| 10-Lead Mini LFCSP (4-Layer Board) θ_{JA} Thermal Impedance | $131.6^\circ\text{C}/\text{W}$ |
| 12-Lead LFCSP (4-Layer Board) θ_{JA} Thermal Impedance | $61^\circ\text{C}/\text{W}$ |
| Pb-Free Temperature, Soldering, IR Reflow | |
| Peak Temperature | $260(+0/-5)^\circ\text{C}$ |
| Time at Peak Temperature | 10 sec to 40 sec |

¹ Overvoltages at the IN1, IN2, S1A, S2A, D1, or D2 pins are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

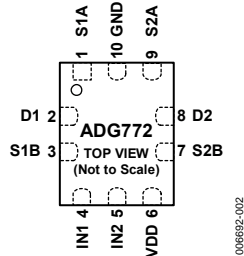


Figure 2. 10-Lead Mini LFCSP Pin Configuration

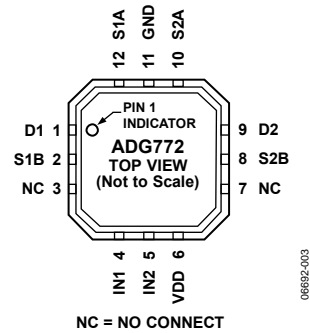


Figure 3. 12-Lead LFCSP Pin Configuration

Table 3. Pin Function Descriptions

| 10-Lead Mini LFCSP | 12-Lead LFCSP | Mnemonic | Description |
|--------------------|---------------|----------|--|
| 1 | 12 | S1A | Source Terminal. Can be an input or an output. |
| 2 | 1 | D1 | Drain Terminal. Can be an input or an output. |
| 3 | 2 | S1B | Source Terminal. Can be an input or an output. |
| 4 | 4 | IN1 | Logic Control Input. Controls Switch S1A/S1B—D1. |
| 5 | 5 | IN2 | Logic Control Input. Controls Switch S2A/S2B—D2. |
| 6 | 6 | VDD | Most Positive Power Supply Potential. |
| 7 | 8 | S2B | Source Terminal. Can be an input or an output. |
| 8 | 9 | D2 | Drain Terminal. Can be an input or an output. |
| 9 | 10 | S2A | Source Terminal. Can be an input or an output. |
| 10 | 11 | GND | Ground (0 V) Reference. |
| N/A | 3, 7 | NC | No Connect. |

TRUTH TABLE

Table 4.

| Logic (IN1/IN2) | Switch A (S1A or S2A) | Switch B (S1B or S2B) |
|-----------------|-----------------------|-----------------------|
| 0 | Off | On |
| 1 | On | Off |

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TYPICAL PERFORMANCE CHARACTERISTICS

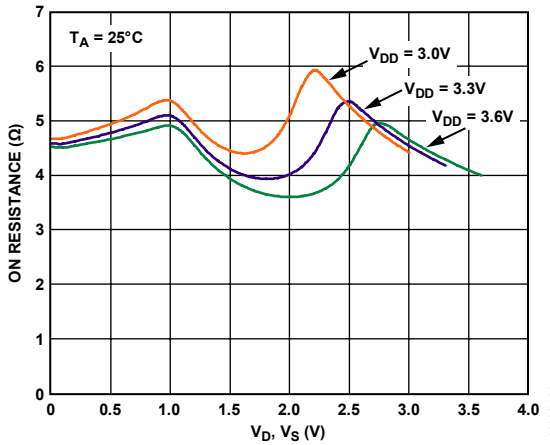


Figure 4. On Resistance vs. V_D (V_S) $V_{DD} = 3.0V$ to $3.6V$

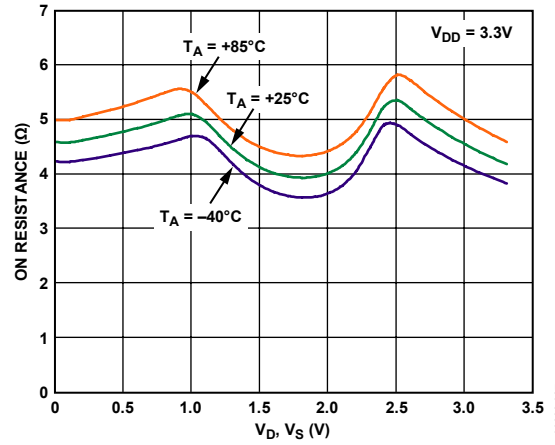


Figure 7. On Resistance vs. V_D (V_S) for Different Temperature, $V_{DD} = 3.3V$

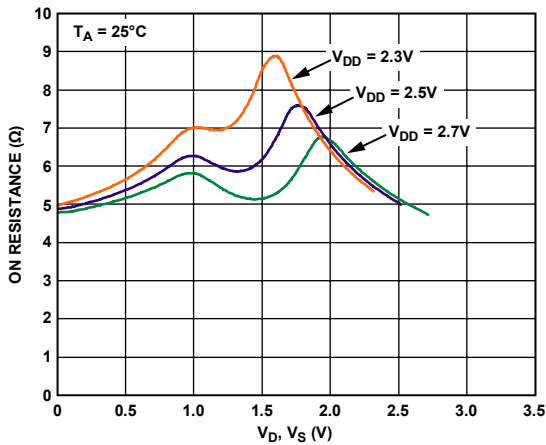


Figure 5. On Resistance vs. V_D (V_S) $V_{DD} = 2.5V \pm 0.2V$

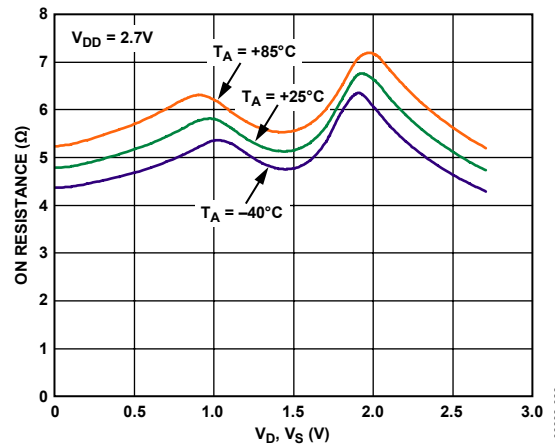


Figure 8. On Resistance vs. V_D (V_S) for Different Temperature, $V_{DD} = 2.7V$

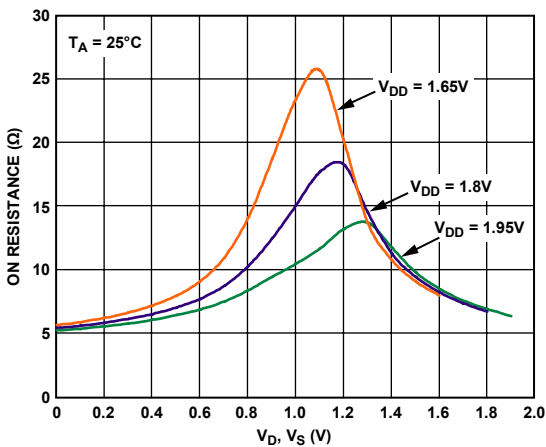


Figure 6. On Resistance vs. V_D (V_S) $V_{DD} = 1.8V \pm 0.15V$

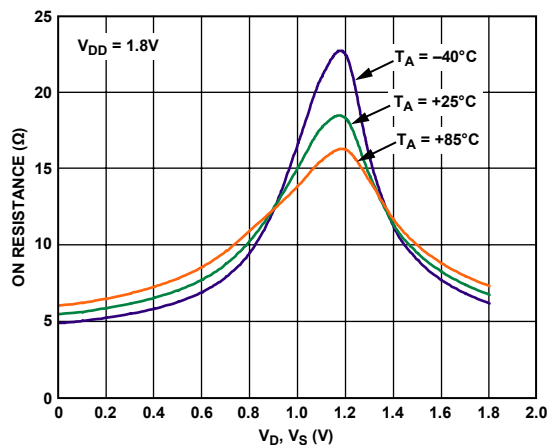


Figure 9. On Resistance vs. V_D (V_S) for Different Temperatures, $V_{DD} = 1.8V$

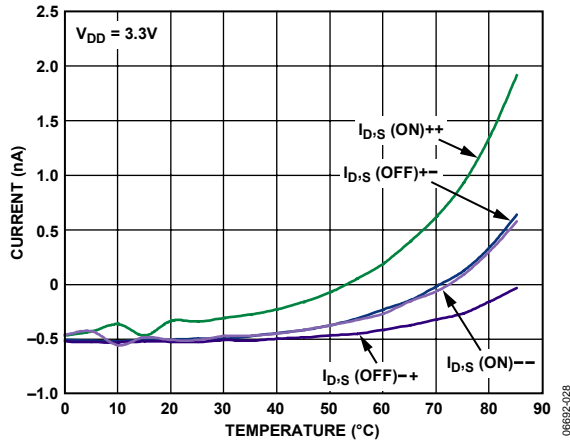


Figure 10. Leakage Current vs. Temperature, $V_{DD} = 3.3V$

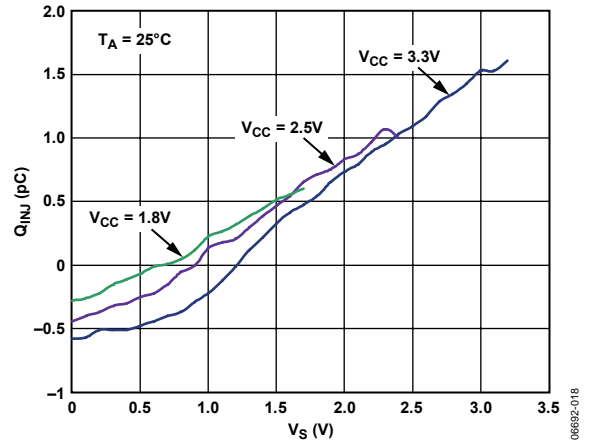


Figure 13. Charge Injection vs. Source Voltage

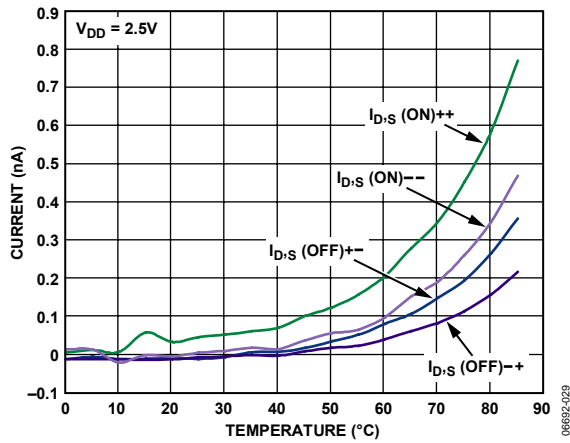


Figure 11. Leakage Current vs. Temperature, $V_{DD} = 2.5V$

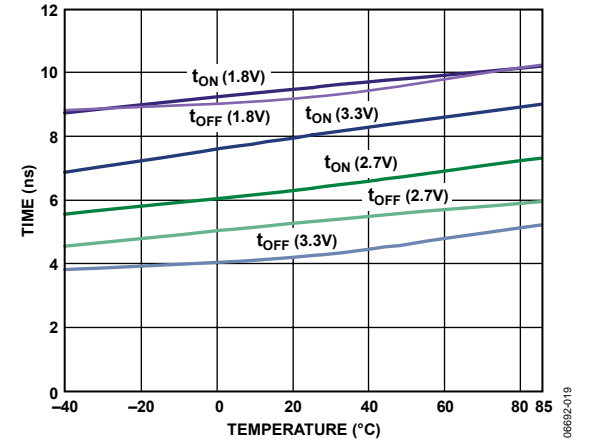


Figure 14. t_{ON}/t_{OFF} Times vs. Temperature

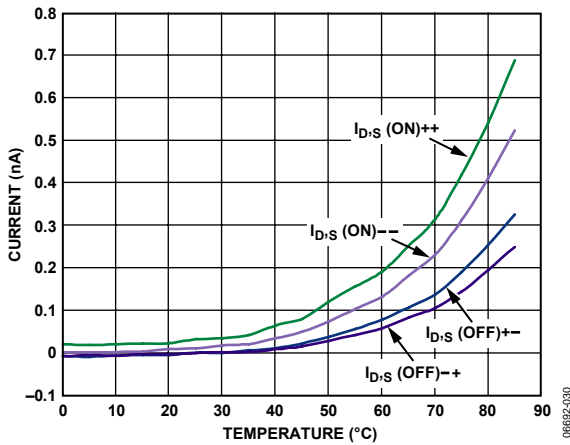


Figure 12. Leakage Current vs. Temperature, $V_{DD} = 1.8V$

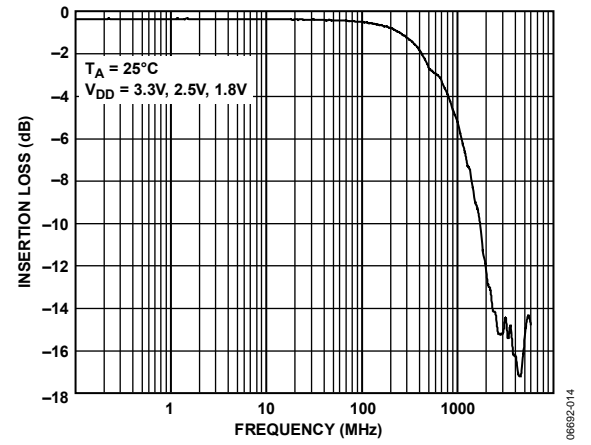


Figure 15. Bandwidth

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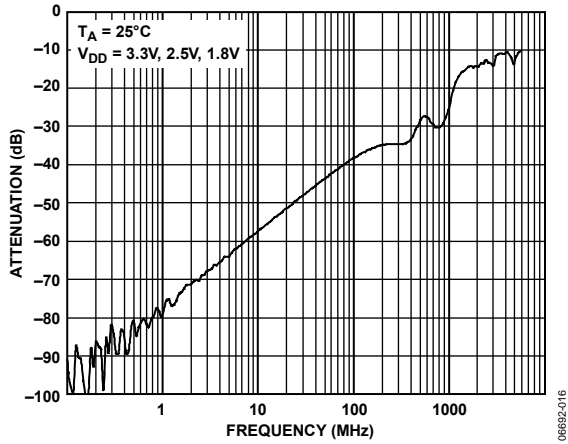


Figure 16. Off Isolation vs. Frequency

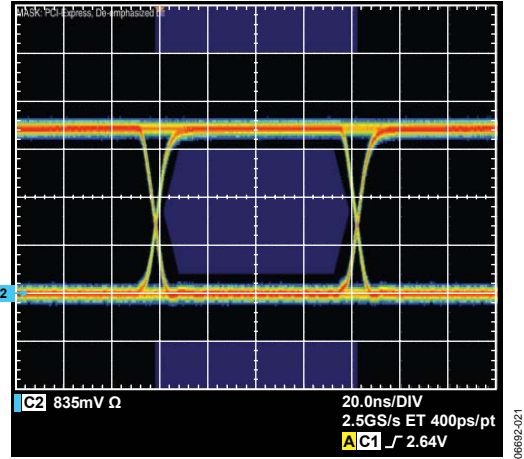


Figure 19. USB 1.1 Eye Diagram

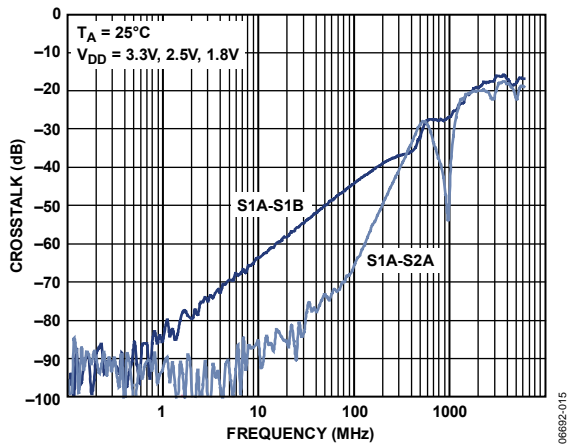


Figure 17. Crosstalk vs. Frequency

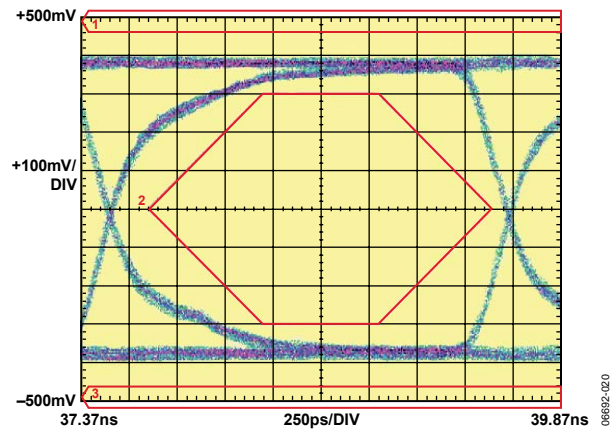


Figure 20. USB 2.0 Eye Diagram

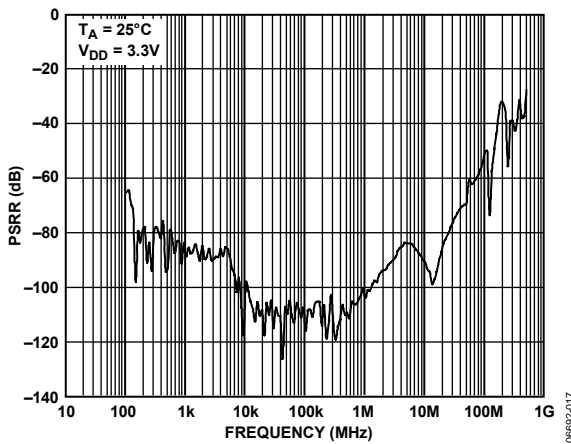


Figure 18. PSRR vs. Frequency

TEST CIRCUITS

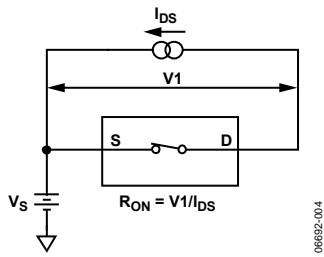


Figure 21. On Resistance

06692-004

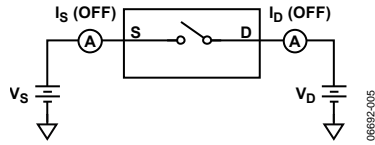


Figure 22. Off Leakage

06692-005

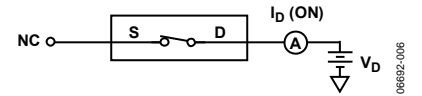


Figure 23. On Leakage

06692-006

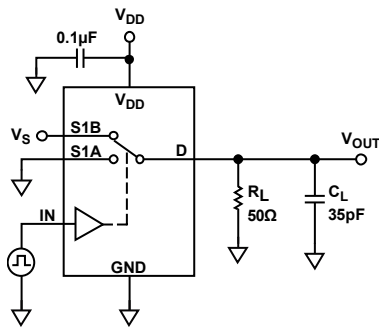


Figure 24. Switching Times, t_{ON} , t_{OFF}

06692-007

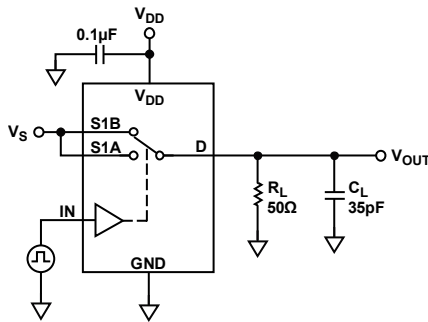


Figure 25. Break-Before-Make Time Delay, t_{BBM}

06692-008

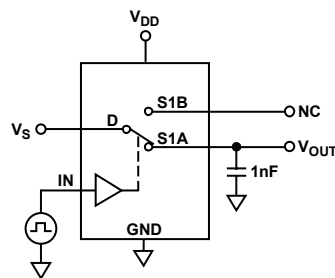
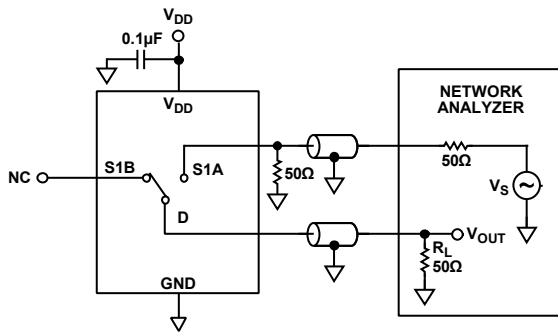


Figure 26. Charge Injection

06692-009

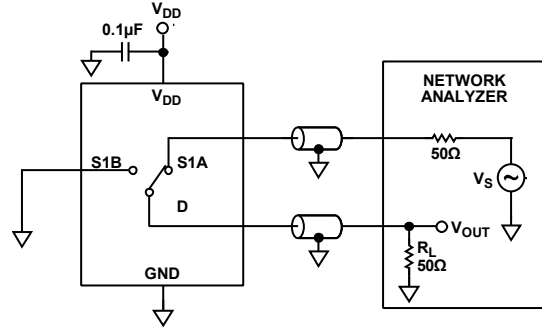
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$$\text{OFF ISOLATION} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

06692-010

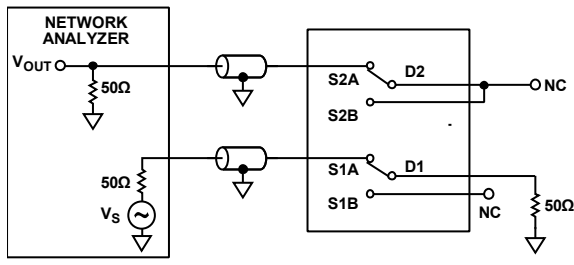
Figure 27. Off Isolation



$$\text{INSERTION LOSS} = 20 \log \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

06692-012

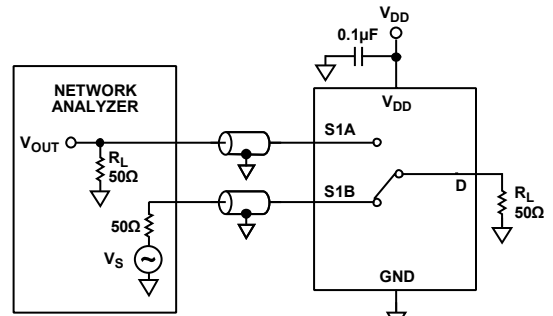
Figure 29. Channel-to-Channel Crosstalk (S1A-S1B)



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

06692-013

Figure 28. Channel-to-Channel Crosstalk (S1A-S2A)



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \log \frac{V_{\text{OUT}}}{V_s}$$

06692-011

Figure 30. Bandwidth

TERMINOLOGY

I_{DD}

Positive supply current.

$V_D (V_S)$

Analog voltage on Terminal D and Terminal S.

R_{ON}

Ohmic resistance between Terminal D and Terminal S.

$R_{FLAT} (On)$

The difference between the maximum and minimum values of on resistance as measured on the switch.

ΔR_{ON}

On resistance match between any two channels.

$I_S (Off)$

Source leakage current with the switch off.

$I_D (Off)$

Drain leakage current with the switch off.

$I_D, I_S (On)$

Channel leakage current with the switch on.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

$I_{INL} (I_{INH})$

Input current of the digital input.

$C_S (Off)$

Off switch source capacitance. Measured with reference to ground.

$C_D (Off)$

Off switch drain capacitance. Measured with reference to ground.

$C_D, C_S (On)$

On switch capacitance. Measured with reference to ground.

C_{IN}

Digital input capacitance.

t_{ON}

Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF}

Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{BBM}

On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection

Measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation

Measure of unwanted signal coupling through an off switch.

Crosstalk

Measure of unwanted signal that is coupled from one channel to another as a result of parasitic capacitance.

-3 dB Bandwidth

Frequency at which the output is attenuated by 3 dB.

On Response

Frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

THD + N

Ratio of the harmonics amplitude plus noise of a signal to the fundamental.

T_{SKEW}

The measure of the variation in propagation delay between each channel.

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OUTLINE DIMENSIONS

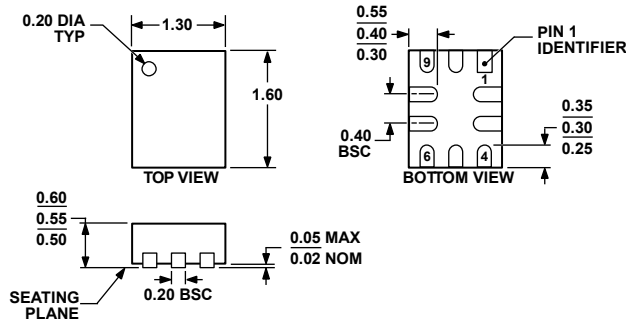
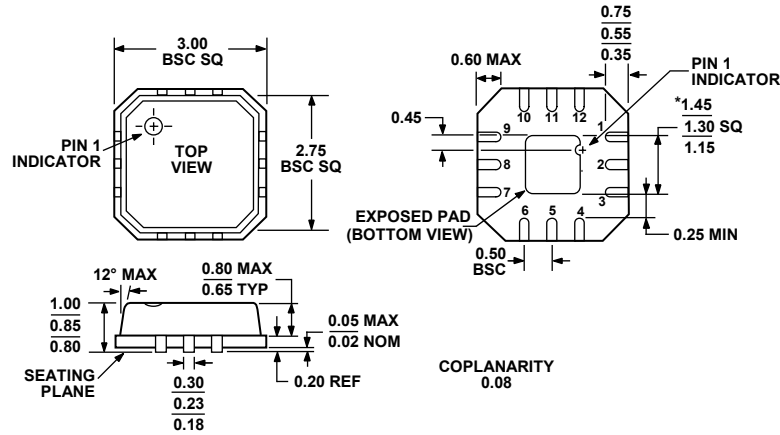


Figure 31. 10-Lead Mini Lead Frame Chip Scale Package (LFCSP_UQ)
1.30 mm × 1.60 mm Body, Ultra Thin Quad
(CP-10-10)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VEED-1 EXCEPT FOR EXPOSED PAD DIMENSION.

Figure 32. 12-Lead Lead Frame Chip Scale Package (LFCSP_VQ)
3 mm × 3 mm Body, Very Thin Quad
(CP-12-1)
Dimensions shown in millimeters

ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option | Branding |
|-------------------------------|-------------------|---|----------------|----------|
| ADG772BCPZ-1REEL ¹ | -40°C to +85°C | 12-Lead Lead Frame Chip Scale Package (LFCSP_VQ) | CP-12-1 | S2P |
| ADG772BCPZ-REEL ¹ | -40°C to +85°C | 10-Lead Mini Lead Frame Chip Scale Package (LFCSP_UQ) | CP-10-10 | B |
| ADG772BCPZ-REEL7 ¹ | -40°C to +85°C | 10-Lead Mini Lead Frame Chip Scale Package (LFCSP_UQ) | CP-10-10 | B |
| EVAL-ADG772EBZ ¹ | -40°C to +85°C | Evaluation Board | | |

¹ Z = RoHS Compliant Part.