Serially-Controlled, High Voltage Latch-Up Proof Quad SPST Switch

Preliminary Technical Data

ADGS5412

FEATURES

SPI interface with Error Detection
Includes CRC, Invalid Read/Write Address and SCLK Count Error detection
Supports burst and daisy-chain mode
Industry standard SPI modes 0 and 3 interface compatible
Latch-up proof
Low on resistance (<10 Ω)
±9 V to ±22 V dual-supply operation
9 V to 40 V single-supply operation
Fully specified at ±15 V, ±20 V, +12 V, and +36 V
V_{SS} to V_{DD} analog signal range

APPLICATIONS

Relay replacement
Automatic test equipment
Data acquisition
Instrumentation
Avionics
Audio and video switching
Communication systems

FUNCTIONAL BLOCK DIAGRAMS

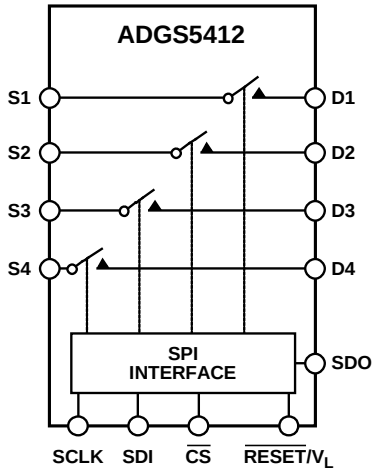


Figure 1.

GENERAL DESCRIPTION

The ADGS5412 contains four independent single-pole/single-throw (SPST) switches. An SPI interface controls the switches. The SPI interface has robust error detection features. These are CRC error detection, Invalid Read/Write Address detection and SCLK count error detection.

It is possible to daisy-chain multiple ADGS5412 devices together. This enables the configuration of multiple device with a minimal amount of digital lines. The ADGS5412 can also operate in burst mode to decrease the time between SPI commands.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The on-resistance profile is very flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals.

PRODUCT HIGHLIGHTS

1. SPI Interface removes the need for parallel conversion, logic traces and reduces GPIO channel count.
2. Daisy chain mode removes additional logic traces when multiple devices are used.
3. CRC error detection, Invalid Read/Write Address and SCLK Count Error detection ensures a robust digital interface.
4. SIL Compatible.
5. Trench isolation analog switch section guards against latch-up. A dielectric trench separates the P and N channel transistors thereby preventing latch-up even under severe overvoltage conditions.

Rev. PrB **Document Feedback**
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2016 Analog Devices, Inc. All rights reserved.
Technical Support **www.analog.com**

ADGS5412* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADGS5412: Serially-Controlled, High Voltage Latch-Up Proof Quad SPST Switch Preliminary Data Sheet

SOFTWARE AND SYSTEMS REQUIREMENTS

- ADGS5412 - No-OS Driver

DESIGN RESOURCES

- ADGS5412 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADGS5412 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

This page is dynamically generated by Analog Devices, Inc., and inserted into this data sheet. A dynamic change to the content on this page will not trigger a change to either the revision number or the content of the product data sheet. This dynamic page may be frequently modified.

TABLE OF CONTENTS

SPECIFICATIONS

±15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, V_L=2.7V to 5.5V, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9.8			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 26
	TBD	TBD	TBD	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = ±10 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.2			Ω typ	V_S = ±10 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓ 10 V; see Figure 29
	TBD	TBD	TBD	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±10 V, V_D = ∓ 10 V; see Figure 29
	TBD	TBD	TBD	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±10 V; see Figure 25
	TBD	TBD	TBD	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	3.3V < V_L ≤ 5.5V
Input Low Voltage, V_{INL}			0.8	V max	
Input High Voltage, V_{INH}			1.35	V min	2.7V ≤ V_L ≤ 3.3V
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	TBD			μA typ	V_{IN} = V_{GND} or V_L
			TBD	μA max	
Digital Input Capacitance, C_{IN}	TBD			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 10 V; see Figure 32
t_{OFF}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 10 V; see Figure 32
Charge Injection, Q_{INJ}	240			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 29
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.009			% typ	R_L = 1 kΩ, 15 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	167			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.7			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	18			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	18			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	60			pF typ	V_S = 0 V, f = 1 MHz

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	45			µA typ	Digital inputs = 0 V or V_L
	TBD		TBD	µA max	
I_L Inactive	TBD			µA typ	Digital inputs = 0 V or V_L
		TBD	TBD	µA max	
I_L Active at 50MHz	TBD			µA typ	Digital inputs toggle between 0 V and V_L
		TBD	TBD	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_L
			TBD	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

±20 V DUAL SUPPLY

V_{DD} = +20 V ± 10%, V_{SS} = −20 V ± 10%, V_L=2.7V to 5.5V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance, R_{ON}	9			Ω typ	V_S = ±15 V, I_S = −10 mA; see Figure 26
	TBD	TBD	TBD	Ω max	V_{DD} = +18 V, V_{SS} = −18 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = ±15 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	1.5			Ω typ	V_S = ±15 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
LEAKAGE CURRENTS					V_{DD} = +22 V, V_{SS} = −22 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓ 15 V; see Figure 29
	TBD	TBD	TBD	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = ±15 V, V_D = ∓ 15 V; see Figure 29
	TBD	TBD	TBD	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = ±15 V; see Figure 25
	TBD	TBD	TBD	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	3.3V < V_L ≤ 5.5V
Input Low Voltage, V_{INL}			0.8	V max	
Input High Voltage, V_{INH}			1.35	V min	2.7V ≤ V_L ≤ 3.3V
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	TBD			µA typ	V_{IN} = V_{GND} or V_L
			TBD	µA max	
Digital Input Capacitance, C_{IN}	TBD			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 10 V; see Figure 32
t_{OFF}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 10 V; see Figure 32
Charge Injection, Q_{INJ}	310			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.007			% typ	R_L = 1 kΩ, 20 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	160			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.6			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	17			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	17			pF typ	V_S = 0 V, f = 1 MHz
C_D (On), C_S (On)	60			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +22 V, V_{SS} = −22 V
I_{DD}	50			µA typ	Digital inputs = 0 V or V_L
	TBD		TBD	µA max	
I_L Inactive	TBD			µA typ	Digital inputs = 0 V or V_L
		TBD	TBD	µA max	
I_L Active at 50MHz	TBD			µA typ	Digital inputs toggle between 0 V and V_L
		TBD	TBD	µA max	
I_{SS}	0.001			µA typ	Digital inputs = 0 V or V_L
			TBD	µA max	
V_{DD}/V_{SS}			±9/±22	V min/V max	GND = 0 V

[1] Guaranteed by design; not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, V_L=2.7V to 5.5V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	19			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 26
	TBD	TBD	TBD	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
On-Resistance Flatness, $R_{FLAT (ON)}$	4.4			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 29
	TBD	TBD	TBD	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 29
	TBD	TBD	TBD	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/10 V; see Figure 25
	TBD	TBD	TBD	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	3.3V < V_L ≤ 5.5V
Input Low Voltage, V_{INL}			0.8	V max	
Input High Voltage, V_{INH}			1.35	V min	2.7V ≤ V_L ≤ 3.3V

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	TBD			µA typ	$V_{IN} = V_{GND}$ or V_L
			TBD	µA max	
Digital Input Capacitance, C_{IN}	TBD			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 8 V; see Figure 32
t_{OFF}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 8 V; see Figure 32
Charge Injection, Q_{INJ}	95			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 27
Total Harmonic Distortion + Noise	0.07			% typ	R_L = 1 kΩ, 6 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	180			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−1.3			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	22			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	22			pF typ	V_S = 6 V, f = 1 MHz
C_D (On), C_S (On)	58			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	40			µA typ	Digital inputs = 0 V or V_L
			TBD	µA max	
I_L Inactive	TBD			µA typ	Digital inputs = 0 V or V_L
		TBD	TBD	µA max	
I_L Active at 50MHz	TBD			µA typ	Digital inputs toggle between 0 V and V_L
		TBD	TBD	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

36 V SINGLE SUPPLY

V_{DD} = 36 V ± 10%, V_{SS} = 0 V, V_L=2.7V to 5.5V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance, R_{ON}	10.6			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA; see Figure 26
	TBD	TBD	TBD	Ω max	V_{DD} = 32.4 V, V_{SS} = 0 V
On-Resistance Match Between Channels, ΔR_{ON}	0.35			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
On-Resistance Flatness, $R_{FLAT(ON)}$	2.7			Ω typ	V_S = 0 V to 30 V, I_S = −10 mA
	TBD	TBD	TBD	Ω max	
LEAKAGE CURRENTS					V_{DD} = 39.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 29
	TBD	TBD	TBD	nA max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/30 V, V_D = 30 V/1 V; see Figure 29
	TBD	TBD	TBD	nA max	
Channel On Leakage, I_D (On), I_S (On)	±0.1			nA typ	V_S = V_D = 1 V/30 V; see Figure 25
	TBD	TBD	TBD	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2	V min	3.3V < V_L ≤ 5.5V
Input Low Voltage, V_{INL}			0.8	V max	
Input High Voltage, V_{INH}			1.35	V min	2.7V ≤ V_L ≤ 3.3V
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	TBD			µA typ	V_{IN} = V_{GND} or V_L
			TBD	µA max	
Digital Input Capacitance, C_{IN}	TBD			pF typ	
DYNAMIC CHARACTERISTICS[1]					
t_{ON}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 18 V; see Figure 32
t_{OFF}	TBD			ns typ	R_L = 300 Ω, C_L = 35 pF
	TBD	TBD	TBD	ns max	V_S = 18 V; see Figure 32
Charge Injection, Q_{INJ}	280			pC typ	V_S = 18 V, R_S = 0 Ω, C_L = 1 nF; see Figure 33
Off Isolation	−78			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Figure 27
Total Harmonic Distortion + Noise	0.03			% typ	R_L = 1 kΩ, 18 V p-p, f = 20 Hz to 20 kHz; see Figure 30
−3 dB Bandwidth	174			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 31
Insertion Loss	−0.8			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
C_S (Off)	18			pF typ	V_S = 18 V, f = 1 MHz
C_D (Off)	18			pF typ	V_S = 18 V, f = 1 MHz
C_D (On), C_S (On)	58			pF typ	V_S = 18 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 39.6 V
I_{DD}	80			µA typ	Digital inputs = 0 V or V_L
	TBD		TBD	µA max	
I_L Inactive	TBD			µA typ	Digital inputs = 0 V or V_L
		TBD	TBD	µA max	
I_L Active at 50MHz	TBD			µA typ	Digital inputs toggle between 0 V and V_L
		TBD	TBD	µA max	
V_{DD}			9/40	V min/V max	GND = 0 V, V_{SS} = 0 V

[1] Guaranteed by design; not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx				
V_{DD} = +15 V, V_{SS} = −15 V				
LFCSP (θ_{JA} = TBD °C/W)	TBD	TBD	TBD	mA maximum
V_{DD} = +20 V, V_{SS} = −20 V				
LFCSP (θ_{JA} = TBD °C/W)	TBD	TBD	TBD	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
LFCSP (θ_{JA} = TBD °C/W)	TBD	TBD	TBD	mA maximum
V_{DD} = 36 V, V_{SS} = 0 V				
LFCSP (θ_{JA} = TBD °C/W)	TBD	TBD	TBD	mA maximum

TIMING CHARACTERISTICS

V_L = 2.7 V to 5.5 V; GND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. Guaranteed by design and characterisation, not production tested.

Table 6.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Conditions/Comments
t_1	20	ns min	SCLK period
t_2	8	ns min	SCLK high pulse width
t_3	8	ns min	SCLK low pulse width
t_4	10	ns min	$\overline{CS}$ falling edge to SCLK rising edge
t_5	6	ns min	Data setup time
t_6	8	ns min	Data hold time
t_7	10	ns min	SCLK rising edge to $\overline{CS}$ rising edge
t_8	40	ns max	$\overline{CS}$ falling edge to SDO data available
t_9[1]	40	ns max	SCLK falling edge to SDO data available
t_{10}	10	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
t_{11}	20	ns min	$\overline{CS}$ high time between SPI commands
t_{12}	8	ns min	$\overline{CS}$ falling edge to SCLK becomes stable
t_{13}	8	ns min	$\overline{CS}$ rising edge to SCLK becomes stable

[1] Measured with the 1 kΩ pull-up resistor to V_L and 20 pF load. t_9 determines the maximum SCLK frequency when SDO is used.

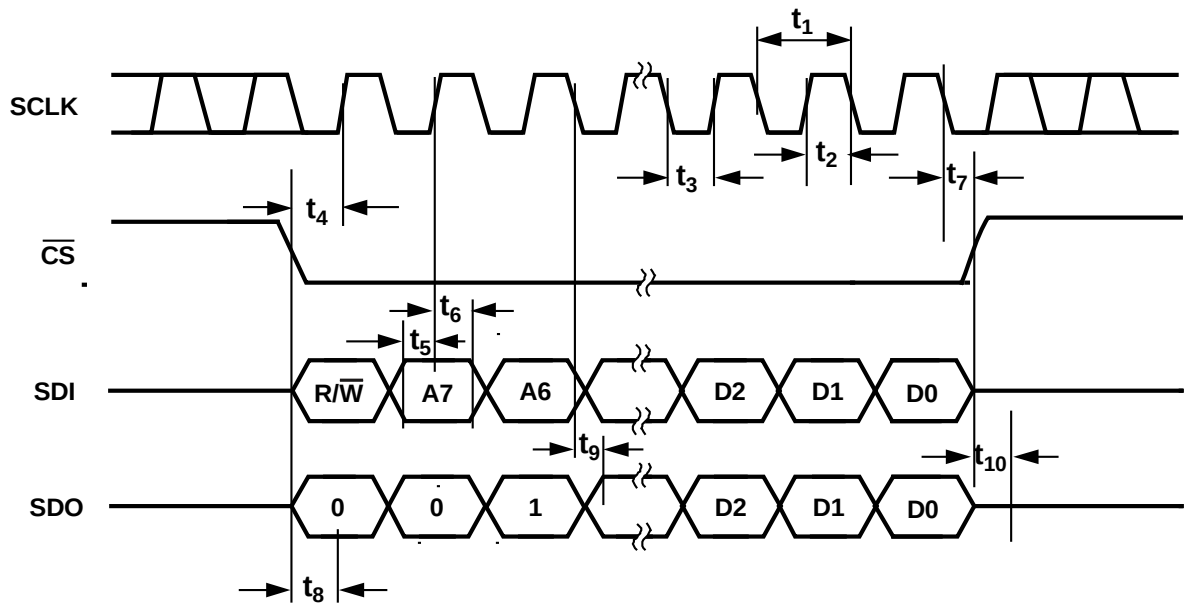


Figure 2. Addressable Mode Timing Diagram

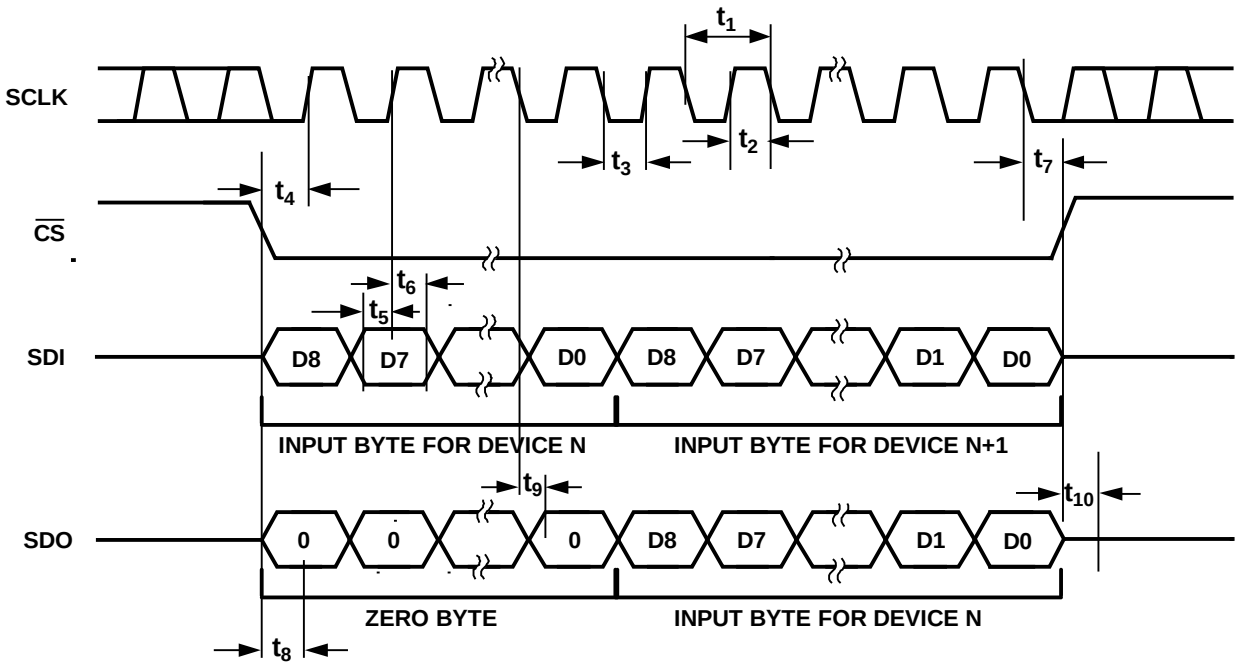


Figure 3. Daisy Chain Timing Diagram

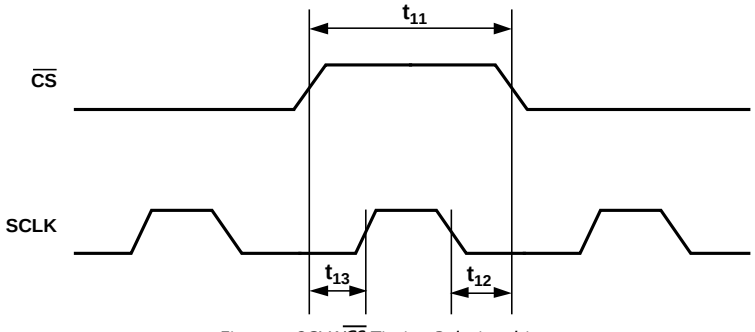


Figure 4. SCLK/$\overline{CS}$ Timing Relationship

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 7.

Parameter	Rating
V_{DD} to V_{SS}	48 V
V_{DD} to GND	−0.3 V to +48 V
V_{SS} to GND	+0.3 V to −48 V
V_L to GND	TBD
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	TBD
Peak Current, Sx or Dx Pins	278 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx[2]	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Thermal Impedance, θ_{JA}	
24-Lead LFCSP (4-Layer Board)	TBD°C/W
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

[1] Overvoltages at the INx, Sx, and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

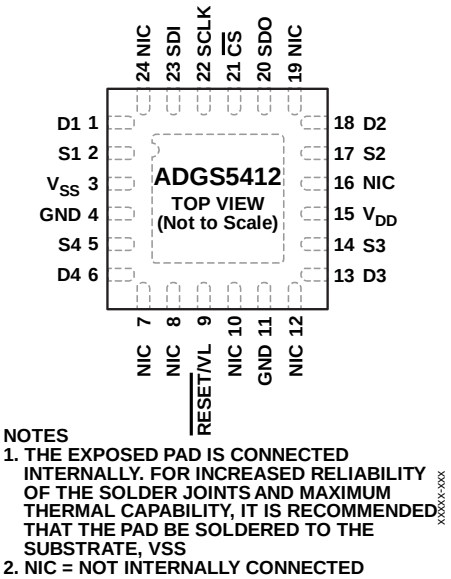


Figure 5. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal 1. This pin can be an input or output.
2	S1	Source Terminal 1. This pin can be an input or output.
3	V_{SS}	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
4	GND	Ground (0 V) Reference.
5	S4	Source Terminal 4. This pin can be an input or output.
6	D4	Drain Terminal 4. This pin can be an input or output.
7	NIC	Not Internally Connected.
8	NIC	Not Internally Connected.
9	$\overline{RESET}/V_L$	$\overline{RESET}$/Logic Power Supply Input (V_L). Under normal operation, drive the $\overline{RESET}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the pin low to complete a hardware reset. All switches are opened, and the appropriate registers are set to their default.
10	NIC	Not Internally Connected.
11	GND	Ground (0V) Reference.
12	NIC	Not Internally Connected.
13	D3	Drain Terminal 3. This pin can be an input or output.
14	S3	Source Terminal 3. This pin can be an input or output.
15	V_{DD}	Most Positive Power Supply Potential.
16	NIC	Not Internally Connected.
17	S2	Source Terminal 2. This pin can be an input or output.
18	D2	Drain Terminal 2. This pin can be an input or output.
19	NIC	Not Internally Connected.
20	SDO	Serial Data Output. This pin can be used for daisy-chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to V_L with an external resistor.
21	$\overline{CS}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{CS}$ goes low, it powers on the SCLK buffers and enables the input shift register. Data is transferred in on the falling edges of the following clocks. Taking $\overline{CS}$ high updates the switch condition.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK . Data can be transferred at rates of up to 50 MHz.
23	SDI	Serial Data Input. Data is captured on the positive edge of the serial clock input.

24	NIC Exposed Pad	Not Internally Connected. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the substrate, V_{SS}.

TYPICAL PERFORMANCE CHARACTERISTICS

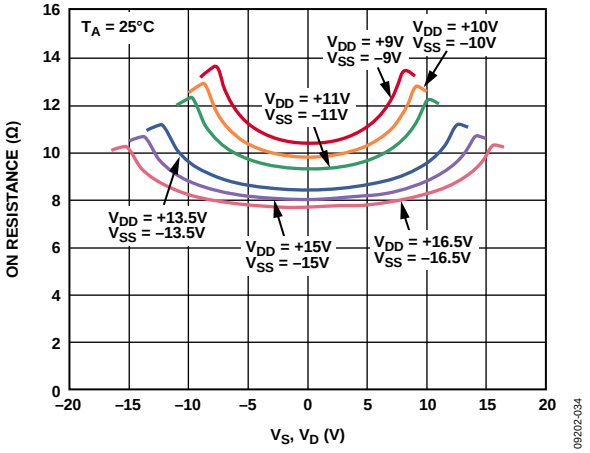


Figure 6. R_{ON} as a Function of V_S, V_D (Dual Supply)

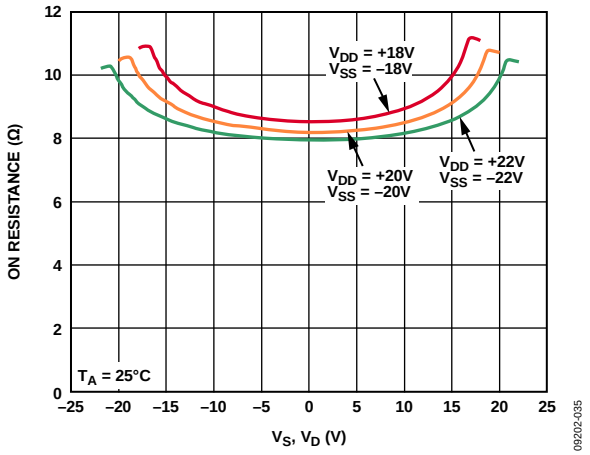


Figure 7. R_{ON} as a Function of V_S, V_D (Dual Supply)

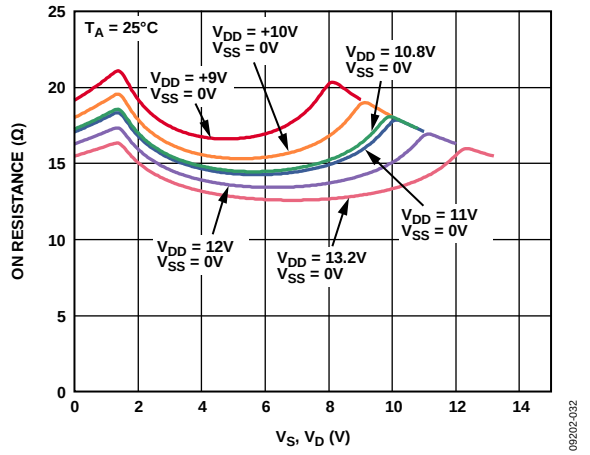


Figure 8. R_{ON} as a Function of V_S, V_D (Single Supply)

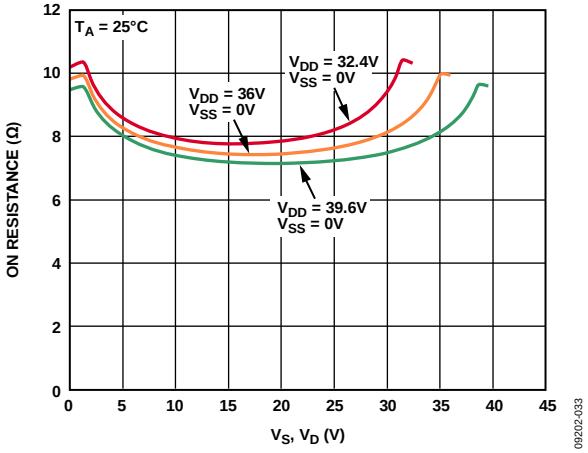


Figure 9. R_{ON} as a Function of V_S, V_D (Single Supply)

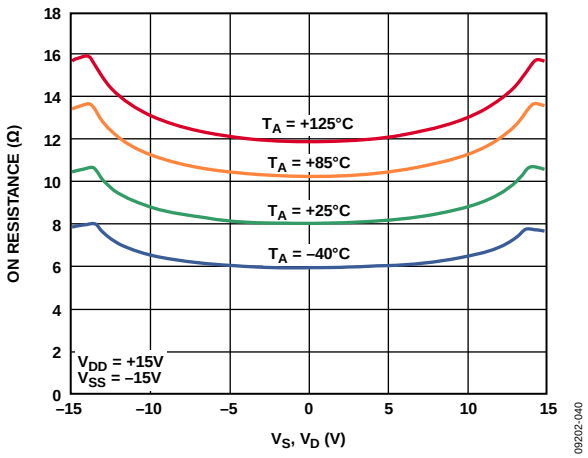


Figure 10. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±15 V Dual Supply

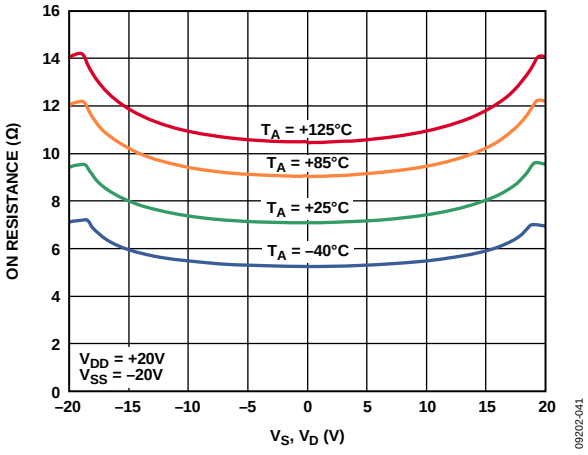


Figure 11. R_{ON} as a Function of V_S (V_D) for Different Temperatures, ±20 V Dual Supply

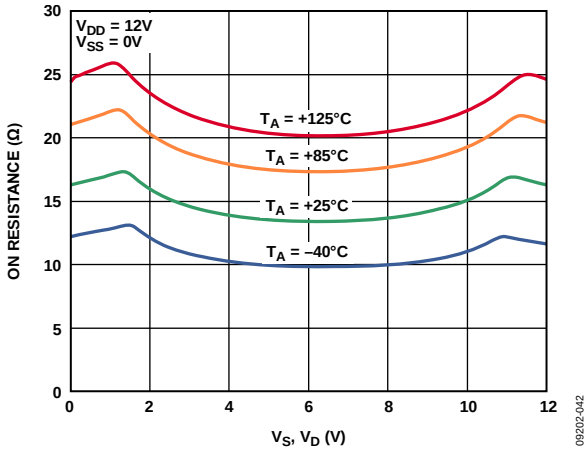


Figure 12. R_{ON} as a Function of V_S (V_D) for Different Temperatures, 12 V Single Supply

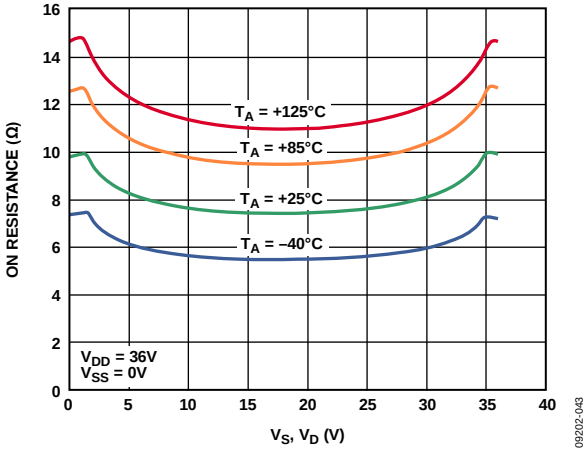


Figure 13. R_{ON} as a Function of V_S (V_D) for Different Temperatures, 36 V Single Supply

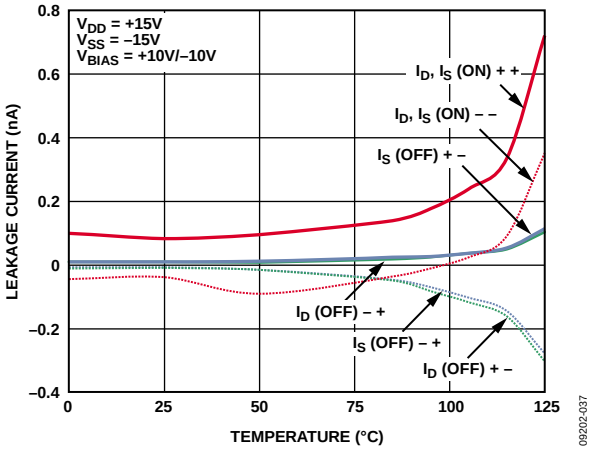


Figure 14. Leakage Currents vs. Temperature, ±15 V Dual Supply

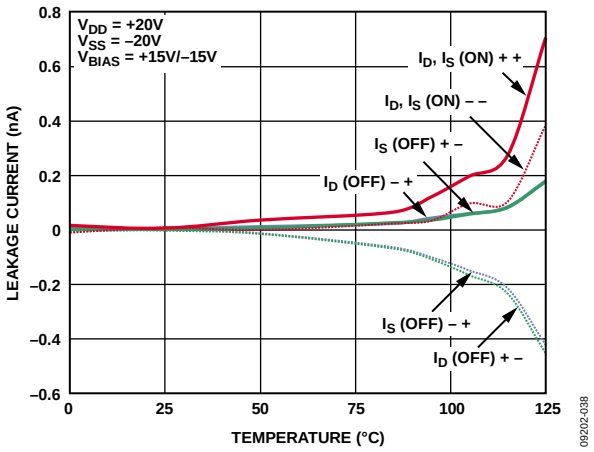


Figure 15. Leakage Currents vs. Temperature, ±20 V Dual Supply

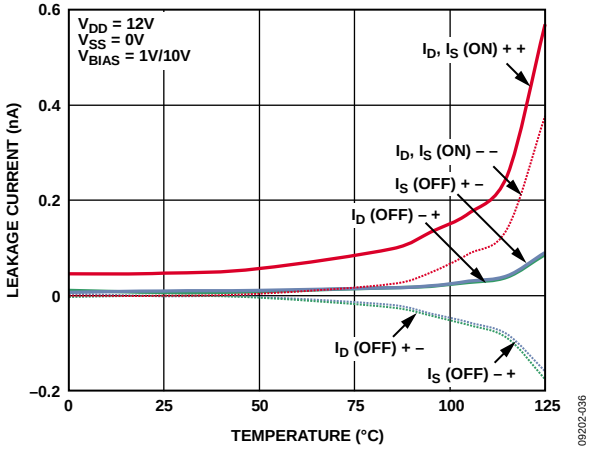


Figure 16. Leakage Currents vs. Temperature, 12 V Single Supply

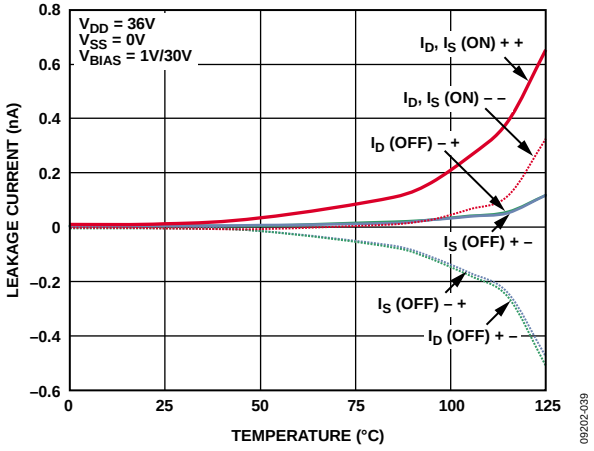


Figure 17. Leakage Currents vs. Temperature, 36 V Single Supply

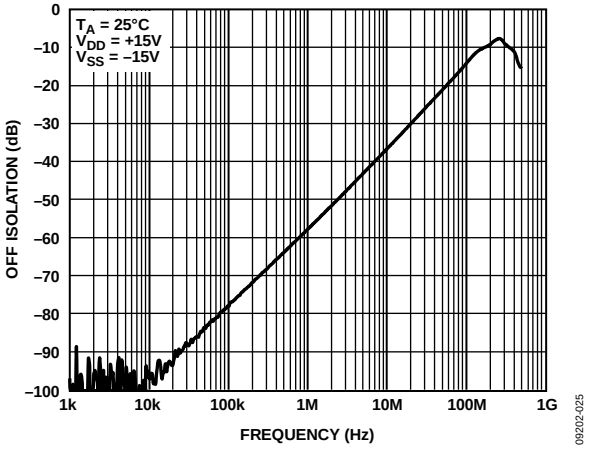


Figure 18. Off Isolation vs. Frequency, ±15 V Dual Supply

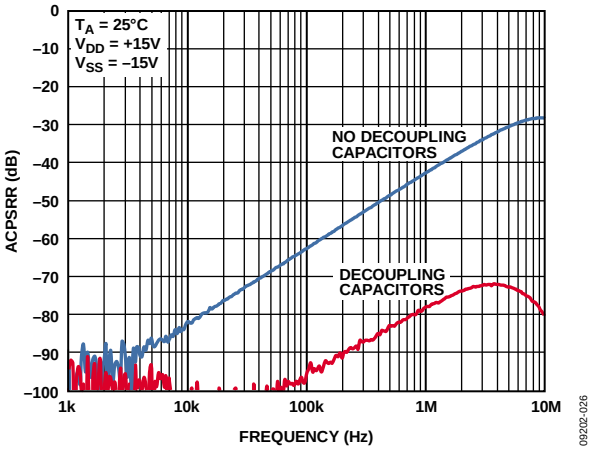


Figure 21. ACPSRR vs. Frequency, ±15 V Dual Supply

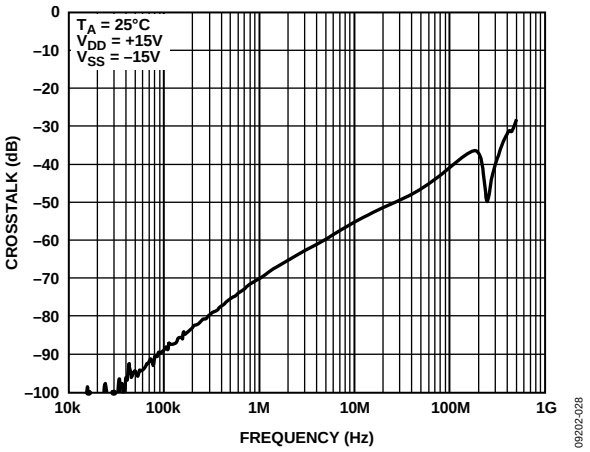


Figure 19. Crosstalk vs. Frequency, ±15 V Dual Supply

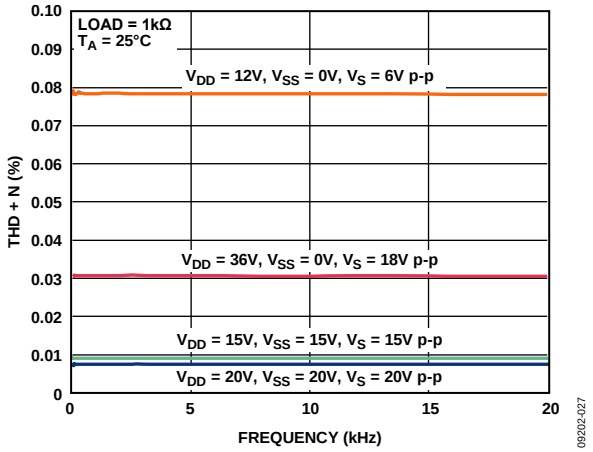


Figure 22. THD + N vs. Frequency, ±15 V Dual Supply

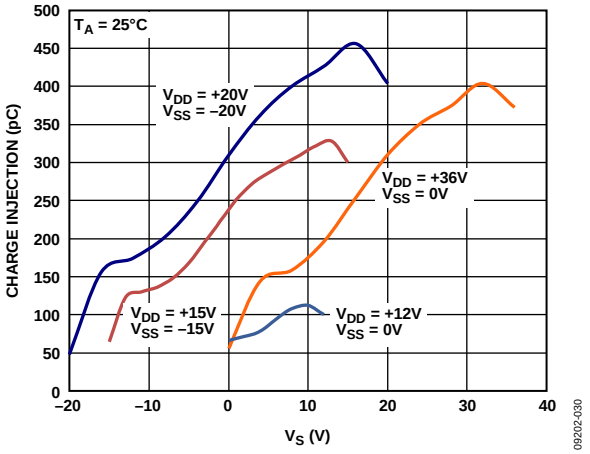


Figure 20. Charge Injection vs. Source Voltage

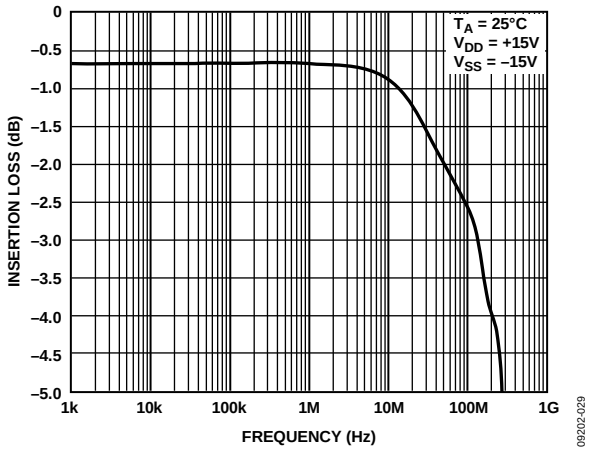


Figure 23. Bandwidth

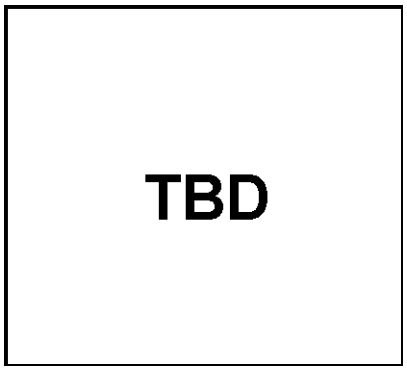


Figure 24. t_{ON}, t_{OFF} Times vs. Temperature

TEST CIRCUITS

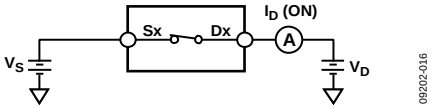


Figure 25. On Leakage

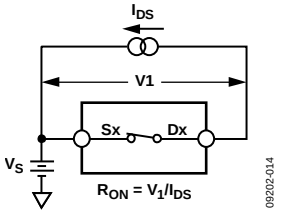


Figure 26. On Resistance

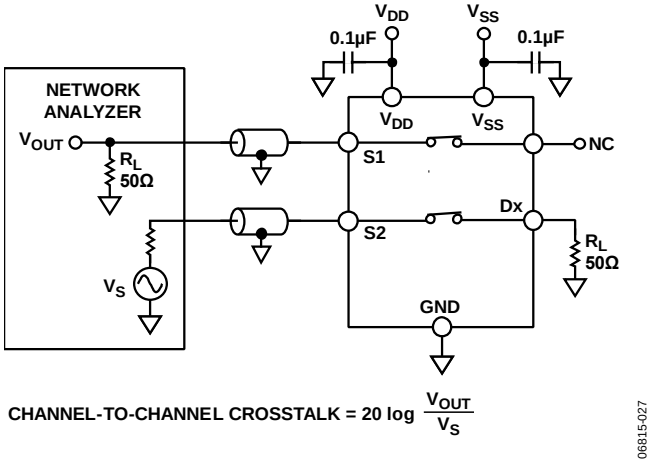


Figure 27. Channel-to-Channel Crosstalk

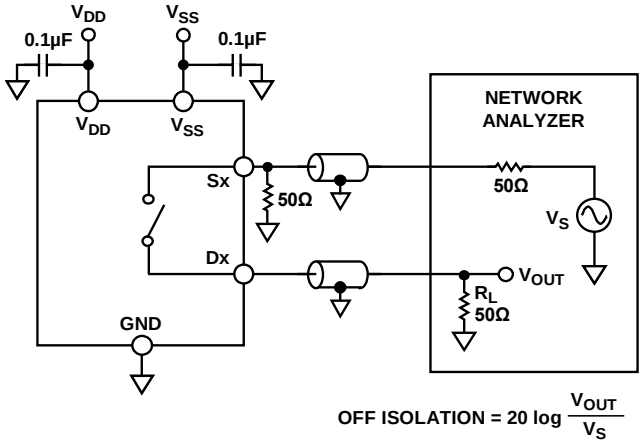


Figure 28. Off Isolation

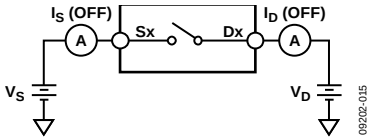


Figure 29. Off Leakage

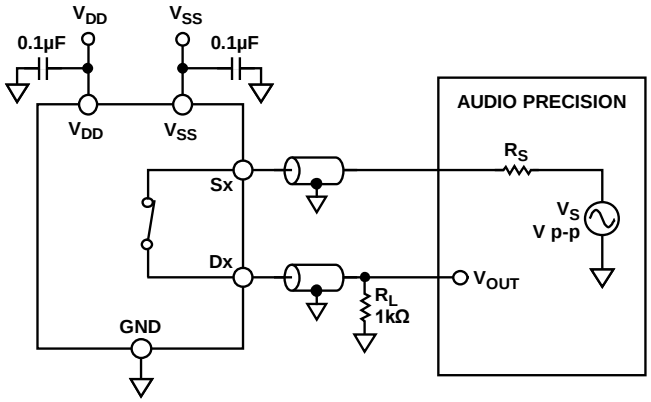


Figure 30. THD + Noise

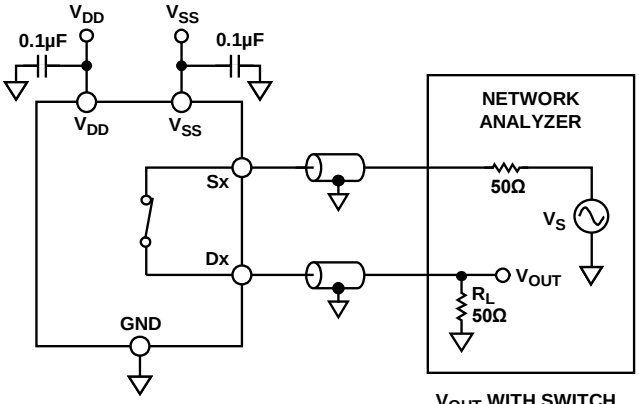


Figure 31. Bandwidth

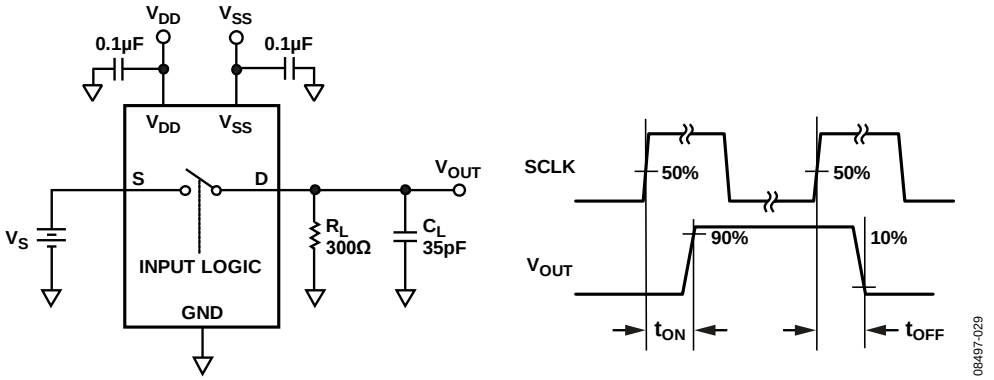


Figure 32. Switching Times

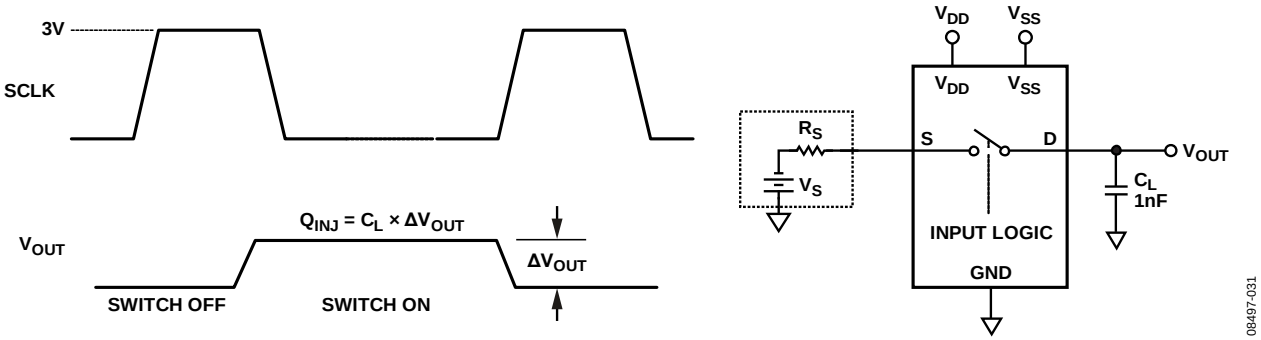


Figure 33. Charge Injection

TERMINOLOGY

I_{DD}
I_{DD} represents the positive supply current.

I_{SS}
I_{SS} represents the negative supply current.

V_D, V_S
V_D and V_S represent the analog voltage on Terminal D and Terminal S, respectively.

R_{ON}
R_{ON} represents the ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
ΔR_{ON} represents the difference between the R_{ON} of any two channels.

$R_{FLAT (ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by $R_{FLAT (ON)}$.

I_S (Off)
I_S (Off) is the source leakage current with the switch off.

I_D (Off)
I_D (Off) is the drain leakage current with the switch off.

I_D (On), I_S (On)
I_D (On) and I_S (On) represent the channel leakage currents with the switch on.

V_{INL}
V_{INL} is the maximum input voltage for Logic 0.

V_{INH}
V_{INH} is the minimum input voltage for Logic 1.

I_{INL}, I_{INH}
I_{INL} and I_{INH} represent the low and high input currents of the digital inputs.

C_D (Off)
C_D (Off) represents the off switch drain capacitance, which is measured with reference to ground.

C_S (Off)
C_S (Off) represents the off switch source capacitance, which is measured with reference to ground.

C_D (On), C_S (On)
C_D (On) and C_S (On) represent on switch capacitances, which are measured with reference to ground.

C_{IN}
C_{IN} is the digital input capacitance.

t_{ON}
t_{ON} represents the delay between applying the digital control input and the output switching on.

t_{OFF}
t_{OFF} represents the delay between applying the digital control input and the output switching off.

t_D
t_D represents the off time measured between the 80% point of both switches when switching from one address state to another.

Off Isolation
Off isolation is a measure of unwanted signal coupling through an off switch.

Charge Injection
Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk
Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
Bandwidth is the frequency at which the output is attenuated by 3 dB.

On Response
On response is the frequency response of the on switch.

Insertion Loss
Insertion loss is the loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

AC Power Supply Rejection Ratio (ACPSRR)
ACPSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADGS5412 is a set of serially controlled, quad SPST switches with error detection features. SPI mode 0 or mode 3 can be used with the device and it will operate with SCLK frequencies up to 50MHz The default mode for the ADGS5412 is Addressable Mode in which the devices registers are accessed by a 16 bit SPI command that is bounded by $\overline{CS}$. The SPI command becomes 24 bit if the user enables CRC error detection. Other error detection features include SCLK Count Error and Invalid Read/Write Error. If any of these SPI interface errors occur, they are detectable by reading the Error Flags Register. The ADGS5412 can also operate in two other modes, namely Burst Mode and Daisy Chain Mode.

The interface pins of the ADGS5412 are $\overline{CS}$, SCLK, SDI and SDO. Hold $\overline{CS}$ low when using the SPI interface. Data is captured on SDI on the rising edge of SCLK and data is propagated out on SDO on the falling edge of SCLK. SDO has an open drain output so connect a pull-up to this output. When not pulled low by the ADGS5412, SDO is in a high-impedance state.

ADDRESSABLE MODE

Addressable mode is the default mode for the ADGS5412 upon power up. A single SPI frame in addressable mode is bounded by a $\overline{CS}$ falling edge and the succeeding $\overline{CS}$ rising edge. It is comprised of 16 SCLK cycles. The timing diagram for Addressable Mode is seen in Figure 34. The first SDI bit indicates if the SPI command is a read or write command. The next seven bits determine the target Register Address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command as during these clock cycles SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the 9th to the 16th SCLK falling edge during SPI reads. A Register write will occur on the 16th SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at SDO are 0x25.

ERROR DETECTION FEATURES

Protocol and communication errors on the SPI interface are detectable. There are three detectable errors which are incorrect SCLK count, invalid R/W address and Cyclic Redundancy Check (CRC). Each of these errors has a corresponding enable bit in the Error Configuration Register. In addition, there is an error flag bit for each of these errors in the Error Flags Register.

Cyclic Redundancy Check Error Detection

The CRC Error Detection feature extends a valid SPI frame by 8 SCLK cycles. These 8 extra cycles are needed to send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: R/$\overline{W}$ bit, Register address bits [6:0] and Register data bits [7:0]. The CRC polynomial used in the SPI block is $x^8+x^2+x^1+1$ with a seed value of 0. For a timing diagram with CRC enabled, see Figure 35. Register writes occur at the 24th SCLK rising edge with CRC Error Checking enabled.

During a SPI write, the microcontroller/CPU should provide the CRC byte through SDI. The SPI block checks the CRC byte just before the 24th SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI interface. The CRC error flag is asserted in the Error Flags Register in the case of the incorrect CRC byte being detected.

During a SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC Error Detection feature is disabled by default and can be configured by the user through the Error Configuration Register.

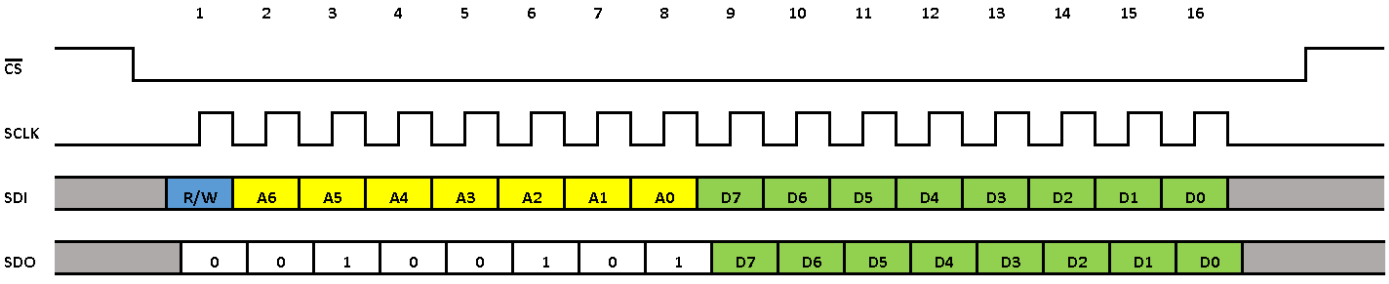


Figure 34. Addressable Mode Timing Diagram

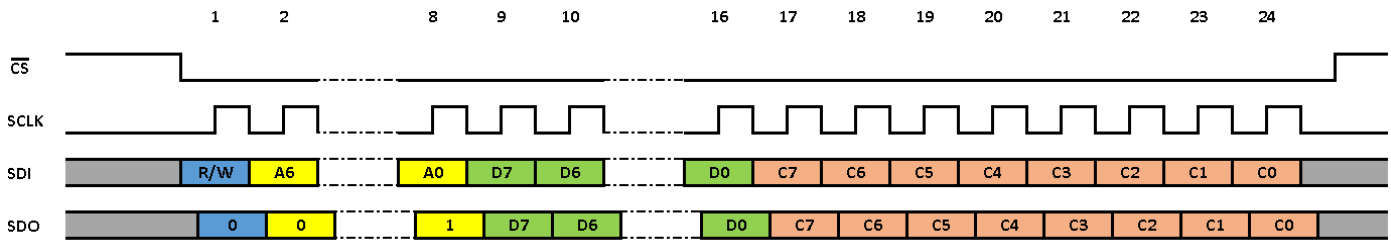


Figure 35. Timing Diagram with CRC enabled

SCLK Count Error Detection

SCLK count error allows the user to detect if an incorrect number of SCLK cycles have been sent by the microcontroller/CPU. When in addressable mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected then the SCLK Count Error Flag will assert in the Error Flags Register. When less than 16 SCLK cycles are received by the device, a write to the register map will never occur. When the ADGS5412 receives more than 16 SCLK cycles, a write to the memory map will still occur at the 16th SCLK rising edge and the flag will assert in the Error Flags Register. With CRC enabled, the expected number of SCLK cycles becomes 24. SCLK Count Error Detection is enabled by default and can be configured by the user through the Error Configuration Register.

Invalid Read/Write Address Error

Invalid Read/Write Address Error detects when a non-existent register address is a target for a read or write. In addition, this error asserts when a write to a read-only register is attempted. The Invalid Read/Write Address Error Flag will assert in the Error Flags Register when an Invalid Read/Write Address Error happens. The Invalid Read/Write Address Error is detected on the 9th SCLK rising edge which means a write to the register will never occur when an invalid address is targeted. Invalid Read/Write Address Error Detection is enabled by default and can be disabled by the user through the Error Configuration Register.

CLEARING THE ERROR FLAGS REGISTER

Clear the Error Flags Register by writing the special 16-bit SPI frame, 0x6CA9, to the device. This SPI command will not trigger the invalid R/W address error. When CRC is enabled, the user must also send the correct CRC byte for a successful error clear command. At the 16th or 24th SCLK rising edge, the Error Flags Register will reset to zero.

BURST MODE

The SPI interface has the ability to accept consecutive SPI commands without the need to de-assert the $\overline{CS}$ line. This is called Burst Mode and it is enabled through the Burst Enable Register. This mode uses the same 16-bit command to communicate with the device. In addition, the device's response at SDO is still aligned with the corresponding SPI command.

Figure 36 shows an example of SDI and SDO during Burst Mode.

Invalid Read/Write Address and CRC Error checking function operate in the same way during burst mode. However, SCLK count error detection operates in a slightly different manner. The total number of SCLK cycles within a given $\overline{CS}$ frame are counted and if the total is not a multiple of 16, or a multiple of 24 when CRC is enabled, then the SCLK count error flag will assert.

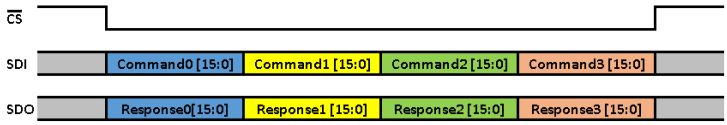


Figure 36. Burst Mode Frame

SOFTWARE RESET

When in Addressable Mode, the user can initiate a Software Reset. To do this write two consecutive SPI commands, namely 0xA3 followed by 0x05, targeting address 0x0B. After a software reset all register values are set to default.

DAISY-CHAIN MODE

The connection of several ADGS5412 devices in a Daisy-Chain configuration is possible and Figure 37 illustrates this. All devices share the same $\overline{CS}$ and SCLK line while the SDO of a device forms a connection to the SDI of the next device creating a shift register. In Daisy-Chain Mode, SDOUT is an 8-cycle delayed version of SDIN. When in Daisy-Chain Mode, all commands target the Switch Data Register. Hence, it is not possible to make configuration changes while in daisy-chain mode.

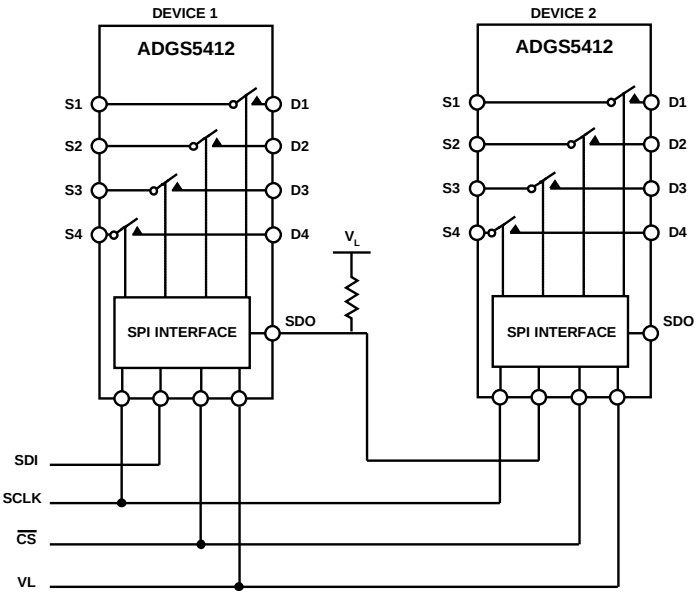


Figure 37. Two ADGS5412 connected in a Daisy-Chain Configuration

The ADGS5412 may only enter daisy-chain mode when in addressable mode by sending the 16-bit SPI command, 0x2500. See Figure 38 for an example of this. When the ADGS5412 receives this command, the SDO of devices sends out the same command. This is because the alignment bits at SDO are 0x25. This allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit Daisy-Chain Mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 39. When $\overline{CS}$ goes high Device1 will write Command0 [7:0] to its Switch Data Register of, Device 2 will write Command1 [7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering daisy-chain mode the first eight bits sent out by SDO are 0x00. When $\overline{CS}$ goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on SDI while data is propagated out SDO on an SCLK falling edge. The expected number of SCLK cycles should be a multiple of eight before CSB goes high. When this is not the case, the SPI interface sends the the last eight bits received to the Switch Data Register.

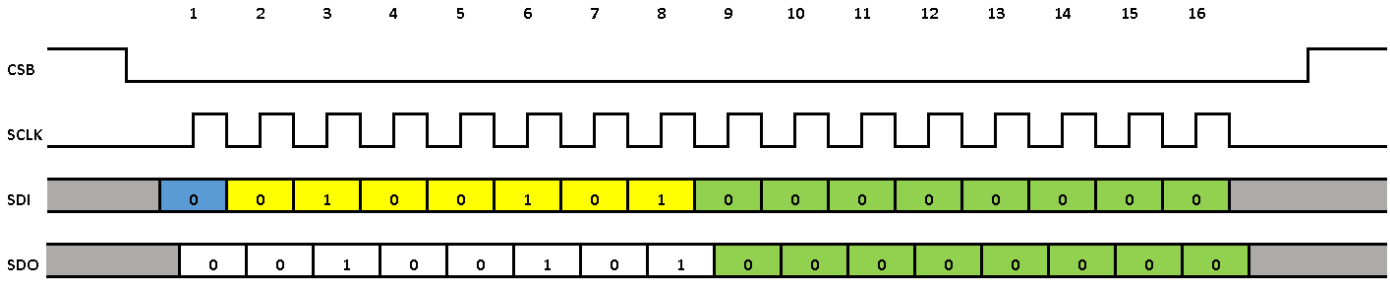


Figure 38. SPI Command to enter Daisy-Chain Mode

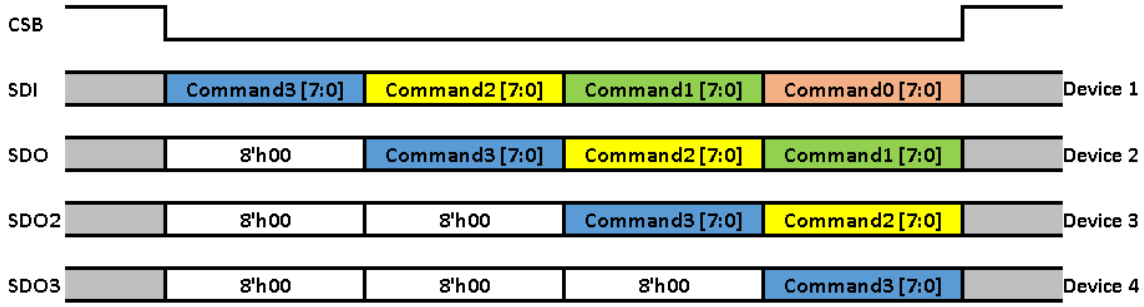


Figure 39. Example of a SPI Frame when Four ADGS5412 are connected in Daisy-Chain Mode

TRENCH ISOLATION

In the analog switch section of the ADGS5412, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, and the result is a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode can become forward-biased. A silicon controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current that, in turn, leads to latch-up. With trench isolation, this diode is removed, and the result is a latch-up proof switch.

The high voltage latch-up proof family of switches and multiplexers provide a robust solution for instrumentation, industrial, automotive, aerospace, and other harsh environments that are prone to latch-up, which is an undesirable high current state that can lead to device failure and persists until the power supply is turned off. The ADGS5412 high voltage switches allow single-supply operation from 9 V to 40 V and dual-supply operation from ±9 V to ±22 V.

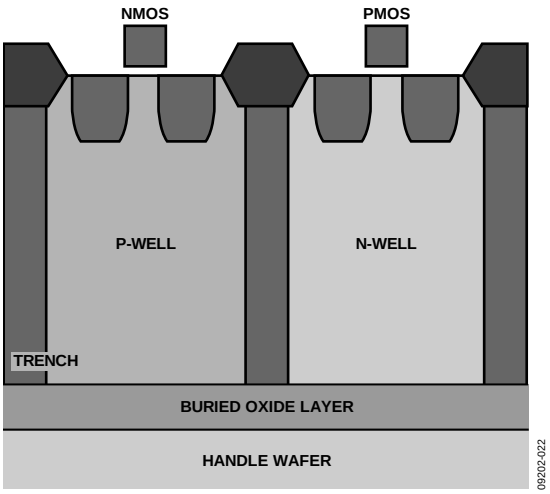


Figure 40. Trench Isolation

REGISTER SUMMARY

Table 9. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	RW
0x01	SW_DATA	[7:0]	RESERVED				SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/W
0x02	ERR_CONFIG	[7:0]	RESERVED					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	[7:0]	RESERVED					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	[7:0]	RESERVED							BURST_MODE_EN	0x00	R/W
0x0B	SOFT_RESETB	[7:0]	SOFT_RESETB								0x00	R/W

REGISTER DETAILS

SWITCH DATA REGISTER

Address: 0x01, Reset: 0x00, Name: SW_DATA

The Switch Data Register controls the status of the four switches of the ADGS5412.

Table 10. Bit Descriptions for SW_DATA

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
3	SW4_EN		Enable bit for SW4.	0x0	R/W
		0	SW4 open		
		1	SW4 closed		
2	SW3_EN		Enable bit for SW3.	0x0	R/W
		0	SW3 open		
		1	SW3 closed		
1	SW2_EN		Enable bit for SW2.	0x0	R/W
		0	SW2 open		
		1	SW2 closed		
0	SW1_EN		Enable bit for SW1.	0x0	R/W
		0	SW1 open		
		1	SW1 closed		

ERROR CONFIGURATION REGISTER

Address: 0x02, Reset: 0x06, Name: ERR_CONFIG

The Error Configuration Register allows the user to enable/disable the relevant error features as required.

Table 11. Bit Descriptions for ERR_CONFIG

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
2	RW_ERR_EN		Enable bit for detecting invalid Read/Write Address.	0x1	R/W
		0	Disabled		
		1	Enabled		
1	SCLK_ERR_EN		Enable bit for detecting the correct number of SCLK cycles in a SPI frame. 16 SCLK cycles are expected when CRC is disabled and burst mode is disabled. 24 SCLK cycles are expected when CRC is enabled and burst mode is disabled. A multiple of 16 SCLK cycles are expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles are expected when CRC is enabled and burst mode is enabled.	0x1	R/W
		0	Disabled		
		1	Enabled		
0	CRC_ERR_EN		Enable bit for CRC error detection. SPI frames should be 24-Bit wide when enabled.	0x0	R/W
		0	Disabled		
		1	Enabled		

ERROR FLAGS REGISTER

Address: 0x03, Reset: 0x00, Name: ERR_FLAGS

The Error Flags Register allows the user determine if an error has occurred. To clear the Error Flags Register the special 16-bit SPI command 0x6CA9 is to be written to the device. This SPI command will not trigger the invalid R/W address error. When CRC is enabled then the user must include the correct CRC byte during the SPI write in order for the clear Error Flags Register command to be successful.

Table 12. Bit Descriptions for ERR_FLAGS

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	RESERVED		These bits are reserved and are set to 0.	0x0	R
2	RW_ERR_FLAG		Error Flag for invalid Read/Write Address. The error flag asserts during a SPI read if the target address does not exist. The error flag will also assert when the target address of a SPI write is does not exist or is read-only.	0x0	R
		0	No Error		
		1	Error		
1	SCLK_ERR_FLAG		Error Flag for the detection of the correct number of SCLK cycles in a SPI frame.	0x0	R
		0	No Error		
		1	Error		
0	CRC_ERR_FLAG		Error Flag that determines if a CRC error has taken place during a register write.	0x0	R
		0	No Error		
		1	Error		

BURST ENABLE REGISTER

Address: 0x05, Reset: 0x00, Name: BURST_EN

The Burst Enable Register allows the user to enable/disable the Burst Mode. When enabled, the user can send multiple consecutive SPI commands without de-asserting $\overline{CS}$.

Table 14. Bit Descriptions for BURST_EN

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	RESERVED		These bits are reserved; set these bits to 0.	0x0	R
0	BURST_MODE_EN		Burst Mode Enable bit.	0x0	R/W
		0	Disabled		
		1	Enabled		

SOFTWARE RESET REGISTER

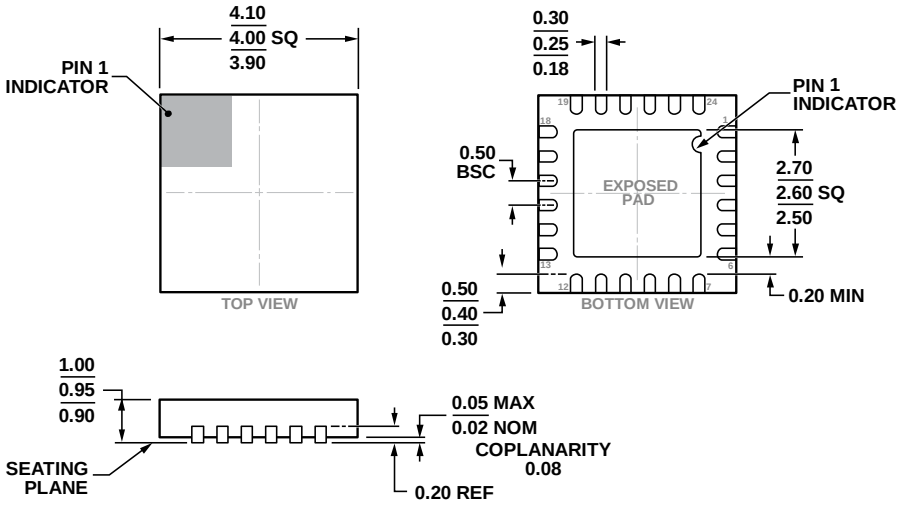
Address: 0x0B, Reset: 0x00, Name: SOFT_RESETB

This register is used to perform a software reset. Consecutively write 0xA3 and 0x05 to this register and the device's registers will reset to their default state.

Table 15. Bit Descriptions for SOFT_RESETB

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To Perform a Software Reset, consecutively write 0xA3 followed by 0x05 to this register.	0x0	R

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 41. 24-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body and 0.95 mm Package Height
(CP-24-17)
Dimensions shown in millimeters

NOTES

©2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
PR15234-0-10/16(PrB)