Data Sheet

ADIS16545/ADIS16547

Tactical Grade, Six Degrees of Freedom Inertial Sensors

FEATURES

- Triaxial, digital gyroscope
  - ±125°/sec, ±450°/sec, ±2000°/sec dynamic range options
  - ±0.15° axis to axis misalignment error (1 σ)
  - ±0.15° axis to package misalignment error (1 σ)
  - 0.5°/hr in run bias stability (1 σ, ADIS16545-1BMLZ, ADIS16547-1BMLZ)
  - 0.07°/√hr angular random walk (1 σ, ADIS16545-1BMLZ, ADIS16547-1BMLZ)
  - 63°/hr bias repeatability
- Triaxial accelerometer, ±8 *g*, ±40 *g*
  - 2.8 µ*g* in run bias stability (ADIS16545)
  - 13 µ*g* in run bias stability (ADIS16547)
- Triaxial delta angle and delta velocity outputs
- Factory calibrated sensitivity, bias, and axial alignment
  - Calibration temperature range: −40°C ≤ T_C ≤ +85°C
- SPI compatible data interface
- Programmable operation and control
  - Automatic and manual bias correction controls
  - Configurable FIR filters, 120 taps
  - Digital input and output: data ready, external clock
  - Sample clock options: internal or external, which includes direct sync or scaled sync
  - Continuous monitoring of inertial sensors
  - On-demand self test of inertial sensors
- Single-supply operation: 3.0 V to 3.6 V
- 1200 *g* mechanical shock survivability
- Operating temperature range: −40°C to +105°C

APPLICATIONS

- Precision instrumentation, stabilization
- Guidance, navigation, control
- Avionics, unmanned vehicles
- Precision autonomous machines, robotics

GENERAL DESCRIPTION

The ADIS16545/ADIS16547 are a complete inertial system that includes a triaxis gyroscope and a triaxis accelerometer. Each inertial sensor in the ADIS16545/ADIS16547 combines with signal conditioning that optimizes dynamic performance. The factory calibration characterizes each sensor for sensitivity, bias, and alignment. As a result, each sensor has its own dynamic compensation formulas that provide accurate sensor measurements.

The ADIS16545/ADIS16547 provide a simple, cost effective method for integrating accurate, multiaxis inertial sensing into industrial systems, especially when compared with the complexity and investment associated with discrete designs. All necessary motion testing and calibration are part of the production process at the factory, greatly reducing system integration time. Tight orthogonal alignment and precision alignment features simplify inertial frame alignment in navigation systems. The serial peripheral interface (SPI) and register structure provide a simple interface for data collection and configuration control.

The footprint and connector system of the ADIS16545/ADIS16547 enable a simple upgrade from the ADIS16488A, ADIS16495 and ADIS16497. Note, however, that there is a small difference in sample rate between the ADIS16495 and the ADIS16545/ADIS16547 if the internal oscillator is used. The same small difference in sample rate exists between the ADIS16497 and the ADIS16545/ADIS16547. Refer to the Specifications section for details about the native sample rate. The ADIS16545/ADIS16547 are available in an aluminum package that is approximately 47 mm × 44 mm × 14 mm and includes a standard connector interface.

FUNCTIONAL BLOCK DIAGRAM

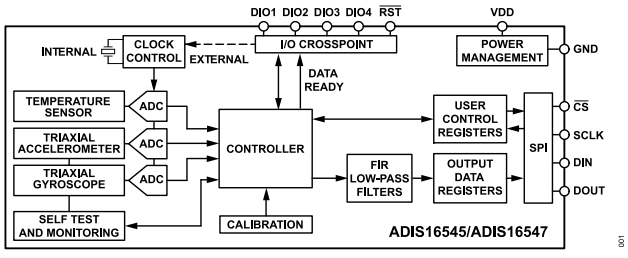

Figure 1. Functional Block Diagram

Rev. A

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

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REVISION HISTORY

5/2024—Rev. 0 to Rev. A

Changes to Features Section ... 1
Changes to Note 2 and Note 5, Table 1 ... 4

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1/2024—Revision 0: Initial Version

SPECIFICATIONS

T_C = 25°C, VDD = 3.3 V, angular rate = 0°/sec, and acceleration= ±1 *g*, unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range	ADIS16545-1BMLZ and ADIS16547-1BMLZ	±125			°/sec
	ADIS16545-2BMLZ and ADIS16547-2BMLZ	±450		±480	°/sec
	ADIS16545-3BMLZ and ADIS16547-3BMLZ	±2000			°/sec
ACCELEROMETERS	Each axis				
Dynamic Range	ADIS16545	±8			*g*
	ADIS16547	±40			*g*
TEMPERATURE SENSOR					
Scale Factor	Output = 0x0000 at 25°C (±5°C)		140		LSB/°C
LOGIC INPUTS[1]					
Input Voltage					
High, V_{IH}		2.0			V
Low, V_{IL}				0.8	V
$\overline{RST}$Pulse Width		1			µs
Input Current					
Logic 1, I_{IH}	V_{IH} = 3.3 V			10	µA
Logic 0, I_{IL}	V_{IL} = 0 V		10		µA
All Pins Except the $\overline{RST}$ and $\overline{CS}$ Pins				10	µA
$\overline{RST}$ and $\overline{CS}$ Pins[2]			0.33		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output Voltage					
High, V_{OH}	Source current (I_{SOURCE}) = 0.5 mA	2.4			V
Low, V_{OL}	Sink current (I_{SINK}) = 2.0 mA			0.4	V
FLASH MEMORY	Endurance[3]	100,000			Cycles
Data Retention[4]	T_J = 85°C	20			Years
CONVERSION RATE, f_{SM}			4		kSPS
Initial Clock Accuracy			0.02		%
Temperature Coefficient			40		ppm/°C
External Sync Input Clock, f_{SYNC}					
Direct Mode		3.0		4.5	kHz
Scaled Sync Mode		1		128	Hz
GROUP DELAY[5]	Time delay from the physical stimulus to it being reported by the inertial measurement unit (IMU)				
Gyroscopes					
≤100 Hz			1.31		ms
455 Hz			1.69		ms
Accelerometers			1.2		ms
POWER SUPPLY, VDD	Operating voltage range	3.0		3.6	V
Power Supply Current[6]	Normal mode, VDD = 3.3 V, µ + σ		140		mA

[1] The digital input and output signals use a 3.3 V system.

[2] The $\overline{RST}$ and $\overline{CS}$ pins are connected to the VDD pin through a pull-up resistor of 63 kΩ and 10 kΩ, respectively.

[3] Endurance is qualified as per JEDEC Standard 22, Method A117, measured at −40°C, +25°C, +85°C, and +125°C.

[4] The data retention specification assumes a junction temperature (T_J) of 85°C per JEDEC Standard 22, Method A117. Data retention lifetime decreases with T_J.

SPECIFICATIONS

[5] The group delay specification is with decimation and finite impulse response (FIR) low-pass filtering disabled. The variation in gyroscope group delay is due to internal digital filtering (see Figure 28).

[6] Supply current transients can reach 250 mA during initial startup or reset recovery. See Figure 58. Also, an additional 10 mA is consumed during flash update.

GYROSCOPE PERFORMANCE SPECIFICATIONS

Table 2. For ±125°/sec (ADIS16545-1BMLZ and ADIS16547-1BMLZ)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±125			°/sec
Sensitivity	32-bit		10,485,760		LSB/°/sec
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		%
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.09		%
Misalignment Error[2]	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis		±0.15		Degrees
	Axis to package		±0.15		Degrees
Nonlinearity	1 σ, FS[3] = 125°/sec, angular rate = ±62.5°/sec		0.05		% FS
	1 σ, FS = 125°/sec, angular rate = ±125°/sec		0.5		% FS
Bias	1 σ				
Repeatability[4]	−40°C ≤ T_C ≤ +85°C		63		°/hr
In Run Stability[5]			0.5		°/hr
Angular Random Walk			0.07		°/√hr
Error over Temperature[6]	−40°C ≤ T_C ≤ +85°C		43		°/hr
Linear Acceleration Effect			0.4		°/hr/*g*
Vibration Rectification Error (VRE)	Random vibration, 10 *g* RMS, 50 Hz to 2 kHz		8		°/hr
Noise					
Output Noise	No filtering, 25°C, 1 σ		0.04		°/sec RMS
Rate Noise Density[7]	1 σ		0.0016		°/sec/√Hz RMS
Bandwidth					
–3 dB			580		Hz
90° Phase Shift			191		Hz
Sensor Resonant Frequency			78		kHz

[1] Sensitivity repeatability is the root sum square (RSS) combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

[2] Cross-axis sensitivity is the sine of this number.

[3] FS means full scale.

[4] Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

[5] In run stability is the minimum of the Allan deviation curve (see Figure 9).

[6] Bias error over temperature indicates bias variation from the 25°C reference.

[7] Rate noise density is specified for 10 Hz to 40 Hz, at nominal f_{SM} sample rate, no digital filtering.

Table 3. For ±450°/sec (ADIS16545-2BMLZ and ADIS16547-2BMLZ)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±450			°/sec
Sensitivity	32-bit		2,621,440		LSB/°/sec
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.2		%
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.09		%

SPECIFICATIONS

Table 3. For ±450°/sec (ADIS16545-2BMLZ and ADIS16547-2BMLZ) (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Misalignment Error[2]	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis		±0.15		Degrees
	Axis to package		±0.15		Degrees
Nonlinearity	1 σ, FS = 450°/sec, angular rate = ±225°/sec		0.05		% FS
	1 σ, FS = 450°/sec, angular rate = ±450°/sec		0.5		% FS
Bias	1 σ				
Repeatability[3]	−40°C ≤ T_C ≤ +85°C		63		°/hr
In Run Stability[4]			0.8		°/hr
Angular Random Walk			0.07		°/√hr
Error over Temperature[5]	−40°C ≤ T_C ≤ +85°C		43		°/hr
Linear Acceleration Effect			0.3		°/hr/*g*
VRE	Random vibration, 10 *g* RMS, 50 Hz to 2 kHz		8		°/hr
Noise					
Output Noise	No filtering, 25°C, 1 σ		0.046		°/sec RMS
Rate Noise Density[6]	1 σ		0.0018		°/sec/√Hz RMS
Bandwidth					
–3 dB			550		Hz
90° Phase Shift			191		Hz
Sensor Resonant Frequency			78		kHz

[1] Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

[2] Cross-axis sensitivity is the sine of this number.

[3] Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

[4] In run stability is the minimum of the Allan deviation curve (see Figure 10).

[5] Bias error over temperature indicates bias variation from the 25°C reference.

[6] Rate noise density is specified for 10 Hz to 40 Hz, at nominal f_{SM} sample rate, no digital filtering.

Table 4. For ±2000°/sec (ADIS16545-3BMLZ and ADIS16547-3BMLZ)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
GYROSCOPES					
Dynamic Range		±2000			°/sec
Sensitivity	32-bit		655,360		LSB/°/sec
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.3		%
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.09		%
Misalignment Error[2]	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis		±0.15		Degrees
	Axis to package		±0.15		Degrees
Nonlinearity	1 σ, FS = 2000°/sec, angular rate = ±1000°/sec		0.05		% FS
	1 σ, FS = 2000°/sec, angular rate = ±2000°/sec		0.5		% FS
Bias	1 σ				
Repeatability[3]	−40°C ≤ T_C ≤ +85°C		63		°/hr
In Run Stability[4]			2.8		°/hr
Angular Random Walk			0.13		°/√hr
Error over Temperature[5]	−40°C ≤ T_C ≤ +85°C		43		°/hr
Linear Acceleration Effect			1.0		°/hr/*g*
VRE	Random vibration, 10 *g* RMS, 50 Hz to 2 kHz		8		°/hr

SPECIFICATIONS

Table 4. For ±2000°/sec (ADIS16545-3BMLZ and ADIS16547-3BMLZ) (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Noise					
Output Noise	No filtering, 25°C, 1 σ		0.08		°/sec RMS
Rate Noise Density[6]	1 σ		0.0031		°/sec/√Hz RMS
Bandwidth					
–3 dB			640		Hz
90° Phase Shift			191		Hz
Sensor Resonant Frequency			78		kHz

1 Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

2 Cross-axis sensitivity is the sine of this number.

3 Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

4 In run stability is the minimum of the Allan deviation curve (see Figure 11).

5 Bias error over temperature indicates bias variation from the 25°C reference.

6 Rate noise density is specified for 10 Hz to 40 Hz, at nominal f_{SM} sample rate, no digital filtering.

ACCELEROMETER PERFORMANCE SPECIFICATIONS

Table 5. For ±8 g (ADIS16545)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS	Each axis				
Dynamic Range		±8			*g*
Sensitivity	32-bit		262,144,000		LSB/*g*
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.014		%
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.04		%
Misalignment Error	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis		±0.15		Degrees
	Axis to package		±0.15		Degrees
Nonlinearity	FS = 8 *g*, 1 σ				
	±4 *g*		0.2		% FS
	±8 *g*		3.5		% FS
Bias	1 σ				
Repeatability[2]	−40°C ≤ T_C ≤ +85°C		1.0		m*g*
In Run Stability			2.8		µ*g*
Velocity Random Walk			0.008		m/sec/√hr
Error over Temperature[3]	−40°C ≤ T_C ≤ +85°C		±0.3		m*g*
VRE	Random vibration, 2 *g* RMS, 50 Hz to 1 kHz		16		m*g*
Noise					
Output Noise	No filtering, 25°C, 1 σ		0.5		m*g* RMS
Noise Density[4]	1 σ		15		µ*g*/√Hz RMS
Bandwidth, −3 dB			750		Hz
Sensor Resonant Frequency			2.5		kHz

1 Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

2 Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

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[3] Bias error over temperature indicates bias variation from the 25°C reference.

[4] Noise density specified for 10 Hz to 40 Hz, at nominal f_{SM} sample rate, no digital filtering.

Table 6. For ±40 g (ADIS16547)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ACCELEROMETERS	Each axis				
Dynamic Range		±40			*g*
Sensitivity	32-bit		52,428,800		LSB/*g*
Repeatability[1]	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.04		%
Error Over Temperature	−40°C ≤ T_C ≤ +85°C, 1 σ		±0.014		%
Misalignment Error	−40°C ≤ T_C ≤ +85°C, 1 σ				
	Axis to axis		±0.025		Degrees
	Axis to package		±0.15		Degrees
Nonlinearity	FS = 40 *g*, 1 σ				
	±20 *g*		0.2		% FS
	±40 *g*		3.5		% FS
Bias	1 σ				
Repeatability[2]	−40°C ≤ T_C ≤ +85°C		6.0		m*g*
In Run Stability			13		µ*g*
Velocity Random Walk			0.04		m/sec/√hr
Error over Temperature[3]	−40°C ≤ T_C ≤ +85°C		±2.2		m*g*
VRE	Random vibration, 50 Hz to 2 kHz				
	2 *g* RMS		1		m*g*
	8 *g* RMS		10		m*g*
Noise					
Output Noise	No filtering, 25°C, 1 σ		2.6		m*g* RMS
Noise Density[4]	1 σ		82		µ*g*/√Hz RMS
Bandwidth, −3 dB			750		Hz
Sensor Resonant Frequency			5.5		kHz

[1] Sensitivity repeatability is the RSS combination of the following sources of bias drift: thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C), and high temperature operating life (500 hours, +105°C).

[2] Bias repeatability is the RSS combination of the following sources of bias drift: turn-on drift, thermal hysteresis, temperature cycling (1000 cycles, −40°C to +85°C) and high temperature operating life (500 hours, +105°C).

[3] Bias error over temperature indicates bias variation from the 25°C reference.

[4] Noise density specified for 10 Hz to 40 Hz, at nominal f_{SM} sample rate, no digital filtering.

TIMING SPECIFICATIONS

T_C = 25°C, and VDD = 3.3 V, unless otherwise noted.

Table 7. Timing Specifications

		Normal Mode			Burst Read Function			
Parameter	Description	Min[1]	Typ	Max[1]	Min	Typ[2]	Max[1]	Unit
f_{SCLK}	SCLK frequency	0.01		15			10	MHz
t_{STALL}[3]	Stall period between data	5				N/A		µs
t_{CLS}	SCLK low period	31			31			ns
t_{CHS}	SCLK high period	31			31			ns
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	32			32			ns
t_{DAV}	DOUT valid after SCLK edge			10			10	ns
t_{DSU}	DIN setup time before SCLK rising edge	2			2			ns
t_{DHD}	DIN hold time after SCLK rising edge	2			2			ns

SPECIFICATIONS

Table 7. Timing Specifications (Continued)

		Normal Mode			Burst Read Function			
Parameter	Description	Min[1]	Typ	Max[1]	Min	Typ[2]	Max[1]	Unit
t_{DR} and t_{DF}	DOUT rise and fall times, ≤100 pF loading		3	8		3	8	ns
t_{DSOE}	$\overline{CS}$ assertion to DOUT active	0		11	0		11	ns
t_{HD}	SCLK edge to DOUT invalid	0			0			ns
t_{SFS}	Last SCLK edge to $\overline{CS}$ deassertion	32			32			ns
t_{DSHI}	$\overline{CS}$ deassertion to DOUT high impedance	0		9	0		9	ns
t_{NV}	Data invalid time		17			17		µs
t_1	Input sync pulse width	5			5			µs
t_2	Input sync to data invalid		240			240		µs
t_3	Input sync period[4]	222			222			µs

[1] Guaranteed by design and characterization, but not tested in production.

[2] N/A means not applicable.

[3] See Table 8 for exceptions to the stall time rating.

[4] This measurement represents the inverse of the maximum frequency for the input sample clock.

Table 8. Functional Times

Parameter	Description	Min	Typ[1]	Max	Unit
FUNCTIONAL TIMES[2]	Time until register value is updated. –40°C ≤ T_C ≤ +85°C				
Power-On Start-Up Time			290		ms
Reset Recovery Time[3]	GLOB_CMD register, Bit 7 = 1 (see Table 149)		250		ms
	$\overline{RST}$ pulled low, then restored to high		290		ms
Flash Memory Update Time, −40°C	GLOB_CMD register, Bit 3 = 1 (see Table 149)		625		ms
Flash Memory Update Time, +25°C	GLOB_CMD register, Bit 3 = 1 (see Table 149)		490		ms
Flash Memory Update Time, +85°C	GLOB_CMD register, Bit 3 = 1 (see Table 149)		450		ms
Clear User Calibration[4]	GLOB_CMD register, Bit 6 = 1 (see Table 149)		375		µs
Self Test Time	GLOB_CMD register, Bit 1 = 1 (see Table 149)		35		ms
Configure DIOx Pin Functions	FNCTIO_CTRL register (see Table 151)		550		µs
Enable and Select FIR Filter Bank 0	FILTR_BNK_0 register (see Table 165)		65		µs
Enable FIR Filter Bank 1	FILTR_BNK_1 register (see Table 167)		65		µs
Configure Autonull Function	NULL_CNFG register (see Table 159)		210		µs
Configure Input Clock Scale Factor	UPSCALE register (see Table 161)		350		µs
Configure Decimation Rate[5]	DEC_RATE Register (see Table 157)		460		µs
Configure General-Purpose Input and Output Lines	GPIO_CTRL register (see Table 153)		25		µs
Configure Miscellaneous Functions	CONFIG register (see Table 155)		45		µs
Factory Calibration Restore	GLOB_CMD, Bit 6 = 1 (see Table 149)		375		µs

[1] Waiting the amount of time listed here, and then monitoring the data ready signal for the return of regular pulsing instead of polling a status register minimizes system wait times.

[2] The functional times do not include the thermal settling and internal filter response times that can affect overall accuracy. The user must wait for the time specified in this table when executing the associated commend.

[3] The $\overline{RST}$ line must be in a low state for at least 10 µs to ensure a proper reset initiation and recovery.

[4] The factory calibration values stored in flash memory are not updated in this operation.

[5] Note that large decimation rate settings require additional time to average the large number of samples.

SPECIFICATIONS

Timing Diagrams

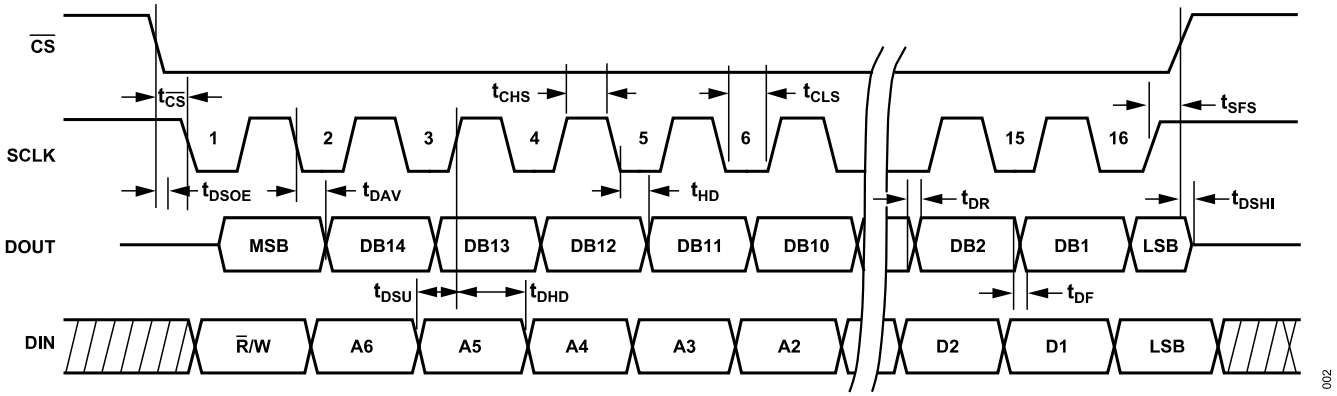


Figure 2. SPI Timing and Sequence

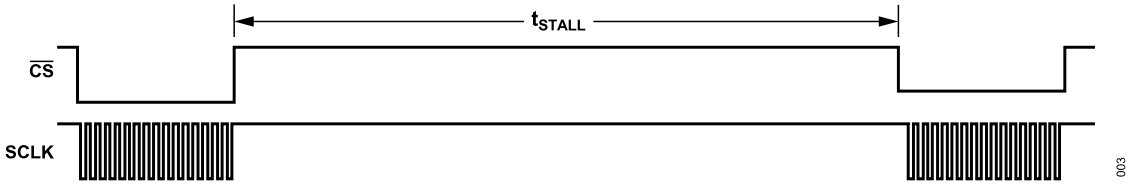


Figure 3. Stall Time and Data Rate

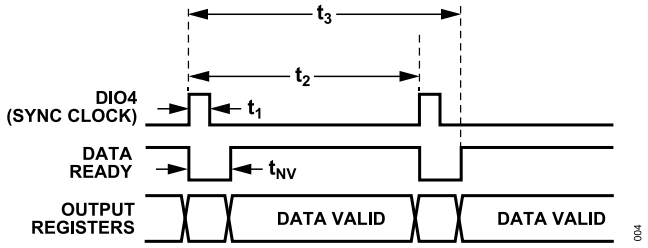
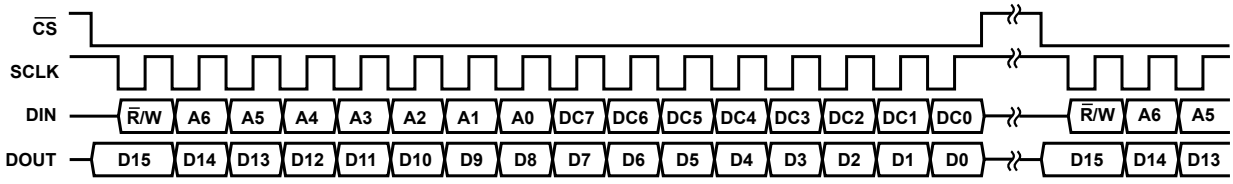


Figure 4. Input Clock Timing Diagram, FNCTIO_CTRL, Bits[7:4] = 0xFD



NOTES
1. DOUT BITS ARE PRODUCED ONLY WHEN THE PREVIOUS 16-BIT DIN SEQUENCE STARTS WITH $\overline{R}/W$ = 0.
2. WHEN $\overline{CS}$ IS HIGH, DOUT IS IN A THREE-STATE, HIGH IMPEDANCE MODE, WHICH ALLOWS MULTIFUNCTIONAL USE OF THE LINE FOR OTHER DEVICES.

Figure 5. SPI Communication Bit Sequence

SPECIFICATIONS

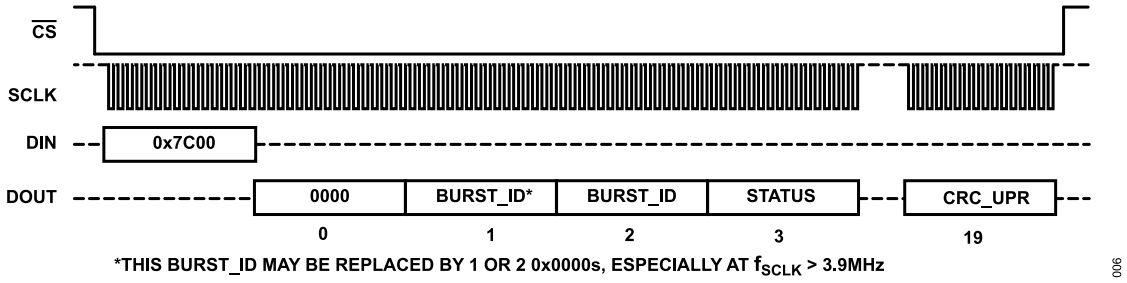


Figure 6. Burst Read Function Sequence Diagram

The burst read sequence behaves differently based on f_{SCLK}. Figure 6 shows a typical burst read sequence for $f_{SCLK} \leq 3.9$ MHz.

A burst payload contains 34 bytes of data, which includes a CRC-32. The payload can start with as many as six leading zeros followed by four burst ID bytes. The burst ID is represented by 0xA5A5. After the last burst ID byte, the subsequent 34 bytes constitute the actual payload. In the worst-case scenario, the total SPI transfer amounts to 46 bytes.

Refer to the Burst Read Code Example section for sample code implement the burst read function in a manner that handles this variation in behavior.

Refer to the Burst Read Function section for details about the registers included in a burst read.

ABSOLUTE MAXIMUM RATINGS

Table 9. Absolute Maximum Ratings

Parameter	Rating
Mechanical Shock Survivability	
Any Axis, Unpowered	1200 *g*
Any Axis, Powered	1200 *g*
VDD to GND	–0.3 V to +3.6 V
Digital Input Voltage to GND	–0.3 V to VDD + 0.2 V
Digital Output Voltage to GND	–0.3 V to VDD + 0.2 V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range[1]	–55°C to +150°C
Barometric Pressure	2 bar

[1] Extended exposure to temperatures that are lower than –40°C or higher than +105°C can adversely affect the accuracy of the factory calibration.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Pay careful attention to PCB thermal design.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction to case thermal resistance.

The ADIS16545/ADIS16547 are a multichip module, which includes many active components. The values in Table 10 identify the thermal response of the hottest component inside of the ADIS16545/ADIS16547, with respect to the overall power dissipation of the module. This approach enables a simple method for predicting the temperature of the hottest junction, based on either ambient or case temperature.

For example, when the T_C = 32.3°C (case temperature of the hottest component), the hottest junction inside of the ADIS16545/ADIS16547 is 33.56°C.

$$T_J = \theta_{JC} \times P_D + 32.3°C$$

$$T_J = 11.1°C/W \times 0.114\ W + 32.3°C$$

$$T_J = 33.56°C$$

Table 10. Package Characteristics

Package Type[1]	θ_{JA}	θ_{JC}[2]	Device Weight
ML-24-9	22.09°C/W	17.07°C/W	45 g

[1] Thermal impedance simulated values come from a case when 4 M2 × 0.4 mm machine screws (torque = 20 inch ounces) secure the ADIS16545/ADIS16547 to the PCB.

[2] θ_{JC} is the junction to the module (ADIS16545/ADIS16547) thermal resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

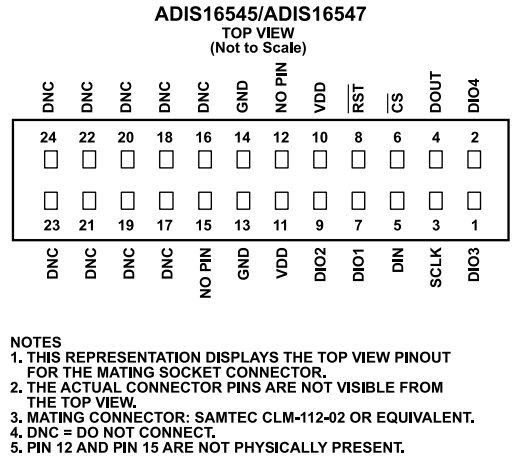


Figure 7. Pin Configuration

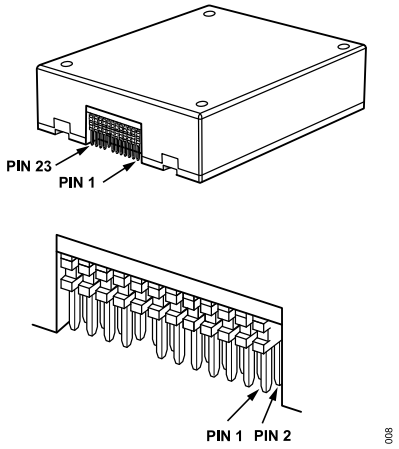


Figure 8. Pin Number Assignments

Table 11. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	DIO3	Input and Output	Configurable Digital Input and Output 3.
2	DIO4	Input and Output	Configurable Digital Input and Output 4.
3	SCLK	Input	SPI Serial Clock.
4	DOUT	Output	SPI Data Output. Clocks output on the SCLK falling edge.
5	DIN	Input	SPI Data Input. Clocks input on the SCLK rising edge.
6	$\overline{CS}$	Input	SPI Chip Select.
7	DIO1	Input and output	Configurable Digital Input and Output 1.
8	$\overline{RST}$	Input	Reset. The $\overline{RST}$ pin has an internal 63 kΩ pull-up resistor.
9	DIO2	Input and output	Configurable Digital Input and Output 2. By default, this pin is the data ready output.
10, 11	VDD	Supply	Power Supply.
12, 15	NO PIN	Not applicable	No Pin. These pins are not physically present.
13, 14	GND	Supply	Power Ground.
16 to 22	DNC	Not applicable	Do Not Connect. Do not connect to these pins.
23	DNC	Not applicable	Do Not Connect. This pin is DNC, but for backwards compatibility with previous-generation IMUs such as the ADIS16375, ADIS16480, ADIS16485, ADIS16486, ADIS16487, ADIS16488, and ADIS16488A, it is acceptable to supply 3.3 V to the DNS pin without incurring any unwanted behavior, including additional power consumption.
24	DNC	Not applicable	Do Not Connect.

TYPICAL PERFORMANCE CHARACTERISTICS

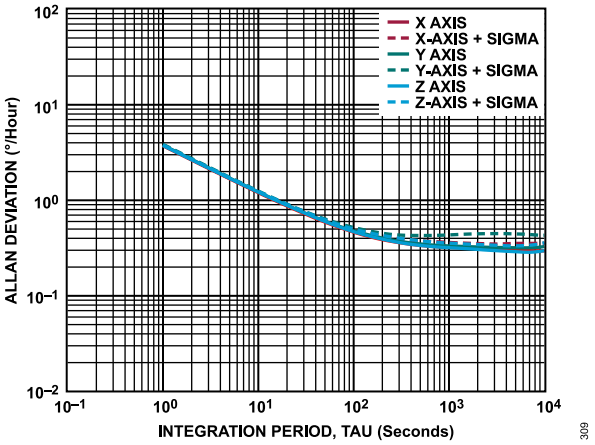


Figure 9. Gyroscope Allan Deviation, ADIS16545-1 and ADIS16547-1

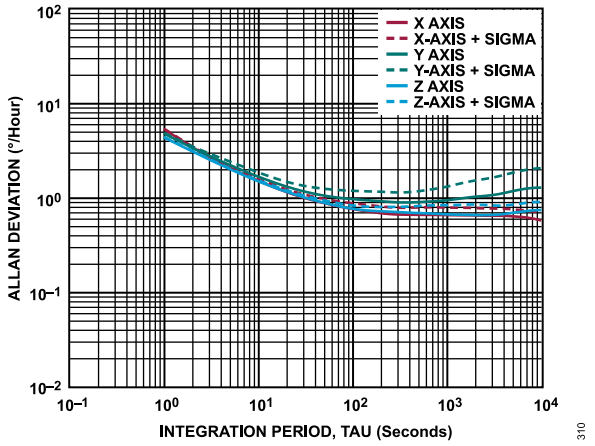


Figure 10. Gyroscope Allan Deviation, ADIS16545-2 and ADIS16547-2

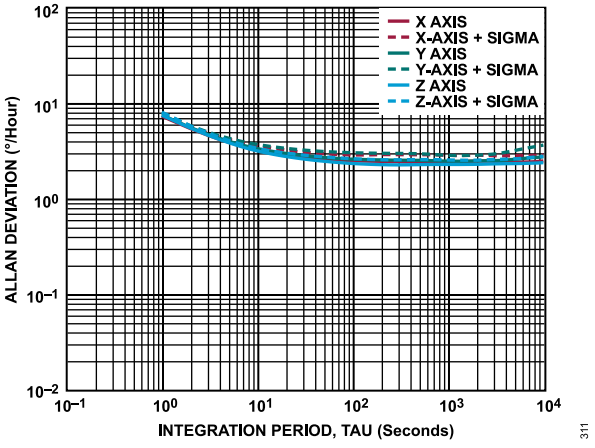


Figure 11. Gyroscope Allan Deviation, ADIS16545-3 and ADIS16547-3

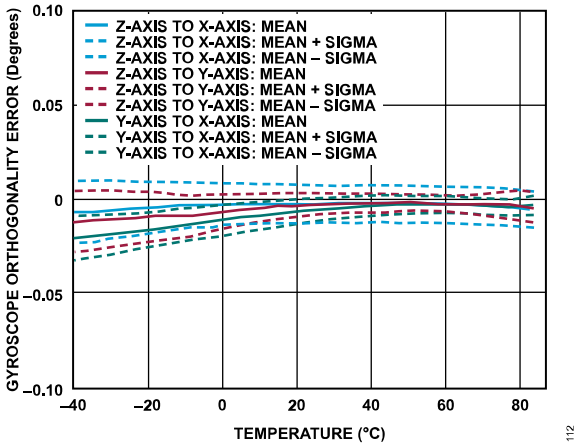


Figure 12. Gyroscope Orthogonality Error vs. Temperature

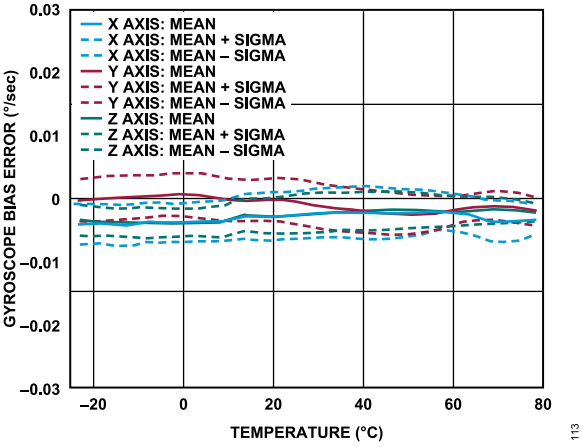


Figure 13. Gyroscope Bias Error vs. Temperature

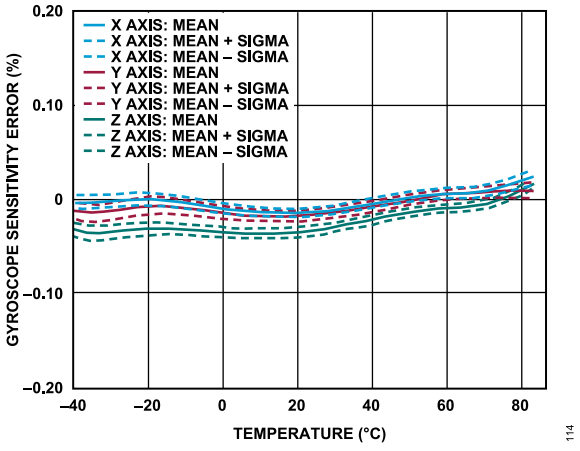


Figure 14. Gyroscope Sensitivity Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

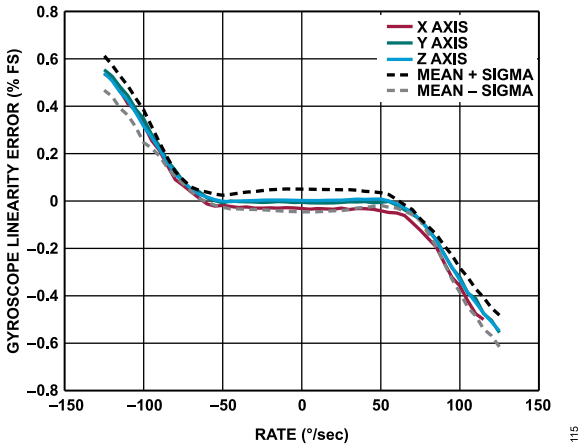


Figure 15. Gyroscope Linearity Error vs. Rate, ADIS16545-1 and ADIS16547-1

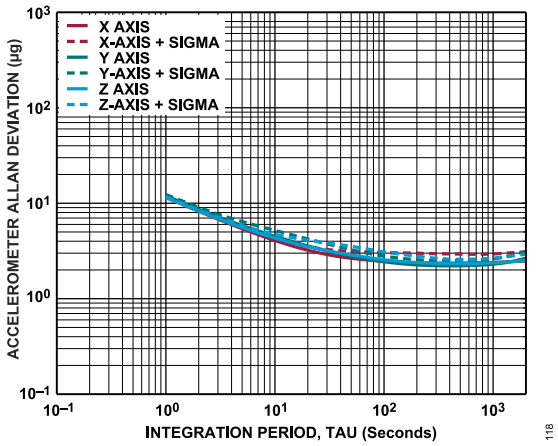


Figure 18. Accelerometer Allan Deviation ADIS16545

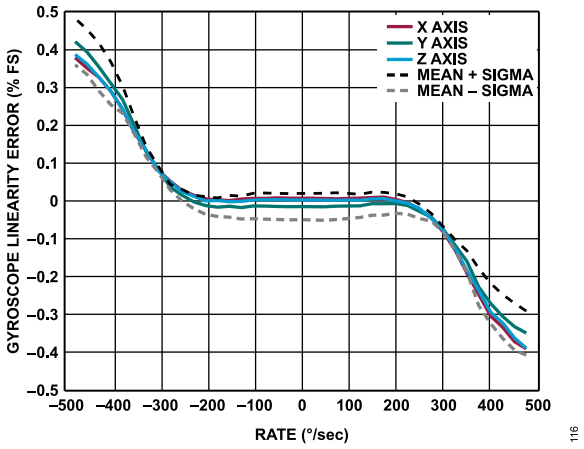


Figure 16. Gyroscope Linearity Error vs. Rate, ADIS16545-2 and ADIS16547-2

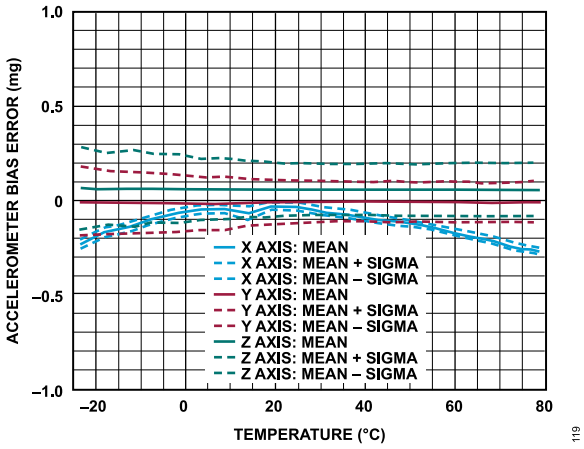


Figure 19. Accelerometer Bias Error vs. Temperature, ADIS16545

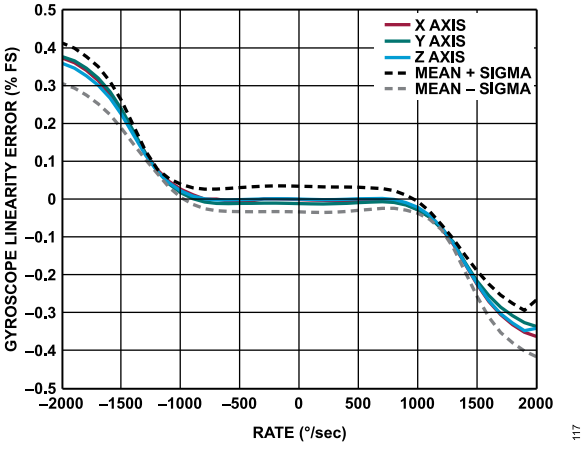


Figure 17. Gyroscope Linearity Error vs. Rate, ADIS16545-3 and ADIS16547-3

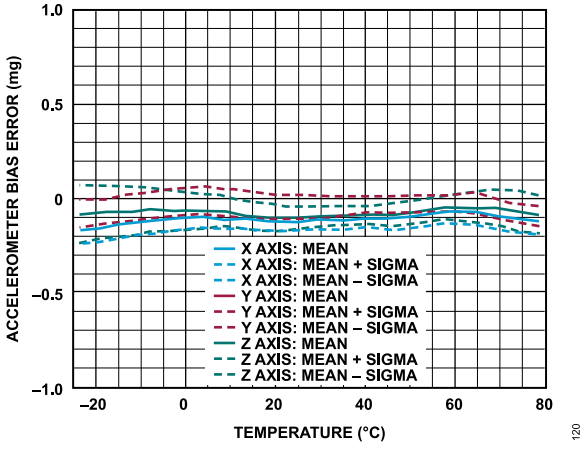


Figure 20. Accelerometer Sensitivity Error vs. Temperature, ADIS16545

TYPICAL PERFORMANCE CHARACTERISTICS

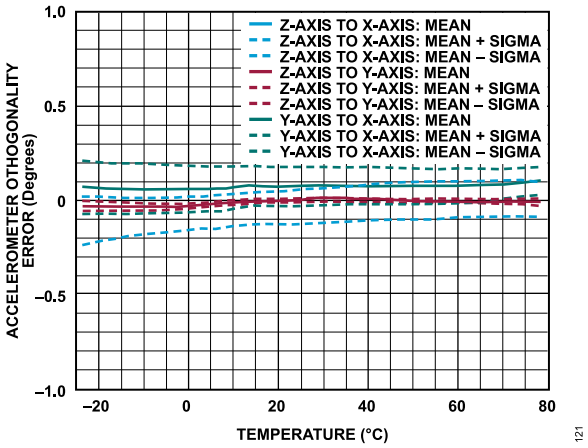


Figure 21. Accelerometer Orthogonality Error vs. Temperature, ADIS16545

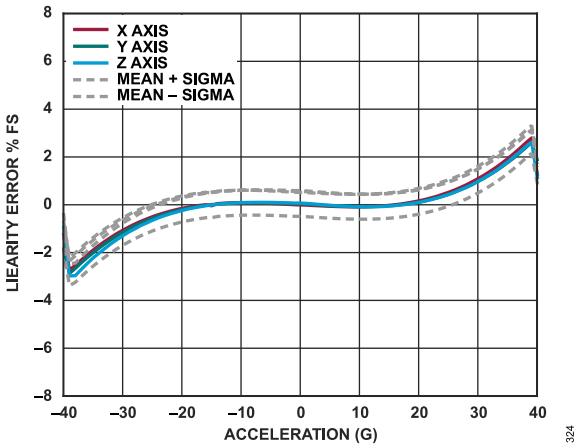


Figure 24. Accelerometer Linearity Error vs. Acceleration, ADIS16547

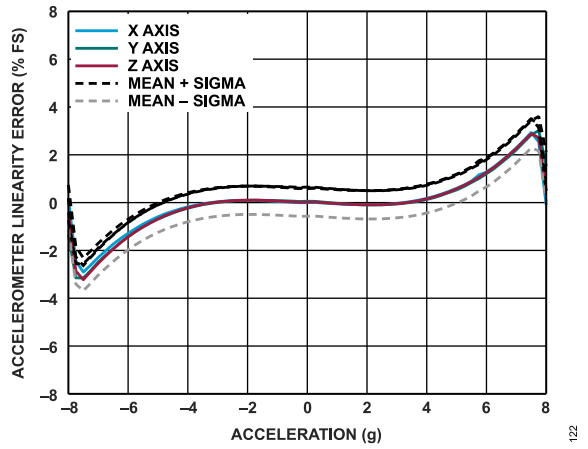


Figure 22. Accelerometer Linearity Error vs. Acceleration, ADIS16545

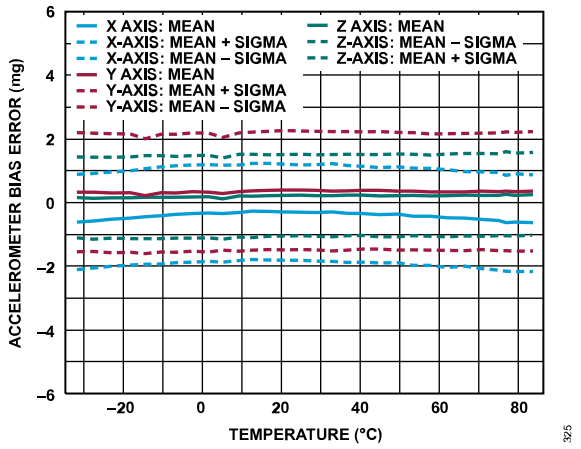


Figure 25. Accelerometer Bias Error vs. Temperature, ADIS16547

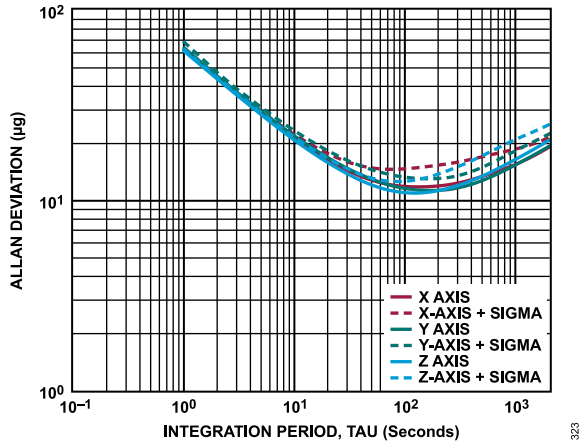


Figure 23. Accelerometer Allan Deviation Plot, ADIS16547

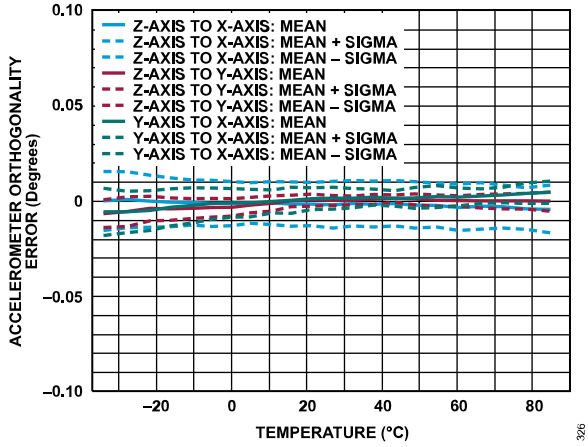


Figure 26. Accelerometer Orthogonality Error vs. Temperature, ADIS16547

TYPICAL PERFORMANCE CHARACTERISTICS

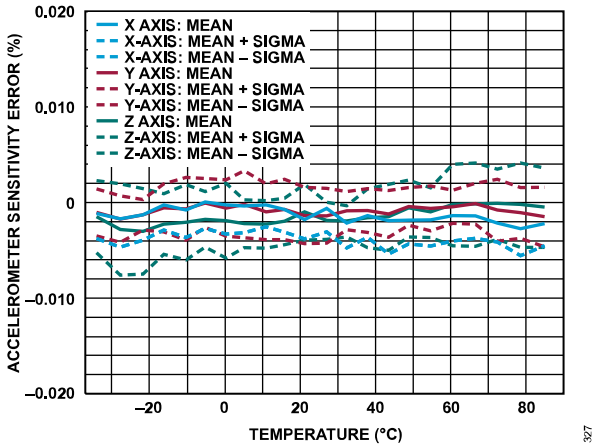


Figure 27. Accelerometer Sensitivity Error vs. Temperature, ADIS16547

THEORY OF OPERATION

The ADIS16545/ADIS16547 arean autonomous sensor system that starts up on their own when the devices have a valid power supply. After running through their initialization process, the ADIS16545/ADIS16547 begin sampling, processing, and loading calibrated sensor data into the output registers which are accessible using the SPI port.

INERTIAL SENSOR SIGNAL CHAIN

Figure 28 shows the basic signal chain for the inertial sensors in the ADIS16545/ADIS16547, which processes data at a rate of f_{SM} (see Specifications for details) when using the internal sample clock. Using one of the external clock options in FNCTIO_CTRL, Bits[7:4] (see Table 151) provides flexibility in selecting this rate.

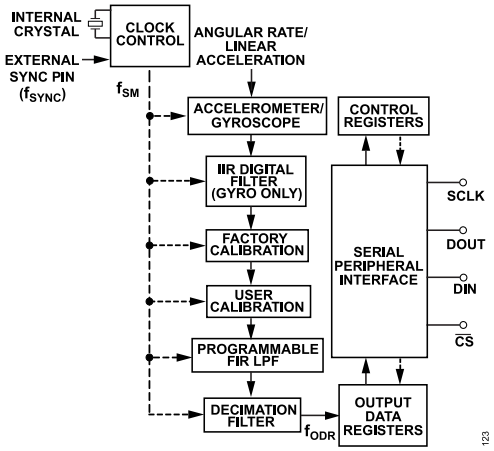


Figure 28. Signal Processing Diagram, Inertial Sensors

Gyroscope Data Sampling

Figure 29 illustrates how the ADIS16545/ADIS16547 measure angular rotation across three axes (x, y, and z). For each axis, there are four digital MEMS gyroscopes (for example, X_{G1} to X_{G4} for the x-axis) with individual ADCs producing separate data. Data processing involves summing the latest samples from all gyroscopes and rescaling. An independent clock with frequency f_{SM} drives further digital processing, including calibration and filtering. This clock, f_{SM}, can be internally produced or synchronized with an external input.

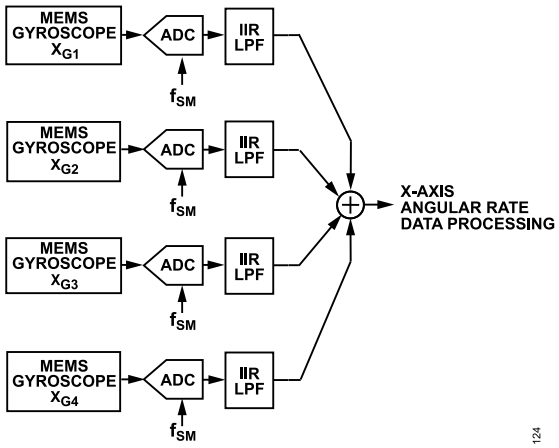


Figure 29. Gyroscope Data Sampling

Accelerometer Data Sampling

The ADIS16545/ADIS16547 produce linear acceleration measurements along the same orthogonal axes (x, y, and z) as the gyroscopes, using the same clock (f_{SM}, see Figure 29 and Figure 30) that triggers data acquisition and subsequent processing of the gyroscope data. However, unlike the gyroscope data processing, there is no infinite impulse response (IIR) low-pass filter (LPF) after the analog-to-digital converter (ADC).

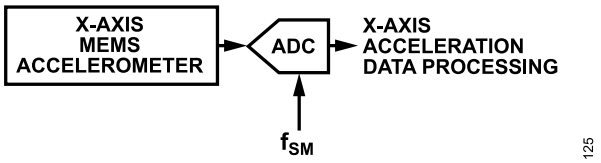


Figure 30. Accelerometer Data Sampling

External Clock Options

The ADIS16545/ADIS16547 offer two modes of operation to control data production with an external clock: direct sync and scaled sync. In direct sync mode, the external clock directly controls the data sampling and production clock (f_{SM} in Figure 29 and Figure 30). In scaled sync mode, the user can provide a lower input clock rate (1 Hz to 128 Hz) and use a scale factor (UPSCALE register, see Table 161) to establish a data collection and processing rate that is in the allowable range as specified in the Specifications. f_{SYNC} is the frequency of the external clock.

Inertial Sensor Calibration

The calibration function for the gyroscopes and the accelerometers has two components: factory and user (see Figure 31).

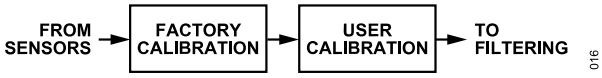


Figure 31. Gyroscope Calibration Processing

THEORY OF OPERATION

Gyroscope Factory Calibration

Gyroscope factory calibration applies the following correction formula to the data of each gyroscope:

$$\begin{pmatrix} \omega_X \\ \omega_Y \\ \omega_Z \end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{pmatrix} \times \begin{pmatrix} g_X + b_X \\ g_Y + b_Y \\ g_Z + b_Z \end{pmatrix} \quad (1)$$

where:
ω_X, ω_Y, and ω_Z are the postcalibration gyroscope data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
g_X, g_Y, and g_Z are the precalibration gyroscope data.
b_X, b_Y, and b_Z are the bias correction factors.

All the correction factors in each matrix/array are derived from direct observation of the response of each gyroscope to a variety of rotation rates at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but these factors are not available for observation. See Figure 51 for more details on the user calibration options that are available for the gyroscopes.

Accelerometer Factory Calibration

The accelerometer factory calibration applies the following correction formulas to the data of each accelerometer:

$$\begin{pmatrix} \alpha_X \\ \alpha_Y \\ \alpha_Z \end{pmatrix} = \begin{pmatrix} m_{11} & m_{12} & m_{13} \\ m_{21} & m_{22} & m_{23} \\ m_{31} & m_{32} & m_{33} \end{pmatrix} \times \begin{pmatrix} a_X + b_X \\ a_Y + b_Y \\ a_Z + b_Z \end{pmatrix} + \begin{pmatrix} 0 & p_{12} & p_{13} \\ p_{21} & 0 & p_{23} \\ p_{31} & p_{32} & 0 \end{pmatrix} \times \begin{pmatrix} {\omega^2}_X \\ {\omega^2}_Y \\ {\omega^2}_Z \end{pmatrix} \quad (2)$$

where:
α_X, α_Y, and α_Z are the postcalibration accelerometer data.
m_{11}, m_{12}, m_{13}, m_{21}, m_{22}, m_{23}, m_{31}, m_{32}, and m_{33} are the scale and alignment correction factors.
a_X, a_Y, and a_Z are the precalibration accelerometer data.
b_X, b_Y, and b_Z are the bias correction factors.
0, p_{12}, p_{13}, p_{21}, p_{23}, p_{31}, and p_{32} are the point of percussion correction factors.
ω^2_X, ω^2_Y, and ω^2_Z are the post-calibration gyroscope data (squared).

All the correction factors in each matrix/array are derived from direct observation of the response of each accelerometer to a variety of inertial test conditions at multiple temperatures across the calibration temperature range (−40°C ≤ T_C ≤ +85°C). These correction factors are stored in the flash memory bank, but these factors are not available for observation. See Figure 52 for more details on the user calibration options that are available for the accelerometers.

Filtering

After calibration, the data of each inertial sensor passes through two digital filters, both of which have user configurable attributes: FIR and decimation (see Figure 32).

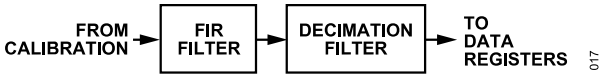


Figure 32. Inertial Sensor Filtering

The FIR filter includes four banks of coefficients that have 120 taps each. Register FILTR_BNK_0 (see Table 165) and Register FILTR_BNK_1 (see Table 167) provide the configuration options for the use of the FIR filters of each inertial sensor. Each FIR filter bank includes a preconfigured filter, but the user can design their own filters and write over these values using the register of each coefficient. Refer to FIR Filter Bank Memory Maps for details about location of the FIR filter taps for Filter Bank A, Filter Bank B, Filter Bank C, and Filter Bank D. Refer to Figure 55 for the frequency response of the factory default filters. The default filter coefficients are for common LPFs and are not tailored to any specific application environment.

The decimation filter averages multiple samples together to produce each register update. In this type of filter structure, the number of samples in the average is equal to the reduction in the update rate for the output data registers. See the DEC_RATE register for the user controls for this filter (see Table 157).

THEORY OF OPERATION

REGISTER STRUCTURE

All communication with the ADIS16545/ADIS16547 involves accessing its user registers. The register structure contains both output data and control registers. The output data registers include the latest sensor data, error flags, and identification data. The control registers include sample rate, filtering, input and output, calibration, and diagnostic configuration options. All communication between the ADIS16545/ADIS16547 and an external processor involves either reading or writing to one of the user registers.

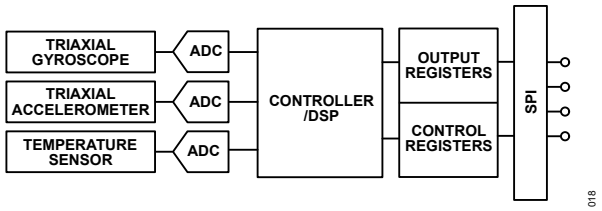


Figure 33. Basic Operation

The register structure uses a paged addressing scheme that contains 13 pages, with each page containing 64 register locations. Each register is 16 bits wide, with each byte having its own unique address within the memory map of that page. The SPI port has access to one page at a time, using the bit sequence shown in Figure 5. Select the page to activate for SPI access by writing its code to the PAGE_ID register. Read the PAGE_ID register to determine which page is currently active. Table 12 displays the PAGE_ID contents for each page and their basic functions. The PAGE_ID register is located at Address 0x00 on every page.

Table 12. User Register Page Assignments

Page	PAGE_ID	Function
0	0x00	Output data, time stamp, data counter, identification
1	0x01	Reserved
2	0x02	User calibration
3	0x03	Control: sample rate, filtering, input and output
4	0x04	Serial number, cyclic redundancy check (CRC) values
5	0x05	FIR Filter Bank A, Coefficient 0 to Coefficient 59
6	0x06	FIR Filter Bank A, Coefficient 60 to Coefficient 119
7	0x07	FIR Filter Bank B, Coefficient 0 to Coefficient 59
8	0x08	FIR Filter Bank B, Coefficient 60 to Coefficient 119
9	0x09	FIR Filter Bank C, Coefficient 0 to Coefficient 59
10	0x0A	FIR Filter Bank C, Coefficient 60 to Coefficient 119
11	0x0B	FIR Filter Bank D, Coefficient 0 to Coefficient 59
12	0x0C	FIR Filter Bank D, Coefficient 60 to Coefficient 119

THEORY OF OPERATION

SERIAL PERIPHERAL INTERFACE

The SPI provides access to all of the user accessible registers (see Table 13) and typically connects to a compatible port on an embedded processor platform.

See Figure 34 for a diagram that provides the most common connections between the ADIS16545/ADIS16547 and an embedded processor. Additional information on the SPI can be found in the Applications Information section.

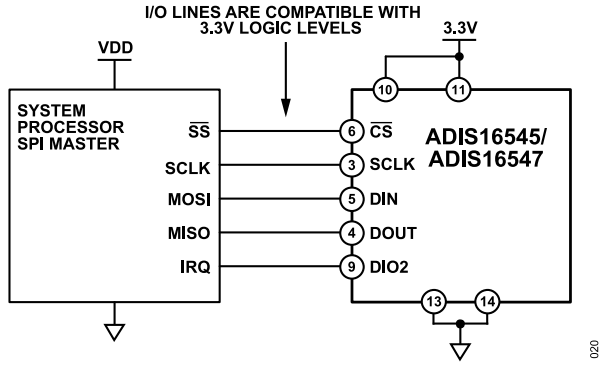


Figure 34. Electrical Connection Diagram

Table 13. Generic Host Processor Pin Names and Functions

Mnemonic	Function
$\overline{SS}$	Device select
SCLK	Serial clock
MOSI	Host output, peripheral input
MISO	Host input, peripheral output
IRQ	Interrupt request

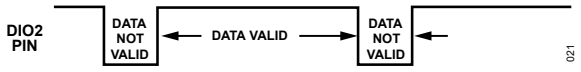
Embedded processors typically use control registers to configure their serial ports for communicating with SPI peripheral devices such as the ADIS16545/ADIS16547. Table 14 provides a list of settings that describe the SPI protocol of the ADIS16545/ADIS16547.

Table 14. Generic Host Processor SPI Settings

Processor Setting	Description
Host controller	ADIS16545/ADIS16547 operates as peripheral
SCLK < f_{SCLK}	Maximum serial clock rate
SPI Mode 3	CPOL = 1 (polarity), CPHA = 1 (phase)
MSB First Mode	Bit sequence, see Figure 5 for coding
16-Bit Mode	Shift register and data length

DATA READY

The factory default configuration provides users with a data ready (DR) signal on the DIO2 pin, which pulses low when the output data registers are updating (see Figure 35). In this configuration, connect DIO2 to an interrupt service pin on the embedded processor to trigger data collection when this signal pulses high. Register FNCTIO_CTRL, Bits[3:0] (see Table 151) provides configuration options for this function.



NOTE: THE OUTPUT DATA AND STATUS REGISTERS ARE UPDATING DURING THE "DATA NOT VALID" PERIOD SHOWN ABOVE.

Figure 35. Data Ready when FNCTIO_CTRL, Bits[3:0] = 0xD (Default)

During the start-up and reset recovery processes, the data ready (DR) signal can exhibit transient behavior before data production begins. Figure 36 provides an example of the DR behavior during startup, and Figure 37 and Figure 38 provide examples of the DR behavior during recovery from reset commands.

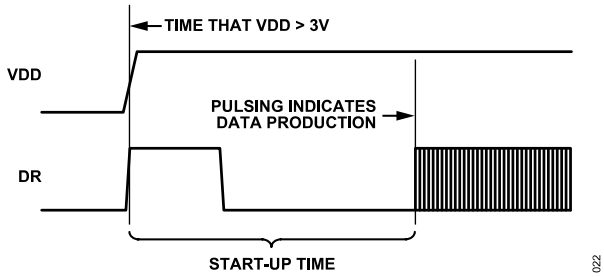


Figure 36. Data Ready Response During Startup

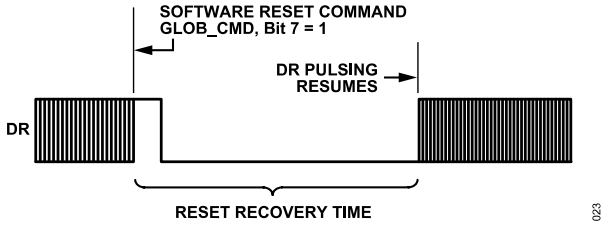


Figure 37. Data Ready Response During Software Reset (Register GLOB_CMD, Bit 7 = 1) Recovery

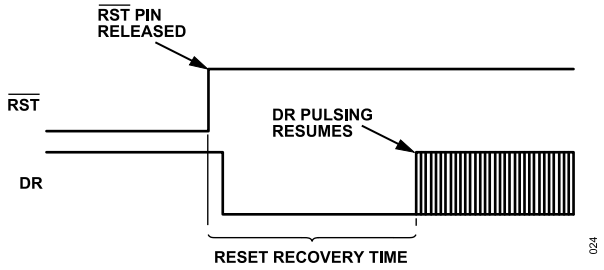


Figure 38. Data Ready Response During Reset ($\overline{RST}$ = 0) Recovery

READING SENSOR DATA

Reading a single register requires two 16-bit cycles on the SPI: one to request the contents of a register and another to receive those contents. The 16-bit command code (see Figure 5) for a read request on the SPI has three parts: the read bit ($\overline{R}/W$ = 0), the 7-bit address code for either address (upper or lower) of the register, Bits[A6:A0], and eight don't care bits, Bits[DC7:DC0]. Figure 39 provides an example that includes two register reads in succession. This example starts with DIN = 0x1A00, to request the contents of the Z_GYRO_OUT register, and follows with 0x1800, to request

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the contents of the Z_GYRO_LOW register (assuming PAGE_ID already equals 0x0000). The sequence in Figure 39 also shows full duplex mode of operation, which means that the ADIS16545/ADIS16547 can receive requests on DIN while also transmitting data out on DOUT within the same 16-bit SPI cycle.

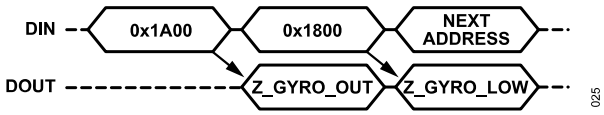

Figure 39. SPI Read Example

Figure 40 provides an example of the four SPI signals when reading the PROD_ID register (see Table 99) in a repeating pattern. This pattern can be helpful when troubleshooting the SPI setup and communications.

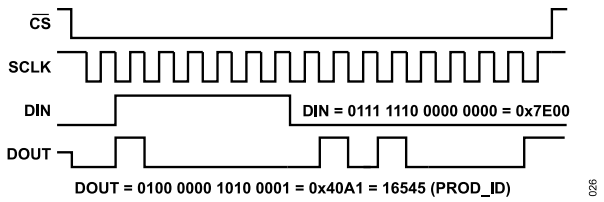

Figure 40. SPI Read Examples, Second 16-Bit Sequence

Burst Read Function

The burst read function (BRF) provides an efficient way to read a batch of data (status, temperature, gyroscopes, accelerometers, time stamp and data counter, and CRC code). The BRF does not require a stall time between each 16-bit segment and only requires one command on the DIN line to initiate. A burst read is initiated by reading the BURST_CMD register (DIN = 0x7C00) and then reading each segment of data in the response while holding the $\overline{CS}$ line low until all of the data in that burst is read. If the $\overline{CS}$ line goes high before the completion of all data acquisition, the burst read is aborted.

To read gyroscope and accelerometer data in the burst, set CONFIG, Bit 8 = 0. In this mode, the burst data format is shown in Table 15. To read the delta angle and delta velocity data in burst mode, set CONFIG, Bit 8 = 1. In this mode, the burst data format is shown in Table 16.

The BRF contains a different number of data segments (16-bits each) depending on f_{SCLK}. When f_{SCLK} < 3.9 MHz, the BRF response uses the sequencing diagram shown in Figure 6. The data format is shown in Table 15. When f_{SCLK} > 3.9 MHz, the first BURST_ID can be replaced by one or two 0x0000s. Note that in the delta angle and delta velocity burst mode, the BURST_ID is 0xC3C3 instead of 0xA5A5.

To manage the variation in burst read formats, see the code examples in the Burst Read Code Example section. These examples look for the first data segment that is not the BURST_ID code (0xA5A5 in Table 15 and 0xC3C3 in Table 16) as an identifier for when the ADIS16545/ADIS16547 BRF response is starting.

Table 15. BRF Data Format (CONFIG, Bit 8 = 0)

Segment	DIN[1]	DOUT
0	0x7C00	Dummy read from the burst command (0x0000).
1	N/A	0xA5A5 (BURST_ID). Note that this BURST_ID can be replaced by one or two 0x0000s, especially if f_{SCLK} > 3.9 MHz.
2	N/A	0xA5A5 (BURST_ID).
3	N/A	STATUS.
4	N/A	TEMP_OUT.
5	N/A	X_GYRO_LOW.
6	N/A	X_GYRO_OUT.
7	N/A	Y_GYRO_LOW.
8	N/A	Y_GYRO_OUT.
9	N/A	Z_GYRO_LOW.
10	N/A	Z_GYRO_OUT.
11	N/A	X_ACCL_LOW.
12	N/A	X_ACCL_OUT.
13	N/A	Y_ACCL_LOW.
14	N/A	Y_ACCL_OUT.
15	N/A	Z_ACCL_LOW.
16	N/A	Z_ACCL_OUT.
17	N/A	DATA_CNT (FNCTIO_CTRL, Bits[8:7] ≠ 11). TIME_STAMP (FNCTIO_CTRL, Bits[8:7] = 11).
18	N/A	CRC_LWR.
19	N/A	CRC_UPR.

[1] N/A means not applicable.

Table 16. BRF Data Format (CONFIG, Bit 8 = 1)

Segment	DIN[1]	DOUT
0	0x7C00	Dummy read from the burst command (0x0000).
1	N/A	0xC3C3 (BURST_ID. Note that this BURST_ID can be replaced by one or two 0x0000s, especially if f_{SCLK} > 3.9 MHz.
2	N/A	0xC3C3 (BURST_ID).
3	N/A	STATUS.
4	N/A	TEMP_OUT.
5	N/A	X_DELTANG_LR.
6	N/A	X_DELTANG_UR.
7	N/A	Y_DELTANG_LR.
8	N/A	Y_DELTANG_UR.
9	N/A	Z_DELTANG_LR.
10	N/A	Z_DELTANG_UR.
11	N/A	X_DELTVEL_LR.
12	N/A	X_DELTVEL_UR.
13	N/A	Y_DELTVEL_LR.
14	N/A	Y_DELTVEL_UR.
15	N/A	Z_DELTVEL_LR.

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Table 16. BRF Data Format (CONFIG, Bit 8 = 1) (Continued)

Segment	DIN[1]	DOUT
16	N/A	Z_DELTVEL_UR.
17	N/A	DATA_CNT (FNCTIO_CTRL, Bits[8:7] ≠ 11). TIME_STAMP (FNCTIO_CTRL, Bits[8:7] = 11).
18	N/A	CRC_LWR.
19	N/A	CRC_UPR.

[1] N/A means not applicable.

DEVICE CONFIGURATION

Each register contains 16 bits (two bytes). Bits[7:0] contain the low byte, and Bits[15:8] contain the high byte. Each byte has its own unique address in the user register map (see Table 17). Updating the contents of a register requires writing to its low byte first and its high byte second. The three parts to coding a SPI command (see Figure 5), which writes a new byte of data to a register, are: the write bit ($\overline{R}/W$ = 1), the 7-bit address code (Bits[A6:A0]) for the byte that this command is updating, and the new data for that location (Bits[DC7:DC0]). Figure 41 provides a coding example for writing 0xFEDC to the XG_BIAS_LOW register (see Table 113), assuming that PAGE_ID already equals 0x0002.

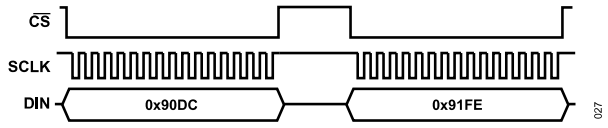

Figure 41. SPI Sequence for Writing 0xFEDC to XG_BIAS_LOW

Dual-Memory Structure

The ADIS16545/ADIS16547 use a dual-memory structure (see Figure 42), with static random access memory (SRAM) supporting real-time operation and on-board flash memory providing nonvolatile storage of operational code, calibration coefficients, and user configurable register settings. The manual flash memory update command (GLOB_CMD, Bit 3, see Table 149) provides a single-command method for storing user configuration settings into flash memory. The user settings stored in flash are automatically loaded during the next power-on or reset.

The flash memory has two parts. The first part is the program memory, which contains the firmware, and the second part contains the factory calibration and user settings.

During power-on or reset recovery, the ADIS16545/ADIS16547 perform a CRC check on the program memory to determine if the backup program memory (second copy) should be used instead. If this memory test fails, the ADIS16545/ADIS16547 reset and boot up from the other flash memory location. STATUS, Bit 1 (see Table 23) provides an error flag for detecting when the backup flash memory supported the last power-on or reset recovery. The program memory CRC error also flags in STATUS, Bit 2.

The second area of flash memory that stores the factory calibration and user settings has two independent banks that operate in a ping-pong manner, alternating with every flash update. The loading of the ping-pong memory for calibration and user settings uses only the newest copy in memory even if it has an error. However, any CRC error in either program memory, calibration values, or user settings are flagged in Bit 2 of the Status and Error Flag Indicators (STATUS) register. See Continuous SRAM Testing for more information on reading both the factory-programmed signature and derived CRC values.

The Table 17 provides a memory map for the user registers in the ADIS16545/ADIS16547 and includes a column indicating if flash backup support is available for a given register. This information is indicated by yes or no in the Flash Backup column.

The user CRC calculation includes the following registers: FNCTIO_CTRL, CONFIG, DEC_RATE, NULL_CNFG, RANGE_MDL, FILTR_BNK_0, and FILTR_BANK1. Also included in the user CRC are all FIR coefficient registers, all user scale and bias registers, and temporary registers holding the users SPI writes until these writes are processed.

Replace the ADIS16545/ADIS16547 if either the continuous CRC error is persistent or if the ADIS16545/ADIS16547 boot up using the backup copy of the firmware.

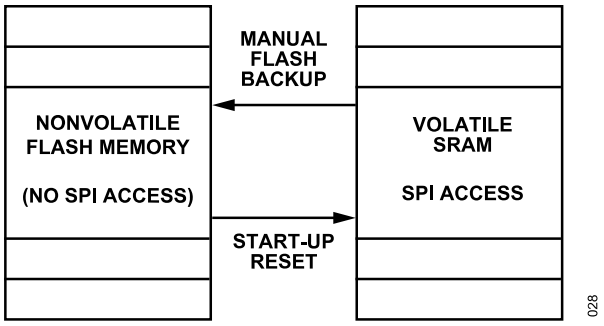

Figure 42. SRAM and Flash Memory Diagram

USER REGISTER MEMORY MAP

Table 17. User Register Memory Map[1]

Register Name	R/W	Flash Backup	PAGE_ID	Addresses	Default	Register Description
PAGE_ID	R/W	No	0x00	0x00, 0x01	0x0000	Page identifier. This register must be set to 0x00 in order to access registers on Page 0.
Reserved	N/A	N/A	0x00	0x02, 0x03	N/A	Reserved.
DATA_CNT	R	No	0x00	0x04, 0x05	N/A	Data counter.
Reserved	N/A	N/A	0x00	0x06, 0x07	N/A	Reserved.
STATUS	R	No	0x00	0x08, 0x09	0x0000	Output, system error flags.
DIAG_STS	R	No	0x00	0x0A, 0x0B	0x0000	Output, self test error flags.
Reserved	N/A	N/A	0x00	0x0C, 0x0D	N/A	Reserved.
TEMP_OUT	R	No	0x00	0x0E, 0x0F	N/A	Output, temperature.
X_GYRO_LOW	R	No	0x00	0x10, 0x11	N/A	Output, x-axis gyroscope, low word.
X_GYRO_OUT	R	No	0x00	0x12, 0x13	N/A	Output, x-axis gyroscope, high word.
Y_GYRO_LOW	R	No	0x00	0x14, 0x15	N/A	Output, y-axis gyroscope, low word.
Y_GYRO_OUT	R	No	0x00	0x16, 0x17	N/A	Output, y-axis gyroscope, high word.
Z_GYRO_LOW	R	No	0x00	0x18, 0x19	N/A	Output, z-axis gyroscope, low word.
Z_GYRO_OUT	R	No	0x00	0x1A, 0x1B	N/A	Output, z-axis gyroscope, high word.
X_ACCL_LOW	R	No	0x00	0x1C, 0x1D	N/A	Output, x-axis accelerometer, low word.
X_ACCL_OUT	R	No	0x00	0x1E, 0x1F	N/A	Output, x-axis accelerometer, high word.
Y_ACCL_LOW	R	No	0x00	0x20, 0x21	N/A	Output, y-axis accelerometer, low word.
Y_ACCL_OUT	R	No	0x00	0x22, 0x23	N/A	Output, y-axis accelerometer, high word.
Z_ACCL_LOW	R	No	0x00	0x24, 0x25	N/A	Output, z-axis accelerometer, low word.
Z_ACCL_OUT	R	No	0x00	0x26, 0x27	N/A	Output, z-axis accelerometer, high word.
TIME_STAMP	R	No	0x00	0x28, 0x29	N/A	Output, time stamp.
CRC_LWR	R	No	0x00	0x2A, 0x2B	N/A	Output, CRC-32 (32 bits total), lower word.
CRC_UPR	R	No	0x00	0x2C, 0x2D	N/A	Output, CRC-32 (32 bits total), upper word.
Reserved	N/A	N/A	0x00	0x2E to 0x3F	N/A	Reserved.
X_DELTANG_LR	R	No	0x00	0x40, 0x41	N/A	Output, x-axis delta angle, low word.
X_DELTANG_UR	R	No	0x00	0x42, 0x43	N/A	Output, x-axis delta angle, high word.
Y_DELTANG_LR	R	No	0x00	0x44, 0x45	N/A	Output, y-axis delta angle, low word.
Y_DELTANG_UR	R	No	0x00	0x46, 0x47	N/A	Output, y-axis delta angle, high word.
Z_DELTANG_LR	R	No	0x00	0x48, 0x49	N/A	Output, z-axis delta angle, low word.
Z_DELTANG_UR	R	No	0x00	0x4A, 0x4B	N/A	Output, z-axis delta angle, high word.
X_DELTVEL_LR	R	No	0x00	0x4C, 0x4D	N/A	Output, x-axis delta velocity, low word.
X_DELTVEL_UR	R	No	0x00	0x4E, 0x4F	N/A	Output, x-axis delta velocity, high word.
Y_DELTVEL_LR	R	No	0x00	0x50, 0x51	N/A	Output, y-axis delta velocity, low word.
Y_DELTVEL_UR	R	No	0x00	0x52, 0x53	N/A	Output, y-axis delta velocity, high word.
Z_DELTVEL_LR	R	No	0x00	0x54, 0x55	N/A	Output, z-axis delta velocity, low word.
Z_DELTVEL_UR	R	No	0x00	0x56, 0x57	N/A	Output, z-axis delta velocity, high word.
Reserved	N/A	N/A	0x00	0x58 to 0x7B	N/A	Reserved.
BURST_CMD	R	No	0x00	0x7C, 0x7D	N/A	Burst read command.
PROD_ID	R	Yes	0x00	0x7E, 0x7F	0x40A1	Output, product identification (16,545 decimal).
PROD_ID	R	Yes	0x00	0x7E, 0x7F	0x40A3	Output, product identification (16,547 decimal).
Reserved	N/A	N/A	0x01	0x00 to 0x7F	N/A	Reserved.
PAGE_ID	R/W	No	0x02	0x00, 0x01	0x0000	Page identifier. This register must be set to 0x02 in order to access registers on Page 2.
Reserved	N/A	N/A	0x02	0x02, 0x03	N/A	Reserved.
X_GYRO_SCALE	R/W	Yes	0x02	0x04, 0x05	0x0000	Calibration, scale, x-axis gyroscope.
Y_GYRO_SCALE	R/W	Yes	0x02	0x06, 0x07	0x0000	Calibration, scale, y-axis gyroscope.
Z_GYRO_SCALE	R/W	Yes	0x02	0x08, 0x09	0x0000	Calibration, scale, z-axis gyroscope.

USER REGISTER MEMORY MAP

Table 17. User Register Memory Map[1] (Continued)

Register Name	R/W	Flash Backup	PAGE_ID	Addresses	Default	Register Description
X_ACCL_SCALE	R/W	Yes	0x02	0x0A, 0x0B	0x0000	Calibration, scale, x-axis accelerometer.
Y_ACCL_SCALE	R/W	Yes	0x02	0x0C, 0x0D	0x0000	Calibration, scale, y-axis accelerometer.
Z_ACCL_SCALE	R/W	Yes	0x02	0x0E, 0x0F	0x0000	Calibration, scale, z-axis accelerometer.
XG_BIAS_LOW	R/W	Yes	0x02	0x10, 0x11	0x0000	Calibration, bias, gyroscope, x-axis, low word.
XG_BIAS_HIGH	R/W	Yes	0x02	0x12, 0x13	0x0000	Calibration, bias, gyroscope, x-axis, high word.
YG_BIAS_LOW	R/W	Yes	0x02	0x14, 0x15	0x0000	Calibration, bias, gyroscope, y-axis, low word.
YG_BIAS_HIGH	R/W	Yes	0x02	0x16, 0x17	0x0000	Calibration, bias, gyroscope, y-axis, high word.
ZG_BIAS_LOW	R/W	Yes	0x02	0x18, 0x19	0x0000	Calibration, bias, gyroscope, z-axis, low word.
ZG_BIAS_HIGH	R/W	Yes	0x02	0x1A, 0x1B	0x0000	Calibration, bias, gyroscope, z-axis, high word.
XA_BIAS_LOW	R/W	Yes	0x02	0x1C, 0x1D	0x0000	Calibration, bias, accelerometer, x-axis, low word.
XA_BIAS_HIGH	R/W	Yes	0x02	0x1E, 0x1F	0x0000	Calibration, bias, accelerometer, x-axis, high word.
YA_BIAS_LOW	R/W	Yes	0x02	0x20, 0x21	0x0000	Calibration, bias, accelerometer, y-axis, low word.
YA_BIAS_HIGH	R/W	Yes	0x02	0x22, 0x23	0x0000	Calibration, bias, accelerometer, y-axis, high word.
ZA_BIAS_LOW	R/W	Yes	0x02	0x24, 0x25	0x0000	Calibration, bias, accelerometer, z-axis, low word.
ZA_BIAS_HIGH	R/W	Yes	0x02	0x26, 0x27	0x0000	Calibration, bias, accelerometer, z-axis, high word.
Reserved	N/A	N/A	0x02	0x28 to 0x73	0x0000	Reserved.
USER_SCR_1	R/W	Yes	0x02	0x74, 0x75	0x0000	User Scratch Register 1.
USER_SCR_2	R/W	Yes	0x02	0x76, 0x77	0x0000	User Scratch Register 2.
USER_SCR_3	R/W	Yes	0x02	0x78, 0x79	0x0000	User Scratch Register 3.
USER_SCR_4	R/W	Yes	0x02	0x7A, 0x7B	0x0000	User Scratch Register 4.
ENDURANCE_LWR	R	Yes	0x02	0x7C, 0x7D	N/A	Diagnostic, flash memory count, low word.
ENDURANCE_UPR	R	Yes	0x02	0x7E, 0x7F	N/A	Diagnostic, flash memory count, high word.
PAGE_ID	R/W	No	0x03	0x00, 0x01	0x0000	Page identifier. This register must be set to 0x03 in order to access registers on Page 3.
GLOB_CMD	W	No	0x03	0x02, 0x03	N/A	Control, global commands.
Reserved	N/A	N/A	0x03	0x04, 0x05	N/A	Reserved.
FNCTIO_CTRL	R/W	Yes	0x03	0x06, 0x07	0x000D	Control, input and output pins, functional definitions.
GPIO_CTRL	R/W	Yes	0x03	0x08, 0x09	0x00X0[2]	Control, input and output pins, general-purpose.
CONFIG	R/W	Yes	0x03	0x0A, 0x0B	0x0040	Control, clock, and miscellaneous correction.
DEC_RATE	R/W	Yes	0x03	0x0C, 0x0D	0x0000	Control, output sample rate decimation.
NULL_CNFG	R/W	Yes	0x03	0x0E, 0x0F	0x070A	Control, automatic bias correction configuration.
UPSCALE	R/W	Yes	0x03	0x10, 0x11	0x109A	Control, input clock scaling (scaled sync mode).
RANGE_MDL	R	Yes	0x03	0x12, 0x13	N/A	Measurement range (model-specific) identifier.
Reserved	N/A	N/A	0x03	0x14, 0x15	N/A	Reserved.
FILTR_BNK_0	R/W	Yes	0x03	0x16, 0x17	0x0000	Filter selection.
FILTR_BNK_1	R/W	Yes	0x03	0x18, 0x19	0x0000	Filter selection.
Reserved	N/A	N/A	0x03	0x1A to 0x77	N/A	Reserved.
FIRM_REV	R	Yes	0x03	0x78, 0x79	N/A	Firmware revision.
FIRM_DM	R	Yes	0x03	0x7A, 0x7B	N/A	Firmware programming date (day/month).
FIRM_Y	R	Yes	0x03	0x7C, 0x7D	N/A	Firmware programming date (year).
BOOT_REV	R	Yes	0x03	0x7E, 0x7F	N/A	Boot loader revision.
PAGE_ID	R/W	No	0x04	0x00, 0x01	0x0000	Page identifier. This register must be set to 0x04 in order to access registers on Page 4.
Reserved	N/A	N/A	0x04	0x02, 0x03	N/A	Reserved.
CAL_SIG_LWR	R	Yes	0x04	0x04, 0x05	N/A	Signature CRC, calibration coefficients, low word.
CAL_SIG_UPR	R	Yes	0x04	0x06, 0x07	N/A	Signature CRC, calibration coefficients, high word.
CAL_DRV_LWR	R	No	0x04	0x08, 0x09	N/A	Real-time CRC, calibration coefficients, low word.
CAL_DRV_UPR	R	No	0x04	0x0A, 0x0B	N/A	Real-time CRC, calibration coefficients, high word.

USER REGISTER MEMORY MAP

Table 17. User Register Memory Map[1] (Continued)

Register Name	R/W	Flash Backup	PAGE_ID	Addresses	Default	Register Description
CODE_SIG_LWR	R	Yes	0x04	0x0C, 0x0D	N/A	Signature CRC, program code, low word.
CODE_SIG_UPR	R	Yes	0x04	0x0E, 0x0F	N/A	Signature CRC, program code, high word.
CODE_DRV_LWR	R	No	0x04	0x10, 0x11	N/A	Real-time CRC, program code, low word.
CODE_DRV_UPR	R	No	0x04	0x12, 0x13	N/A	Real-time CRC, program code, high word.
Reserved	N/A	N/A	0x04	0x1C to 0x1F	N/A	Reserved.
SERIAL_NUM	R	Yes	0x04	0x20, 0x21	N/A	Serial number.
Reserved	N/A	N/A	0x04	0x22 to 0x7F	N/A	Reserved.
PAGE_ID	R/W	No	0x05	0x00, 0x01	0x0000	Page identifier. This register must be set to 0x05 in order to access registers on Page 5.
Reserved	N/A	N/A	0x05	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Axxx[3]	R/W	Yes	0x05	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 0 through Coefficient 59.
PAGE_ID	R/W	No	0x06	0x00	0x0000	Page identifier. This register must be set to 0x06 in order to access registers on Page 6.
Reserved	N/A	N/A	0x06	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Axxx[3]	R/W	Yes	0x06	0x08 to 0x7F	N/A	FIR Filter Bank A: Coefficient 60 through Coefficient 119.
PAGE_ID	R/W	No	0x07	0x00	0x0000	Page identifier. This register must be set to 0x07 in order to access registers on Page 7.
Reserved	N/A	N/A	0x07	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Bxxx[4]	R/W	Yes	0x07	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 0 through Coefficient 59.
PAGE_ID	R/W	No	0x08	0x00	0x0000	Page identifier. This register must be set to 0x08 in order to access registers on Page 8.
Reserved	N/A	N/A	0x08	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Bxxx[4]	R/W	Yes	0x08	0x08 to 0x7F	N/A	FIR Filter Bank B: Coefficient 60 through Coefficient 119.
PAGE_ID	R/W	No	0x09	0x00	0x0000	Page identifier. This register must be set to 0x09 in order to access registers on Page 9.
Reserved	N/A	N/A	0x09	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Cxxx[5]	R/W	Yes	0x09	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 0 through Coefficient 59.
PAGE_ID	R/W	No	0x0A	0x00	0x0000	Page identifier. This register must be set to 0x0A in order to access registers on Page 10.
Reserved	N/A	N/A	0x0A	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Cxxx[5]	R/W	Yes	0x0A	0x08 to 0x7F	N/A	FIR Filter Bank C: Coefficient 60 through Coefficient 119.
PAGE_ID	R/W	No	0x0B	0x00	0x0000	Page identifier. This register must be set to 0x0B in order to access registers on Page 11.
Reserved	N/A	N/A	0x0B	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Dxxx[6]	R/W	Yes	0x0B	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 0 through Coefficient 59.
PAGE_ID	R/W	No	0x0C	0x00	0x0000	Page identifier. This register must be set to 0x0C in order to access registers on Page 12.
Reserved	N/A	N/A	0x0C	0x02 to 0x07	N/A	Reserved.
FIR_COEF_Dxxx[6]	R/W	Yes	0x0C	0x08 to 0x7F	N/A	FIR Filter Bank D: Coefficient 60 through Coefficient 119.

[1] N/A means not applicable.

[2] The GPIO_CTRL[7:4] bits reflect the logic levels on the DIOx lines and do not have a default setting.

[3] See the FIR Filter Bank A, FIR_COEF_A000 to FIR_COEF_A119 section for additional information.

[4] See the FIR Filter Bank B, FIR_COEF_B000 to FIR_COEF_B119 section for additional information.

[5] See the FIR Filter Bank C, FIR_COEF_C000 to FIR_COEF_C119 section for additional information.

[6] See the FIR Filter Bank D, FIR_COEF_D000 to FIR_COEF_D119 section for additional information.

USER REGISTER DEFINITIONS

PAGE NUMBER (PAGE_ID)

The contents in the PAGE_ID register (see Table 18 and Table 19) contain the current page setting and provide a control for selecting another page for SPI access. For example, set DIN = 0x8002 to select Page 2 in order to access the registers on Page 2. See Table 17 for the page assignments associated with each user accessible register.

Table 18. PAGE_ID Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x00, 0x01	0x0000	R/W	No

Table 19. PAGE_ID Bit Descriptions

Bits	Description
[15:0]	Page number, binary numerical format

DATA AND SAMPLE COUNTER (DATA_CNT)

The DATA_CNT register (see Table 20 and Table 21) is a continuous, real-time, sample counter. The counter starts at 0x0000, increments every time the output data registers update, and wraps around from 0xFFFF (65,535 decimal) to 0x0000 (0 decimal).

Table 20. DATA_CNT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x04, 0x05	Not applicable	R	No

Table 21. DATA_CNT Bit Descriptions

Bits	Description
[15:0]	Data counter, binary format

STATUS AND ERROR FLAG INDICATORS (STATUS)

The STATUS register (see Table 22 and Table 23) provides various error flags. Reading this register causes all of its bits to return to 0, with the exception of Bit 7. If an error condition persists, its flag (bit) automatically returns to an alarm value of 1.

Table 22. STATUS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x08, 0x09	0x0000	R	No

Table 23. STATUS Bit Descriptions

Bits	Description
15	Watchdog timer flag. A 1 indicates that the ADIS16545/ADIS16547 automatically reset themselves to clear an issue.
[14:9]	Not used.
8	Sync error. When operating in scaled sync mode (FNCTIO_CTRL, Bit 8 = 1, see Table 151), a 1 indicates the sample timing is not scaling correctly. When this error occurs, verify that the input sync frequency is correct and that UPSCALE (see Table 161) has the correct value.
7	Processing overrun. A 1 indicates the occurrence of a processing overrun. Initiate a reset to recover. Replace the ADIS16545/ADIS16547 if this error persists.

Table 23. STATUS Bit Descriptions (Continued)

Bits	Description
6	Flash memory update failure. A 1 indicates that the most recent flash memory update failed (GLOB_CMD, Bit 3, see Table 149). Repeat the flash memory update and replace the ADIS16545/ADIS16547 if this error persists.
5	Sensor failure. A 1 indicates failure in at least one of the inertial sensors from either a continuous monitoring (CST) or on-demand self test (ODST). Read the DIAG_STS register (see Table 25) to determine which sensor is failing. Replace the ADIS16545/ADIS16547 if the error persists, when the device is operating in static inertial conditions.
4	Not used.
3	SPI communication error. A 1 indicates that the total number of SCLK cycles is not equal to an integer multiple of 16. Repeat the previous communication sequence to recover. Persistence in this error can indicate a weakness in the SPI signal integrity from the host processor.
2	CRC error condition. A 1 indicates a failure in a CRC calculation. This bit is the logical OR of the firmware CRC, the calibration coefficients CRC, and the user settings CRC. Initiate a reset to recover. Replace the ADIS16545/ADIS16547 if this error persists. See Dual-Memory Structure for more details about CRC checking and for information about reading the actual CRC values.
1	Boot memory failure. A 1 indicates that the device booted up using code from the backup memory bank. Replace the ADIS16545/ADIS16547 if this error occurs.
0	Not used.

SELF TEST ERROR FLAGS (DIAG_STS)

The DIAG_STS register (see Table 24 and Table 25) contains pass and fail flags (0 = pass) for each inertial sensor. This register works together with STATUS, Bit 5 (see Table 23) which is the logical OR of the bits in this register. Note that 0 = pass for both CST and ODST operations. Reading the DIAG_STS register causes all of its bits to restore to 0. If the error conditions persist, the bits in DIAG_STS return to 1.

Table 24. DIAG_STS Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0A, 0x0B	0x0000	R	No

Table 25. DIAG_STS Bit Descriptions

Bits	Description (Default = 0x0000)
[15:6]	Not used
5	Self test failure, z-axis accelerometer (1 = failure)
4	Self test failure, y-axis accelerometer (1 = failure)
3	Self test failure, x-axis accelerometer (1 = failure)
2	Self test failure, z-axis gyroscope (1 = failure)
1	Self test failure, y-axis gyroscope (1 = failure)
0	Self test failure, x-axis gyroscope (1 = failure)

USER REGISTER DEFINITIONS

INTERNAL TEMPERATURE (TEMP_OUT)

The TEMP_OUT register in the ADIS16545/ADIS16547 (see Table 26 and Table 27) provides an internal temperature measurement. This data is valuable for monitoring relative shifts in the thermal environment. However, TEMP_OUT measurements are not calibrated to track any specific location or application mounting approach. Table 28 offer more details and data format examples for this register.

Table 26. TEMP_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x0E, 0x0F	Not applicable	R	No

Table 27. TEMP_OUT Bit Descriptions

Bits	Description
[15:0]	Temperature data; twos complement, 1°C per 140 LSB, 25°C = 0x0000

Table 28. TEMP_OUT Data Format Examples

Temperature (°C)	Decimal	Hexadecimal
+85	+8400	0x20D0
+25 + 2/140	+2	0x0002
+25 + 1/140	+1	0x0001
+25	0	0x0000
+25 – 1/140	−1	0xFFFF
+25 – 2/140	−2	0xFFFE
−40	−9100	0xDC74

GYROSCOPE DATA

The gyroscopes in the ADIS16545/ADIS16547 measure the angular rate of rotation around three orthogonal axes (x, y, and z). Figure 44 shows the orientation of each gyroscope axis, which defines the direction of rotation that produces a positive response in each of the angular rate measurements.

Each gyroscope has two output data registers. Figure 43 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis gyroscope measurements with Bit 31 being the sign bit. This format also applies to the y-axis and z-axis.

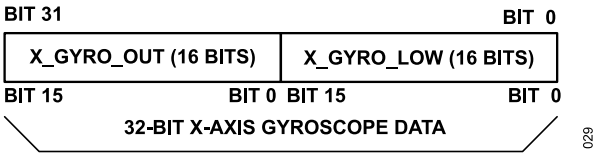

Figure 43. Gyroscope Output Data Structure

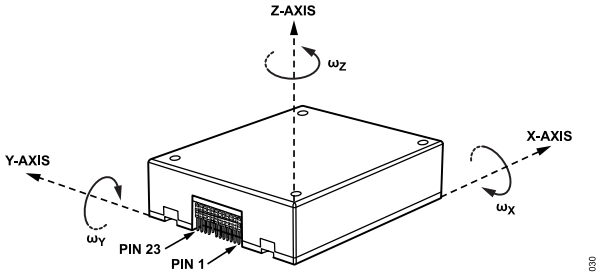

Figure 44. Gyroscope Axis and Polarity Assignments

Gyroscope Measurement Range and Scale Factor

Table 29 provides the range and 16-bit scale factor (K_G) for the angular rate (gyroscope) measurements in each ADIS16545/ADIS16547 model.

Table 29. Gyroscope Measurement Range and 16-Bit Scale Factors

Model	Range	16-Bit Scale Factor, K_G
ADIS16545-1BMLZ and ADIS16547-1BMLZ	±125°/sec	0.00625°/sec/LSB
ADIS16545-2BMLZ and ADIS16547-2BMLZ	±450°/sec	0.025°/sec/LSB
ADIS16545-3BMLZ and ADIS16547-3BMLZ	±2000°/sec	0.1°/sec/LSB

Gyroscope Data Formatting

Table 30 and Table 31 offer various numerical examples that demonstrate the format of the rotation rate data in both 16-bit and 32-bit formats. See Table 29 for the scale factor (K_G) associated with each ADIS16545/ADIS16547 model.

Table 30. 16-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hexadecimal
+20000 K_G	+20,000	0x4E20
+19200 K_G (ADIS16545-2 and ADIS16547-2 Maximum)	+19,200	0x4B00
+2 K_G	+2	0x0002
+K_G	+1	0x0001
0°/sec	0	0x0000
−K_G	−1	0xFFFF
−2 K_G	−2	0xFFFE
−19200 K_G (ADIS16545-2 and ADIS16547-2 Minimum)	−19,200	0xB500
−20000 K_G	−20,000	0xB1E0

Table 31. 32-Bit Gyroscope Data Format Examples

Rotation Rate (°/sec)	Decimal	Hexadecimal
+20000 K_G	+1,310,720,000	0x4E200000
+19200 K_G (ADIS16545-2 and ADIS16547-2 Maximum)	+1,258,291,200	0x4B000000
$+K_G/2^{15}$	+2	0x00000002
$+K_G/2^{16}$	+1	0x00000001

USER REGISTER DEFINITIONS

Table 31. 32-Bit Gyroscope Data Format Examples (Continued)

Rotation Rate (°/sec)	Decimal	Hexadecimal
0	0	0x00000000
$-K_G/2^{16}$	−1	0xFFFFFFFF
$-K_G/2^{15}$	−2	0xFFFFFFFE
−19200 K_G(ADIS16545-2 and ADIS16547-2 Minimum)	−1,258,291,200	0xB5000000
−20000 K_G	−1,310,720,000	0xB1E00000

X-Axis Gyroscope (X_GYRO_LOW and X_GRYO_OUT)

The X_GYRO_LOW (see Table 32 and Table 33) and X_GRYO_OUT (see Table 34 and Table 35) registers contain the gyroscope data for the x-axis.

Table 32. X_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x10, 0x11	Not applicable	R	No

Table 33. X_GYRO_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis gyroscope data, lower word

Table 34. X_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x12, 0x13	Not applicable	R	No

Table 35. X_GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	X-axis gyroscope data; upper word, twos complement, 0°/sec = 0x0000, and see Table 29 for the scale factor

Y-Axis Gyroscope (Y_GYRO_LOW and Y_GYRO_OUT)

The Y_GYRO_LOW (see Table 36 and Table 37) and Y_GYRO_OUT (see Table 38 and Table 39) registers contain the gyroscope data for the y-axis.

Table 36. Y_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x14, 0x15	Not applicable	R	No

Table 37. Y_GYRO_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope data, lower word

Table 38. Y_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x16, 0x17	Not applicable	R	No

Table 39. Y_GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope data, upper word, twos complement, 0°/sec = 0x0000, and see Table 29 for the scale factor

Z-Axis Gyroscope (Z_GYRO_LOW and Z_GYRO_OUT)

The Z_GYRO_LOW (see Table 40 and Table 41) and Z_GRYO_OUT (see Table 42 and Table 43) registers contain the gyroscope data for the z-axis.

Table 40. Z_GYRO_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x18, 0x19	Not applicable	R	No

Table 41. Z_GYRO_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope data, lower word

Table 42. Z_GYRO_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1A, 0x1B	Not applicable	R	No

Table 43. Z_GYRO_OUT Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope data, upper word, twos complement, 0°/sec = 0x0000, and see Table 29 for the scale factor

ACCELERATION DATA

The accelerometers in the ADIS16545/ADIS16547 measure both dynamic and static (response to gravity) acceleration along three orthogonal axes (x, y, and z). Figure 46 shows the orientation of each accelerometer axis, which defines the direction of linear acceleration that produces a positive response in each of the acceleration measurements.

Each accelerometer has two output data registers. Figure 45 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis accelerometer measurements with Bit 31 being the sign bit. This format also applies to the y-axis and z-axis.

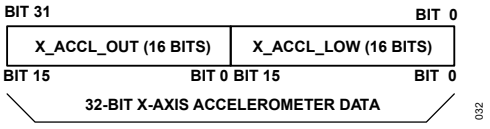

Figure 45. Accelerometer Output Data Structure

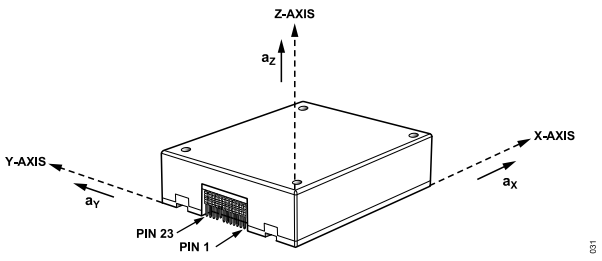

Figure 46. Accelerometer Axis and Polarity Assignments

USER REGISTER DEFINITIONS

Accelerometer Measurement Range and Scale Factor

Table 44 provides the measurement range (±A_{MAX}) and scale factor (K_A) for the accelerometer.

Table 44. Accelerometer Measurement Range and Scale Factors

Model	Range, ±A_{MAX} (g)	Scale Factor, K_A (LSB/g)
ADIS16545	±8	4000
ADIS16547	±40	800

Accelerometer Resolution

Table 45 and Table 46 offer various numerical examples that demonstrate the format of the linear acceleration data in both 16-bit and 32-bit formats.

Table 45. 16-Bit Accelerometer Data Format Examples

Acceleration (g)	Decimal	Hexadecimal	Binary
+A_{MAX}	+32,000	0x7D00	0111 1101 0000 0000
+2/K_A	+2	0x0002	0000 0000 0000 0010
+1/K_A	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−1/K_A	−1	0xFFFF	1111 1111 1111 1111
−2/K_A	−2	0xFFFE	1111 1111 1111 1110
−A_{MAX}	−32,000	0x8300	1000 0011 0000 0000

Table 46. 32-Bit Accelerometer Data Format Examples

Acceleration (g)	Decimal	Hexadecimal
+A_{MAX}	+2,097,152,000	0x7D000000
+2/(K_A × 2^{16})	+2	0x00000002
+1/(K_A × 2^{16})	+1	0x00000001
0	0	0x00000000
−1/(K_A × 2^{16})	−1	0xFFFFFFFF
−2/(K_A × 2^{16})	−2	0xFFFFFFFE
−A_{MAX}	−2,097,152,000	0x83000000

X-Axis Accelerometer (X_ACCL_LOW and X_ACCL_OUT)

The X_ACCL_LOW (see Table 47 and Table 48) and X_ACCL_OUT (see Table 49 and Table 50) registers contain the accelerometer data for the x-axis.

Table 47. X_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1C, 0x1D	Not applicable	R	No

Table 48. X_ACCL_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis accelerometer data, lower word

Table 49. X_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x1E, 0x1F	Not applicable	R	No

Table 50. X_ACCL_OUT Bit Descriptions

Bits	Description
[15:0]	X-axis accelerometer data, upper word, twos complement, ±8 *g* range, 0 *g* = 0x0000, 1 LSB = 1/K_A (see Table 44 for K_A)

Y-Axis Accelerometer (Y_ACCL_LOW and Y_ACCL_OUT)

The Y_ACCL_LOW (see Table 51 and Table 52) and Y_ACCL_OUT (see Table 53 and Table 54) registers contain the accelerometer data for the y-axis.

Table 51. Y_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x20, 0x21	Not applicable	R	No

Table 52. Y_ACCL_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer data, lower word

Table 53. Y_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x22, 0x23	Not applicable	R	No

Table 54. Y_ACCL_OUT Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer data, upper word, twos complement, ±8 *g* range, 0 *g* = 0x0000, 1 LSB = 1/K_A (see Table 44 for K_A)

Z-Axis Accelerometer (Z_ACCL_LOW and Z_ACCL_OUT)

The Z_ACCL_LOW (see Table 55 and Table 56) and Z_ACCL_OUT (see Table 57 and Table 58) registers contain the accelerometer data for the z-axis.

Table 55. Z_ACCL_LOW Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x24, 0x25	Not applicable	R	No

Table 56. Z_ACCL_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer data, lower word

Table 57. Z_ACCL_OUT Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x26, 0x27	Not applicable	R	No

Table 58. Z_ACCL_OUT Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer data, upper word, twos complement, ±8 *g* range, 0 *g* = 0x0000, 1 LSB = 1/K_A (see Table 44 for K_A)

USER REGISTER DEFINITIONS

TIME STAMP

When using scaled sync mode (FNCTIO_CTRL, Bits[8:7] = 11 (binary), see Table 151), the TIME_STAMP register (see Table 59 and Table 60) provides the time between the rising edge of the most recent pulse on the input clock signal and the most recent data update.

Table 59. TIME_STAMP Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x28, 0x29	Not applicable	R	No

Table 60. TIME_STAMP Bit Descriptions

Bits	Description
[15:0]	Time stamp, binary format. 1 LSB = $1/f_{SM}$ (see Figure 29, Figure 30, and Table 161). The leading edge of the input clock pulse resets the value in this register to 0x0000.

When using the decimation filter (DEC_RATE > 0x0000), the value in the TIME_STAMP register represents the time of the first sample (taken at the rate of f_{SM}, per Figure 29 and Figure 30).

For example, when DEC_RATE = 0x0003, the decimation filter reduces the update by a factor of four, and the TIME_STAMP register updates to 1 (decimal) during the first data update, then to 5 on the second update, 9 on the third update, for example, until the next clock signal pulse.

CYCLICAL REDUNDANCY CHECK (CRC-32)

The ADIS16545/ADIS16547 perform a CRC-32 computation using the data registers that are shown in Table 61. See the CRC-32 Code Example section for sample code implementing the CRC-32 calculation.

Table 61. CRC-32 Source Data and Example Values

Register	Example Value
STATUS	0x0000
TEMP_OUT	0x083A
X_GYRO_LOW	0x0000
X_GYRO_OUT	0xFFF7
Y_GYRO_LOW	0x0000
Y_GYRO_OUT	0xFFFE
Z_GYRO_LOW	0x0000
Z_GYRO_OUT	0x0001
X_ACCL_LOW	0x5001
X_ACCL_OUT	0x0003
Y_ACCL_LOW	0xE00A
Y_ACCL_OUT	0x0015
Z_ACCL_LOW	0xC009
Z_ACCL_OUT	0x0320
TIME_STAMP	0x8A54

The CRC_LWR (see Table 62 and Table 63) and CRC_UPR (see Table 64 and Table 65) registers contain the result of the CRC-32 computation. For the example, the register values from Table 61 are the following:

- CRC_LWR = 0x15B4
- CRC_UPR = 0xB6C8

Table 62. CRC_LWR Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x2A, 0x2B	Not applicable	R	No

Table 63. CRC_LWR Bit Descriptions

Bits	Description
[15:0]	CRC-32 code from most recent data update cycle, lower word

Table 64. CRC_UPR Register Definition

Page	Addresses	Default	Access	Flash Backup
0x00	0x2C, 0x2D	Not applicable	R	No

Table 65. CRC_UPR Bit Descriptions

Bits	Description
[15:0]	CRC-32 code from most recent data update cycle, upper word

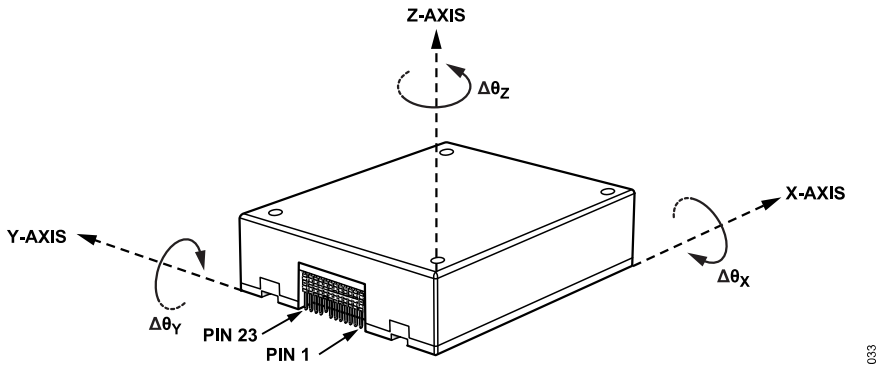

Figure 47. Delta Angle Axis and Polarity Assignments

USER REGISTER DEFINITIONS

DELTA ANGLES

In addition to the angular rate of rotation (gyroscope) measurements around each axis (x, y, and z), the ADIS16545/ADIS16547 also provide delta angle measurements that represent a computation of angular displacement between each sample update. Figure 47 shows the orientation of each delta angle output, which defines the direction of rotation that produces a positive response in each of the angular displacement (delta angle) measurements.

The delta angle outputs represent an integration of the gyroscope measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta\theta_{x,nD} = \frac{1}{2f_{SM}} \times \sum_{d=0}^{D-1} \left(\omega_{x,nD+d} + \omega_{x,nD+d-1}\right) \quad (3)$$

where:
$\Delta\theta_x$ is the delta angle measurement for the x-axis.
n is the sample time, prior to the decimation filter.
D is the decimation rate = DEC_RATE + 1 (see Table 157).
f_{SM} is the sample rate.
d is the incremental variable in the summation formula.
ω_x is the x-axis rate of rotation (gyroscope).

When using the internal sample clock, f_{SM} is equal to 4000 SPS. When using an external clock in sync mode, f_{SM} is equal to the frequency of the external clock. When using an external clock in scaled sync mode, f_{SM} is equal to the frequency of the external clock multiplied by the scale factor. The range in the delta angle registers accommodates the maximum rate of rotation (Table 29), the nominal sample rate (4000 SPS), and an update rate of 1 Hz (DEC_RATE = 0x0F9F; divide by 3999 plus 1, see Table 157), all at the same time. When using an external clock that is higher than 4000 SPS, reduce the DEC_RATE setting to avoid overranging the delta angle registers.

Each axis of the delta angle measurements has two output data registers. Figure 48 shows how these two registers combine to support a 32-bit, twos complement data format for the x-axis delta angle measurements with Bit 31 being the sign bit. This format also applies to the y-axis and z-axis.

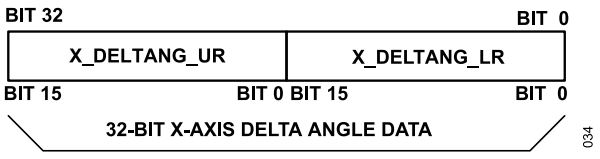

Figure 48. Delta Angle Data Output Structure

Delta Angle Measurement Range

Table 66 offers the measurement range and scale factor for each ADIS16545/ADIS16547 model.

Table 66. Delta Angle Measurement Range and Scale Factor

Model	Measurement Range, $\pm\Delta\theta_{MAX}$
ADIS16545-1BMLZ and ADIS16547-1BMLZ	±360°
ADIS16545-2BMLZ and ADIS16547-2BMLZ	±720°
ADIS16545-3BMLZ and ADIS16547-3BMLZ	±2160°

X-Axis Delta Angle (X_DELTANG_LR and X_DELTANG_UR)

The X_DELTANG_LR (see Table 67 and Table 68) and X_DELTANG_UR (see Table 69 and Table 70) registers contain the delta angle data for the x-axis.

Table 67. X_DELTANG_LR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x40, 0x41	Not applicable	R	No

Table 68. X_DELTANG_LR Bit Descriptions

Bits	Description
[15:0]	X-axis delta angle data, lower word

Table 69. X_DELTANG_UR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x42, 0x43	Not applicable	R	No

Table 70. X_DELTANG_UR Bit Descriptions

Bits	Description
[15:0]	X-axis delta angle data, upper word, twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 66 for $\Delta\theta_{MAX}$)

Y-Axis Delta Angle (Y_DELTANG_LR and Y_DELTANG_UR)

The Y_DELTANG_LR (see Table 71 and Table 72) and Y_DELTANG_UR (see Table 73 and Table 74) registers contain the delta angle data for the y-axis.

Table 71. Y_DELTANG_LR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x44, 0x45	Not applicable	R	No

Table 72. Y_DELTANG_LR Bit Descriptions

Bits	Description
[15:0]	Y-axis delta angle data, lower word

Table 73. Y_DELTANG_UR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x46, 0x47	Not applicable	R	No

USER REGISTER DEFINITIONS

Table 74. Y_DELTANG_UR Bit Descriptions

Bits	Description
[15:0]	Y-axis delta angle data, upper word, twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 66 for $\Delta\theta_{MAX}$)

Z-Axis Delta Angle (Z_DELTANG_LR and Z_DELTANG_UR)

The Z_DELTANG_LR (see Table 75 and Table 76) and Z_DELTANG_UR (see Table 77 and Table 78) registers contain the delta angle data for the z-axis.

Table 75. Z_DELTANG_LR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x48, 0x49	Not applicable	R	No

Table 76. Z_DELTANG_LR Bit Descriptions

Bits	Description
[15:0]	Z-axis delta angle data, lower word

Table 77. Z_DELTANG_UR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4A, 0x4B	Not applicable	R	No

Table 78. Z_DELTANG_UR Bit Descriptions

Bits	Description
[15:0]	Z-axis delta angle data, upper word, twos complement, 0° = 0x0000, 1 LSB = $\Delta\theta_{MAX}/2^{15}$ (see Table 66 for $\Delta\theta_{MAX}$)

Delta Angle Resolution

Table 79 and Table 80 shows various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 79. 16-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hexadecimal	Binary
$\Delta\theta_{MAX} \times (2^{15}-1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+\Delta\theta_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta\theta_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta\theta_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta\theta_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta\theta_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 80. 32-Bit Delta Angle Data Format Examples

Delta Angle (°)	Decimal	Hexadecimal
$+\Delta\theta_{MAX} \times (2^{31}-1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta\theta_{MAX}/2^{30}$	+2	0x00000002
$+\Delta\theta_{MAX}2000/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta\theta_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta\theta_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta\theta_{MAX}$	−2,147,483,648	0x80000000

DELTA VELOCITY

In addition to the linear acceleration measurements along each axis (x, y, and z), the ADIS16545/ADIS16547 also provide delta velocity measurements that represent a computation of linear velocity change between each sample update. Figure 50 shows the orientation of each delta-velocity measurement, which defines the direction of linear velocity increase that produces a positive response in each of the delta velocity rate measurements.

The delta velocity outputs represent an integration of the acceleration measurements and use the following formula for all three axes (x-axis displayed):

$$\Delta V_{x,nD} = \frac{1}{2f_{SM}} \times \sum_{d=0}^{D-1} \left(a_{x,nD+d} + a_{x,nD+d-1}\right) \quad (4)$$

where:
ΔV_X is the delta velocity measurement for the x-axis.
n is the sample time, prior to the decimation filter.
D is the decimation rate = DEC_RATE + 1 (see Table 157).
f_{SM} is the sample rate.
d is the incremental variable in the summation formula.
a_x is the x-axis linear acceleration (accelerometer).

When using the internal sample clock, f_{SM} is equal to 4000 SPS. When using the external clock option, f_{SM} is equal to the frequency of the external clock. The range in the delta velocity registers accommodates the maximum linear acceleration (40 *g*), the nominal sample rate (4000 SPS), and an update rate of 1 Hz (DEC_RATE = 0x0F9F; divide by 3999 plus 1, see Table 157), all at the same time. When using an external clock that is higher than 4000 SPS, reduce the DEC_RATE setting to avoid overranging the delta velocity registers.

Each axis of the delta velocity measurements has two output data registers. Figure 49 shows how these two registers combine to support 32-bit, twos complement data format for the delta velocity measurements along the x-axis with Bit 31 being the sign bit. This format also applies to the y-axis and z-axis.

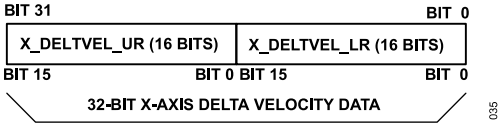

Figure 49. Delta Velocity Data Output Structure

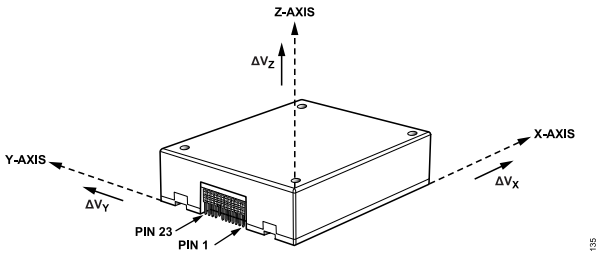

Figure 50. Delta Velocity Axis and Polarity Assignments

USER REGISTER DEFINITIONS

Delta Velocity Measurement Range

Table 81 shows the measurement range for each model.

Table 81. Delta Velocity Measurement Range

Model	Measurement Range, $\pm\Delta V_{MAX}$ (m/sec)
ADIS16545	± 100
ADIS16547	± 400

X-Axis Delta Velocity (X_DELTVEL_LR and X_DELTVEL_UR)

The X_DELTVEL_LR (see Table 82 and Table 83) and X_DELTVEL_UR (see Table 84 and Table 85) registers contain the delta velocity data for the x-axis.

Table 82. X_DELTVEL_LR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4C, 0x4D	Not applicable	R	No

Table 83. X_DELTVEL_LR Bit Descriptions

Bits	Description
[15:0]	X-axis delta angle data, lower word

Table 84. X_DELTVEL_UR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x4E, 0x4F	Not applicable	R	No

Table 85. X_DELTVEL_UR Bit Descriptions

Bits	Description
[15:0]	X-axis delta velocity data, upper word, twos complement, 0 m/sec = 0x0000, 1 LSB = $\Delta V_{MAX} \div 2^{15}$ (see Table 81 for ΔV_{MAX})

Y-Axis Delta Velocity (Y_DELTVEL_LR and Y_DELTVEL_UR)

The Y_DELTVEL_LR (see Table 86 and Table 87) and Y_DELTVEL_UR (see Table 88 and Table 89) registers contain the delta velocity data for the y-axis.

Table 86. Y_DELTVEL_LR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x50, 0x51	Not applicable	R	No

Table 87. Y_DELTVEL_LR Bit Descriptions

Bits	Description
[15:0]	Y-axis delta angle data, lower word

Table 88. Y_DELTVEL_UR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x52, 0x53	Not applicable	R	No

Table 89. Y_DELTVEL_UR Bit Descriptions

Bits	Description
[15:0]	Y-axis delta velocity data, upper word, twos complement, 0 m/sec = 0x0000, 1 LSB = $\Delta V_{MAX} \div 2^{15}$ (see Table 81 for ΔV_{MAX})

Z-Axis Delta Velocity (Z_DELTVEL_LR and Z_DELTVEL_UR)

The Z_DELTVEL_LR (see Table 90 and Table 91) and Z_DELTVEL_UR (see Table 92 and Table 93) registers contain the delta velocity data for the z-axis.

Table 90. Z_DELTVEL_LR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x54, 0x55	Not applicable	R	No

Table 91. Z_DELTVEL_LR Bit Descriptions

Bits	Description
[15:0]	Z-axis delta angle data, lower word

Table 92. Z_DELTVEL_UR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x56, 0x57	Not applicable	R	No

Table 93. Z_DELTVEL_UR Bit Descriptions

Bits	Description
[15:0]	Z-axis delta velocity data, upper word, twos complement, 0 m/sec = 0x0000, 1 LSB = $\Delta V_{MAX} \div 2^{15}$ (see Table 81 for ΔV_{MAX})

Delta Velocity Resolution

Table 94 and Table 95 details various numerical examples that demonstrate the format of the delta angle data in both 16-bit and 32-bit formats.

Table 94. 16-Bit Delta Velocity Data Format Examples

Velocity (m/sec)	Decimal	Hexadecimal	Binary
$+\Delta V_{MAX} \times (2^{15} - 1)/2^{15}$	+32,767	0x7FFF	0111 1111 1110 1111
$+\Delta V_{MAX}/2^{14}$	+2	0x0002	0000 0000 0000 0010
$+\Delta V_{MAX}/2^{15}$	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
$-\Delta V_{MAX}/2^{15}$	−1	0xFFFF	1111 1111 1111 1111
$-\Delta V_{MAX}/2^{14}$	−2	0xFFFE	1111 1111 1111 1110
$-\Delta V_{MAX}$	−32,768	0x8000	1000 0000 0000 0000

Table 95. 32-Bit Delta Angle Data Format Examples

Velocity (m/sec)	Decimal	Hexadecimal
$+\Delta V_{MAX} \times (2^{31} - 1)/2^{31}$	+2,147,483,647	0x7FFFFFFF
$+\Delta V_{MAX}/2^{30}$	+2	0x00000002
$+\Delta V_{MAX}/2^{31}$	+1	0x00000001
0	0	0x00000000
$-\Delta V_{MAX}/2^{31}$	−1	0xFFFFFFFF
$-\Delta V_{MAX}/2^{30}$	−2	0xFFFFFFFE
$-\Delta V_{MAX}$	−2,147,483,648	0x80000000

USER REGISTER DEFINITIONS

Burst Read Command, BURST_CMD

Reading the BURST_CMD register (see Table 96 and Table 97) starts the BRF. See Table 15, Table 16, and Figure 6 for more information on the BRF function.

Table 96. BURST_CMD Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x00	0x7C, 0x7D	Not applicable	R	No

Table 97. BURST_CMD Bit Descriptions

Bits	Description
[15:0]	Burst read command register

Product Identification, PROD_ID

The PROD_ID register (see Table 98 and Table 99) contains the numerical portion of the device number (16,545 and 16,547). See Figure 40 for an example of how to use a looping read of this register to validate the integrity of the communication.

Table 98. PROD_ID Register Definitions

Page	Addresses	Default	Access	Flash Backup	Device
0x00	0x7E, 0x7F	0x40A1	R	Yes	ADIS16545
0x00	0x7E, 0x7F	0x40A3	R	Yes	ADIS16547

Table 99. PROD_ID Bit Descriptions

Bits	Description	Device
[15:0]	Product identification = 0x40A1	ADIS16545
[15:0]	Product identification = 0x40A3	ADIS16547

USER BIAS AND SCALE ADJUSTMENT

The signal chain of each inertial sensor (accelerometers and gyroscopes) on every ADIS16545/ADIS16547 includes application of correction factors that are unique to that part and come from characterization of bias, sensitivity, and alignment over a temperature range of −40°C to +85°C for the ADIS16545/ADIS16547. Note that the ADIS16545/ADIS16547 are rated over a −40°C to +105°C temperature range, even though the calibration range is −40°C to +85°C. These correction factors are not user-accessible, but the user does have the opportunity to adjust the bias and the scale factor for each sensor individually through user-accessible registers. In the signal chain, the user correction factors are applied immediately after the factory derived correction factors.

Gyroscope Scale Adjustment, X_GYRO_SCALE

The X_GYRO_SCALE register (see Table 100 and Table 101) provides the user with the opportunity to adjust the scale factor for the x-axis gyroscopes. See Figure 51 for an illustration of how this scale factor influences the x-axis gyroscope data.

Table 100. X_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x04, 0x05	0x0000	R/W	Yes

Table 101. X_GYRO_SCALE Bit Definitions

Bits	Description
[15:0]	X-axis gyroscope scale correction, twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} \cong 0.003052\%$

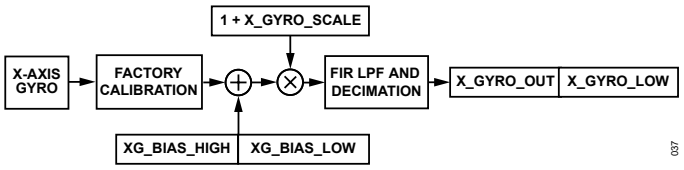

Figure 51. User Bias and Scale Adjustment Registers in Gyroscope Signal Path

Gyroscope Scale Adjustment, Y_GYRO_SCALE

The Y_GYRO_SCALE register (see Table 102 and Table 103) allows the user to adjust the scale factor for the y-axis gyroscopes. This register influences the y-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 51).

Table 102. Y_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x06, 0x07	0x0000	R/W	Yes

Table 103. Y_GYRO_SCALE Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope scale correction, twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} \cong 0.003052\%$

Gyroscope Scale Adjustment, Z_GYRO_SCALE

The Z_GYRO_SCALE register (see Table 104 and Table 105) allows the user to adjust the scale factor for the z-axis gyroscopes. This register influences the z-axis gyroscope measurements in the same manner that X_GYRO_SCALE influences the x-axis gyroscope measurements (see Figure 51).

Table 104. Z_GYRO_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x08, 0x09	0x0000	R/W	Yes

USER REGISTER DEFINITIONS

Table 105. Z_GYRO_SCALE Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope scale correction, twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} \cong 0.003052\%$

Accelerometer Scale Adjustment, X_ACCL_SCALE

The X_ACCL_SCALE register (see and Table 107) allows users to adjust the scale factor for the x-axis accelerometers. See Figure 52 for an illustration of how this scale factor influences the x-axis accelerometer data.

Table 106. X_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0A, 0x0B	0x0000	R/W	Yes

Table 107. X_ACCL_SCALE Bit Descriptions

Bits	Description
[15:0]	X-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} \cong 0.003052\%$

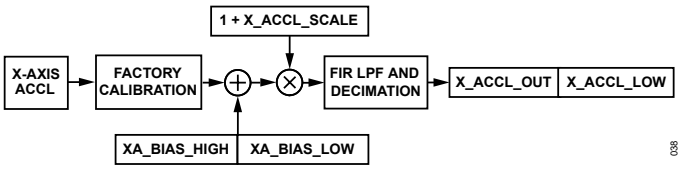

Figure 52. User Bias and Scale Adjustment Registers in Accelerometer Signal Path

Accelerometer Scale Adjustment, Y_ACCL_SCALE

The Y_ACCL_SCALE register (see Table 108 and Table 109) allows the user to adjust the scale factor for the y-axis accelerometers. This register influences the y-axis accelerometer measurements in the same manner that X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 52).

Table 108. Y_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0C, 0x0D	0x0000	R/W	Yes

Table 109. Y_ACCL_SCALE Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} \cong 0.003052\%$

Accelerometer Scale Adjustment, Z_ACCL_SCALE

The Z_ACCL_SCALE register (see Table 110 and Table 111) allows the user to adjust the scale factor for the z-axis accelerometers. This register influences the z-axis accelerometer measurements in the same manner that X_ACCL_SCALE influences the x-axis accelerometer measurements (see Figure 52).

Table 110. Z_ACCL_SCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x0E, 0x0F	0x0000	R/W	Yes

Table 111. Z_ACCL_SCALE Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer scale correction, twos complement, 0x0000 = unity gain, 1 LSB = $1 \div 2^{15} \cong 0.003052\%$

Gyroscope Bias Adjustment, XG_BIAS_LOW and XG_BIAS_HIGH

The XG_BIAS_LOW (see Table 112 and Table 113) and XG_BIAS_HIGH (see Table 114 and Table 115) registers combine to allow the user to adjust the bias of the x-axis gyroscopes. The digital format examples in Table 30 also apply to the XG_BIAS_HIGH register, and the digital format examples in Table 31 apply to the number that comes from combining the XG_BIAS_LOW and XG_BIAS_HIGH registers. See Figure 51 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Table 112. XG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x10, 0x11	0x0000	R/W	Yes

Table 113. XG_BIAS_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis gyroscope offset correction, lower word, twos complement, 0°/sec = 0x0000, 1 LSB = $K_G \div 2^{16}$ (see Table 29)

Table 114. XG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x12, 0x13	0x0000	R/W	Yes

Table 115. XG_BIAS_HIGH Bit Descriptions

Bits	Description
[15:0]	X-axis gyroscope offset correction, upper word, twos complement, 0°/sec = 0x0000, 1 LSB = K_G (see Table 29)

Gyroscope Bias Adjustment, YG_BIAS_LOW and YG_BIAS_HIGH

The YG_BIAS_LOW (see Table 116 and Table 117) and YG_BIAS_HIGH (see Table 118 and Table 119) registers combine to allow users to adjust the bias of the y-axis gyroscopes. The digital format examples in Table 30 also apply to the YG_BIAS_HIGH register, and the digital format examples in Table 31 apply to the number that comes from combining the YG_BIAS_LOW and YG_BIAS_HIGH registers. These registers influence the y-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 51).

USER REGISTER DEFINITIONS

Table 116. YG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x14, 0x15	0x0000	R/W	Yes

Table 117. YG_BIAS_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, lower word, twos complement, 0°/sec = 0x0000, 1 LSB = $K_G \div 2^{16}$ (see Table 29)

Table 118. YG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x16, 0x17	0x0000	R/W	Yes

Table 119. YG_BIAS_HIGH Bit Descriptions

Bits	Description
[15:0]	Y-axis gyroscope offset correction, upper word, twos complement, 0°/sec = 0x0000, 1 LSB = K_G (see Table 29)

Gyroscope Bias Adjustment, ZG_BIAS_LOW and ZG_BIAS_HIGH

The ZG_BIAS_LOW (see Table 120 and Table 121) and ZG_BIAS_HIGH (see Table 122 and Table 123) registers combine to allow users to adjust the bias of the z-axis gyroscopes. The digital format examples in Table 30 also apply to the ZG_BIAS_HIGH register, and the digital format examples in Table 31 apply to the number that comes from combining the ZG_BIAS_LOW and ZG_BIAS_HIGH registers. These registers influence the z-axis gyroscope measurements in the same manner that the XG_BIAS_LOW and XG_BIAS_HIGH registers influence the x-axis gyroscope measurements (see Figure 51).

Table 120. ZG_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x18, 0x19	0x0000	R/W	Yes

Table 121. ZG_BIAS_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, lower word, twos complement, 0°/sec = 0x0000, 1 LSB = $K_G \div 2^{16}$ (see Table 29)

Table 122. ZG_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1A, 0x1B	0x0000	R/W	Yes

Table 123. ZG_BIAS_HIGH Bit Descriptions

Bits	Description
[15:0]	Z-axis gyroscope offset correction, upper word, twos complement, 0°/sec = 0x0000, 1 LSB = K_G (see Table 29)

Accelerometer Bias Adjustment, XA_BIAS_LOW and XA_BIAS_HIGH

The XA_BIAS_LOW (see Table 124 and Table 125) and XA_BIAS_HIGH (see Table 126 and Table 127) registers combine to allow the user to adjust the bias of the x-axis accelerometers. The digital format examples in Table 45 also apply to the XA_BIAS_HIGH register and the digital format examples in Table 46 apply to the number that comes from combining the XA_BIAS_LOW and XA_BIAS_HIGH registers. See Figure 52 for an illustration of how these two registers combine and influence the x-axis gyroscope measurements.

Table 124. XA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1C, 0x1D	0x0000	R/W	Yes

Table 125. XA_BIAS_LOW Bit Descriptions

Bits	Description
[15:0]	X-axis accelerometer offset correction, lower word, twos complement, 0 *g* = 0x0000, 1 LSB = $K_A \div 2^{16}$ (see Table 44)

Table 126. XA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x1E, 0x1F	0x0000	R/W	Yes

Table 127. XA_BIAS_HIGH Bit Descriptions

Bits	Description
[15:0]	X-axis accelerometer offset correction, upper word, twos complement, 0 *g* = 0x0000, 1 LSB = K_A (see Table 44)

Accelerometer Bias Adjustment, YA_BIAS_LOW and YA_BIAS_HIGH

The YA_BIAS_LOW (see Table 128 and Table 129) and YA_BIAS_HIGH (see Table 130 and Table 131) registers combine to allow the user to adjust the bias of the y-axis accelerometers. The digital format examples in Table 45 also apply to the YA_BIAS_HIGH register, and the digital format examples in Table 46 apply to the number that comes from combining the YA_BIAS_LOW and YA_BIAS_HIGH registers. These registers influence the y-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 52).

Table 128. YA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x20, 0x21	0x0000	R/W	Yes

Table 129. YA_BIAS_LOW Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, lower word, twos complement, 0 *g* = 0x0000, 1 LSB = $K_A \div 2^{16}$ (see Table 44)

Table 130. YA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x22, 0x23	0x0000	R/W	Yes

Table 131. YA_BIAS_HIGH Bit Descriptions

Bits	Description
[15:0]	Y-axis accelerometer offset correction, upper word, twos complement, 0 *g* = 0x0000, 1 LSB = K_A (see Table 44)

USER REGISTER DEFINITIONS

Accelerometer Bias Adjustment, ZA_BIAS_LOW and ZA_BIAS_HIGH

The ZA_BIAS_LOW (see Table 132 and Table 133) and ZA_BIAS_HIGH (see Table 134 and Table 135) registers combine to allow users to adjust the bias of the z-axis accelerometers. The digital format examples in Table 45 also apply to the ZA_BIAS_HIGH register and the digital format examples in Table 46 apply to the number that comes from combining the ZA_BIAS_LOW and ZA_BIAS_HIGH registers. These registers influence the z-axis accelerometer measurements in the same manner that the XA_BIAS_LOW and XA_BIAS_HIGH registers influence the x-axis accelerometer measurements (see Figure 52).

Table 132. ZA_BIAS_LOW Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x24, 0x25	0x0000	R/W	Yes

Table 133. ZA_BIAS_LOW Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, lower word, twos complement, 0 *g* = 0x0000, 1 LSB = $K_A \div 2^{16}$ (see Table 44)

Table 134. ZA_BIAS_HIGH Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x26, 0x27	0x0000	R/W	Yes

Table 135. ZA_BIAS_HIGH Bit Descriptions

Bits	Description
[15:0]	Z-axis accelerometer offset correction, upper word, twos complement, 0 *g* = 0x0000, 1 LSB = K_A (see Table 44)

SCRATCH REGISTERS, USER_SCR_X

The USER_SCR_1 (see Table 136 and Table 137), USER_SCR_2 (see Table 138 and Table 139), USER_SCR_3 (see Table 140 and Table 141), and USER_SCR_4 (see Table 142 and Table 143) registers provide four locations for the user to store information.

Table 136. USER_SCR_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x74, 0x75	0x0000	R/W	Yes

Table 137. USER_SCR_1 Bit Descriptions

Bits	Description
[15:0]	User defined

Table 138. USER_SCR_2 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x76, 0x77	0x0000	R/W	Yes

Table 139. USER_SCR_2 Bit Descriptions

Bits	Description
[15:0]	User defined

Table 140. USER_SCR_3 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x78, 0x79	0x0000	R/W	Yes

Table 141. USER_SCR_3 Bit Descriptions

Bits	Description
[15:0]	User defined

Table 142. USER_SCR_4 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7A, 0x7B	0x0000	R/W	Yes

Table 143. USER_SCR_4 Bit Descriptions

Bits	Description
[15:0]	User defined

FLASH MEMORY ENDURANCE COUNTER, ENDURANCE_LWR AND ENDURANCE_UPR

The ENDURANCE_LWR (see Table 144 and Table 145) and ENDURANCE_UPR (see Table 146 and Table 147) registers combine to provide a 32-bit, binary counter that tracks the number of flash memory write cycles. In addition to the number of write cycles, the flash memory has a finite service lifetime, which depends on the junction temperature. Figure 53 provides guidance for estimating the retention life for the flash memory at specific junction temperatures. The junction temperature is approximately 7°C more than the case temperature under normal conditions, including no airflow nor local heat sources.

Table 144. ENDURANCE_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7C, 0x7D	Not applicable	R	Yes

Table 145. ENDURANCE_LWR Bit Descriptions

Bits	Description
[15:0]	Flash memory write counter, low word

Table 146. ENDURANCE_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x02	0x7E, 0x7F	Not applicable	R	Yes

Table 147. ENDURANCE_UPR Bit Descriptions

Bits	Description
[15:0]	Flash memory write counter, high word

USER REGISTER DEFINITIONS

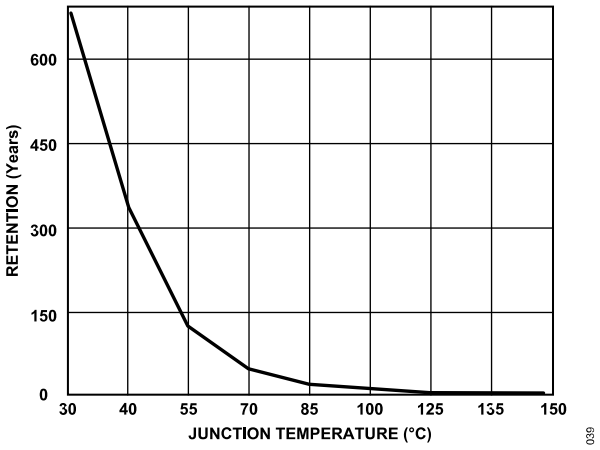

Figure 53. Flash Memory Retention

GLOBAL COMMANDS, GLOB_CMD

The GLOB_CMD register (see Table 148 and Table 149) provides trigger bits for several operations. Write a 1 to the appropriate bit in GLOB_CMD to start a particular function.

Table 148. GLOB_CMD Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x02, 0x03	Not applicable	W	No

Table 149. GLOB_CMD Bit Descriptions

Bits	Description
[15:8]	Not used
7	Software reset
6	Clear user calibration
[5:4]	Not used
3	Flash memory update
2	Not used
1	Self test
0	Bias correction update

Software Reset

Set page to Page 3 (DIN = 0x8003) and then set GLOB_CMD, Bit 7 = 1 (DIN = 0x8280, then DIN = 0x8300) to initiate a reset in the operation of the ADIS16545/ADIS16547. This reset removes all data, initializes all registers from their flash settings, and restarts data sampling and processing. This function provides a firmware alternative to providing a low pulse on the $\overline{\text{RST}}$ pin (see Table 11, Pin 8).

Clear User Calibration

Set page to Page 3 (DIN = 0x8003) and then set GLOB_CMD, Bit 6 = 1 (DIN = 0x8240, then DIN = 0x8300) to clear all user bias/scale adjustments for each accelerometer and gyroscope. This command writes 0x0000 to the all of the registers on Page 2 except for the PAGE_ID and USER_SCR_x registers (where x = 1 to 4). However, this command does not alter the user values stored in the flash memory.

Flash Memory Update

Set page to Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 3 = 1 (DIN = 0x8208, then DIN = 0x8300) to initiate a manual flash update. STATUS, Bit 6 (see Table 23) identifies success (0) or failure (1) in completing this process.

On Demand Self Test (ODST)

Set page to page 3 (DIN = 0x8003) and then set GLOB_CMD, Bit 1 = 1 (DIN = 0x8202, then DIN = 0x8300) to run the ODST routine. False positive results are possible when the executing the ODST while the device is in motion.

The ODST routine performs the following steps on the gyroscopes:

1. Measures the output on each sensor.
2. Activates an internal force on the mechanical elements of each sensor, which simulates the force associated with actual inertial motion.
3. Measures the output response on each sensor.
4. Deactivates the internal force on each sensor.
5. Calculates the difference between the force on and normal operating conditions (force off).
6. Compares the difference between the internal pass or fail criteria.
7. Reports the pass or fail results for each sensor in DIAG_STS (see Table 25) and the overall pass or fail flag in STATUS, Bit 5 (see Table 23).

The ODST routine performs the following on the accelerometers:

1. Activates an internal force on the mechanical elements of each sensor, which simulates the force associated with actual inertial motion.
2. Measures the output response on each sensor.
3. Activates a second internal force of higher magnitude on the mechanical elements of each sensor.
4. Measures the output response on each sensor.
5. Calculates and compares the difference between the two stimuli to internal pass or fail criteria.
6. Reports the pass or fail results for each sensor in DIAG_STS (see Table 25) and the overall pass or fail flag in STATUS, Bit 5 (see Table 23).

Bias Correction Update

Set page to Page 3 (DIN = 0x8003) and set GLOB_CMD, Bit 0 = 1 (DIN = 0x8201, then DIN = 0x8300) to update the user offset registers with the correction factors of the continuous bias estimation (CBE) (see Table 159). Ensure that the inertial platform is stable during the entire average time for optimal bias estimates.

USER REGISTER DEFINITIONS

AUXILIARY INPUT AND OUTPUT LINE CONFIGURATION, FNCTIO_CTRL

The FNCTIO_CTRL register (see Table 150 and Table 151) provides configuration control for each input and output pin (DIO1, DIO2, DIO3, and DIO4). Each DIOx pin supports only one function at a time. When a single pin has two assignments, the enable bit for the lower priority function automatically resets to zero (disabling the lower priority function). The order of priority is as follows, from highest priority to lowest priority: data ready, sync clock input, alarm indicator, and general-purpose. The ADIS16545/ADIS16547 can take up to 20 ms to execute a write command to the FNCTIO_CTRL register. During this time, the operational state and the contents of the register remain unchanged, but the SPI interface supports normal communication (for accessing other registers).

Table 150. FNCTIO_CTRL Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x06, 0x07	0x000D	R/W	Yes

Table 151. FNCTIO_CTRL Bit Descriptions

Bits	Description
[15:13]	Not used
12	Alarm indicator enable 1 = enabled 0 = disabled (default)
11	Alarm indicator polarity 1 = active high 0 = active low (default)
[10:9]	Alarm indicator select 00 = DIO1 (default) 01 = DIO2 10 = DIO3 11 = DIO4
8	Sync clock mode 1 = scaled sync mode 0 = direct sync mode (default, external sync input frequency equals the sample rate)
7	Sync clock input enable 1 = enabled 0 = disabled (default)
6	Sync clock input polarity 1 = rising edge 0 = falling edge (default)
[5:4]	Sync clock input line selection 00 = DIO1 (default) 01 = DIO2 10 = DIO3 11 = DIO4
3	Data ready enable 1 = enabled(default) 0 = disabled
2	Data ready polarity 1 = active high (default) 0 = active low
[1:0]	Data ready line selection 00 = DIO1 01 = DIO2 (default) 10 = DIO3 11 = DIO4

Data Ready Indicator

The FNCTIO_CTRL, Bits[3:0] provide three configuration options for the data ready function: enable and disable, polarity, and which DIOx line to use. The primary purpose of this signal is to drive the interrupt control line of an embedded processor, which synchronizes data collection and minimizes latency. The factory default assigns DIO2 as a positive polarity, data ready signal, which means the data in the output registers is valid when the DIO2 line is high (see Figure 35). This configuration works well when DIO2 drives an interrupt service pin that activates on a low to high pulse.

Use the following sequence to change this assignment to DIO3 with negative polarity:

1. Set page to Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL, Bits[3:0] = 1010 (DIN = 0x860A, then DIN = 0x8700).

When using DIO1 to support the data ready function, the data ready signal can experience transient pulses on start up before the ADIS16545/ADIS16547 start data production. If it is necessary to use DIO1 for this function, use it with a delay or other control mechanism to prevent premature data acquisition activity during the start-up process. See the Timing Specifications for the time required for the ADIS16545/ADIS16547 to produce reliable data outputs.

Input Sync and Clock Control

FNCTIO_CTRL, Bits[8:4] provide several configuration options for using one of the DIOx lines as an external clock signal and for controlling inertial sensor data collection and processing. For example, use the following sequence to establish DIO4 as a positive polarity, input clock pin that operates in sync mode and preserves the factory default setting for the data ready function:

1. Set page to Page 3 (DIN = 0x8003).
2. Set FNCTIO_CTRL, Bits[7:0] = 0xFD (DIN = 0x86FD).
3. Set FNCTIO_CTRL, Bits[15:8] = 0x00 (DIN = 0x8700).

In direct sync mode, the ADIS16545/ADIS16547 disable their internal sample clock, and the frequency of the external clock signal establishes the rate of data collection and processing (f_{SM} in Figure 29 and Figure 30). When using scaled sync mode (FNCTIO_CTRL,

USER REGISTER DEFINITIONS

Bit 8 = 1), the rate of data collection and production (f_{SM}) is equal to the product of the external clock frequency and scale factor (K_{ECSF}) in the UPSCALE register (see Table 161).

GENERAL-PURPOSE INPUT AND OUTPUT CONTROL, GPIO_CTRL

When FNCTIO_CTRL does not configure a DIOx pin, the GPIO_CTRL register (see Table 152 and Table 153) provides user controls for general-purpose use of the DIOx pins. GPIO_CTRL, Bits[3:0], provide input and output assignment controls for each line. When the DIOx lines are inputs, monitor their level by reading GPIO_CTRL, Bits[7:4]. When the DIOx lines are used as outputs, set their level by writing to GPIO_CTRL, Bits[7:4].

For example, use the following sequence to set DIO1 and DIO3 as high and low output lines, respectively, and set DIO2 and DIO4 as input lines:

1. Set page to Page 3 (DIN = 0x8003).
1. Set GPIO_CTRL, Bits[7:0] = 0x15 (DIN = 0x8815, then DIN = 0x8900).

Table 152. GPIO_CTRL Register Definitions[1]

Page	Addresses	Default	Access	Flash Backup
0x03	0x08, 0x09	0x00X0	R/W	Yes

[1] GPIO_CTRL, Bits[7:4] reflect the logic levels on the DIOx lines and do not have a default setting.

Table 153. GPIO_CTRL Bit Descriptions[1]

Bits	Description
[15:8]	Don't care
7	General-Purpose Input and Output Line 4 (DIO4) data level
6	General-Purpose Input and Output Line 3 (DIO3) data level
5	General-Purpose Input and Output Line 2 (DIO2) data level
4	General-Purpose Input and Output Line 1 (DIO1) data level
3	General-Purpose Input and Output Line 4 (DIO4) direction control (1 = output, 0 = input)
2	General-Purpose Input and Output Line 3 (DIO3) direction control (1 = output, 0 = input)
1	General-Purpose Input and Output Line 2 (DIO2) direction control (1 = output, 0 = input)
0	General-Purpose Input and Output Line 1 (DIO1) direction control (1 = output, 0 = input)

[1] GPIO_CTRL, Bits[7:4] reflect the logic levels on the DIOx lines and do not have a default setting.

MISCELLANEOUS CONFIGURATION, CONFIG

The CONFIG register (see Table 154 and Table 155) provides configuration options for the data contained in a burst transfer, as well as the point of percussion alignment (enable and disable).

Table 154. CONFIG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0A, 0x0B	0x0040	R/W	Yes

Table 155. CONFIG Bit Descriptions

Bits	Description
[15:9]	Not used.
8	Burst read output array selection bit (BURST_SEL). This bit is used to select the type of inertial output that is part of the burst read. When BURST_SEL = 0 (default), the output includes the calibrated gyroscope and accelerometer outputs. When BURST_SEL = 1, the output includes the delta angle and delta velocity outputs. See the Burst Read Function section for details about the format of the burst array for both options. The user must wait until a full data ready cycle until the burst array updates with the desired data type.
7	Not used. Set to 0.
6	Point of percussion alignment. When set, this bit allows for relocation of the acceleration sensors to a common point of percussion on package surface. 0: disabled. 1: enabled (default).
[5:0]	Not used. Set the bits in this field to all 0s.

Point of Percussion

CONFIG, Bit 6, offers a point of percussion alignment function that maps the accelerometer sensors to the corner of the package identified in Figure 54. To activate this feature, turn to Page 3 (DIN = 0x8003) and set CONFIG, Bit 6 = 1 (DIN = 0x8A40, then DIN = 0x8B00).

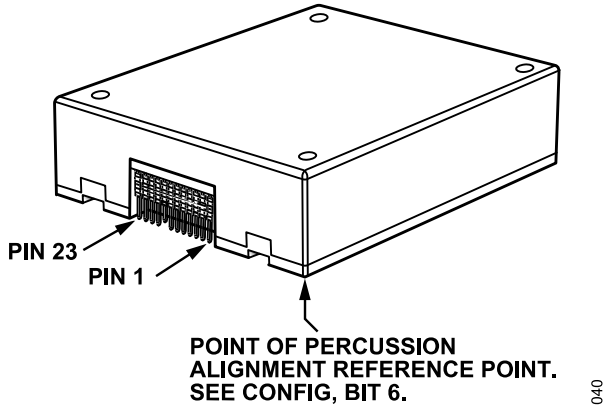

Figure 54. Point of Percussion Reference Point

USER REGISTER DEFINITIONS

DECIMATION FILTER, DEC_RATE

The DEC_RATE register (see Table 156 and Table 157) provides user control for the final filter stage (see Figure 32), which averages and decimates the accelerometers and gyroscopes data, and extends the time that the delta angle and delta velocity track between each update. The output sample rate is equal to 4000/(DEC_RATE + 1). For example, turn to Page 3 (DIN = 0x8003) and set DEC_RATE = 0x27 (DIN = 0x8C27, then DIN = 0x8D00) to reduce the output sample rate by a factor of 40. If f_{SM} equals the default value of 4000, this setting reduces the sample rate to 100 SPS (f_{SM} ÷ 40).

To prevent processing overflows, the post-decimation sample rate must never be less than 1 SPS.

Table 156. DEC_RATE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0C, 0x0D	0x0000	R/W	Yes

Table 157. DEC_RATE Bit Descriptions

Bits	Description
[15:11]	Don't care
[10:0]	Decimation rate, binary format, maximum = 3999

CONTINUOUS BIAS ESTIMATION (CBE), NULL_CNFG

The NULL_CNFG register (see Table 158 and Table 159) provides the configuration controls for the CBE, which associates with the bias correction update command in GLOB_CMD, Bit 0 (see Table 149). NULL_CNFG, Bits[3:0], establishes the total average time (t_A) for the bias estimates and NULL_CNFG, Bits[13:8], provides on and off controls for each sensor. The factory default configuration for NULL_CNFG enables the bias null command for the gyroscopes, disables the bias null command for the accelerometers, and sets t_A to ~15.42 seconds (assuming f_{SM} = 4000 SPS). Note that the time calculations for the CBE scale with f_{SM}. To calculate the time base (t_B) and the t_A, use the following equations:

$$t_B = 2^{TBC}/f_{SM} = 2^{10}/f_{SM} \cong 0.241 \text{ (assuming } f_{SM} = 4000 \text{ SPS)}$$

$$t_A = 64 \times t_B = 64 \times 0.241 = 15.42 \text{ seconds}$$

When a sensor bit in NULL_CNFG is active (equal to 1), setting GLOB_CMD, Bit 0 = 1 (DIN sequence: 0x8003, 0x8201, 0x8300) causes the respective bias correction register for each axis to automatically update with a value that corrects for the bias error on each axis. These correction factors come from the CBE calculations.

For example, setting NULL_CNFG, Bit 8 equal to 1 enables an update in the XG_BIAS_LOW (see Table 113) and XG_BIAS_HIGH (see Table 115) registers.

Table 158. NULL_CNFG Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x0E, 0x0F	0x070A	R/W	Yes

Table 159. NULL_CNFG Bit Descriptions

Bits	Description
[15:14]	Not used
13	Z-axis acceleration bias correction enable (1 = enabled)
12	Y-axis acceleration bias correction enable (1 = enabled)
11	X-axis acceleration bias correction enable (1 = enabled)
10	Z-axis gyroscope bias correction enable (1 = enabled)
9	Y-axis gyroscope bias correction enable (1 = enabled)
8	X-axis gyroscope bias correction enable (1 = enabled)
[7:4]	Not used
[3:0]	Time base control (TBC) range: 0 to 13 (default = 10), $t_B = 2^{TBC}/f_{SM}$, time base, and $t_A = 64 \times t_B$, average time

SCALING THE INPUT CLOCK (SCALED SYNC MODE), UPSCALE

The scaled sync mode (FNCTIO_CTRL, Bit 8 = 1, see Table 151) supports the use of an input sync frequency that is slower than the data sample rates of the inertial sensors. This mode supports a frequency range of 1 Hz to 128 Hz for the input sync mode. In this mode, the data sample rate is equal to the product of the value in the UPSCALE register (see Table 160 and Table 161) and the input sync frequency.

For example, the following command sequence sets the data collection and processing rate (f_{SM} in Figure 29 and Figure 30) to 4000 Hz (UPSCALE = 0x0FA0) when using a 1 Hz signal on the DIO3 line as the external clock input, and preserves the factory default configuration for the data ready signal:

1. Turn to Page 3 (DIN = 0x8003).
2. Set UPSCALE, Bits[7:0] = 0xA0 (DIN = 0x90A0).
3. Set UPSCALE, Bits[15:8] = 0x0F (DIN = 0x910F).
4. Set FNCTIO_CTRL, Bits[7:0] = 0xED (DIN = 0x86ED).
5. Set FNCTIO_CTRL, Bits[15:8] = 0x01 (DIN = 0x8701).

Table 160. UPSCALE Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x10, 0x11	0x0FA0	R/W	Yes

Table 161. UPSCALE Bit Descriptions

Bits	Description
[15:0]	External clock scale factor (K_{ECSF}), binary format

USER REGISTER DEFINITIONS

MEASUREMENT RANGE IDENTIFIER, RANGE_MDL

The RANGE_MDL register (see Table 162 and Table 163) provides a convenient method for identifying the model (and gyroscope measurement range) of the ADIS16545/ADIS16547.

Table 162. RANGE_MDL Register Definitions[1]

Page	Addresses	Default	Access	Flash Backup
0x03	0x12, 0x13	N/A	R	Yes

[1] N/A means not applicable.

Table 163. RANGE_MDL Bit Descriptions

Bits	Description	Range
[15:3]	Not used	
[3:0]	0011 = ADIS16545-1AMLZ and ADIS16547-1AMLZ	±125°/sec
	0111 = ADIS16545-2AMLZ and ADIS16547-2AMLZ	±450°/sec
	1111 = ADIS16545-3AMLZ and ADIS16547-3AMLZ	±2000°/sec

FIR FILTERS

FIR Filters Control, FILTR_BNK_0 and FILTR_BNK_1

The FILTR_BNK_0 (see Table 164 and Table 165) and FILTR_BNK_1 (see Table 166 and Table 167) registers provide the configuration controls for the FIR filter bank in the signal chain of each sensor (see Figure 32). These registers provide on and off control for the FIR bank for each inertial sensor, along with the FIR bank (A, B, C, or D) that each sensor uses.

Table 164. FILTR_BNK_0 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x16, 0x17	0x0000	R/W	Yes

Table 165. FILTR_BNK_0 Bit Descriptions

Bits	Description (Default = 0x0000)
15	Don't care
14	Y-axis accelerometer filter enable (1 = enabled)
[13:12]	Y-axis accelerometer filter bank selection 00 = Bank A 01 = Bank B 10 = Bank C 11 = Bank D
11	X-axis accelerometer filter enable (1 = enabled)
[10:9]	X-axis accelerometer filter bank selection: 00 = Bank A 01 = Bank B 10 = Bank C 11 = Bank D
8	Z-axis gyroscope filter enable (1 = enabled)
[7:6]	Z-axis gyroscope filter bank selection: 00 = Bank A 01 = Bank B

Table 165. FILTR_BNK_0 Bit Descriptions (Continued)

Bits	Description (Default = 0x0000)
	10 = Bank C 11 = Bank D
5	Y-axis gyroscope filter enable (1 = enabled)
[4:3]	Y-axis gyroscope filter bank selection: 00 = Bank A 01 = Bank B 10 = Bank C 11 = Bank D
2	X-axis gyroscope filter enable (1 = enabled)
[1:0]	X-axis gyroscope filter bank selection 00 = Bank A 01 = Bank B 10 = Bank C 11 = Bank D

Table 166. FILTR_BNK_1 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x18, 0x19	0x0000	R/W	Yes

Table 167. FILTR_BNK_1 Bit Descriptions

Bits	Description
[15:3]	Don't care
2	Z-axis accelerometer filter enable (1 = enabled)
[1:0]	Z-axis accelerometer filter bank selection: 00 = Bank A 01 = Bank B 10 = Bank C 11 = Bank D

FIR Filter Bank Memory Maps

The ADIS16545/ADIS16547 provide four FIR filter banks to configure and select for each individual inertial sensor using the FILTR_BNK_0 (see Table 165) and FILTR_BNK_1 (see Table 167) registers. Each FIR filter bank (A, B, C, and D) has 120 taps that consume two pages of memory. The coefficient associated with each tap, in each filter bank, has its own dedicated register that uses a 16-bit, twos complement format. The FIR filter has unity gain when the sum of all of the coefficients is equal to 32,768. For filter designs that require fewer than 120 taps, write 0x0000 to all unused registers to eliminate the latency associated with that particular tap.

FIR Filter Bank A, FIR_COEF_A000 to FIR_COEF_A119

Table 168. FIR Filter Bank A Memory Map

Page	PAGE_ID	Addresses	Register
5	0x05	0x00, 0x01	PAGE_ID
5	0x05	0x02 to 0x07	Not used
5	0x05	0x08, 0x09	FIR_COEF_A000
5	0x05	0x0A, 0x0B	FIR_COEF_A001

USER REGISTER DEFINITIONS

Table 168. FIR Filter Bank A Memory Map (Continued)

Page	PAGE_ID	Addresses	Register
5	0x05	0x0C to 0x7D	FIR_COEF_A002 to FIR_COEF_A058
5	0x05	0x7E, 0x07F	FIR_COEF_A059
6	0x06	0x00, 0x01	PAGE_ID
6	0x06	0x02 to 0x07	Not used
6	0x06	0x08, 0x09	FIR_COEF_A060
6	0x06	0x0A, 0x0B	FIR_COEF_A061
6	0x06	0x0C to 0x7D	FIR_COEF_A062 to FIR_COEF_A118
6	0x06	0x7E, 0x7F	FIR_COEF_A119

Table 169 and Table 170 provide detailed register and bit definitions for one of the FIR coefficient registers in Bank A, FIR_COEF_A071. Table 171 provides a configuration example, which sets this register to a decimal value of −169 (0xFF57).

Table 169. FIR_COEF_A071 Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x06	0x1E, 0x1F	Not applicable	R/W	Yes

Table 170. FIR_COEF_A071 Bit Descriptions

Bits	Description
[15:0]	FIR Bank A, Coefficient 71, twos complement

Table 171. Configuration Example, FIR Coefficient

DIN Command	Description
0x8006	Turn to Page 6
0x9E57	FIR_COEF_A071, Bits[7:0] = 0x57
0x9FFF	FIR_COEF_A071, Bits[15:8] = 0xFF

FIR Filter Bank B, FIR_COEF_B000 to FIR_COEF_B119

Table 172. Filter Bank B Memory Map

Page	PAGE_ID	Addresses	Register
7	0x07	0x00, 0x01	PAGE_ID
7	0x07	0x02 to 0x07	Not used
7	0x07	0x08, 0x09	FIR_COEF_B000
7	0x07	0x0A, 0x0B	FIR_COEF_B001
7	0x07	0x0C to 0x7D	FIR_COEF_B002 to FIR_COEF_B058
7	0x07	0x7E, 0x07F	FIR_COEF_B059
8	0x08	0x00, 0x01	PAGE_ID
8	0x08	0x02 to 0x07	Not used
8	0x08	0x08, 0x09	FIR_COEF_B060
8	0x08	0x0A, 0x0B	FIR_COEF_B061
8	0x08	0x0C to 0x7D	FIR_COEF_B062 to FIR_COEF_B118
8	0x08	0x7E, 0x7F	FIR_COEF_B119

FIR Filter Bank C, FIR_COEF_C000 to FIR_COEF_C119

Table 173. Filter Bank C Memory Map

Page	PAGE_ID	Addresses	Register
9	0x09	0x00, 0x01	PAGE_ID
9	0x09	0x02 to 0x07	Not used
9	0x09	0x08, 0x09	FIR_COEF_C000
9	0x09	0x0A, 0x0B	FIR_COEF_C001
9	0x09	0x0C to 0x7D	FIR_COEF_C002 to FIR_COEF_C058
9	0x09	0x7E, 0x07F	FIR_COEF_C059
10	0x0A	0x00, 0x01	PAGE_ID
10	0x0A	0x02 to 0x07	Not used
10	0x0A	0x08, 0x09	FIR_COEF_C060
10	0x0A	0x0A, 0x0B	FIR_COEF_C061
10	0x0A	0x0C to 0x7D	FIR_COEF_C062 to FIR_COEF_C118
10	0x0A	0x7E, 0x7F	FIR_COEF_C119

FIR Filter Bank D, FIR_COEF_D000 to FIR_COEF_D119

Table 174. Filter Bank D Memory Map

Page	PAGE_ID	Addresses	Register
11	0x0B	0x00, 0x01	PAGE_ID
11	0x0B	0x02 to 0x07	Not used
11	0x0B	0x08, 0x09	FIR_COEF_D000
11	0x0B	0x0A, 0x0B	FIR_COEF_D001
11	0x0B	0x0C to 0x7D	FIR_COEF_D002 to FIR_COEF_D058
11	0x0B	0x7E, 0x07F	FIR_COEF_D059
12	0x0C	0x00, 0x01	PAGE_ID
12	0x0C	0x02 to 0x07	Not used
12	0x0C	0x08, 0x09	FIR_COEF_D060
12	0x0C	0x0A, 0x0B	FIR_COEF_D061
12	0x0C	0x0C to 0x7D	FIR_COEF_D062 to FIR_COEF_D118
12	0x0C	0x7E, 0x7F	FIR_COEF_D119

Default Filter Performance

The FIR filter banks have factory programmed filter designs that are all LPFs that have unity DC gain. Table 175 provides a summary of each filter design, and Figure 55 shows the frequency response characteristics. The phase delay is equal to ½ of the total number of taps.

Table 175. FIR Filter Descriptions, Default Configuration

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
A	120	300
B	120	100
C	32	300

USER REGISTER DEFINITIONS

Table 175. FIR Filter Descriptions, Default Configuration (Continued)

FIR Filter Bank	Taps	−3 dB Frequency (Hz)
D	32	100

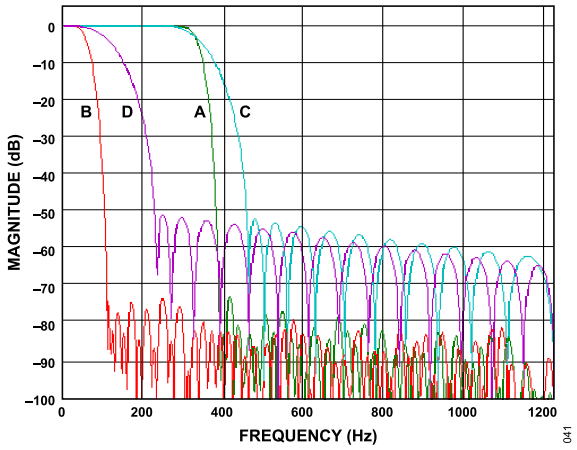

Figure 55. FIR Filter Frequency Response Curves

FIRMWARE REVISION, FIRM_REV

The FIRM_REV register (see Table 176 and Table 177) provide the firmware revision for the internal processor. Each nibble represents a digit in the revision code For example, if FIRM_REV = 0x0102, the firmware revision is 1.02.

Table 176. FIRM_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x78, 0x79	Not applicable	R	Yes

Table 177. FIRM_REV Bit Descriptions

Bits	Description
[15:12]	Firmware revision BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Firmware revision BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Firmware revision BCD code, tenths digit, numerical format = 4-bit binary, range = 0 to 9
[3:0]	Firmware revision BCD code, hundredths digit, numerical format = 4-bit binary, range = 0 to 9

FIRMWARE REVISION MONTH AND DAY, FIRM_DM

The FIRM_DM register (see Table 176 and Table 177) contains the month and day of the factory configuration date. Bits[15:12] and Bits[11:8] of Register FIRM_DM contain digits that represent the month of the factory configuration in a binary coded decimal (BCD) format. For example, November is the 11th month in a year and is represented by Register FIRM_DM, Bits[15:8] = 0x11. Bits[7:4] and Bits[3:0] of Register FIRM_DM contain digits that represent the day of factory configuration in a BCD format. For example, the 27th day of the month is represented by Register FIRM_DM, Bits[7:0] = 0x27.

Table 178. FIRM_DM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7A, 0x7B	Not applicable	R	Yes

Table 179. FIRM_DM Bit Descriptions

Bits	Description
[15:12]	Factory configuration month BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 2
[11:8]	Factory configuration month BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration day BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration day BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

FIRMWARE REVISION YEAR, FIRM_Y

The FIRM_Y register (see Table 180 and Table 181) contains the year of the factory configuration date. For example, the year 2023 is represented by FIRM_Y = 0x2023.

Table 180. FIRM_Y Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7C, 0x7D	Not applicable	R	Yes

Table 181. FIRM_Y Bit Descriptions

Bits	Description
[15:12]	Factory configuration year BCD code, thousands digit, numerical format = 4-bit binary, range = 0 to 9
[11:8]	Factory configuration year BCD code, hundreds digit, numerical format = 4-bit binary, range = 0 to 9
[7:4]	Factory configuration year BCD code, tens digit, numerical format = 4-bit binary, range = 0 to 3
[3:0]	Factory configuration year BCD code, ones digit, numerical format = 4-bit binary, range = 0 to 9

BOOT REVISION NUMBER, BOOT_REV

The BOOT_REV register (see Table 182 and Table 183) contains the revision of the boot code in the ADIS16545/ADIS16547 processor core.

Table 182. BOOT_REV Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x03	0x7E, 0x7F	Not applicable	R	Yes

Table 183. BOOT_REV Bit Descriptions

Bits	Description
[15:8]	Binary, major revision number
[7:0]	Binary, minor revision number

CONTINUOUS SRAM TESTING

This device employs a CRC function on the SRAM memory blocks that contain the program code (CODE_SIG_xxx) and the calibration coefficients (CAL_DRV_xxx). This process operates in the background and generates real-time, 32-bit CRC values for

USER REGISTER DEFINITIONS

the program code and calibration coefficients, respectively. At the conclusion of each cycle, the processor writes these calculated values in the CAL_DRV_xxx and CODE_DRV_xxx registers (see Table 189, Table 191, Table 197, and Table 199) and compares them with the signature values, which reflect the state of these memory locations at the time of factory configuration. When the calculation results do not match the signature values, STATUS, Bit 2 increases to a 1. The respective signature values are available for user access through the CAL_SIG_xxx and CODE_SIG_xxx registers (see Table 185, Table 187, Table 193, and Table 195). The following conditions must be met for STATUS, Bit 2 to remain at the zero level:

- CAL_SIG_LWR = CAL_DRV_LWR
- CAL_SIG_UPR = CAL_DRV_UPR
- CODE_SIG_LWR = CODE_DRV_LWR
- CODE_SIG_UPR = CODE_DRV_UPR

SIGNATURE CRC, CALIBRATION VALUES, CAL_SIG_LWR

Table 184. CAL_SIG_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x04, 0x05	Not applicable	R	Yes

Table 185. CAL_SIG_LWR Bit Descriptions

Bits	Description
[15:0]	Factory programmed CRC value for the calibration coefficients, lower word

SIGNATURE CRC, CALIBRATION VALUES, CAL_SIG_UPR

Table 186. CAL_SIG_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x06, 0x07	Not applicable	R	Yes

Table 187. CAL_SIG_UPR Bit Descriptions

Bits	Description
[15:0]	Factory programmed CRC value for the calibration coefficients, upper word

DERIVED CRC, CALIBRATION VALUES, CAL_DRV_LWR

Table 188. CAL_DRV_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x08, 0x09	Not applicable	R	No

Table 189. CAL_DRV_LWR Bit Definitions

Bits	Description
[15:0]	Calculated CRC value for the calibration coefficients, lower word

DERIVED CRC, CALIBRATION VALUES, CAL_DRV_UPR

Table 190. CAL_DRV_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x0A, 0x0B	Not applicable	R	No

Table 191. CAL_DRV_UPR Bit Descriptions

Bits	Description
[15:0]	Calculated CRC value for the calibration coefficients, upper word

SIGNATURE CRC, PROGRAM CODE, CODE_SIG_LWR

Table 192. CODE_SIG_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x0C, 0x0D	Not applicable	R	Yes

Table 193. CODE_SIG_LWR Bit Descriptions

Bits	Description
[15:0]	Factory programmed CRC value for the program code, low word

SIGNATURE CRC, PROGRAM CODE, CODE_SIG_UPR

Table 194. CODE_SIG_UPR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x0E, 0x0F	Not applicable	R	Yes

Table 195. CODE_SIG_UPR Bit Definitions

Bits	Description
[15:0]	Factory programmed CRC value for the program code, upper word

DERIVED CRC, PROGRAM CODE, CODE_DRV_LWR

Table 196. CODE_DRV_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x10, 0x11	Not applicable	R	No

Table 197. CODE_DRV_LWR Bit Descriptions

Bits	Description
[15:0]	Calculated CRC value for the program code, lower word

DERIVED CRC, PROGRAM CODE, CODE_DRV_UPR

Table 198. CODE_DRV_LWR Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x12, 0x13	Not applicable	R	No

Table 199. CODE_DRV_UPR Bit Descriptions

Bits	Description
[15:0]	Calculated CRC value for the program code, upper word

USER REGISTER DEFINITIONS

LOT SPECIFIC SERIAL NUMBER, SERIAL_NUM

Table 200. SERIAL_NUM Register Definitions

Page	Addresses	Default	Access	Flash Backup
0x04	0x20, 0x21	Not applicable	R	Yes

Table 201. SERIAL_NUM Bit Descriptions

Bits	Description
[15:0]	Lot specific serial number

APPLICATIONS INFORMATION

MECHANICAL INTERFACE DESIGN

For the best performance, follow these guidelines when installing the ADIS16545/ADIS16547 into a system:

- Eliminate opportunity for translational force (x- and y-axis direction, per Figure 46) application on the electrical connector.
- Use uniform mounting forces on all four corners. The suggested torque setting is 40 inch-ounces (0.285 Nm).
- When mounting the ADIS16545/ADIS16547 on the PCB with a mating connector (see Figure 56), use a diameter of at least 2.85 mm for the pass-through holes.

These guidelines help prevent irregular force profiles, which can warp the package and introduce bias errors in the sensors. Figure 56 and Figure 57 provide details for mounting hole and connector alignment pin drill locations.

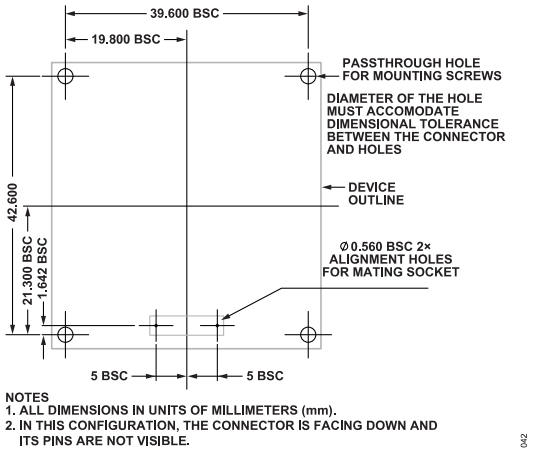

Figure 56. Suggested PCB Layout Pattern, Connector Down

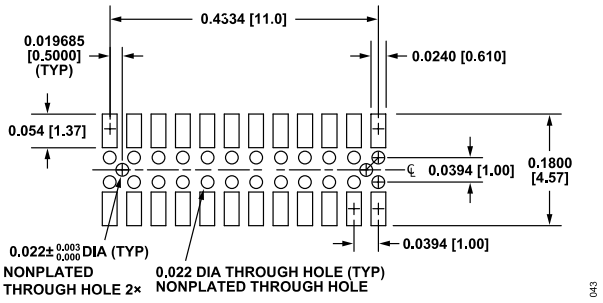

Figure 57. Suggested Layout and Mechanical Design when Using Samtec CLM-112-02-G-D-A for the Mating Connector

PREVENTING MISINSERTION

The ADIS16545/ADIS16547 connector uses the same pattern as the ADIS16485, but with Pin 12 and Pin 15 missing. This pin configuration enables a mating connector to plug these holes which helps prevent misinsertion with the ADIS16545/ADIS16547. Samtec has a custom part that provides this type of mating socket: ASP-193371-04.

The Samtec CLM-112-02 or equivalent is usable, but Pin 12 and Pin 15 are not plugged. Connectors with these pins plugged (such as the ASP-193371-04) offer greater protection against misinsertion and are recommended.

EVALUATION TOOLS

Breakout Board, ADIS16IMU1/PCBZ

The ADIS16IMU1/PCBZ (sold separately) provides a breakout board function for the ADIS16545/ADIS16547, which means that it provides access to the ADIS16545/ADIS16547 through larger connectors that support standard 1 mm ribbon cabling. This board also provides four mounting holes for attachment of the ADIS16545/ADIS16547 to the breakout board.

EVAL-ADIS-FX3 PC-Based Evaluation

In addition to supporting quick prototype connections between the ADIS16545/ADIS16547 and an embedded processing system, J1 on the ADIS16IMU1/PCBZ breakout board also connects directly to P3 on the EVAL-ADIS-FX3 evaluation system.

EVAL-ADIS-FX3 is a completely open source evaluation platform for Windows®-based systems. The FX3 application programming interface (API) manages all the complex USB transactions and implements all the necessary tools to begin capturing high-speed, high-performance data in custom applications. This .NET-compatible API, written in VB.NET and C#, includes data streaming features tailored to reliably capturing inertial sensor data at the maximum data rate. The API is also fully documented, open-source, and is licensed under the MIT license. The API also includes a wrapper library, allowing users to use the same API in any development environment with support for .NET (MATLAB, LabVIEW, Python, and so on).

POWER SUPPLY CONSIDERATIONS

The VDD power supply must charge 24 µF of capacitance (inside of the ADIS16545/ADIS16547, across the VDD and GND pins) during its initial ramp and settling process. When VDD reaches 2.85 V, the ADIS16545/ADIS16547 begin their internal start-up process, which generates additional transient current demand. See Figure 58 for a typical current profile during the start-up process. The first peak in Figure 58 relates to charging the 24 µF capacitor bank, whereas the other transient activity relates to numerous functions turning on during the initialization process of the ADIS16545/ADIS16547.

APPLICATIONS INFORMATION

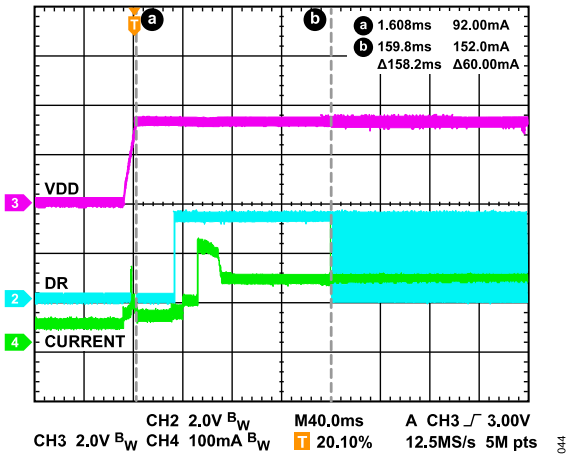

Figure 58. Transient Current Demand, Startup (DR Means Data Ready)

BURST READ CODE EXAMPLE

The following code example illustrates how to implement the ADIS16545/ADIS16547 burst read function.

```
unsigned char test_burst(void)
{
    unsigned short i;
    unsigned short start_index = 1;
    unsigned char burst_id;
    unsigned short buffer[20];
    unsigned long crc, crc_dut;

    /* Burst Read, read 34 bytes */
    /* + 2 bytes for read command */
    /* + 2 bytes for rx response delay */
    /* + 2 bytes for burst_id (0xA5A5) */
    /* burst_id=0xA5A5 for accel/gyro */
    /* burst_id=0xC3C3 for delta ang/vel */
    spi_read(0x7C, 0x00, 40, buffer);
    /* clear burst_id flag */
    burst_id = 0;
    /* loop through each 16-bit word */
    /* and search for last burst_id */
    for(i = 0; i < 20; i++)
    {
    /* detect first burst id then flag it */
        if(buffer[i]==0xA5A5 && burst_id==0)
        {
            burst_id = 1;
        }
        /* detect first data (i.e., detected */
        /* burst id and first data where */
        /* value is not eqaul to A5A5 */
        if(buffer[i]!=0xA5A5 && burst_id==1)
        {
            start_index = i;burst_id = 2;
        }
    }

    /* --- Compute CRC --- */
    /* Initialize CRC */
    crc = 0xFFFFFFFFu;

    /* Compute CRC in the order of */
    /* bytes low-high STATUS - TIME_STAMP */
    crc = crc32_block(crc,
    &buffer[start_index], 15);

    /* Final operation per IEEE-802.3 */
    crc ^= 0xFFFFFFFFu;

    /* get dut CRC */
    crc_dut = (buffer[start_index+16] << 16)
    + buffer[start_index+15];
    return (crc_dut == crc);
}
```

CRC-32 CODE EXAMPLE

The following is the computation example for CRC-32 error checking.

The 32-bit CRC for the primary outputs is provided for burst mode and normal mode. The CRC_LWR and CRC_UPR registers contain the CRC-32 computation for normal (nonburst) transfers.

The CRC is calculated in the order of bytes from low to high as the outputs occur in the burst read list. Note that the BURST_ID (0xA5A5 or 0xC3C3) is not included in the sequence for the CRC. When computing the CRC one must start with the low byte of the data following the BURST_ID.

The 32-bit CRC is first initialized with 0xFFFFFFFF and then each word passes through the CRC computation. Finally, the CRC is xor'ed with 0xFFFFFFFF.

```
/* Initialize CRC */
crc = 0xFFFFFFFFU;
/* Compute CRC in the order of bytes */
/* low-high starting at 0-14, BurstID, */
/* STATUS, TIME_STAMP */
crc = crc32_block(crc, DATA, 15);
/* Final operation per IEEE-802.3 */
crc ^= 0xFFFFFFFFU;
```

The crc32_block function takes a 16-bit array and computes the CRC byte by byte from the low byte to the high byte:

```
unsigned long crc32_block(unsigned long crc,
 const unsigned short data[], in )
{
    unsigned long long_c;
```

APPLICATIONS INFORMATION

```
    int i;
    /* cycle through memory */
    for ( i=0; i<n; i++ )
    {
        /* Get lower byte */
        long_c = 0x000000ff &
        (unsigned long)data[i];
        /* Process with CRC */
        crc = ((crc>>8) & 0x00ffffff) ^
        crc_tab32[(crc^long_c)&0xff];
        /* Get upper byte */
        long_c = (0x000000ff &
        ((unsigned long)data[i]>>8);
        /* Process with CRC */
        crc = ((crc>>8) & 0x00ffffff) ^
        crc_tab32[(crc^long_c)&0xff];
    }
    return crc;
}
```

The CRC table (crc_tab32) is computed with the following function:

```
void init_crc32_table(void)
{
    unsigned long P_32;
    int i, j;
    unsigned long crc;
    /* IEEE-802.3 CRC32 polynomial */
    P_32 = 0xEDB88320
    /* 8bit require 256 entries in Table */
    for (i=0; i<256; i++)
    {
        /* start with table entry number */
        crc = (unsigned long) i;

        /* process all bits in entry number */
        for (j=0; j<8; j++)
        {
            /* LSBit set? */
            if ((crc&(unsigned long)
            0x00000001)!=(unsigned long)0)
            {
            /* process for bit set */
            crc = (crc>>1) ^ P_32;
            }
            else
            {
                /* process for bit clear */
                crc = (crc>>1);
            }
        }
    /* Store calculated value into table */
    crc_tab32[i] = crc;
    }
}
```

See the Cyclical Redundancy Check (CRC-32) section for an example of a CRC-32 calculation on a data sample.

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
ML-24-9	MODULE	24-Lead Module with Connector Interface

For the latest package outline information and land patterns (footprints), go to Package Index.

Updated: January 11, 2024

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16545-1BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-9
ADIS16545-2BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-9
ADIS16545-3BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-9
ADIS16547-1BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-9
ADIS16547-2BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-9
ADIS16547-3BMLZ	−40°C to +105°C	24-Lead Module with Connector Interface	ML-24-9

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADIS16IMU1/PCBZ	Evaluation Board
EVAL-ADIS-FX3Z	Evaluation Board

[1] Z = RoHS Compliant Part.