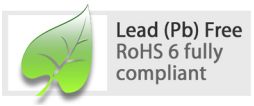
ADJD-J823

Color Management Controller with Integrated RGB Photosensor

AVAGO TECHNOLOGIES

Data Sheet



Description

The ADJD-J823 is a CMOS mixed-signal IC with integrated RGB photosensors designed to be the optical feedback device of an RGB LED-based backlighting system. A typical system consists of an array of red, green and blue (RGB) LEDs, LED drivers and the ADJD-J823. The device samples the light output from the RGB LED array, processes the color information and adjusts the light output from the RGB LEDs until the target color is achieved. To achieve this, the device integrates an RGB photosensor array, an analog-to-digital converter front-end, a color data processing logic core and a high-resolution 12-bit PWM output generator.

By employing a feedback system and the ADJD-J823, the light output produced by the LED array maintains its color over time and temperature. In addition, using a serial interface, specifying the color of the LED array's light output is as simple as picking the target color co-ordinates from the CIE color space and writing several bytes of data to the device.

The sensitivity of the device to light can be adjusted through an automated process. The PWM output signals control the on-time duration of the red, green and blue LEDs. That duration is continually adjusted in real-time to match the light output from the RGB LED array to the target color.

Features

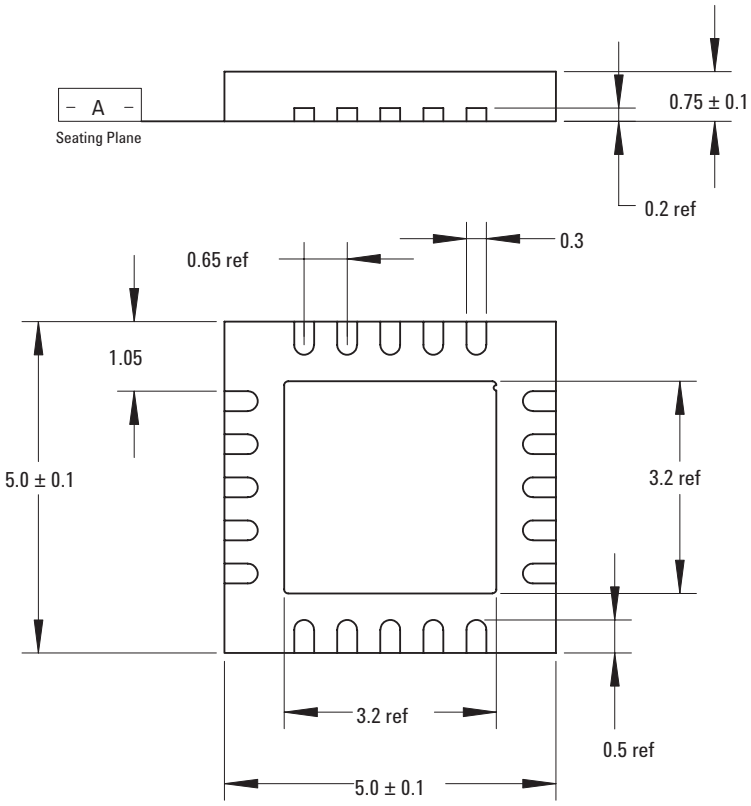
- Integrated RGB photosensor
- Integrated color management feedback controller
- Serial Interface
- Direct interface to standard I2C EEPROM
- 3-channel 12-bit PWM output – Red, Green and Blue LED channels
- Built-in oscillator

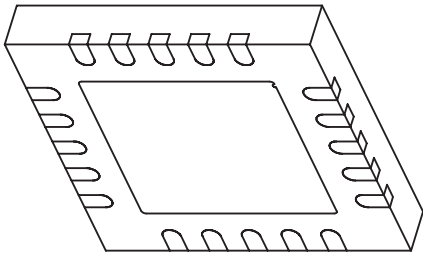
Applications

- LCD Backlighting

ESD WARNING: *Standard CMOS handling precautions should be observed to avoid static discharge.*

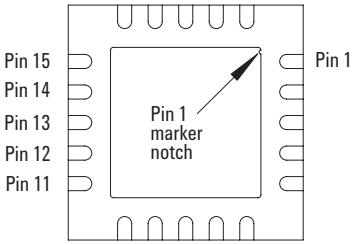
Package Dimensions





Note: Dimensions are in millimeter (mm)

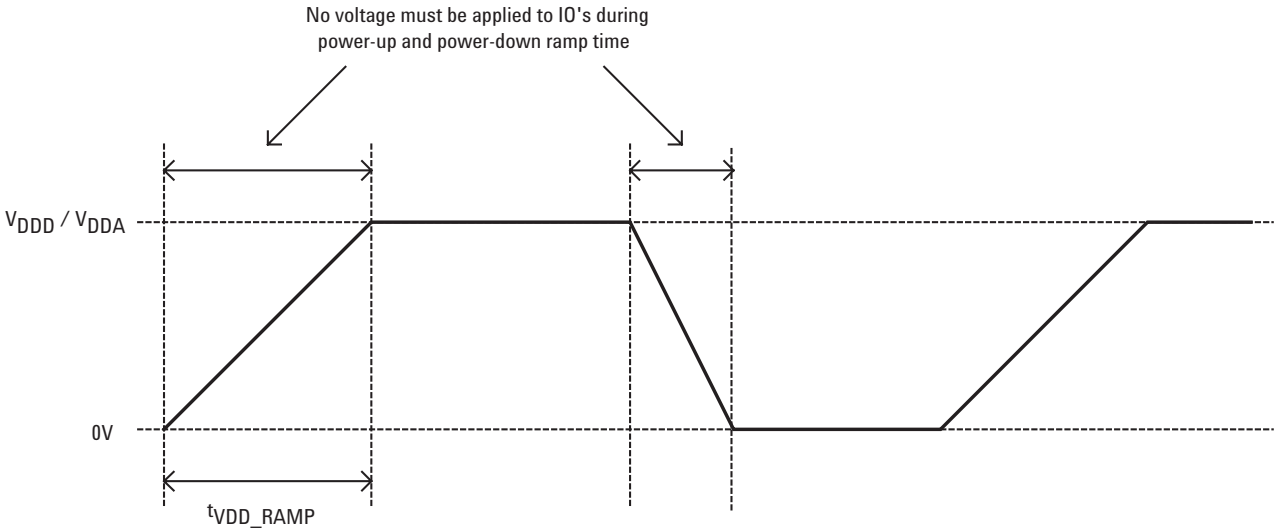
Bottom View



Pin Information

PIN	NAME	TYPE	DESCRIPTION
1	NC	No connect	No connect. Leave floating.
2	PWMB	Output	PWMB is the active-high blue pulse width modulation output pin. Tie it to the blue LED driver channel.
3	PWMG	Output	PWMG is the active-high green pulse width modulation output pin. Tie it to the green LED driver channel.
4	PWMR	Output	PWMR is the active-high red pulse width modulation output pin. Tie it to the red LED driver channel.
5	DGND	Ground	Tie to digital ground.
6	DGND	Ground	Tie to digital ground.
7	DVDD	Power	Digital power pin.
8	AGND	Ground	Tie to analog ground.
9	CLKIO	Output	CLKIO outputs a reference internal clock signal.
10	XRST	Input	Global, asynchronous, active low system reset. When asserted low, XRST resets all registers. Minimum reset pulse low is 10us and must be provided by external circuitry.
11	SCLSLV	Input	SDASLV and SCLSLV are the serial interface communications pins. SDASLV is the bidirectional data pin and SCLSLV is the interface clock. A pull-up resistor should be tied to SDASLV because it goes tri-state to output logic 1.
12	SDASLV	Input/Output (tri-state high)	
13	SCLPROM	Output	An external serial I2C EEPROM can be connected to the device to store calibration and configuration data. SDAPROM and SCLPROM should be tied to the I2C data (SDA) and clock (SCL) pins of the EEPROM. A pull-up resistor should be tied to SDAPROM because it goes tri-state to output logic 1.
14	SDAPROM	Input/Output (tri-state high)	
15	SLEEP	Input	When SLEEP=1, the device goes into sleep mode. In sleep mode, all analog circuits are powered down and the clock signal is gated away from the core logic resulting in very low current consumption.
16	AGND	Ground	Tie to analog ground.
17	AGND	Ground	Tie to analog ground.
18	AGND	Ground	Tie to analog ground.
19	AVDD	Power	Analog power pin.
20	NC	No connect	No connect. Leave floating.

Powering the Device



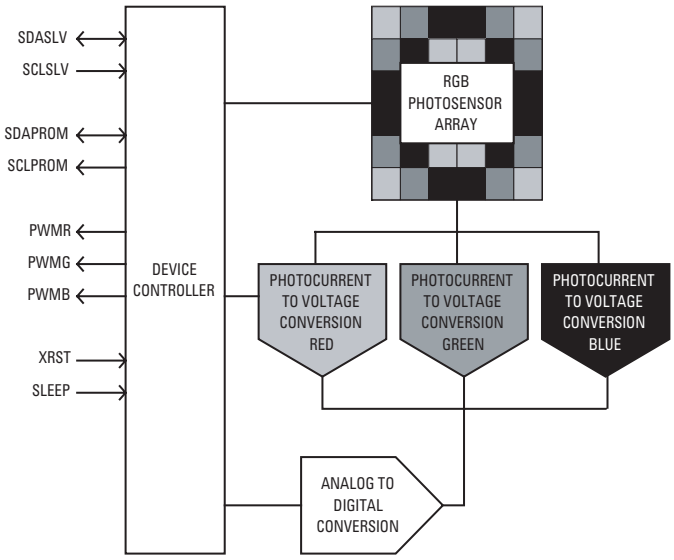
ESD Protection Diode Turn-On During Power-Up and Power-Down

A particular power-up and power-down sequence must be used to prevent any ESD diode from turning on inadvertently. The figure above describes the sequence. In general, AVDD and DVDD should power-up and power-down together to prevent ESD diodes from turning on inadvertently. During this period, no voltage should be applied to the IO's for the same reason.

Ground Connection

AGND and DGND must both be set to 0V and preferably star-connected to a central power source as shown in the application diagram. A potential difference between AGND and DGND may cause the ESD diodes to turn on inadvertently.

Block Diagram



General Specifications

Feature	Value
Interface	100kHz serial interface
Input color format	CIE Yxy
Output PWM frequency	6.35kHz (nominal)
Output PWM resolution	12 bits
Supply	2.6V digital (nominal), 2.6V analog (nominal)

High Level Description

A hardware reset (by asserting XRST) should be performed before starting any operation. It is assumed that factory calibration was performed prior deployment of ADJD-J823. Calibration is discussed at the end of this section.

The user controls and configures the device by programming a set of internal registers through a serial interface. At the start of application, the following register data must be written to it:

- Frequency registers
- Setup data
- Calibration data
- Bright and color input registers.

The register data is usually gathered during a calibration process which is performed once in manufacturing. Factory calibration is needed at a system level to map the integrated tri-color sensor's reading (device dependent) with a standard device independent color space.

Once the register data is entered, the feedback operation begins; the device starts to sample the RGB sensor using the internal ADC. That data is compared to a user-controlled color point target. The PWM duty factor for each channel is adjusted in response to any error signal generated by that comparison operation.

Thus, the actual color produced by the LEDs is maintained close to the target.

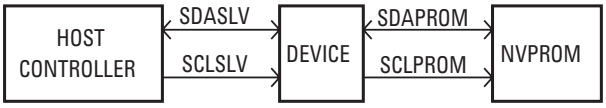
There are three methods to operate the device. They are differentiated by the technique in which the register data is stored and used. The three figures below describe the methods. NVPROM stands for Non-Volatile Programmable Read-Only Memory such as an EEPROM.

Independent NVPROM

The NVPROM is independent from the device. During factory calibration, the host must read the register data from the device and write it to the NVPROM. At the start of application, the host must read the register data from the NVPROM and write it back to the device, after which the device will wait for further instructions in normal mode.

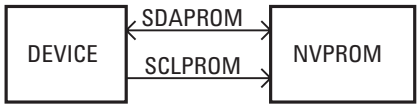
Dedicated NVPROM in Interactive Mode

A dedicated NVPROM is connected to the device. During factory calibration, the host can instruct the device to upload the register data to the NVPROM. At the start of application, the host can instruct the device to download the register data from the NVPROM, after which the device will wait for further instructions in normal mode. The serial interface protocol between device and NVPROM is hard coded. A standard NVPROM such as a serial I2C EEPROM with address 0x50 (7-bit) must be used.



Dedicated NVPROM in Standalone Mode

A dedicated NVPROM is connected to the device. During factory calibration, the host can instruct the device to upload the register data to the NVPROM. The difference versus Interactive Mode is that, in application, the device itself will download the register data and immediately after, enter normal mode. Then, it will start driving the PWM channels to achieve a default target color point. The default color point is programmed after factory calibration. A host controller is not necessary during application. The serial interface protocol between device and NVPROM is hard coded. So, a standard NVPROM such as a serial I2C EEPROM with address 0x50 (7-bit) must be used.



Factory Calibration

Factory calibration is needed at a system level to create a 'snapshot' of the initial conditions of the system. The color management algorithm references the snapshot data. In effect, the calibration data trims out variation in the entire signal chain from LEDs to sensor to ADC. The figure below shows the calibration procedure in brief.

First, the device is put into "open loop" mode in which the color management algorithm is turned off.

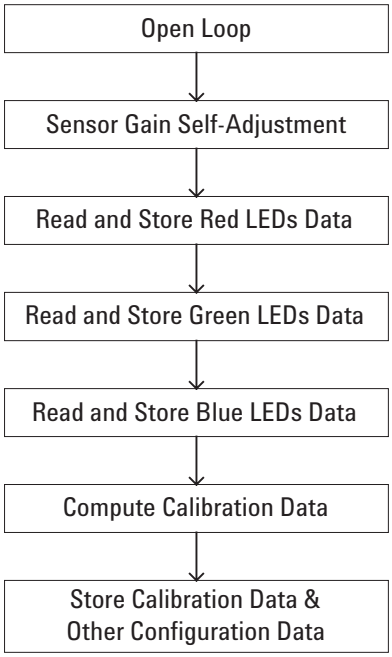
Second, the host controller needs to determine the optimum sensor sensitivity for the given brightness detection level. The sensitivity is a combination of several internal settings. Searching for the optimum settings can be performed manually or through an automatic search routine which is built into the device. The host can start the routine by issuing a command to the device. The device will then turn the LEDs (usually at maximum duty factor) and start the search routine.

Next, the host needs to turn only the Red LEDs on. An external camera must be set up to capture the CIE coordinates of the RED LEDs. The scaled XYZ readings are then written to the device. At the same time, the host needs to instruct the device to sample the RGB sensor and store the results.

This is repeated for the Green and Blue LEDs.

Lastly, the host needs to instruct the device to start a calibration calculator. The calculator uses the camera and sensor readings for each color to develop a mapping matrix that maps the RGB sensor to the standard CIE color space.

The mapping matrix and other configuration data is the device setup data referred to in the previous section.



Factory Calibration Flow Chart

For details, refer to application note 5241 ADJD-J823 programming manual

Electrical Specifications

Absolute Maximum Ratings (Notes 1 & 2)

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage temperature	T_{STG_ABS}	-40	85	°C	
Digital supply voltage, DVDD to DVSS	V_{DDD_ABS}	-0.5	3.7	V	
Analog supply voltage, AVDD to AVSS	V_{DDA_ABS}	-0.5	3.7	V	
Input voltage	V_{IN_ABS}	-0.5	V_{DDD}+0.5	V	All I/O pins
Solder Reflow Peak temperature	T_{L_ABS}		235	°C	
Human Body Model ESD rating	ESD_{HBM_ABS}		2	kV	All pins, human body model per JESD22-A114-B

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units
Free air operating temperature	T_A	0	25	70	°C
Digital supply voltage, DVDD to DVSS	V_{DDD}	2.5	2.6	3.6	V
Analog supply voltage, AVDD to AVSS	V_{DDA}	2.5	2.6	3.6	V
Output current load high	I_{OH}			3	mA
Output current load low	I_{OL}			3	mA
Input voltage high level (Note 4)	V_{IH}	$0.7V_{DDD}$		V_{DDD}	V
Input voltage low level (Note 4)	V_{IL}	0		$0.3V_{DDD}$	V
Power supply ramp period	t_{VDD_RAMP}			100	ms

DC Electrical Specifications Over Recommended Operating Conditions (unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Output voltage high level (Note 5)	V_{OH}	I_{OH} = 3mA	V_{DDD}-0.8	V_{DDD}-0.4		V
Output voltage low level (Note 6)	V_{OL}	I_{OL} = 3mA		0.2	0.4	V
Dynamic supply current (Note 7,8)	I_{DD_DYN}	(Note 9)		9.4	14	mA
Static supply current (Note 8)	I_{DD_STATIC}	(Note 9)		2.7	6	mA
Sleep-mode supply current (Note 8)	I_{DD_SLP}	(Note 9)		0.2	15	uA
Input leakage current	I_{LEAK}		-10		10	uA

AC Electrical Specifications Over Recommended Operating Conditions (unless otherwise specified)

Parameter	Symbol	Conditions	Minimum	Typical (Note 3)	Maximum	Units
Internal clock frequency	f_{CLK}		16	26	38	MHz

Optical Specifications

Parameter	Symbol	Conditions	Minimum	Maximum	Units
Sensor operating detection range	E_V	(Note 3 &10)	800	10000	Lux

Serial Interface Timing Information

Parameter	Symbol	Minimum	Maximum	Units
SCL clock frequency	f_{scl}	0	100	kHz
(Repeated) START condition hold time	$t_{HD:STA}$	4	-	µs
Data hold time	$t_{HD:DAT}$	0 (Note 11)	3.45	µs
SCL clock low period	t_{LOW}	4.7	-	µs
SCL clock high period	t_{HIGH}	4.0	-	µs
Repeated START condition setup time	$t_{SU:STA}$	4.7	-	µs
Data setup time	$t_{SU:DAT}$	250	-	ns
STOP condition setup time	$t_{SU:STO}$	4.0	-	µs
Bus free time between START and STOP conditions	t_{BUF}	4.7	-	µs

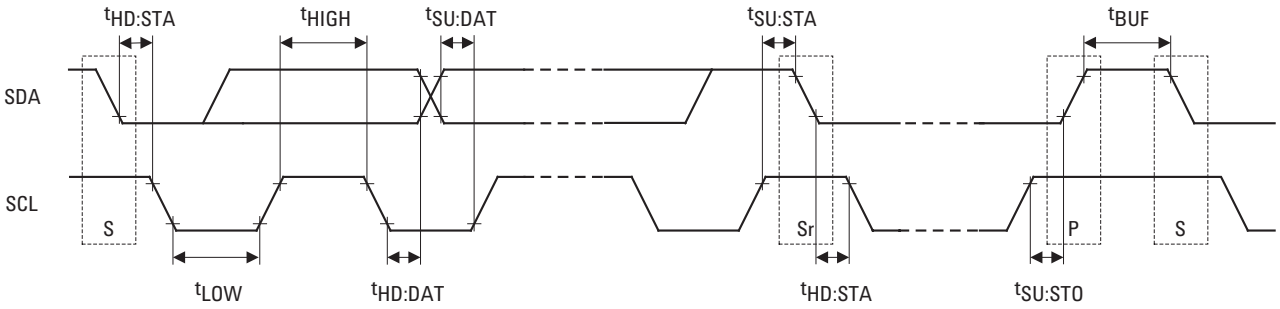


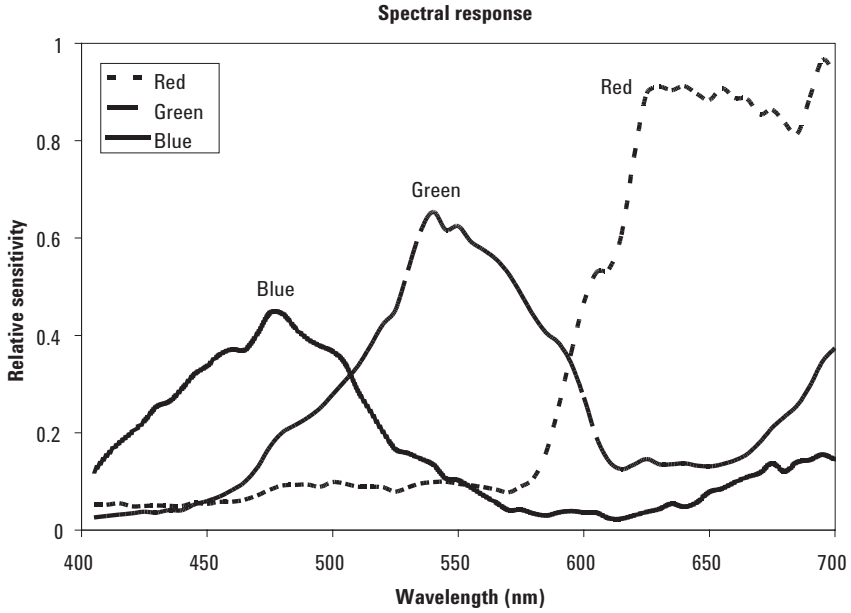
Figure 1. Serial Interface Bus Timing Waveforms

Notes:

1. The "Absolute Maximum Ratings" are those values beyond which damage to the device may occur. The device should not be operated at these limits. The parametric values defined in the "Electrical Specifications" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.
2. Unless otherwise specified, all voltages are referenced to ground.
3. Specified at room temperature (25°C) and VDDD = VDDA = 2.6V.
4. Applies to all digital input pins.
5. Applies to all digital output pins and CLKIO pin. SDASLV and SDAPROM pins go tri-state when output logic high. Minimum V_{OH} depends on the pull-up resistor value.
6. Applies to all digital output and digital input-output pins.
7. Dynamic testing is performed with the IC operating in a mode representative of typical operation.
8. Refers to total device current consumption.
9. Output and bidirectional pins are not loaded.
10. Using R:G:B LED light source brightness ratio of 7:13:1 to achieve white D90 color point
    Red LED (x,y) = (0.700, 0.300)
    Green LED (x,y) = (0.171, 0.715)
    Blue LED (x,y) = (0.158, 0.019)
11. A hold time of at least 300ns must be provided internally by a device for the SDA signal (with reference to the minimum VIH of SCL) to bridge the undefined region of the falling edge of SCL.

Sensor Optical Performance

The integrated sensor spectral respond graph from 400 to 700nm. The color indicates the color channel of the color sensor.

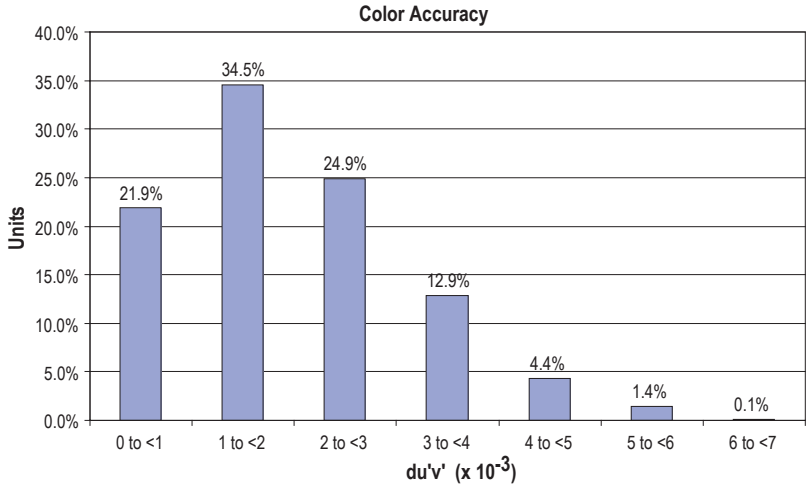


System Performance

Color Accuracy chart.

Data obtain from 1078 units at 25ºC and V_{DDD} & V_{DDA} at 2.6V. Color set point at CIE x=0.287, y=0.296 (9000K)

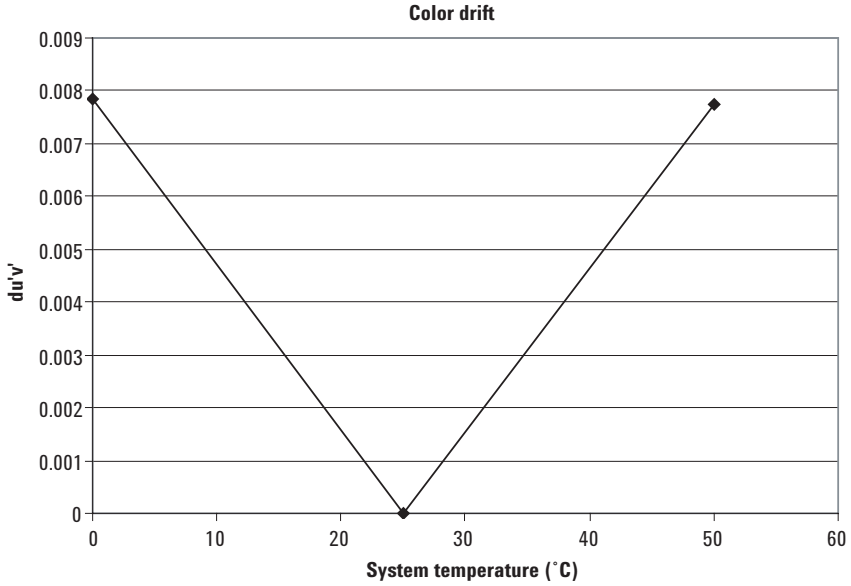
The average du'v' is 0.002 with standard deviation 0.0012 and a maximum value of 0.0062.



Color drift over temperature

Data obtain from 5 units. Color set point is at 9000K and V_{DDD} & V_{DDA} at 2.6V.

System consists of ADJD-J823 and RGB LEDs with color coordinates, Red (x,y) = (0.691, 0.309), Green (x,y) = (0.161, 0.704), Blue (x,y) = (0.131, 0.073). The R:G:B luminance ratio is 2.6 : 3.9 : 1.0



Note: The starting point is at 25ºC and is zero color drift as all measurements are made relative to the starting point at 25ºC.

Calculating Sampling Frequency and PWM Output Frequency

The sampling frequency, f_{SAMP}, which is the frequency at which ADJD-J823 samples the tricolor photosensor, is related to the system clock frequency, f_{CLK}. The output PWM frequency, f_{PWM}, is also related to f_{CLK}.

Calculation example:

f_{CLK} = 26 MHz (nominal)

$$f_{SAMP} = \frac{f_{CLK}}{SAMPFREQ \times 8} = 108Hz(nominal)$$

$$f_{PWM} = \frac{f_{CLK}}{(PWMFREQ + 1) \times 4096} = 6.35kHz(nominal)$$

SAMPFREQ = Sampling frequency register setting = concatenation of registers [0x06][0x07]

PWMFREQ = PWM frequency register setting = register [0x05]

The internal oscillator frequency varies from part-to-part but it will not vary as significantly during operation.

Serial Interface Reference

Description

The programming interface to the ADJD-J823 is a 2-wire serial bus. The bus consists of a serial clock (SCL) and a serial data (SDA) line. The SDA line is bi-directional on ADJD-J823 and must be connected through a pull-up resistor to the positive power supply. When the bus is free, both lines are HIGH.

The 2-wire serial bus on ADJD-J823 requires one device to act as a master while all other devices must be slaves. A master is a device that initiates a data transfer on the bus, generates the clock signal and terminates the data transfer while a device addressed by the master is called a slave. Slaves are identified by unique device addresses.

Both master and slave can act as a transmitter or a receiver but the master controls the direction for data transfer. A transmitter is a device that sends data to the bus and a receiver is a device that receives data from the bus.

The ADJD-J823 serial bus interface always operates as a slave transceiver with a data transfer rate of up to 100kbit/s.

START/STOP Condition

The master initiates and terminates all serial data transfers. To begin a serial data transfer, the master must send a unique signal to the bus called a START condition. This is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH.

The master terminates the serial data transfer by sending another unique signal to the bus called a STOP condition. This is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

The bus is considered to be busy after a START (S) condition. It will be considered free a certain time after the STOP (P) condition. The bus stays busy if a repeated START (Sr) is sent instead of a STOP condition.

The START and repeated START conditions are functionally identical.

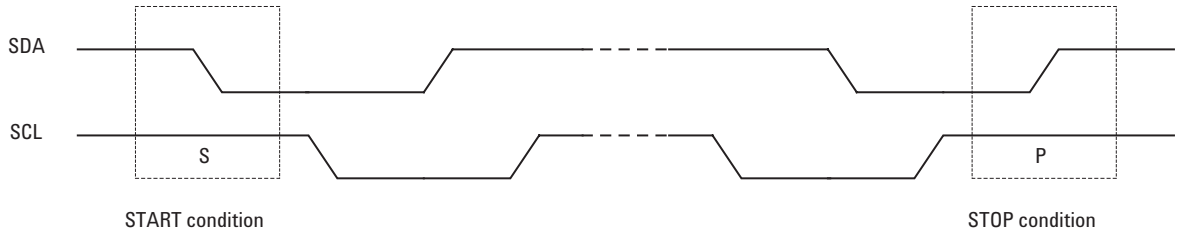


Figure 2. START/STOP Condition

Data Transfer

The master initiates data transfer after a START condition. Data is transferred in bits with the master generating one clock pulse for each bit sent. For a data bit to be valid, the SDA data line must be stable during the HIGH period of the SCL clock line. Only during the LOW period of the SCL clock line can the SDA data line change state to either HIGH or LOW.

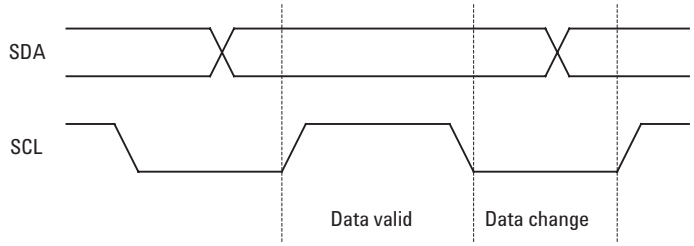


Figure 3. Data Bit Transfer

The SCL clock line synchronizes the serial data transmission on the SDA data line. It is always generated by the master. The frequency of the SCL clock line may vary throughout the transmission as long as it still meets the minimum timing requirements.

The master by default drives the SDA data line. The slave drives the SDA data line only when sending an acknowledge bit after the master writes data to the slave or when the master requests the slave to send data.

The SDA data line driven by the master may be implemented on the negative edge of the SCL clock line. The master may sample data driven by the slave on the positive edge of the SCL clock line. Figure 4 shows an example of a master implementation and how the SCL clock line and SDA data line can be synchronized.

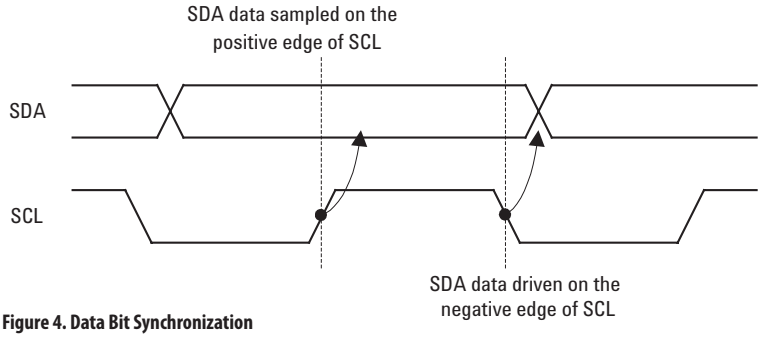


Figure 4. Data Bit Synchronization

A complete data transfer is 8-bits long or 1-byte. Each byte is sent the most significant bit (MSB) first followed by an acknowledge or not acknowledge bit. Each data transfer can send an unlimited number of bytes (depending on the data format).

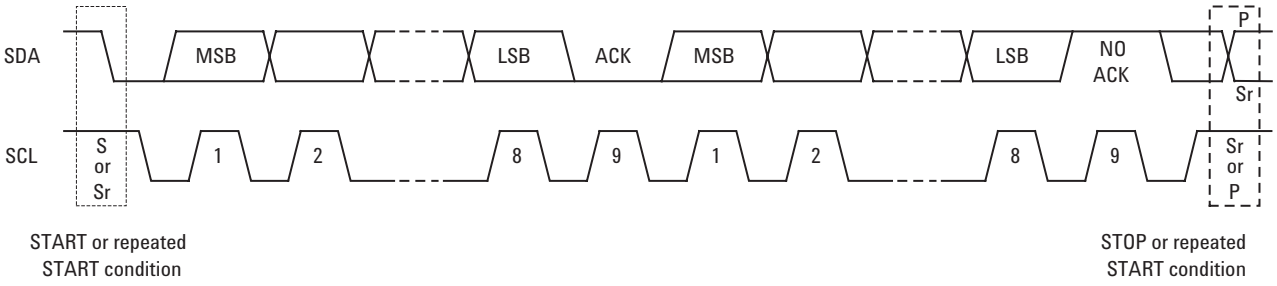


Figure 5. Data Byte Transfer

Acknowledge/Not acknowledge

The receiver must always acknowledge each byte sent in a data transfer. In the case of the slave-receiver and master-transmitter, if the slave-receiver does not send an acknowledge bit, the master-transmitter can either STOP the transfer or generate a repeated START to start a new transfer.

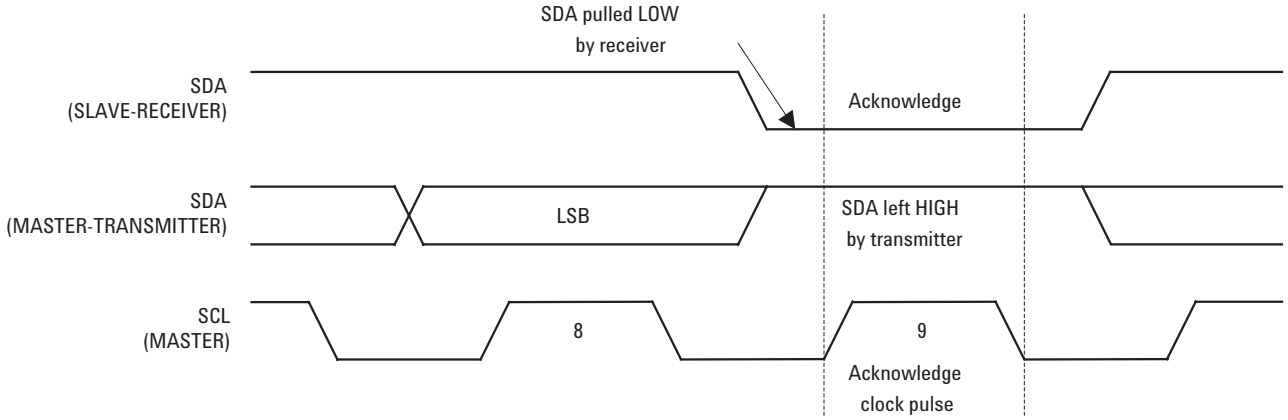


Figure 6. Slave-Receiver Acknowledge

In the case of the master-receiver and slave-transmitter, the master generates a not acknowledge to signal the end of the data transfer to the slave-transmitter. The master can then send a STOP or repeated START condition to begin a new data transfer.

In all cases, the master generates the acknowledge or not acknowledge SCL clock pulse.

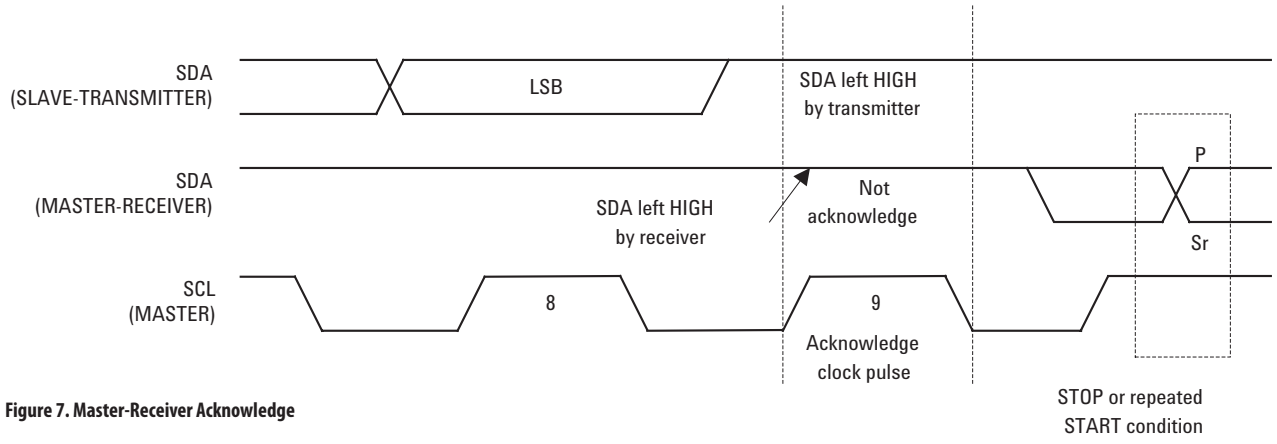


Figure 7. Master-Receiver Acknowledge

Addressing

Each slave device on the serial bus needs to have a unique address. This is the first byte that is sent by the master-transmitter after the START condition. The address is defined as the first seven bits of the first byte.

The eighth bit or least significant bit (LSB) determines the direction of data transfer. A 'one' in the LSB of the first byte indicates that the master will read data from the addressed slave (master-receiver and slave-transmitter). A 'zero' in this position indicates that the master will write data to the addressed slave (master-transmitter and slave-receiver).

A device whose address matches the address sent by the master will respond with an acknowledge for the first byte and set itself up as a slave-transmitter or slave-receiver depending on the LSB of the first byte.

The slave address on ADJD-J823 is 0x58 (7-bits).

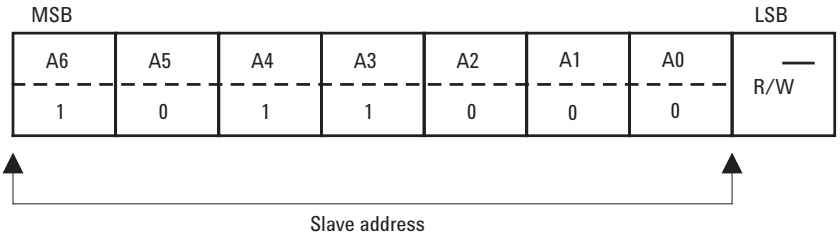


Figure 8. Slave Addressing

Data format

ADJD-J823 uses a register-based programming architecture. Each register has a unique address and controls a specific function inside the chip.

To write to a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then writes the new register data. Once the slave acknowledges, the master generates a STOP condition to end the data transfer.

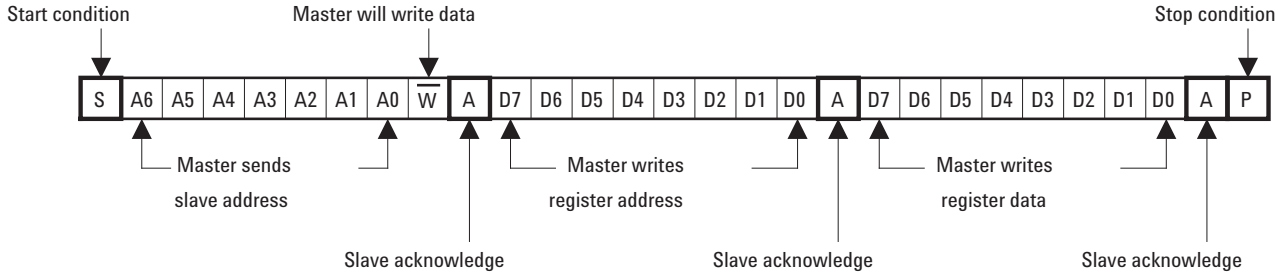


Figure 9. Register Byte Write Protocol

To read from a register, the master first generates a START condition. Then it sends the slave address for the device it wants to communicate with. The least significant bit (LSB) of the slave address must indicate that the master wants to write to the slave. The addressed device will then acknowledge the master.

The master writes the register address it wants to access and waits for the slave to acknowledge. The master then generates a repeated START condition and resends the slave address sent previously. The least significant bit (LSB) of the slave address must indicate that the master wants to read from the slave. The addressed device will then acknowledge the master.

The master reads the register data sent by the slave and sends a no acknowledge signal to stop reading. The master then generates a STOP condition to end the data transfer.

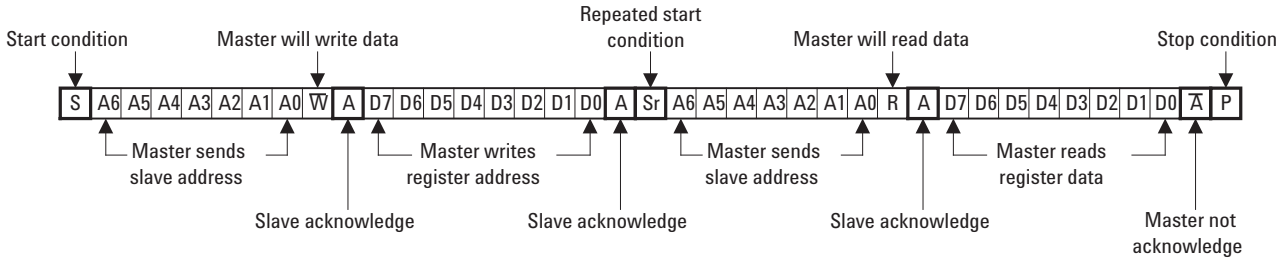
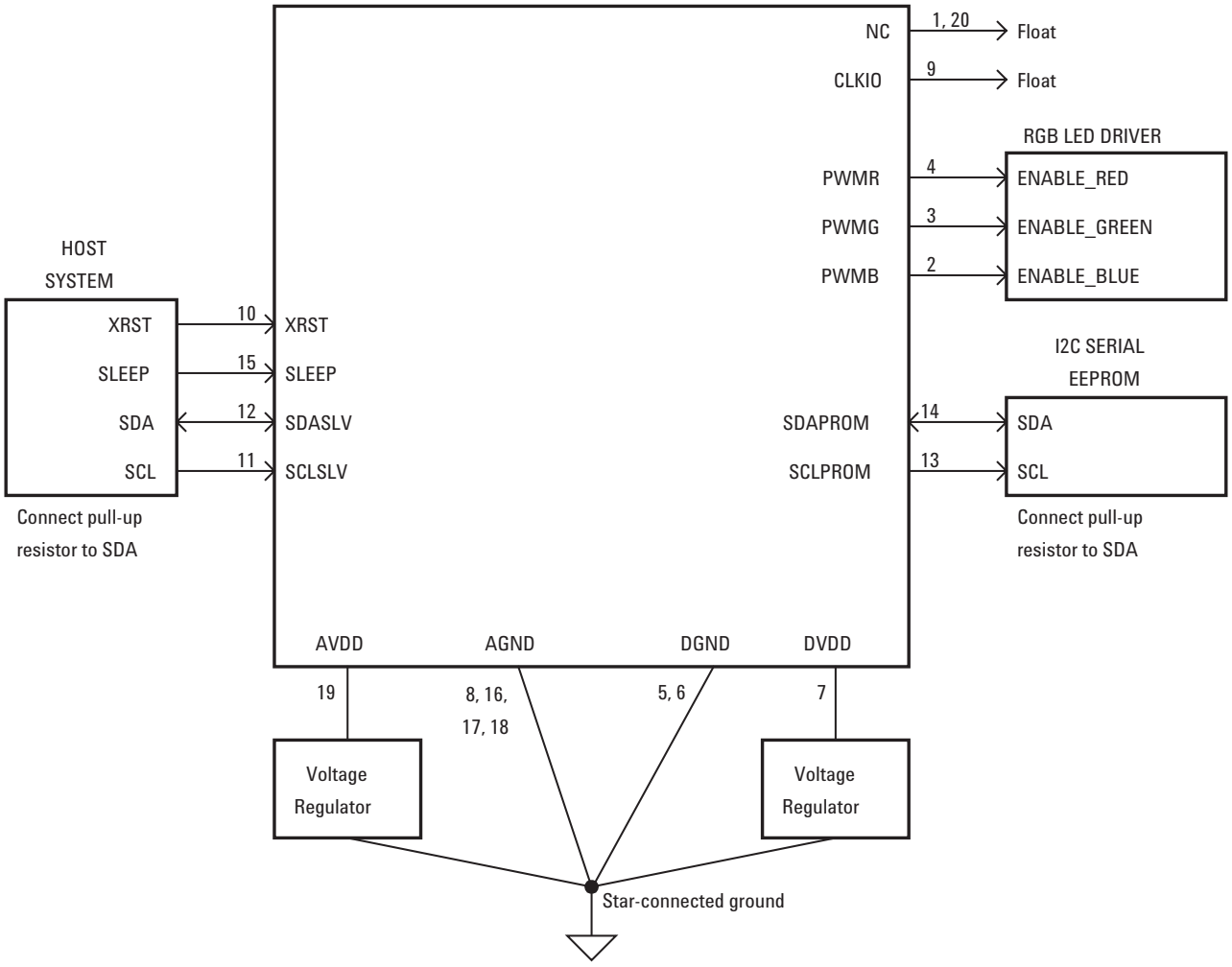


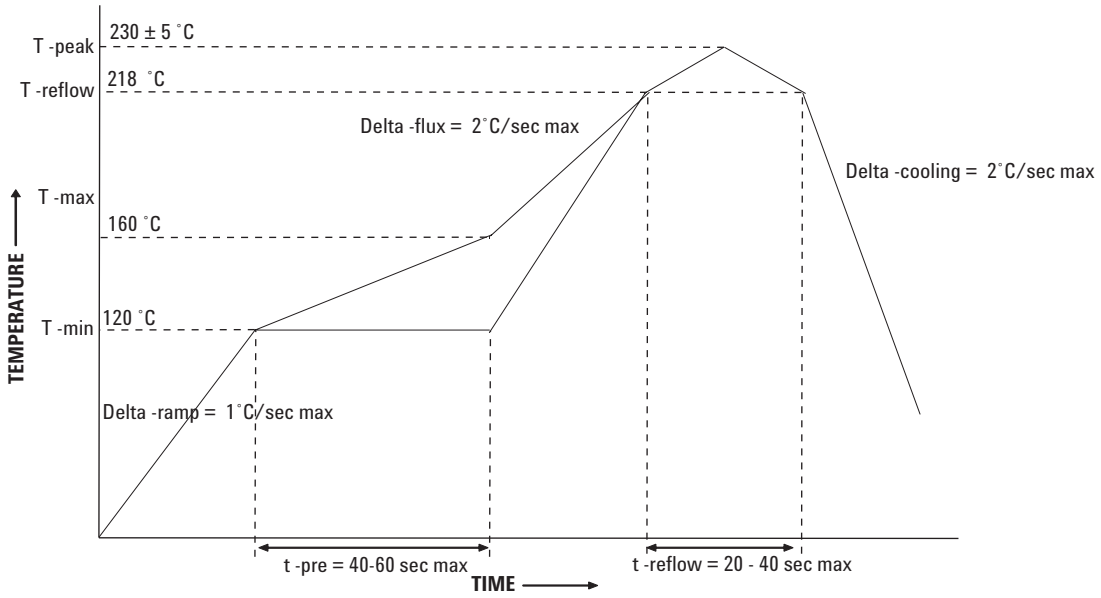
Figure 10. Register Byte Read Protocol

Application Diagrams



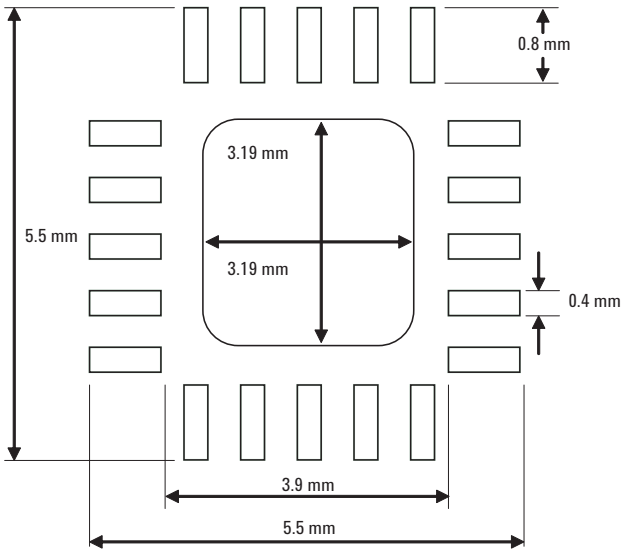
Recommended Reflow Profile

It is recommended that Henkel Pb-free solder paste LF310 be used for soldering ADJD-J823. Below is the recommended soldering profile.



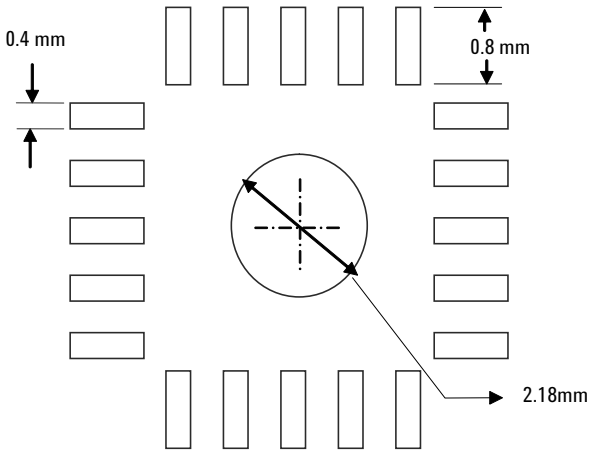
20 Lead QFN Recommended PCB Land Pad Design

IPC-SM-782 is used as the standard for the PCB land pad design. Recommended PCB finishing is gold plated.



20 Lead QFN Recommended Stencil Design

A stencil thickness of 2.18mm (6 mils) for this QFN package is recommended

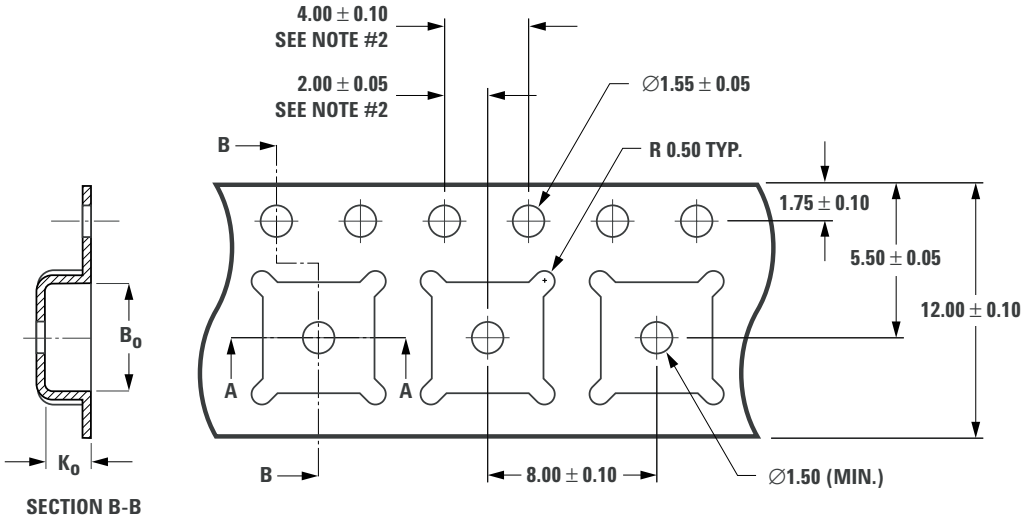


Recommendations for Handling and Storage of ADJD-J823

- Before Opening the MBB (Moisture Barrier Bag)
  - The sensor component must be kept sealed in a MBB (Moisture Barrier Bag) stored at 30°C and 70%RH or less at all times.
  - It should also be seal with a moisture absorbent material (Silica Gel) and an indicator card (Cobalt Chloride) to indicate the moisture within the bag.
- After Opening the MBB (Moisture Barrier Bag)
  - The sensor component must be kept at 30°C and 60%RH or less
  - The sensor component should have a MET (Manufacturing Exposure Time) of 24 hours starting from the time of removal from the MBB to the soldering oven.
  - If unused sensor component remain, it is recommended to store them back to the MBB.
  - If the indicator card has turned from blue to pink or it has exceeded the recommended MET (Manufacturing Exposure Time) of 24hrs, baking treatment should be performed using the following conditions before continue to IR reflow soldering.
  - Baking treatment: 24 hours at 125°C.

Package Tape and Reel Dimensions

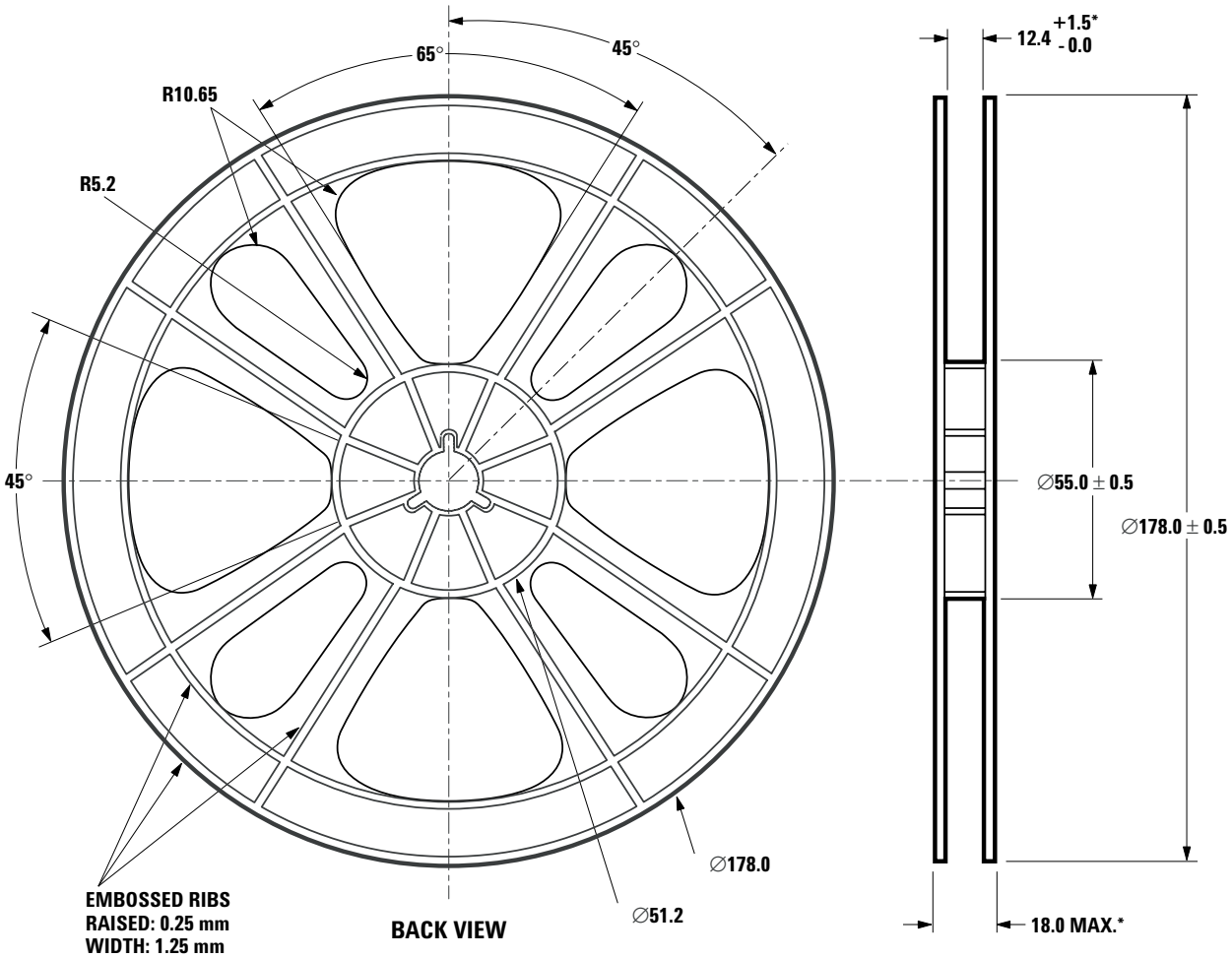
Carrier Tape Dimensions



A_0:	5.30
B_0:	5.30
K_0:	2.20
PITCH:	8.00
WIDTH:	12.00

NOTES:
1. A_0 AND B_0 MEASURED AT 0.3 mm ABOVE BASE OF POCKET.
2. 10 PITCHES CUMULATIVE TOLERANCE IS ± 0.2 mm.
3. DIMENSIONS ARE IN MILLIMETERS (mm).

Reel Dimensions



NOTES:
1. *MEASURED AT HUB AREA.
2. ALL FLANGE EDGES TO BE ROUNDED.

ESD WARNING: *Standard CMOS handling precautions should be observed to avoid static discharge.*

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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