400 MHz to 2700 MHz RF Driver Amplifier

ADL5320

FEATURES

Operation: 400 MHz to 2700 MHz
Gain of 17 dB at 880 MHz
OIP3 of 45 dBm at 880 MHz
P1dB of 25.4 dBm at 880 MHz
Noise figure: 4 dB at 880 MHz
Power supply: 5 V
Power supply current: 104 mA typical
Internal active biasing
Thermally efficient SOT-89 package
ESD rating of ±4 kV (Class 3A)

FUNCTIONAL BLOCK DIAGRAM

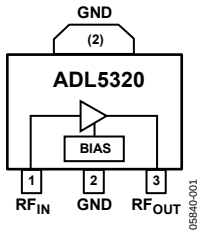


Figure 1.

GENERAL DESCRIPTION

The ADL5320 is a broadband, linear driver RF amplifier that operates at frequencies from 400 MHz to 2700 MHz. The device can be used in a wide variety of wired and wireless applications, including ISM, WLL, PCS, GSM, CDMA, and W-CDMA.

The ADL5320 operates with a 5 V supply voltage and a supply current of 104 mA.

The ADL5320 is fabricated on a GaAs HBT process. The device is packaged in a low cost SOT-89 that uses an exposed paddle for excellent thermal impedance. It operates from −40°C to +85°C, and a fully populated evaluation board is available.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062–9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

2/08—Revision 0: Initial Version

SPECIFICATIONS

VSUP = 5 V and T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
OVERALL FUNCTION					
Frequency Range		400		2700	MHz
FREQUENCY = 880 MHz					
Gain[1]		16.3	16.9	17.5	dB
vs. Frequency	±50 MHz		±0.3		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.6		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			25.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 10 dBm per tone		45		dBm
Noise Figure			4.1		dB
FREQUENCY = 2140 MHz					
Gain[1]		12.4	13.2	14.0	dB
vs. Frequency	±50 MHz		±0.33		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±0.8		dB
vs. Supply	4.75 V to 5.25 V		±0.06		dB
Output 1 dB Compression Point			25.7		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 10 dBm per tone		42		dBm
Noise Figure			4.4		dB
FREQUENCY = 2600 MHz					
Gain[1]		11.5	12.5	13.4	dB
vs. Frequency	±100 MHz		±0.6		dB
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±1.1		dB
vs. Supply	4.75 V to 5.25 V		±0.1		dB
Output 1 dB Compression Point			27.4		dBm
Output Third-Order Intercept	Δf = 1 MHz, P_{OUT} = 10 dBm per tone		37		dBm
Noise Figure			5.1		dB
POWER INTERFACE	Pin RF_{OUT}				
Supply Voltage		4.5	5	5.5	V
Supply Current			104	124	mA
vs. Temperature	−40°C ≤ T_A ≤ +85°C		±6.0		mA
Power Dissipation	VSUP = 5 V		520		mW

[1] Guaranteed maximum and minimum specified limits on this parameter are based on 6 sigma calculations.

TYPICAL SCATTERING PARAMETERS

VSUP = 5 V and T_A = 25°C; the effects of the test fixture have been de-embedded up to the pins of the device.

Table 2.

	S11		S21		S12		S22	
Freq (MHz)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)	Magnitude (dB)	Angle (°)
400	−1.51	164.18	14.18	+128.37	−32.37	+6.77	−3.44	160.94
500	−1.38	155.33	14.03	+118.16	−31.75	+1.48	−3.70	156.73
550	−1.42	151.34	13.79	+112.76	−31.68	−3.93	−3.79	154.66
600	−1.46	147.66	13.72	+108.71	−31.46	−4.60	−3.83	152.89
650	−1.46	144.12	13.53	+104.05	−31.56	−6.81	−3.90	151.08
700	−1.50	140.66	13.45	+98.89	−31.13	−9.87	−3.99	149.38
750	−1.56	137.19	13.21	+95.44	−31.12	−11.14	−4.02	147.87
800	−1.61	133.97	13.29	+90.33	−31.00	−13.96	−4.07	146.36
850	−1.66	130.74	13.04	+86.67	−30.60	−14.90	−4.12	144.94
900	−1.72	127.65	13.03	+81.59	−30.72	−17.78	−4.21	143.60
950	−1.85	124.15	12.92	+77.91	−30.31	−20.23	−4.25	142.41
1000	−1.92	120.90	12.93	+73.13	−30.22	−22.21	−4.27	141.31
1050	−2.02	117.54	12.92	+68.80	−29.98	−24.19	−4.32	140.51
1100	−2.20	114.21	12.76	+64.12	−29.80	−28.18	−4.37	139.63
1150	−2.41	110.72	12.97	+59.95	−29.39	−29.56	−4.43	138.68
1200	−2.62	107.22	12.69	+54.62	−29.46	−33.00	−4.42	138.09
1250	−2.87	103.77	12.98	+50.95	−29.03	−37.13	−4.47	137.74
1300	−3.16	99.97	12.87	+44.96	−28.75	−38.18	−4.44	137.08
1350	−3.65	96.51	12.94	+40.47	−28.81	−44.64	−4.45	136.77
1400	−4.09	92.23	12.87	+35.36	−28.26	−46.78	−4.40	136.49
1450	−4.59	88.76	13.04	+30.47	−28.43	−49.56	−4.37	136.43
1500	−5.28	84.62	13.00	+24.40	−28.13	−56.47	−4.29	135.79
1550	−6.09	80.71	12.89	+19.39	−27.96	−59.31	−4.20	135.63
1600	−6.98	77.02	13.13	+14.80	−27.98	−62.71	−4.05	135.39
1650	−8.06	72.69	13.07	+7.27	−27.73	−69.93	−3.88	134.43
1700	−9.38	68.92	13.00	+2.17	−27.49	−73.80	−3.71	133.76
1750	−11.15	66.21	12.97	−3.27	−27.78	−77.79	−3.59	132.94
1800	−13.20	63.18	13.18	−9.57	−27.23	−85.28	−3.29	131.04
1850	−15.83	63.73	13.03	−17.27	−27.36	−89.22	−3.11	129.62
1900	−19.87	71.29	12.84	−22.35	−27.40	−96.30	−2.93	127.46
1950	−24.51	103.69	13.08	−29.10	−27.26	−102.96	−2.69	124.63
2000	−22.66	156.61	12.86	−36.58	−27.33	−109.25	−2.54	122.53
2050	−18.02	171.65	12.88	−43.14	−27.33	−117.37	−2.50	118.78
2100	−14.34	174.52	12.63	−51.83	−27.54	−124.60	−2.35	115.97
2150	−12.10	172.15	12.45	−55.83	−27.77	−132.56	−2.44	112.52
2200	−10.23	166.81	12.65	−67.28	−27.74	−141.32	−2.42	108.19
2250	−8.65	160.58	11.82	−73.99	−28.34	−149.30	−2.43	104.65
2300	−7.90	153.80	11.84	−79.82	−28.62	−161.50	−2.74	100.98
2350	−6.66	145.88	11.55	−91.28	−28.92	−165.89	−2.62	96.52
2400	−6.35	138.01	10.97	−96.39	−29.75	+179.97	−2.94	92.52
2450	−5.77	128.87	10.36	−108.43	−30.13	+170.82	−3.03	88.07
2500	−5.51	118.44	9.65	−110.92	−30.41	+163.00	−3.24	83.25
2550	−5.35	112.21	9.46	−122.10	−32.29	+152.20	−3.41	79.98
2600	−5.15	99.40	7.99	−130.39	−31.60	+138.60	−3.55	73.08
2650	−5.22	92.84	7.70	−132.72	−33.19	+135.12	−3.80	69.85
2700	−5.06	82.21	6.61	−143.64	−33.61	+120.22	−3.93	63.87

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, VSUP	6.5 V
Input Power (50 Ω Impedance)	20 dBm
Internal Power Dissipation (Paddle Soldered)	683 mW
θ_{JC} (Junction to Paddle)	28.5°C/W
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

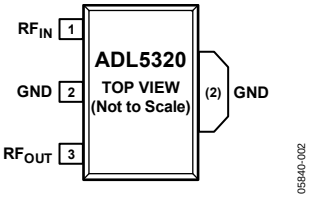


Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RF_{IN}	RF Input. Requires a dc blocking capacitor.
2	GND	Ground. Connect to a low impedance ground plane.
3	RF_{OUT}	RF Output and Supply Voltage. DC bias is provided to this pin through an inductor that is connected to the external power supply. RF path requires a dc blocking capacitor.
Exposed Paddle		Expose Paddle. Internally connected to GND. Solder to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

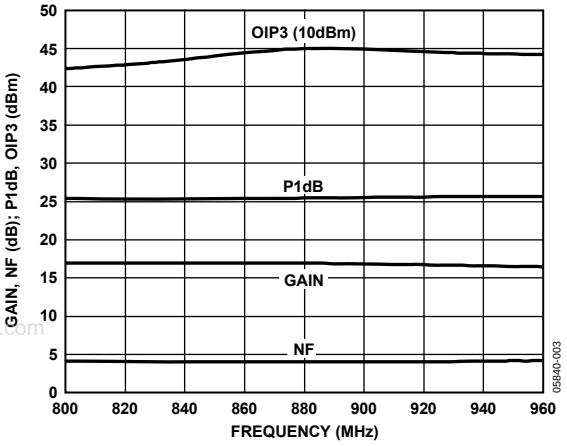


Figure 3. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 800 MHz to 960 MHz

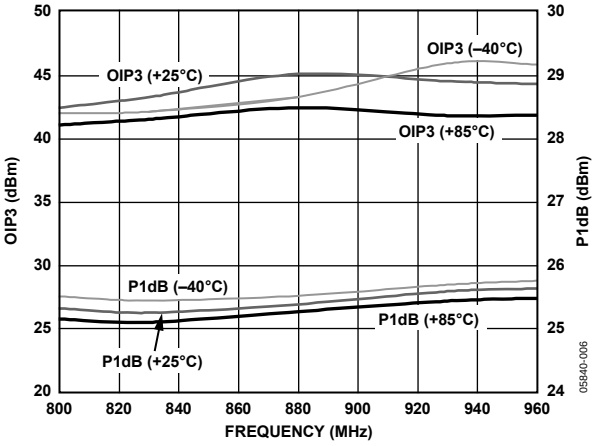


Figure 6. OIP3 and P1dB vs. Frequency and Temperature, 800 MHz to 960 MHz

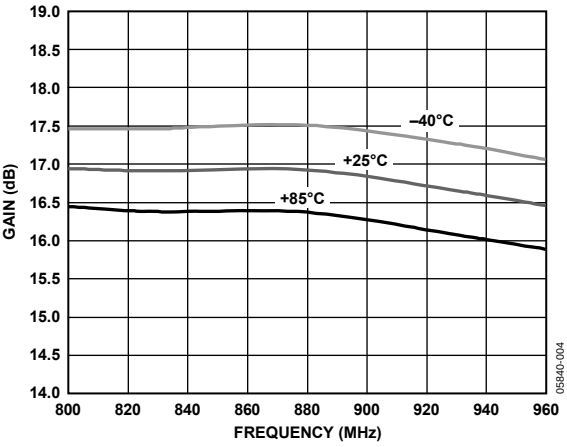


Figure 4. Gain vs. Frequency and Temperature, 800 MHz to 960 MHz

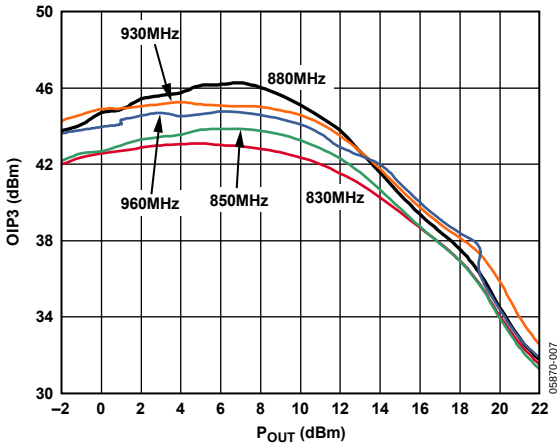


Figure 7. OIP3 vs. P_{OUT} and Frequency, 800 MHz to 960 MHz

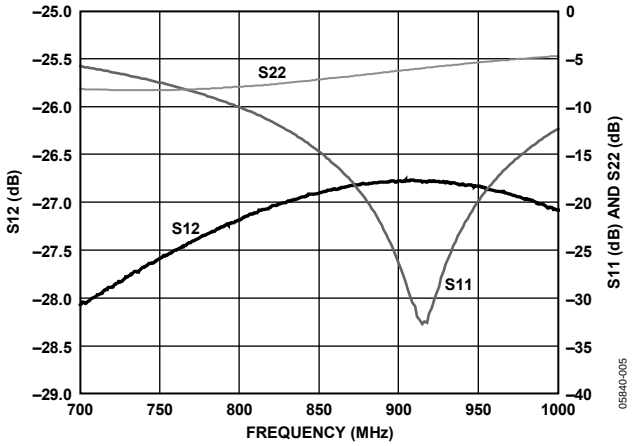


Figure 5. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, 800 MHz to 960 MHz

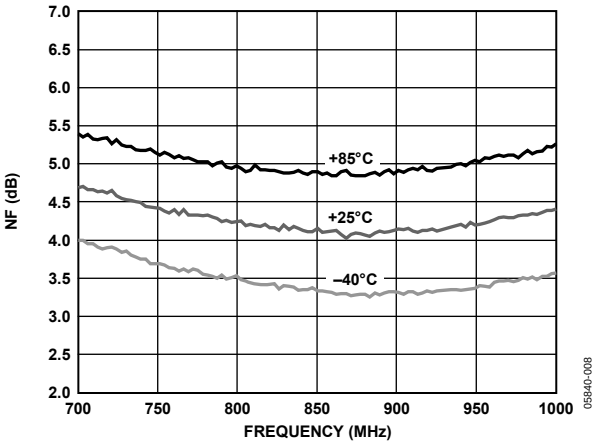


Figure 8. Noise Figure vs. Frequency and Temperature, 800 MHz to 960 MHz

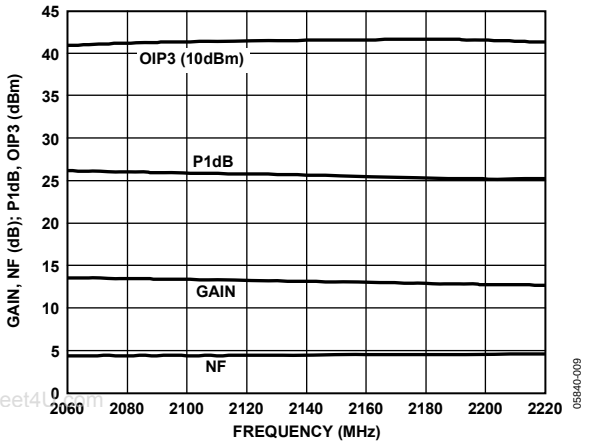


Figure 9. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 2060 MHz to 2200 MHz

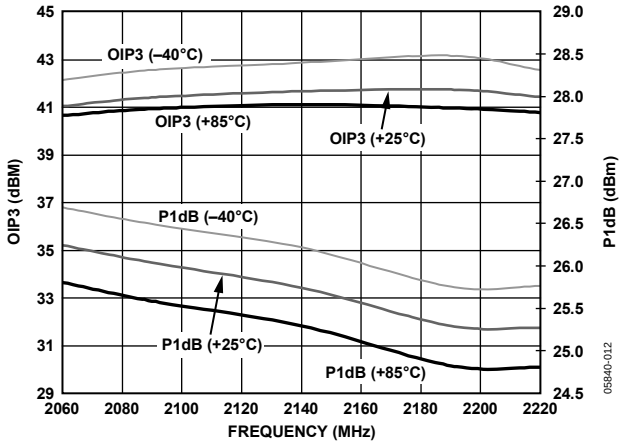


Figure 12. OIP3 and P1dB vs. Frequency and Temperature, 2060 MHz to 2200 MHz

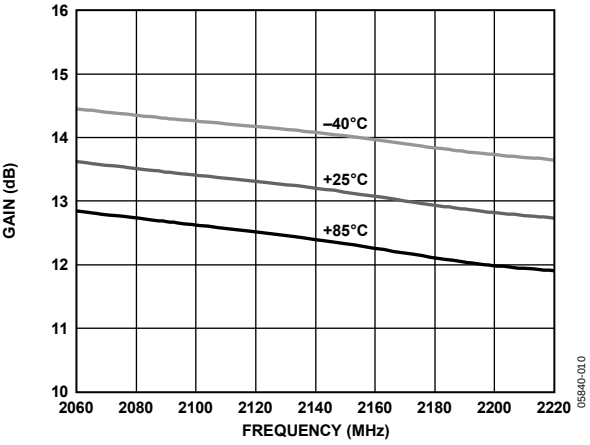


Figure 10. Gain vs. Frequency and Temperature, 2060 MHz to 2200 MHz

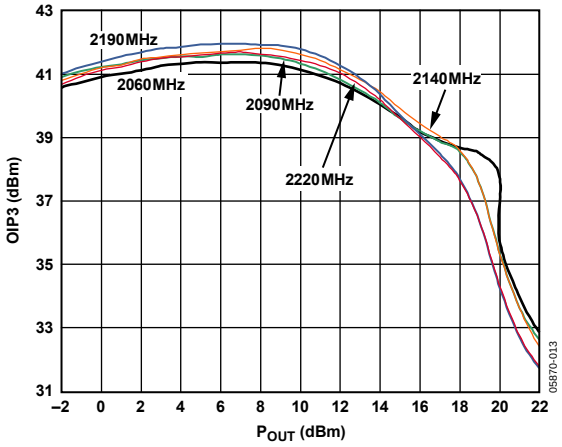


Figure 13. OIP3 vs. P_{OUT} and Frequency, 2060 MHz to 2200 MHz

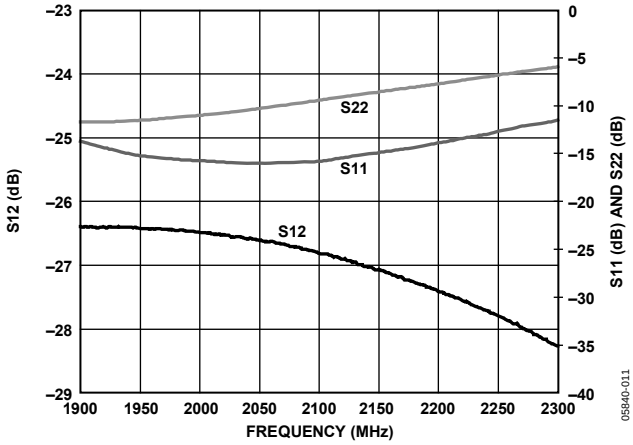


Figure 11. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, 2060 MHz to 2200 MHz

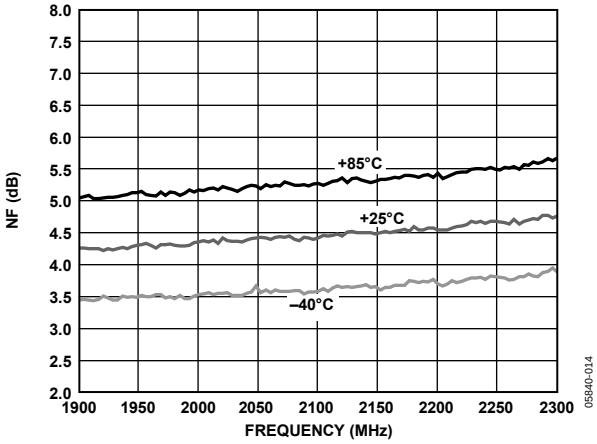


Figure 14. Noise Figure vs. Frequency and Temperature, 2060 MHz to 2200 MHz

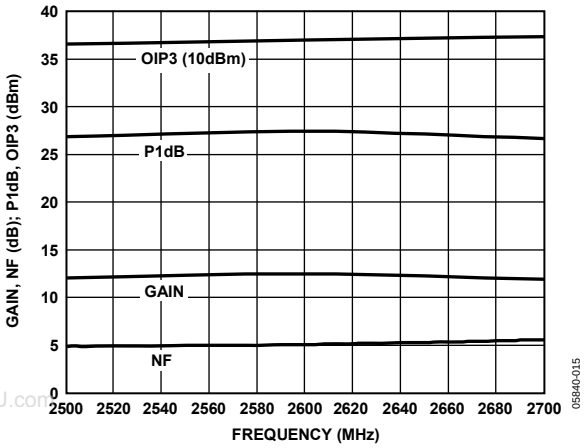


Figure 15. Gain, P1dB, OIP3, and Noise Figure vs. Frequency, 2500 MHz to 2700 MHz

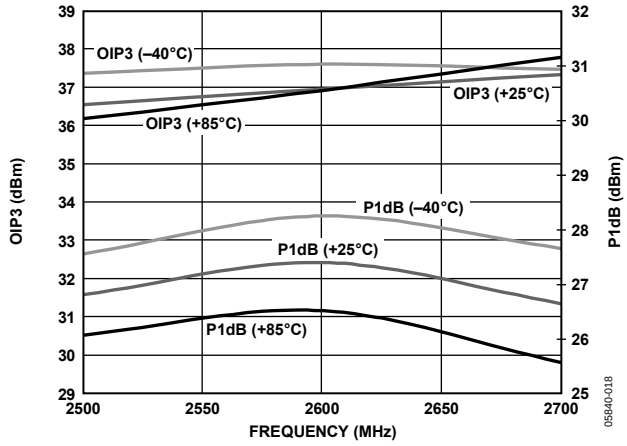


Figure 18. OIP3 and P1dB vs. Frequency and Temperature, 2500 MHz to 2700 MHz

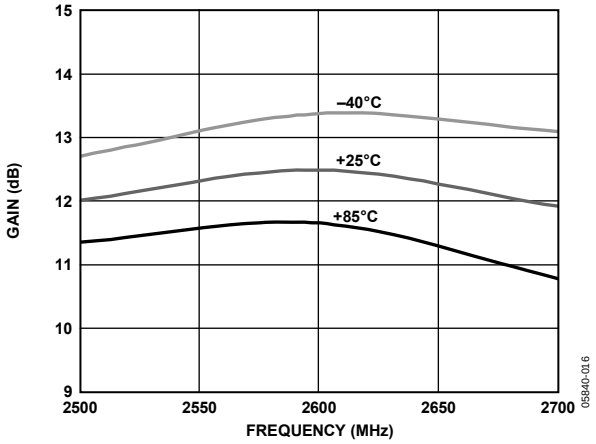


Figure 16. Gain vs. Frequency and Temperature, 2500 MHz to 2700 MHz

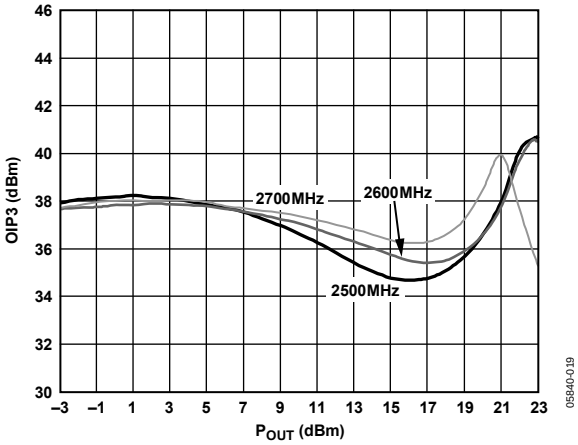


Figure 19. OIP3 vs. P_{OUT} and Frequency, 2500 MHz to 2700 MHz

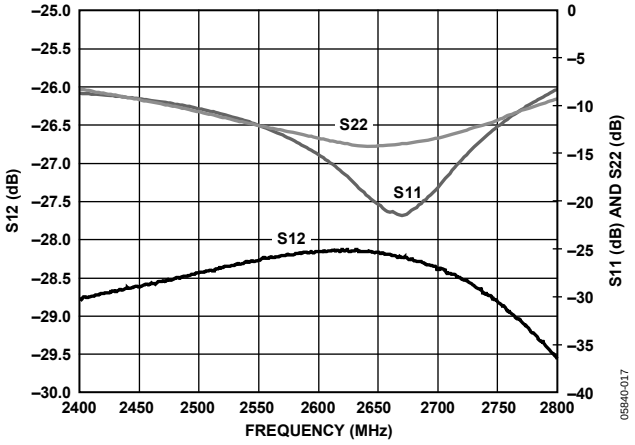


Figure 17. Input Return Loss (S11), Output Return Loss (S22), and Reverse Isolation (S12) vs. Frequency, 2500 MHz to 2700 MHz

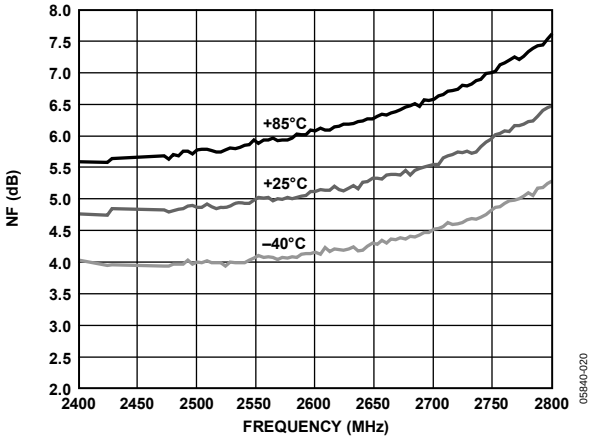


Figure 20. Noise Figure vs. Frequency and Temperature, 2500 MHz to 2700 MHz

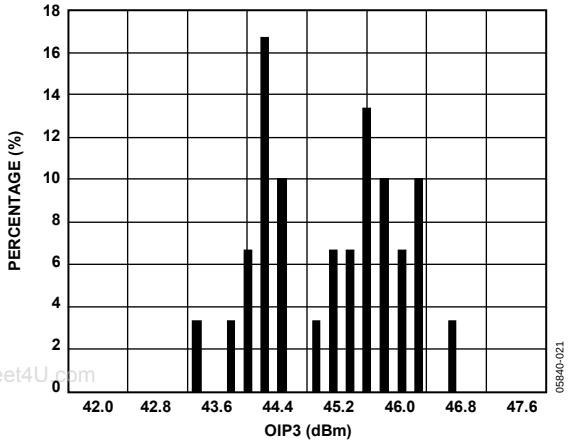


Figure 21. OIP3 Distribution at 880 MHz

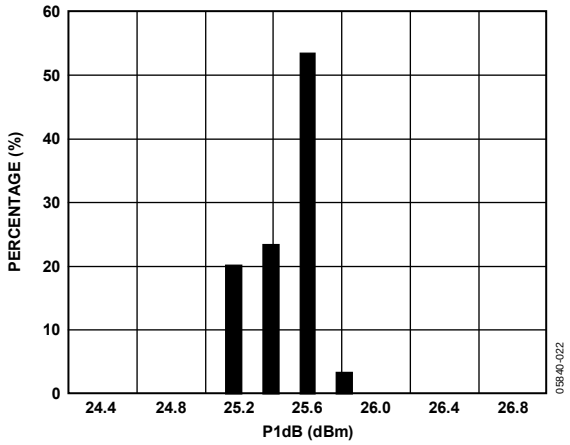


Figure 22. P1dB Distribution at 880 MHz

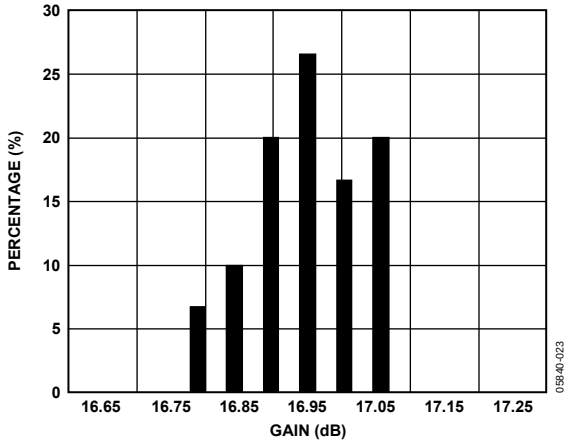


Figure 23. Gain Distribution at 880 MHz

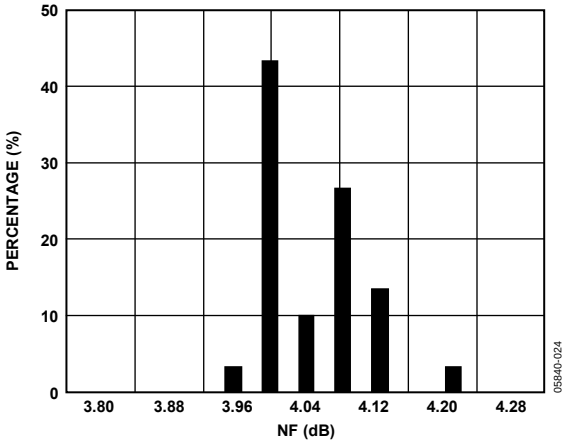


Figure 24. Noise Figure Distribution at 880 MHz

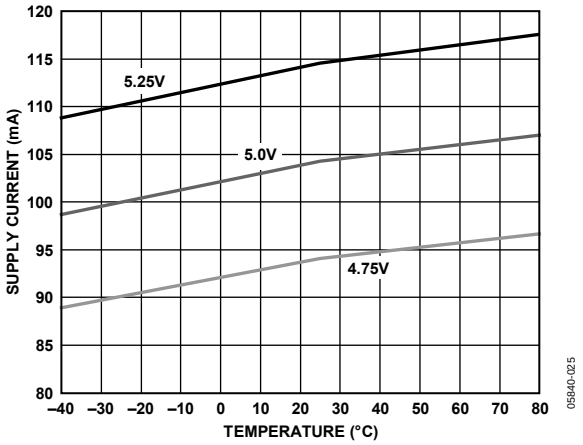


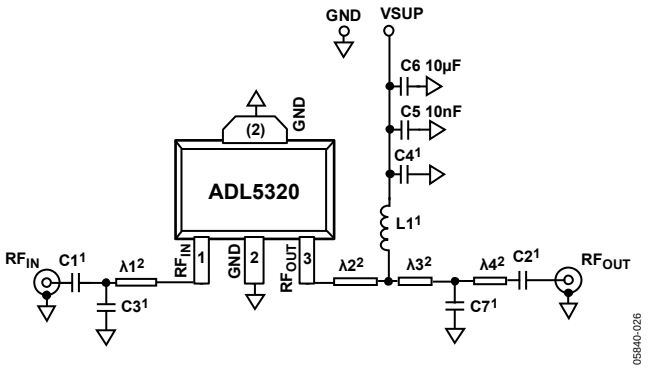
Figure 25. Supply Current vs. Supply Voltage and Temperature (Using 880 MHz Matching Components)

BASIC LAYOUT CONNECTIONS

The basic connections for operating the ADL5320 are shown in Figure 26.

Table 5 lists the required matching components. Capacitors C1, C2, C3, C4, and C7 are Murata GRM155 series (0402 size) and Inductor L1 is a Coilcraft 0603CS series (0603 size). For all frequency bands, the placement of C3 and C7 are critical. From 2300 MHz to 2700 MHz, the placement of C2 is also important. Table 6 lists the recommended component placement for various frequencies.

A 5 V dc bias is supplied through L1 which is connected to RF_{OUT} (Pin 3). In addition to C4, 10 nF and 10 µF power supply decoupling capacitors are also required. The typical current consumption for the ADL5320 is 110 mA.



[1]SEE TABLE 5 FOR FREQUENCY SPECIFIC COMPONENTS.
[2]SEE TABLE 10 FOR RECOMMENDED COMPONENT SPACING.

Figure 26. Basic Connections

SOLDERING INFORMATION AND RECOMMENDED PCB LAND PATTERN

Figure 27 shows the recommended land pattern for the ADL5320. To minimize thermal impedance, the exposed paddle on the SOT-89 package underside is soldered down to a ground plane along with Pin 2. If multiple ground layers exist, they should be stitched together using vias. For more information on land pattern design and layout, refer to the Application Note AN-772, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

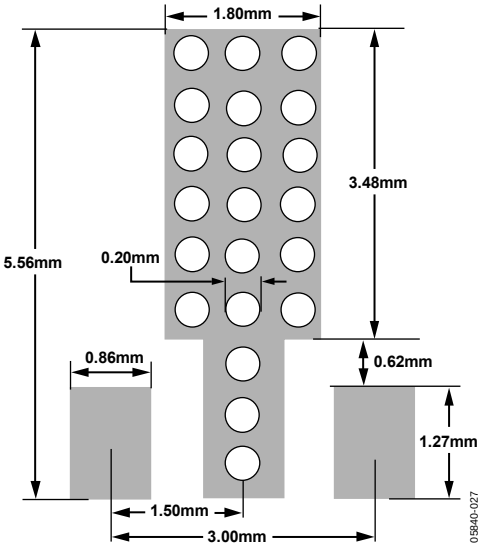


Figure 27. Recommended Land Pattern

Table 5. Recommended Components for Basic Connections

Frequency (MHz)	C1 (pF)	C2 (pF)	C3 (pF)	C4 (pF)	C7 (pF)	L1 (nH)
450 to 500	100	100	18	100	6.8	47
800 to 960	47	47	6.8	100	2.2	47
1805 to 1880	22	22	0.5	22	1.5	15
1930 to 1990	22	22	0.5	22	1.5	15
2110 to 2170	22	22	0.5	22	1.5	15
2300 to 2400	12	2.2	1.2	12	1.0	15
2500 to 2700	12	1.0	1.8	12	0.5	15

Table 6. Matching Component Spacing

Frequency (MHz)	λ1 (mils)	λ2 (mils)	λ3 (mils)	λ4 (mils)
450 to 500	391	75	364	50
800 to 960	200	75	100	350
1805 to 2170	300	75	175	275
2300 to 2400	225	75	125	125
2500 to 2700	142	75	89	75

MATCHING PROCEDURE

The ADL5320 is designed to achieve excellent gain and IP3 performance. To achieve this, both input and output matching networks must present specific impedance to the device. The matching components listed in Table 6 were chosen to provide −10 dB input return loss while maximizing OIP3. The load-pull plots (Figure 28, Figure 29, and Figure 30) show the load impedance points on the Smith chart where optimum OIP3, gain, and output power can be achieved. These load impedance values (that is, the impedance that the device sees when looking into the output matching network) are listed in Table 7 and Table 8 for maximum gain and maximum OIP3, respectively. The contours show how each parameter degrades as it is moved away from the optimum point.

From the data shown in Table 7 and Table 8 it becomes clear that maximum gain and maximum OIP3 do not occur at the same impedance. This can also be seen on the load-pull contours in Figure 28 through Figure 30. Thus, output matching generally involves compromising between gain and OIP3. In addition, the load-pull plots demonstrate that the quality of the output impedance match must be compromised to optimize gain and/or OIP3. In most applications where line lengths are short and where the next device in the signal chain presents a low input return loss, compromising on the output match is acceptable.

To adjust the output match for operation at a different frequency or if a different trade-off between OIP3, gain, and output impedance is desired, the following procedure is recommended.

For example, to optimize the ADL5320 for optimum OIP3 and gain at 700 MHz use the following steps:

1. Install the recommended tuning components for a 800 MHz to 960 MHz tuning band, but do not install C3 and C7.
2. Connect the evaluation board to a vector network analyzer so that input and output return loss can be viewed simultaneously.
3. Starting with the recommended values and positions for C3 and C7, adjust the positions of these capacitors along the transmission line until the return loss and gain are acceptable. Push-down capacitors that are mounted on small sticks can be used in this case as an alternative to soldering. If moving the component positions does not yield satisfactory results, then the values of C3 and C7 should be increased or decreased (most likely increased in this case as the user is tuning for a lower frequency). Repeat the process.
4. Once the desired gain and return loss are realized, OIP3 should be measured. Most likely, it will be necessary to go back and forth between return loss/gain and OIP3 measurements (probably compromising most on output return loss) until an acceptable compromise is achieved.

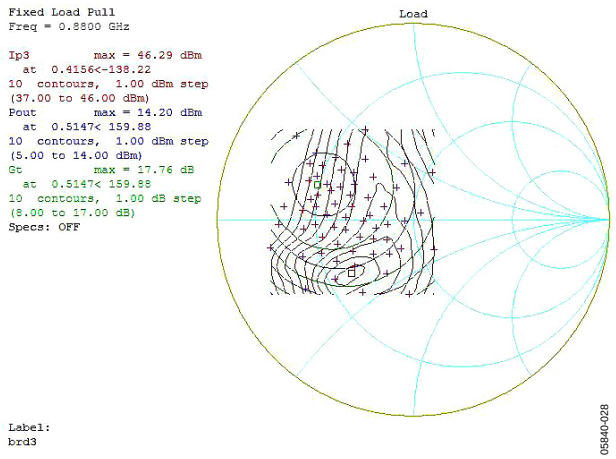


Figure 28. Load-Pull Contours, 880 MHz

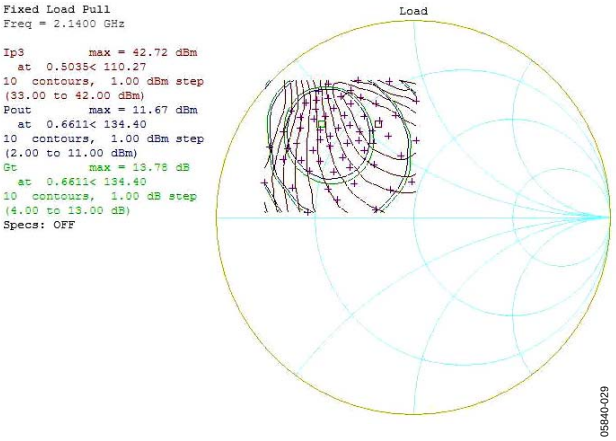


Figure 29. Load-Pull Contours, 2140 MHz

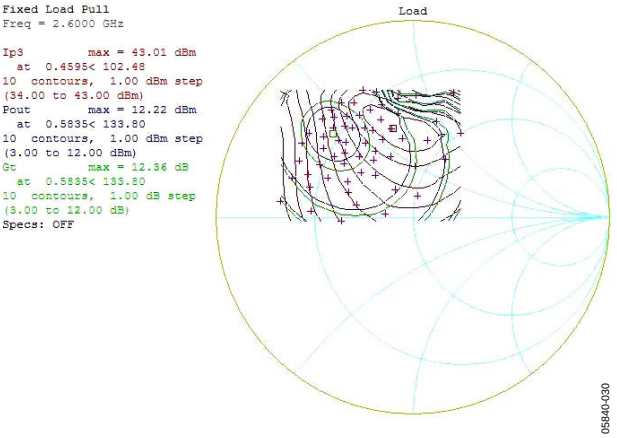


Figure 30. Load-Pull Contours, 2600 MHz

Table 7. Load Conditions for Gain $_{MAX}$

Frequency (MHz)	ΓLoad (Magnitude)	ΓLoad (°)	Gain $_{MAX}$ (dB)
880	0.5147	159.88	17.76
2140	0.6611	134.40	13.78
2600	0.5835	133.80	12.36

Table 8. Load Conditions for IP3 $_{MAX}$

Frequency (MHz)	ΓLoad (Magnitude)	ΓLoad (°)	IP3 $_{MAX}$ (dBm)
880	0.4156	−138.22	46.29
2140	0.5035	+110.27	42.72
2600	0.4595	+102.48	43.01

W-CDMA ACPR PERFORMANCE

Figure 31 shows a plot of adjacent channel power ratio (ACPR) vs. P_{OUT} for the ADL5320. The signal type being used is a single W-CDMA carrier (Test Model 1−64) at 2140 MHz. This signal is generated by a very low ACPR source. ACPR is measured at the output by a high dynamic range spectrum analyzer, which incorporates an instrument noise correction function.

The ADL5320 achieves an ACPR of −82 dBc at 0 dBm output, at which point device noise and not distortion is beginning to dominate the power in the adjacent channels. At an output power of 10 dBm, ACPR is still very low at −70 dBc making the device particularly suitable for PA driver applications.

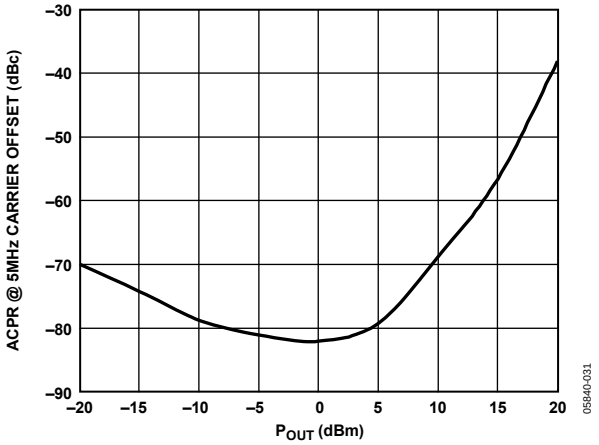


Figure 31. ACPR vs. P_{OUT}, Single Carrier W-CDMA (Test Model 1−64) at 2140 MHz Evaluation Board

EVALUATION BOARD

The schematic of the ADL5320 evaluation board is shown in Figure 32. This evaluation board uses 25 mil wide traces and is made from FR4 material. The evaluation board comes tuned for operation in the 1805 MHz to 2140 MHz tuning band. Tuning options for other frequency bands are also provided in Table 9. The recommended placement for these components is provided in Table 10. The inputs and outputs should be ac-coupled with appropriately sized capacitors. DC bias is provided to the amplifier via an inductor connected to the RF_{OUT} pin. A bias voltage of 5 V is recommended.

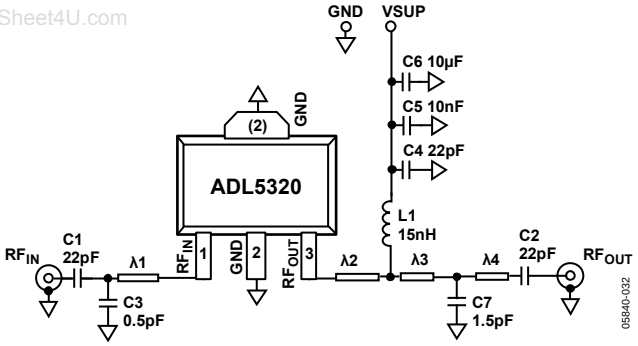


Figure 32. Evaluation Board, 1805 MHz to 2170 MHz

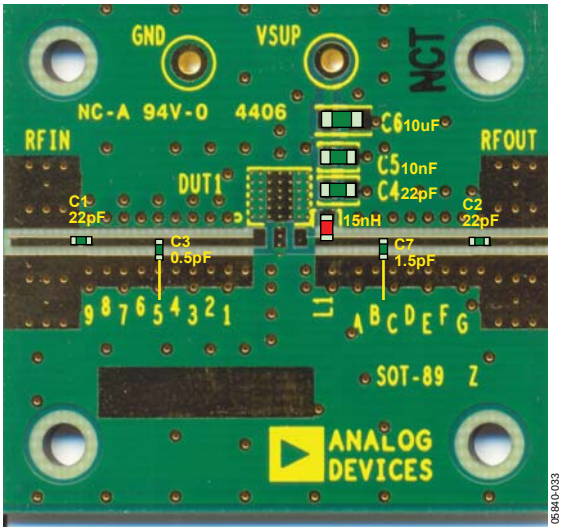


Figure 33. Evaluation Board Layout and Default Component Placement for Operation from 1805 MHz to 2170 MHz

Table 9. Evaluation Board Configuration Options

Component	Function	450 MHz to 500 MHz	800 MHz to 960 MHz	1805 MHz to 2170 MHz (Default Configuration)	2300 MHz to 2400 MHz	2500 MHz to 2700 MHz
C1, C2	AC coupling capacitors	0402, 100 pF	0402, 47 pF	0402, 22pF	C1= 0402 12 pF C2 = 0402 2.2 pF	C1 = 0402 12 pF C2 = 0402 1.0 pF
C4, C5, C6	Power supply bypassing capacitors	C4 = 0603 100 pF C5 = 0603 10 nF C6 = 1206 10 µF	C4 = 0603 100 pF C5 = 0603 10 nF C6 = 1206 10 µF	C4 = 0402 22pF C5 = 0603 10 nF C6 = 1206 10 µF	C4 = 0603 12 pF C5 = 0603 10 nF C6 = 1206 10 µF	C4 = 0603 12 pF C5 = 0603 10 nF C6 = 1206 10 µF
L1	DC bias inductor	0603, 47 nH	0603, 47 nH	0603, 15 nH	0603, 15 nH	0603, 15 nH
C3, C7	Tuning capacitors	C3 = 0402 18 pF C7 = 0402 6.8 pF	C3 = 0402 6.8 pF C7 = 0402 2.2 pF	C3 = 0402 0.5 pF C7 = 0402 1.5 pF	C3 = 0402 1.2 pF C7 = 0402 1.0 pF	C3 = 0402 1.8 pF C7 = 0402 0.5 pF
R1					R1 = 0402 0 Ω	R1 = 0402 0 Ω
VSUP, GND	Power supply connections	VSUP red test loop, GND black test loop	VSUP red test loop, GND black test loop	VSUP red test loop, GND black test loop	VSUP red test loop, GND black test loop	VSUP red test loop, GND black test loop

Table 10. Recommended Component Spacing on Evaluation Board

Frequency (MHz)	λ1 (mils)	λ2 (mils)	λ3 (mils)	λ4 (mils)
450 to 500	391	75	364	50
800 to 960	200	75	100	350
1805 to 2170	300	75	175	275
2300 to 2400	225	75	125	125
2500 to 2700	142	75	89	75

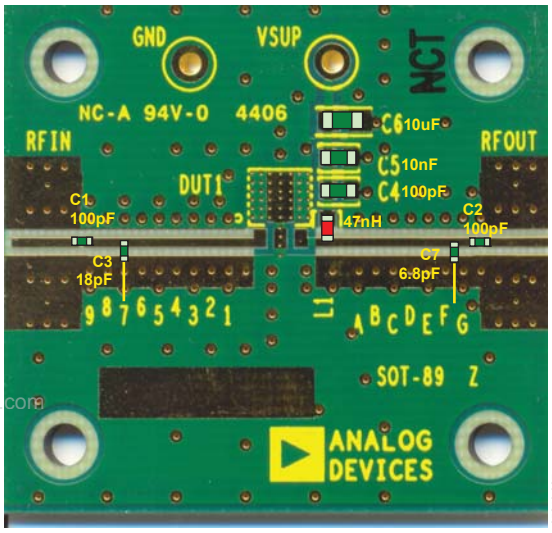


Figure 34. Evaluation Board Layout and Component Placement
450 MHz to 500 MHz Operation

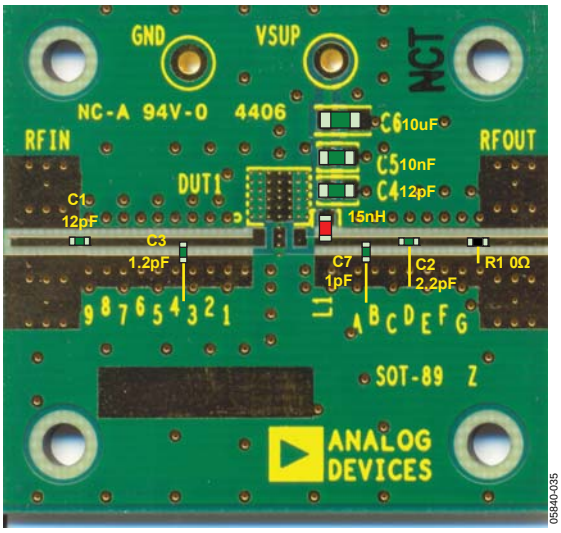


Figure 36. Evaluation Board Layout and Component Placement
2300 MHz to 2400 MHz Operation

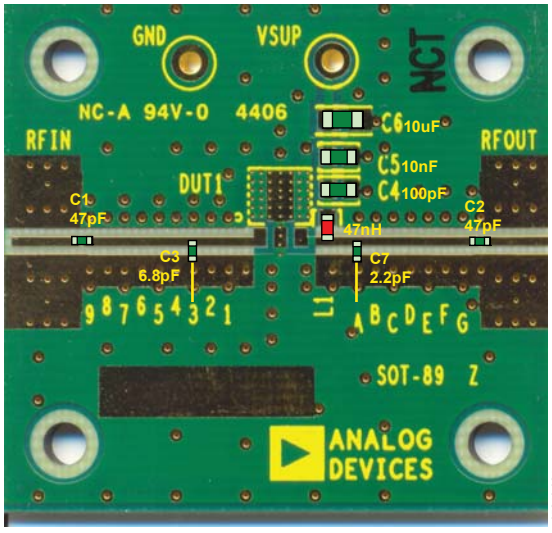


Figure 35. Evaluation Board Layout and Component Placement
800 MHz to 960 MHz Operation

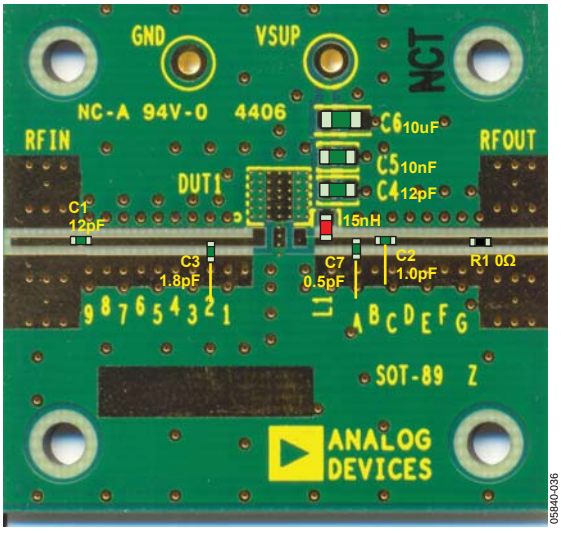


Figure 37. Evaluation Board Layout and Component Placement
2500 MHz to 2700 MHz Operation

OUTLINE DIMENSIONS

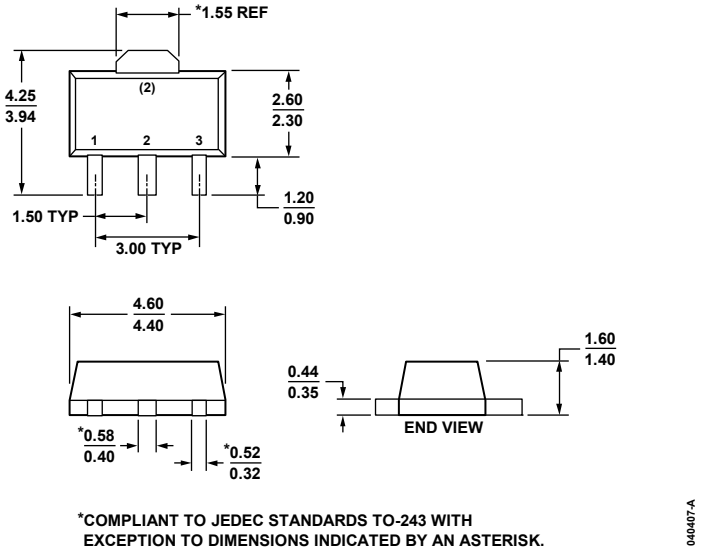


Figure 38. 3–Lead Small Outline Transistor Package [SOT-89]
(RK-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADL5320ARKZ-R7[1]	−40°C to +85°C	3-Lead SOT-89, 7" Tape and Reel	RK-3
ADL5320-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

D05840-0-2/08(0)