700 MHz to 4200 MHz, Tx DGA

Data Sheet

ADL5335

FEATURES

Differential input to single-ended output conversion
Broad input frequency range: 700 MHz to 4200 MHz
Maximum gain: 12.0 dB typical
Gain range of 20 dB typical
Gain step size: 0.5 dB typical
Glitch free, thermometer-based digital step attenuator
Fast attack, gain switching with programmable gain step
Matched 50 Ω inputs and output

APPLICATIONS

RF power control and calibration in wireless transmitters

FUNCTIONAL BLOCK DIAGRAM

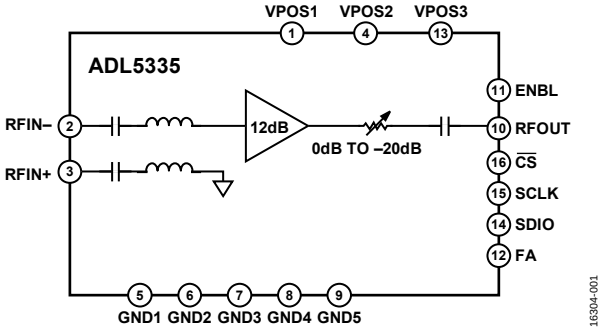


Figure 1.

GENERAL DESCRIPTION

The ADL5335 is a digital gain amplifier (DGA) optimized for use in wireless transmitters. A differential input and single-ended output facilitates a balun free connection between the broadband integrated transceivers with differential outputs and the RF gain blocks and drivers amplifiers with single-ended inputs.

The gain is programmable via a standard Analog Devices, Inc., serial peripheral interface (SPI) port from a maximum gain of 12.0 dB down to a minimum gain of −8.0 dB with a gain step size of 0.5 dB. The ADL5335 also features a fast attack function where the gain can rapidly increase or decrease by the application of a single pulse.

The use of a thermometer-based digital step attenuator (DSA) ensures that gain changes are fundamentally glitch free. The ADL5335 is packaged in a 4 mm × 4 mm, 16-lead LFCSP. A fully populated evaluation board and system demonstration platform (SDP)-based control software are available.

Rev. 0 **Document Feedback**

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **Technical Support**

www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

12/2017—Revision 0: Initial Version

SPECIFICATIONS

VPOS1, VPOS2, VPOS3 = 5 V, T_A = 25°C, impedance out (Z_{OUT}) = 50 Ω, and a differential input drive, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OVERALL FUNCTION					
Input Frequency Range		700		4200	MHz
Impedance					
Input	Differential input drive		50		Ω
Output	Single-ended output		50		Ω
GAIN CONTROL					
Gain Range			20		dB
Maximum Gain			12.0		dB
Minimum Gain			−8.0		dB
Gain Step Size			0.5		dB
BAND 8: 925 MHz TO 960 MHz					
Gain Range			20		dB
Maximum Gain			13.0		dB
Minimum Gain			−7.0		dB
Gain Flatness	±200 MHz, all gains		0.3		dB
Gain Step Error	All gain states		0.2		dB
Group Delay Variation	Between any attenuation step		50		ps
Output Third-Order Intercept (IP3)	Maximum gain, 4 dBm per tone		34		dBm
	Minimum gain, −18 dBm per tone		13.6		dBm
Output 1 dB Compression Point (P1dB)	Maximum gain		18.0		dBm
	Minimum gain		−0.6		dBm
Noise Figure	Maximum gain		5.4		dB
	Minimum gain		8.3		dB
Return Loss					
Input			−18		dB
Output	Minimum gain		−17		dB
	Maximum gain		−30		dB
Common-Mode Rejection Ratio (CMRR)	vs. frequency (±200 MHz)		20		dB
BAND 3: 1805 MHz TO 1880 MHz					
Gain Range			20		dB
Maximum Gain			12.8		dB
Minimum Gain			−7.2		dB
Gain Flatness	±200 MHz, all gains		0.5		dB
Gain Step Error	All gain states		0.4		dB
Group Delay Variation	Between any attenuation step		45		ps
Output IP3	Maximum gain, 4 dBm per tone		33		dBm
	Minimum gain, −18 dBm per tone		12		dBm
Output P1dB	Maximum gain		18.3		dBm
	Minimum gain		0		dBm
Noise Figure	Maximum gain		6.9		dB
	Minimum gain		10.6		dB
Return Loss					
Input			−32		dB
Output	Minimum gain		−23		dB
	Maximum gain		−17		dB
CMRR	vs. frequency (±200 MHz)		22		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BAND 1: 2110 MHz TO 2170 MHz					
Gain Range			20		dB
Maximum Gain			12.5		dB
Minimum Gain			−7.5		dB
Gain Flatness	±200 MHz, all gains		0.5		dB
Gain Step Error	All gain states		0.38		dB
Group Delay Variation	Between any attenuation step		20		ps
Output IP3	Maximum gain, 4 dBm per tone		32		dBm
	Minimum gain, −18 dBm per tone		11.6		dBm
Output P1dB	Maximum gain		18.1		dBm
	Minimum gain		−0.2		dBm
Noise Figure	Maximum gain		6.9		dB
	Minimum gain		10.4		dB
Return Loss					
Input			−32		dB
Output	Minimum gain		−25		dB
	Maximum gain		−19		dB
CMRR	vs. frequency (±200 MHz)		25		dB
BAND 7: 2620 MHz TO 2690 MHz					
Gain Range			20		dB
Maximum Gain			12.0		dB
Minimum Gain			−8.0		dB
Gain Flatness	±200 MHz, all gains		0.7		dB
Gain Step Error	All gain states		0.37		dB
Group Delay Variation	Between any attenuation step		30		ps
Output IP3	Maximum gain, 4 dBm per tone		32		dBm
	Minimum gain, −18 dBm per tone		13.1		dBm
Output P1dB	Maximum gain		17.8		dBm
	Minimum gain		−1.1		dBm
Noise Figure	Maximum gain		7.5		dB
	Minimum gain		10.5		dB
Return Loss					
Input			−19		dB
Output	Minimum gain		−24		dB
	Maximum gain		−17		dB
CMRR	vs. frequency (±200 MHz)		26		dB
BAND 42: 3400 MHz TO 3600 MHz					
Gain Range			20		dB
Maximum Gain			10.2		dB
Minimum Gain			−9.8		dB
Gain Flatness	±200 MHz, all gains		0.7		dB
Gain Step Error	All gain states		0.36		dB
Group Delay Variation	Between any attenuation step		20		ps
Output IP3	Maximum gain, 4 dBm per tone		31		dBm
	Minimum gain, −18 dBm per tone		10.9		dBm
Output P1dB	Maximum gain		16.8		dBm
	Minimum gain		2.3		dBm
Noise Figure	Maximum gain		7.5		dB
	Minimum gain		12.2		dB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Return Loss					
Input			−19		dB
Output	Minimum gain		−17		dB
	Maximum gain		−11		dB
CMRR	vs. frequency (±200 MHz)		28		dB
FREQUENCY = 4.2 GHz					
Gain Range			20		dB
Maximum Gain			9.3		dB
Minimum Gain			−10.7		dB
Gain Flatness	±200 MHz, all gains		0.9		dB
Gain Step Error	All gain states		0.49		dB
Group Delay Variation	Between any attenuation step		25		ps
Output IP3	Maximum gain, −4 dBm per tone		29		dBm
	Minimum gain, −18 dBm per tone		11		dBm
Output P1dB	Maximum gain		15.8		dBm
	Minimum gain		−3.7		dBm
Noise Figure	Maximum gain		8.7		dB
	Minimum gain		13.5		dB
Return Loss					
Input			−24		dB
Output	Minimum gain		−12		dB
	Maximum gain		−11		dB
CMRR			29		dB
SPI PORT AND FAST ATTACK	SDIO, SCLK, $\overline{CS}$, FA pins				
Logic Low				0.18	V
Logic High		1.62		1.8	V
Fast Attack Response Time			20		ns
ENABLE INTERFACE	ENBL pin				
Voltage Level					
To Enable	ENBL voltage (V_{ENBL}) increasing	1.62		1.8	V
To Disable	Enable/disable voltage (V_{ENBLDN}) increasing	0		0.18	V
Time					
Enable			30		ns
Disable			30		ns
POWER SUPPLY INTERFACE	VPOSx pins				
Supply Voltage	Main supply	4.75	5	5.25	V
Quiescent Current	Device enabled		125		mA
Power Consumption	Device enabled		625		mW
	Power-down mode		18.5		mW

DIGITAL LOGIC TIMING

Table 2.

Parameter	Description	Min	Typ	Max	Unit
t_{CLK}	Maximum serial clock rate		25		MHz
t_{HI}	Minimum period that SCLK is in a logic high state		10		ns
t_{LO}	Minimum period that SCLK is in a logic low state		10		ns
t_S	Setup time between falling edge of $\overline{CS}$ and SCLK		15		ns
t_H	Hold time between data and rising edge of SCLK		5		ns
t_{DS}	Setup time between data and rising edge of SCLK		15		ns
t_{DH}	SCLK to SDIO Hold Time		10		ns
t_Z	Maximum time delay between $\overline{CS}$ deactivation and SDIO bus to return to high impedance		5		ns
t_{ACCESS}	Maximum time delay between falling edge of SCLK and out data valid for a read operation		5		ns

SPI Timing Diagram

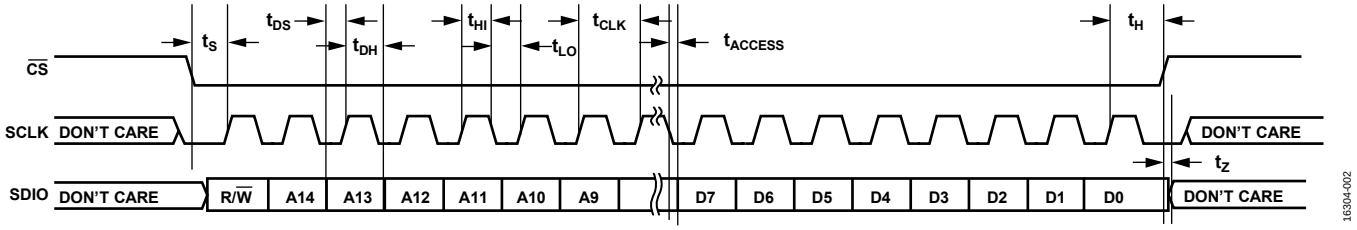


Figure 2. SPI Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
SCLK, SDIO, $\overline{CS}$, FA	3.9 V
Enable Voltage, ENBL	2.2 V
Input Average RF Power	12 dBm
Equivalent Voltage, Sine Wave Input[1]	2.5 V p-p
Internal Power Dissipation	725 mW
Maximum Junction Temperature	150°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] If the common-mode voltage at the inputs (V_{COM}) is closer than 0.625 V from either rail voltage (V_{RAIL}), the equivalent voltage reduces to ($|V_{RAIL} - V_{COM}|$) × 4, where V_{RAIL} is the rail closest to V_{COM}.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THREMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 4 shows the thermal resistance from the die to ambient (θ_{JA}) and die to lead (θ_{JC}), respectively.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-16-39	58.7	2.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

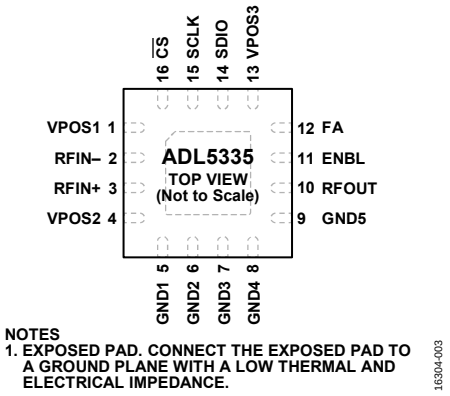


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 13	VPOS1, VPOS2, VPOS3	Power Supplies. Separately decouple each power supply pin using 100 pF and 0.1µF capacitors.
2, 3	RFIN–, RFIN+	RF Negative and Positive Inputs. These pins have a 50 Ω differential input pair and are internally ac-coupled.
5 to 9	GND1, GND2, GND3, GND4, GND5	Ground. Connect these ground pins to a low impedance ground plane.
10	RFOUT	RF Output. This pin has a 50 Ω single-ended output and is internally ac-coupled.
11	ENBL	Enable. A logic high on this pin (1.8 V logic) enables operation and a logic low on this pin puts the device in a low power sleep mode.
12	FA	Fast Attack. A logic high on this pin (1.8 V logic) decreases the programmed gain by an additional 2 dB, 4 dB, 8 dB, or 16 dB. The fast attack attenuation step is defined by the last two bits of an 8-bit programming byte that is written to the device via the SPI. When FA returns to a logic low, the gain returns to its normal programmed level. When not using the fast attack function, tie the FA pin to ground.
14	SDIO	Serial Data Input/Output (SDIO), 1.8 V Logic. The gain and fast attack attenuation levels are programmed using eight bits (Register Address 0x100). The 24-bit write consists of an R/W bit, a 15-bit register address, and the eight bits of data. The first six bits of data set the gain and the last two bits set the fast attack attenuation (−2 dB, −4 dB, −8 dB, or −16 dB).
15	SCLK	Serial Clock (SCLK), 1.8 V Logic. The gain and fast attack attenuation levels are programmed using eight bits (Register Address 0x100). The 24-bit write consists of an R/W bit, a 15-bit register address, and the eight bits of data. The first six bits of data set the gain and the last two bits set the fast attack attenuation (−2 dB, −4 dB, −8 dB, or −16 dB).
16	$\overline{CS}$	Chip Select Bar ($\overline{CS}$), 1.8 V Logic. The gain and fast attack attenuation levels are programmed using eight bits (Register Address 0x100). The 24-bit write consists of an R/W bit, a 15-bit register address, and the eight bits of data. The first six bits of data set the gain and the last two bits set the fast attack attenuation (−2 dB, −4 dB, −8 dB, or −16 dB).
	EP	Exposed Pad. Connect the exposed pad to a ground plane with a low thermal and electrical impedance.

TYPICAL PERFORMANCE CHARACTERISTICS

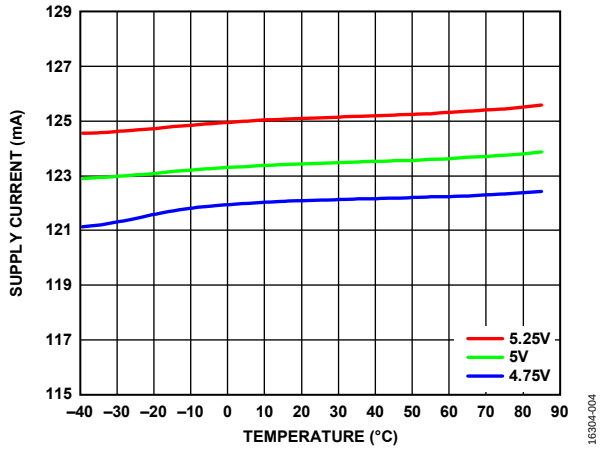


Figure 4. Supply Current vs. Temperature for Various Power Supplies (V_{POS})

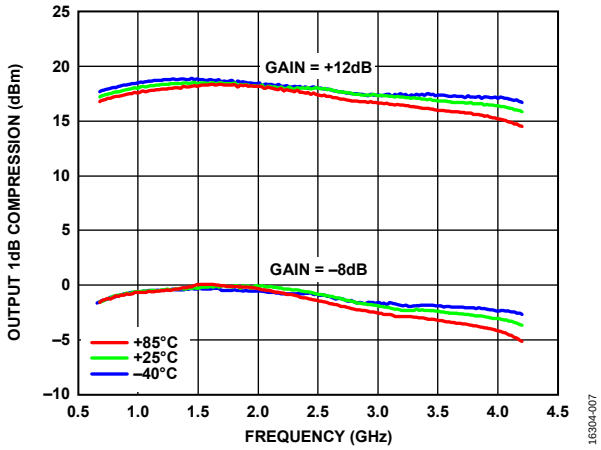


Figure 7. Output 1dB Compression vs. Frequency for Various Temperatures and Gains, V_{POS} = 5 V

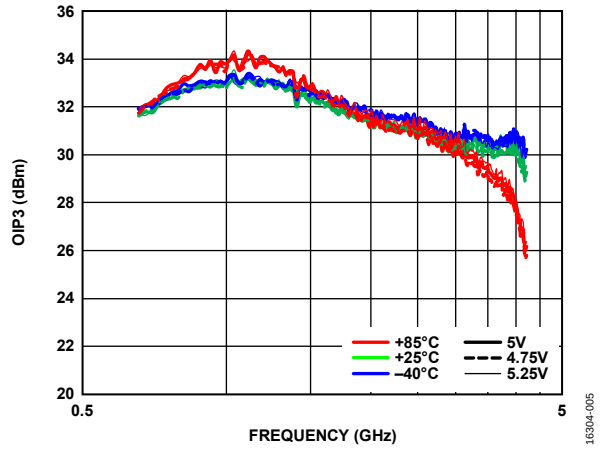


Figure 5. Output Third-Order Intercept (OIP3) vs. Frequency for Various V_{POS} and Temperatures, Maximum Gain = 12 dB, Output Tones = 4 dBm

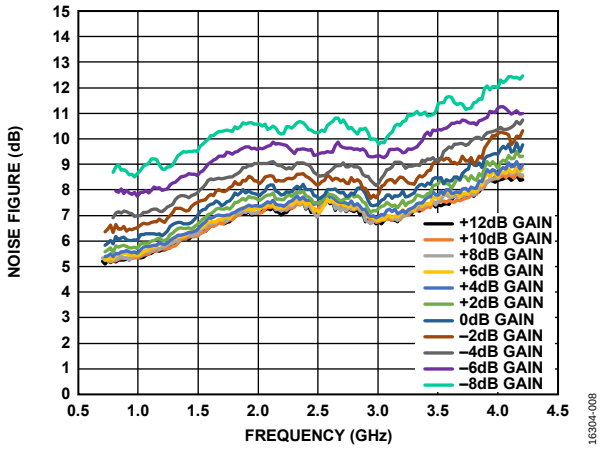


Figure 8. Noise Figure vs. Frequency for Various Gain Steps at V_{POS} = 5 V

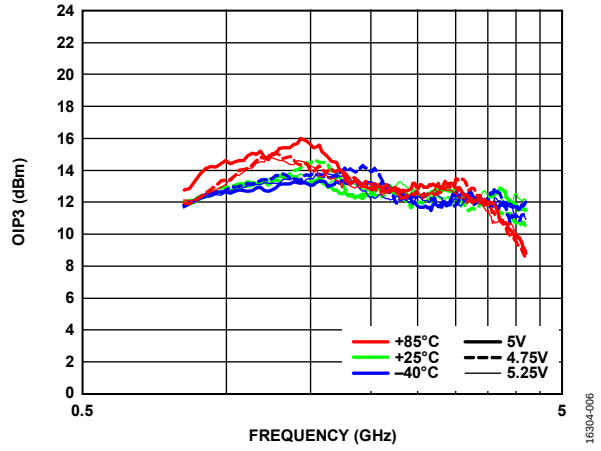


Figure 6. OIP3 vs. Frequency for Various V_{POS} and Temperatures, Minimum Gain = –8 dB, Output Tones = –18 dBm

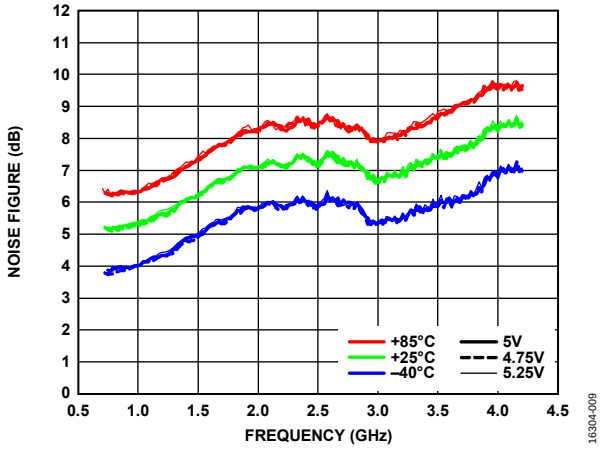


Figure 9. Noise Figure vs. Frequency for Various Temperatures and V_{POS} at Maximum Gain = 12 dB

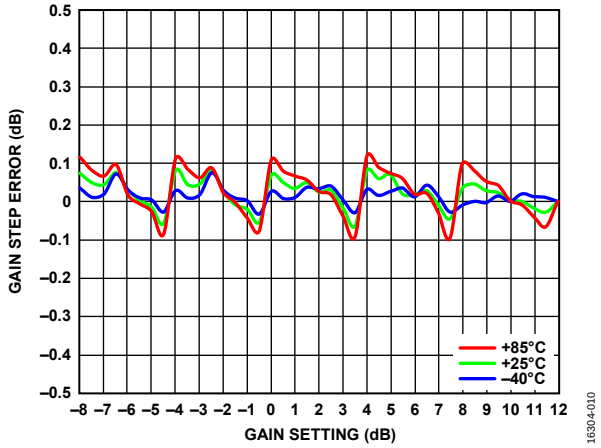


Figure 10. Gain Step Error vs. Gain Setting for Various Temperatures, V_{POS} = 5 V

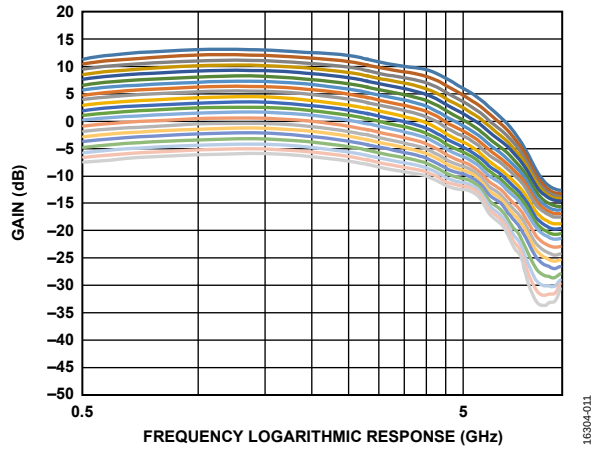


Figure 11. Gain vs. Frequency Logarithmic Response with a Maximum Gain = +12 dB to a Minimum Gain = −8 dB in 1 dB Steps

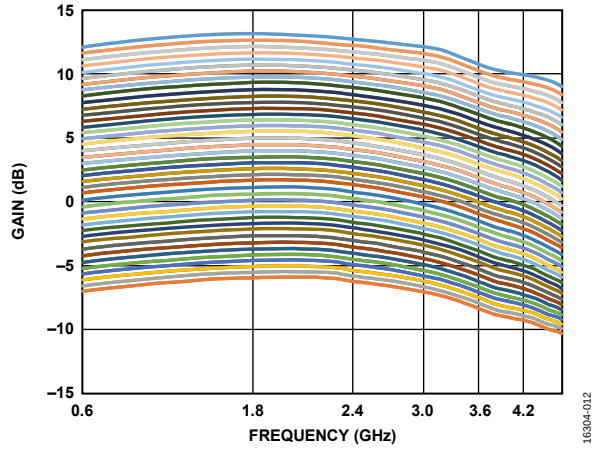


Figure 12. Gain vs. Frequency for All Gain Steps (+12 dB to −8 dB, 0.5 dB Step Size), V_{POS} = 5 V, Temperature = 25°C

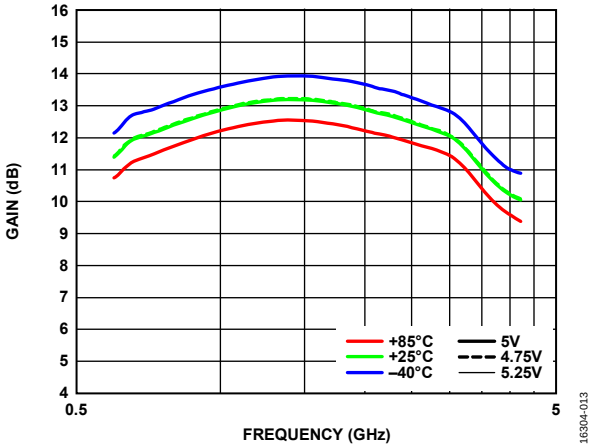


Figure 13. Gain vs. Frequency for Various Temperatures and V_{POS}

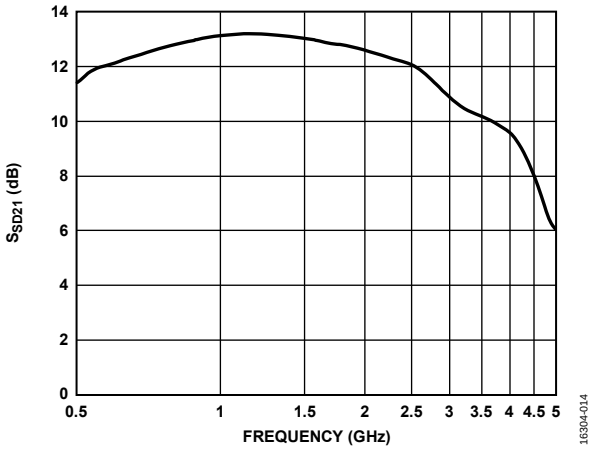


Figure 14. Forward Transmission (S_{SD21}) vs. Frequency, Gain = 12 dB

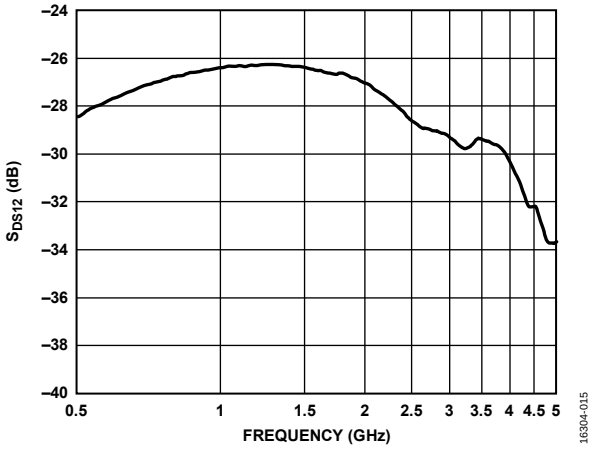


Figure 15. Reverse Transmission (S_{DS12}) vs. Frequency, Gain = 12 dB

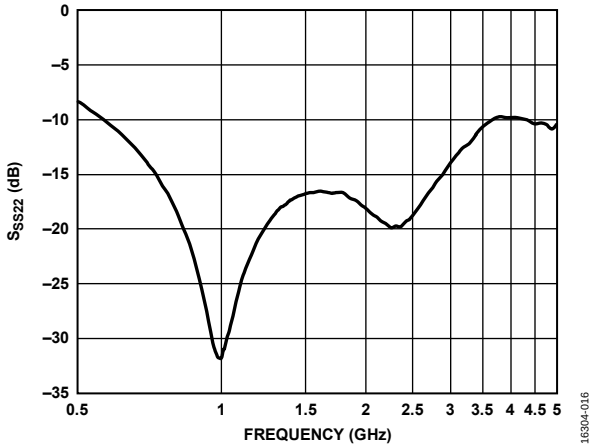


Figure 16. Output Reflection Coefficient (S_{SS22}) vs. Frequency, Gain = 12 dB

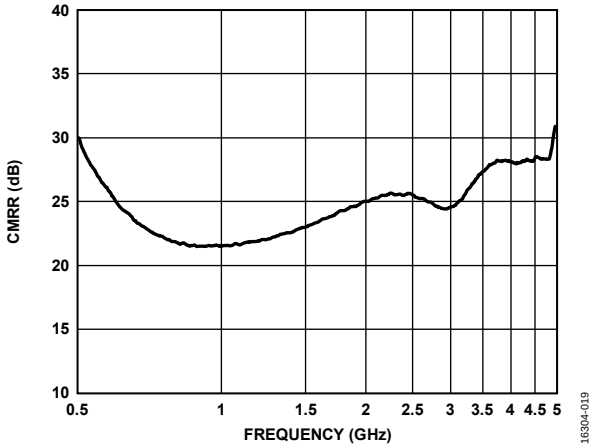


Figure 19. Common-Mode Rejection Ratio (CMRR) vs. Frequency, Gain = 12 dB

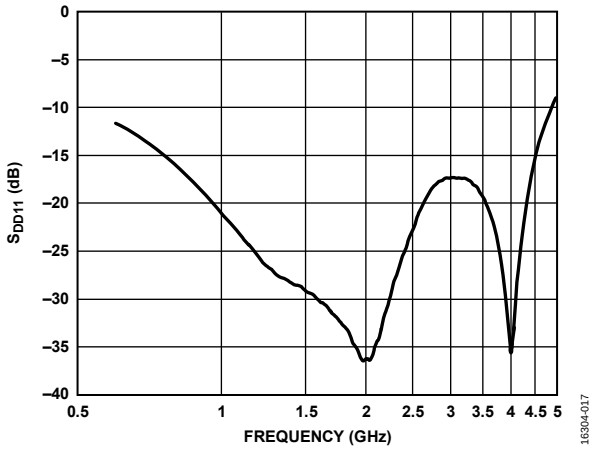


Figure 17. Input Reflection Coefficient (S_{DD11}) vs. Frequency, Gain = 12 dB

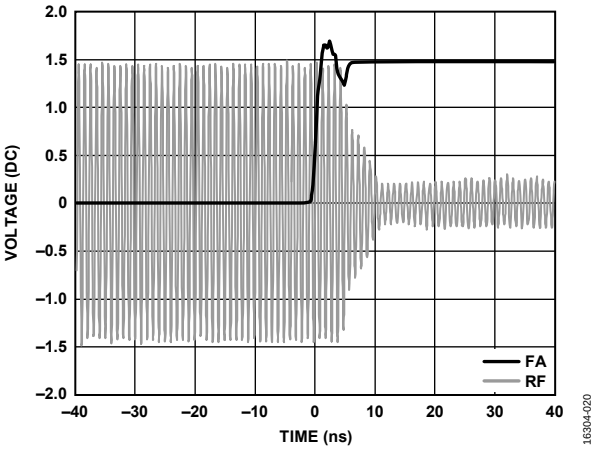


Figure 20. Fast Attack Response, On at 16 dB

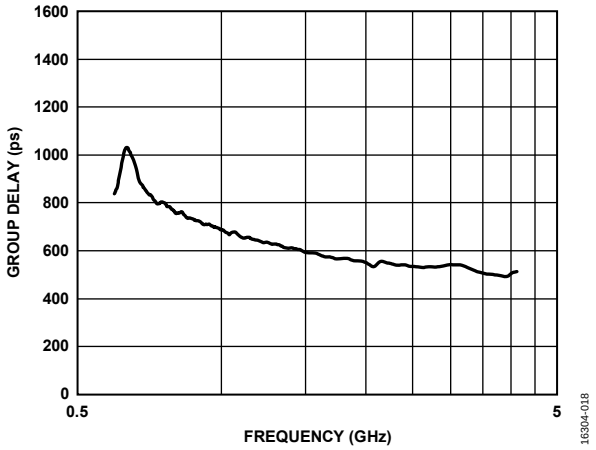


Figure 18. Group Delay vs. Frequency, Gain = 12 dB

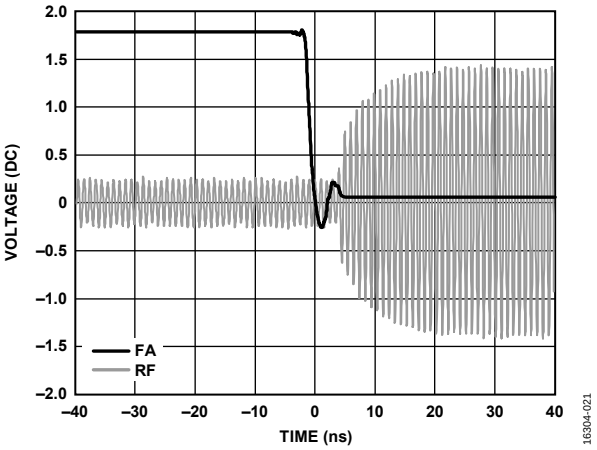


Figure 21. Fast Attack Response, Off at 16 dB

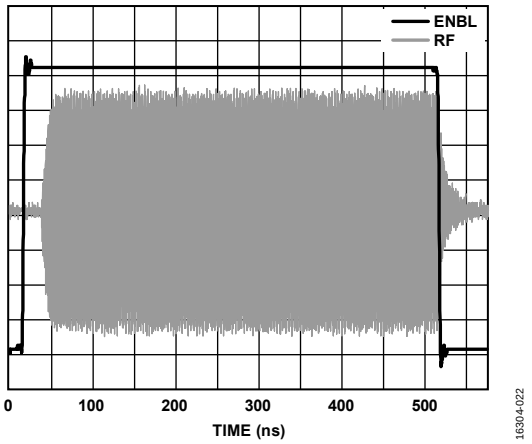


Figure 22. Enable/Disable Time Domain Response

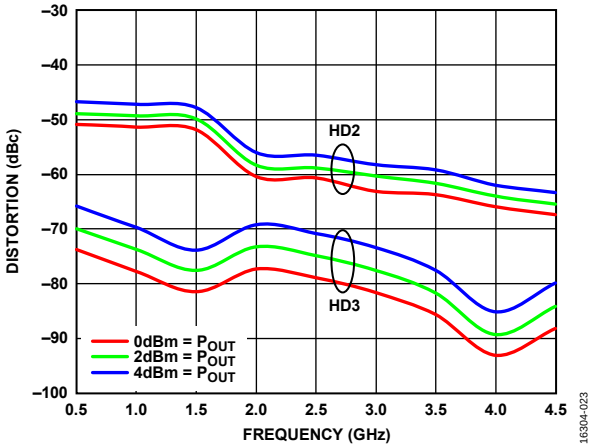


Figure 23. Distortion (HD2 and HD3) vs. Frequency for Various Output Powers (P_{OUT})

THEORY OF OPERATION

BASIC STRUCTURE

The ADL5335 is an SPI controlled DGA. An integrated, on-chip balun converts a 50 Ω differential RF input into a 50 Ω single-ended RF output. The RF inputs and the RF output utilize internal ac coupling capacitors.

The DGA core consists of a fixed gain amplifier and digitally controlled attenuator. The amplifier has a gain of 12.0 dB. The attenuator has a range of 0 dB to −8.0 dB with +0.5 dB steps and uses a thermometer coding technique to eliminate transient glitches during gain changes.

DIGITAL INTERFACE OVERVIEW

The ADL5335 digital section includes an enable pin (ENBL), a fast attack pin (FA), and a SPI.

Serial Peripheral Interface (SPI)

The SPI uses the three following pins: the serial data input/output (SDIO), the serial clock (SCLK), and the chip select bar ($\overline{CS}$).

The SPI data register consists of three bytes: one read/write bit (R/W), 15 address bits (A14 to A0), two fast attack (FA) attenuation step size bits (D7 and D6), and six gain control bits (D5 to D0), as shown in Figure 24.

The gain code and fast attack attenuation step size bits are controlled via Register Address 0x100. See Table 6 and Table 7, respectively, for their truth tables.

Table 6. Gain Code Truth Table

6-Bit Binary Gain Code, Bits[D5:D0]	Gain (dB)
000000	+12.0
000001	+11.5
000010	+11.0
000011	+10.5
000100	+10.0
000101	+9.5
000110	+9.0
000111	+8.5
001000	+8.0
001001	+7.5
001010	+7.0
001011	+6.5
001100	+6.0
001101	+5.5
001110	+5.0
001111	+4.5
010000	+4.0
010001	+3.5
010010	+3.0
010011	+2.5
010100	+2.0
010101	+1.5
010110	+1.0
010111	+0.5
011000	0
011001	−0.5
011010	−1.0
011011	−1.5
011100	−2.0
011101	−2.5
011110	−3.0
011111	−3.5
100000	−4.0
100001	−4.5
100010	−5.0
100011	−5.5
100100	−6.0
100101	−6.5
100110	−7.0
100111	−7.5
101000	−8.0
100011 to 111111	−8.0

Fast Attack (FA)

The fast attack feature allows the gain to be reduced from its present setting by a predetermined step size. Four different attenuation step sizes are available (see Table 7).

The FA pin controls fast attack mode. A logic high on the FA pin results in an attenuation that is selected by Bits[D7:D6] in the SPI register (Register Address 0x100).

Table 7. Fast Attack Attenuation Step Size Truth Table

6-Bit Binary Gain Code, Bits[D7:D6]	Step Size (dB)
00	−2
01	−4
10	−8
11	−16

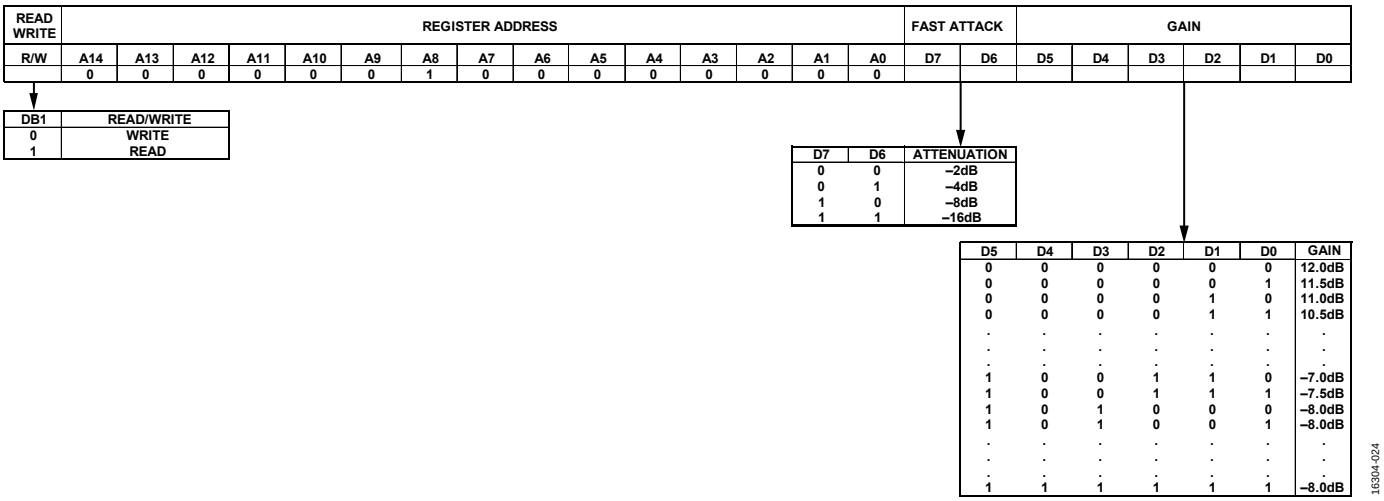


Figure 24. Gain and Fast Attack Programming via Register Address 0x100

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 25 shows the basic connections for operating the ADL5335. Apply a 5 V voltage to the supply pins (VPOS1, VPOS2, and VPOS3). Decouple each supply pin with at least one low inductance, surface-mount ceramic, 0.1 µF capacitor placed as close to the device as possible. The balanced differential inputs are decoupled using 100 pF capacitors and so is the 50 Ω load on the RF output. The serial peripheral interface pins (SCLK, SDIO, and $\overline{CS}$), fast attack (FA), and enable (ENBL) pins operate at an 1.8 V voltage. To enable the ADL5335, pull the ENBL pin high (1.8 V). A low on the ENBL pin sets the device to power-down mode, reducing the current to approximately 3.7 mA.

For additional information on device operation, see the EV-ADL5335SD1Z User Guide.

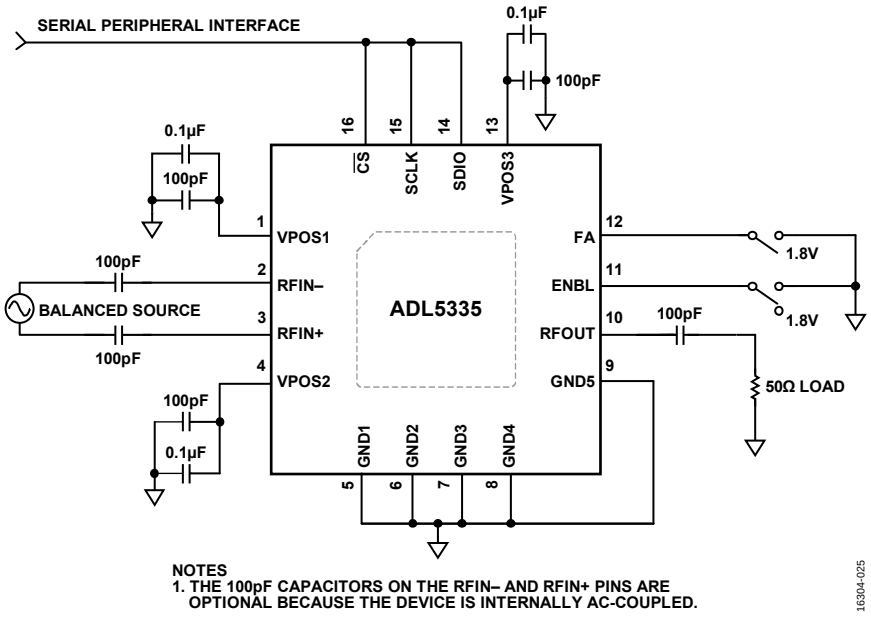
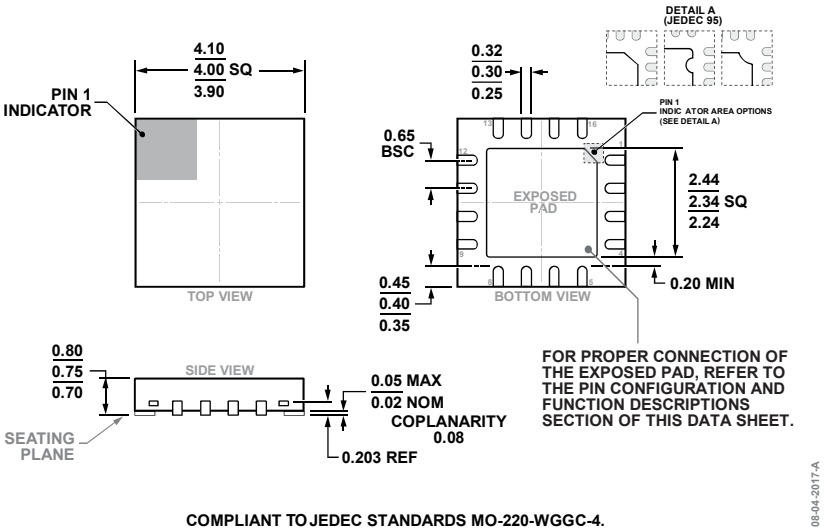


Figure 25. Basic Connections

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC-4.

Figure 26. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-39)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADL5335ACPZN	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-39
ADL5335ACPZN-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-39
EV-ADL5335SD1Z		Evaluation Board	

[1] Z = RoHS Compliant Part.