Dual 900MHz Balanced Mixer with Low Side LO Buffer, IF Amp, and RF Balun

Preliminary Technical Data

ADL5360

FEATURES

RF Frequency 700MHz to 1000MHz
IF Frequency 50MHZ to 350MHz
Power Conversion Gain of 8.5dB
SSB Noise Figure of 9.5dB
SSB NF with +10dBm blocker of 16.5dB
Input IP3 of 26dBm
Input P_{1dB} of 10 dBm
Typical LO Drive of 0 dBm
Single-ended, 50Ω RF and LO Input Ports
High Isolation SPDT LO Input Switch
Single Supply Operation: 3.3 to 5 V
Exposed Paddle 6 x 6 mm, 36 Lead LFCSP Package

APPLICATIONS

Cellular Base Station Receivers
Main and Diversity Receiver Designs
Radio Link Downconverters

GENERAL DESCRIPTION

The ADL5360 utilizes two highly linear doubly balanced passive mixer cores along with integrated RF and LO balancing circuitry to enable single-ended operation. The ADL5360 incorporates two RF baluns allowing for optimal main and diversity mixer performance over a 700 to 1000 MHz RF input frequency range using low-side LO injection. The balanced passive mixer arrangement provides good LO to RF leakage, typically better than -25dBm, and excellent intermodulation performance. The balanced mixer cores also provide extremely high input linearity allowing the device to be used in demanding cellular applications where in-band blocking signals may otherwise result in the degradation of dynamic performance. High linearity IF buffer amps follow the passive mixer cores, to yield a typical power conversion gain of 9.5dB. (For a higher IIP3 version of the dual mixer without the IF amplifiers, please contact the factory).

The ADL5360 provides two switched LO paths that can be utilized in TDD applications where it is desirable to rapidly alternate between two local oscillators. LO current can be externally set using a resistor to minimize DC current

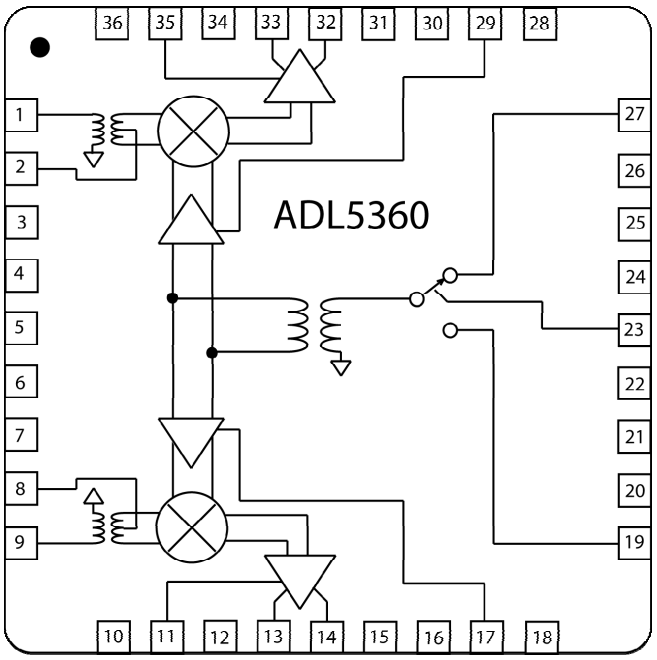

Figure 1. Functional Block Diagram

commensurate with the desired level of performance. An additional 3V logic pin is provided to power down (<100uA) the circuit when desired.

For low voltage applications, the ADL5360 is capable of operation at voltages down to 3V with substantially reduced DC current.

The ADL5360 is fabricated using a BiCMOS high performance IC process. The device is available in a 6mm x 6mm 36-lead LFCSP package and operates over a −40°C to +85°C temperature range. An evaluation board is also available.

REV. PrA

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ADL5360—Specifications at V_S=5V

Table 1. V_S = 5 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = 703 MHz, LO power = 0 dBm, Zo = 50Ω, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
RF INPUT INTERFACE					
Return Loss	Tunable to >20dB over a limited bandwidth		12		dB
Input Impedance			50		Ω
RF Frequency Range		700		1000	MHz
OUTPUT INTERFACE					
Output Impedance	Differential impedance, f = 200 MHz		200		Ω
IF Frequency Range		40		450	MHz
DC Bias Voltage[1]	Externally generated	4.75	V_S	5.25	V
LO INTERFACE					
LO Power		-6	0	+10	dBm
Return Loss	Tunable to >20dB over a limited bandwidth		12		dB
Input Impedance			50		Ω
LO Frequency Range	Low Side LO injection	250		960	MHz
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		8.5		dB
Voltage Conversion Gain	Z_{SOURCE} = 50Ω, Differential Z_{LOAD} = 200Ω Differential		15		dB
SSB Noise Figure	Including 4:1 IF port transformer and PCB loss		9.2		dB
SSB Noise Figure Under-Blocking	8dBm Blocker present +/-10MHz from wanted RF input, LO source filtered		18		dB
Input Third Order Intercept	f_{RF1} = 899.5 MHz, f_{RF2} = 900.5 MHz, f_{LO} = 703 MHz, each RF tone at -10 dBm		26		dBm
Input Second Order Intercept	f_{RF1} = 899.5 MHz, f_{RF2} = 900.5 MHz, f_{LO} = 703 MHz, each RF tone at -10 dBm		55		dBm
Input 1 dB Compression Point			11		dBm
LO to IF Output Leakage	Unfiltered IF Output, Improves substantially with external filter components.		-20		dBm
LO to RF Input Leakage			-33		dBm
RF to IF Output Isolation	Unfiltered IF Output, Improves substantially with external filter components.		33		dBc
RFI1 to RFI2 Channel Isolation			50		
IF/2 Spurious	-10 dBm Input Power		-65		dBc
IF/3 Spurious	-10 dBm Input Power		-74		dBc
POWER INTERFACE					
Supply Voltage			5		V
Quiescent Current	Resistor Programmable		380		mA

[1] Supply voltage must be applied from external circuit through external inductors.

ADL5360—Specifications at VS=3.3v

Table 2. V_S = 3.3 V, T_A = 25°C, f_{RF} = 900 MHz, f_{LO} = 703 MHz, LO power = 0 dBm, Zo = 50Ω, unless otherwise noted

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Power Conversion Gain	Including 4:1 IF port transformer and PCB loss		9.5		dB
Voltage Conversion Gain	Z_{SOURCE} = 50Ω, Differential Z_{LOAD} = 200Ω Differential		16		dB
SSB Noise Figure	Including 4:1 IF port transformer and PCB loss		8.6		dB
Input Third Order Intercept	f_{RF1} = 899.5 MHz, f_{RF2} = 900.5 MHz, f_{LO} = 703 MHz, each RF tone at -10 dBm		19		dBm
Input Second Order Intercept	f_{RF1} = 899.5 MHz, f_{RF2} = 900.5 MHz, f_{LO} = 703 MHz, each RF tone at -10 dBm		50		dBm
Input 1 dB Compression Point			6		dBm
POWER INTERFACE					
Supply Voltage		3.0	3.3	3.6	V
Quiescent Current	Resistor Programmable		265		mA

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_{POS}	5.5 V
PWDN, LOSW, VGS0, VGS1, VGS2	3.3 V
RF Input Power, DVIN, MNIN	TBD
Internal Power Dissipation	TBD
θ_{JA} (Exposed Paddle Soldered Down)	TBD
θ_{JC} (At Exposed Paddle)	TBD
Maximum Junction Temperature	TBD
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

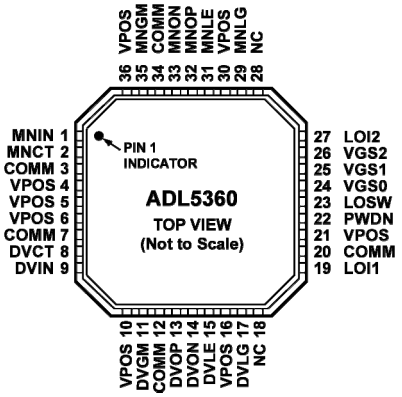

Figure 2. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Function
1	MNIN	RF Input for Main Channel. Internally matched to 50Ω. Must be ac-coupled.
2	MNCT	Center Tap for Main Channel Input Balun. Should be bypassed to ground using low inductance capacitor.
3, 5, 7, 12, 20, 34	COMM	Device Common (DC Ground).
4,, 6, 10, 16, 21, 30, 36	VPOS	Positive Supply Voltage.
8	DVCT	Center Tap for Diversity Channel Input Balun. Should be bypassed to ground using low inductance capacitor.
9	DVIN	RF Input for Diversity Channel. Internally matched to 50Ω. Must be ac-coupled.
11	DVGM	Diverstiy Amplifier Bias Setting. Connect 1.2kΩ resistor to ground for typical operation.
13, 14	DVOP, DVON	Diversity Channel Differential Open-Collector Outputs. DVOP and DVON should be pulled-up to VCC using pull-up choke inductors.
15	DVLE	Diversity Channel External Inductor. Connect 10nH inductor to ground for typical operation.
17	DVLG	Diverstiy Channel LO Buffer Bias Setting. Connect 390Ω resistor to ground for typical operation.
18, 28	NC	No Connect.
19,	L0I1	Local Oscillator Input 1. Internally matched to 50Ω. Must be ac-coupled.
22	PWDN	Connect to Ground for Normal Operation. Connect pin to 3.3V for disable mode.
23	LOSW	Local Oscillator Input Selection Switch. Set LOSW high to select LOI1, and set low to select LOI2.
24, 25, 26	VGS0, VGS1, VGS2	Gate to Source Control Voltages. For typical operation set VGS2 high and VGS0 and VGS1 to low logic level.
27	LOI2	Local Oscillator Input 2. Internally matched to 50Ω. Must be ac-coupled.
29	MNLG	Main Channel LO Buffer Bias Setting. Connect 390Ω resistor to ground for typical operation.
31	MNLE	Main Channel External Inductor. Connect 10nH inductor to ground for typical operation.
32, 33	MNOP, MNON	Main Channel Differential Open-Collector Outputs. MNOP and MNON should be pulled-up to VCC using pull-up choke inductors.
35	MNGM	Main Amplifier Bias Setting. Connect 1.2kΩ resistor to ground for typical operation.

TYPICAL PERFORMANCE CHARACTERISTICS–PRELIMINARY DATA

V_S = 5 V, T_A = 25°C, as measured using typical circuit schematic with low-side LO unless otherwise noted.

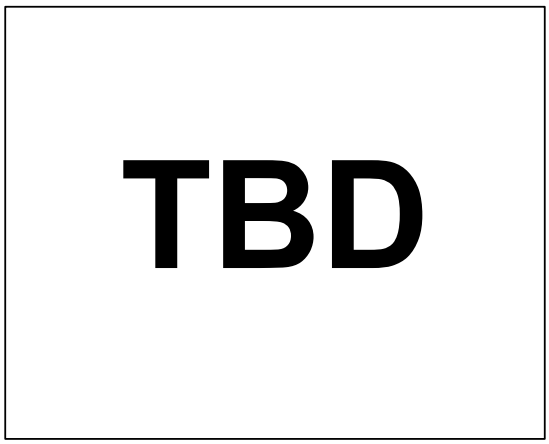

Figure 3. Conversion Gain versus RF Frequency

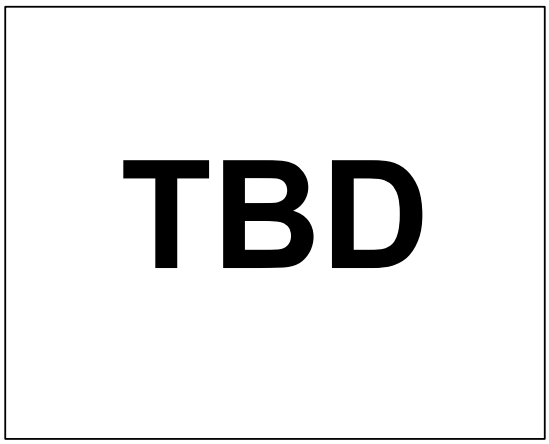

Figure 6. Single-Sideband NF versus RF Frequency

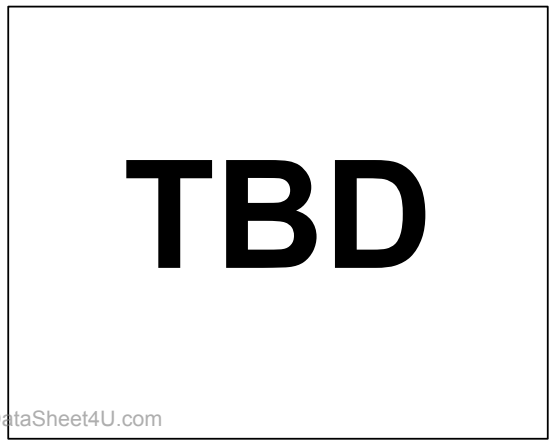

Figure 4. IIP3 versus RF Frequency

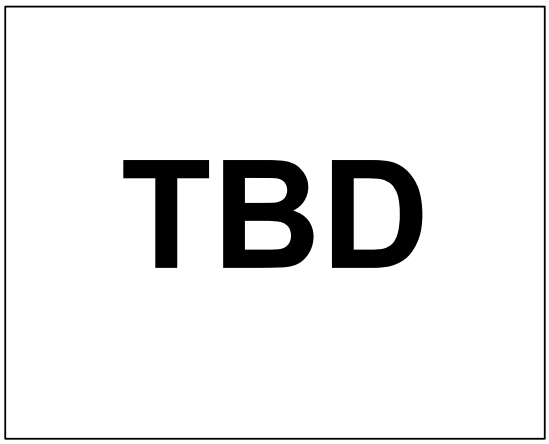

Figure 7. Single-Sideband NF versus Blocker Level at 1900MHz

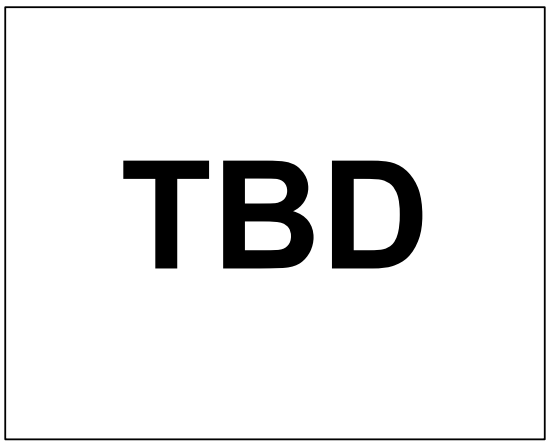

Figure 5. IP1dB versus RF Frequency

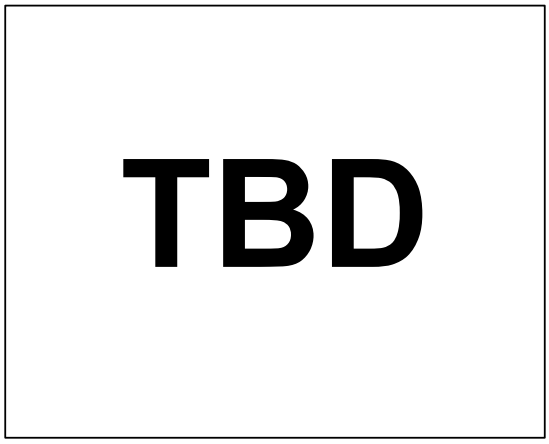

Figure 8. LO to RF Leakage versus LO Frequency

EVALUATION BOARD SCHEMATIC

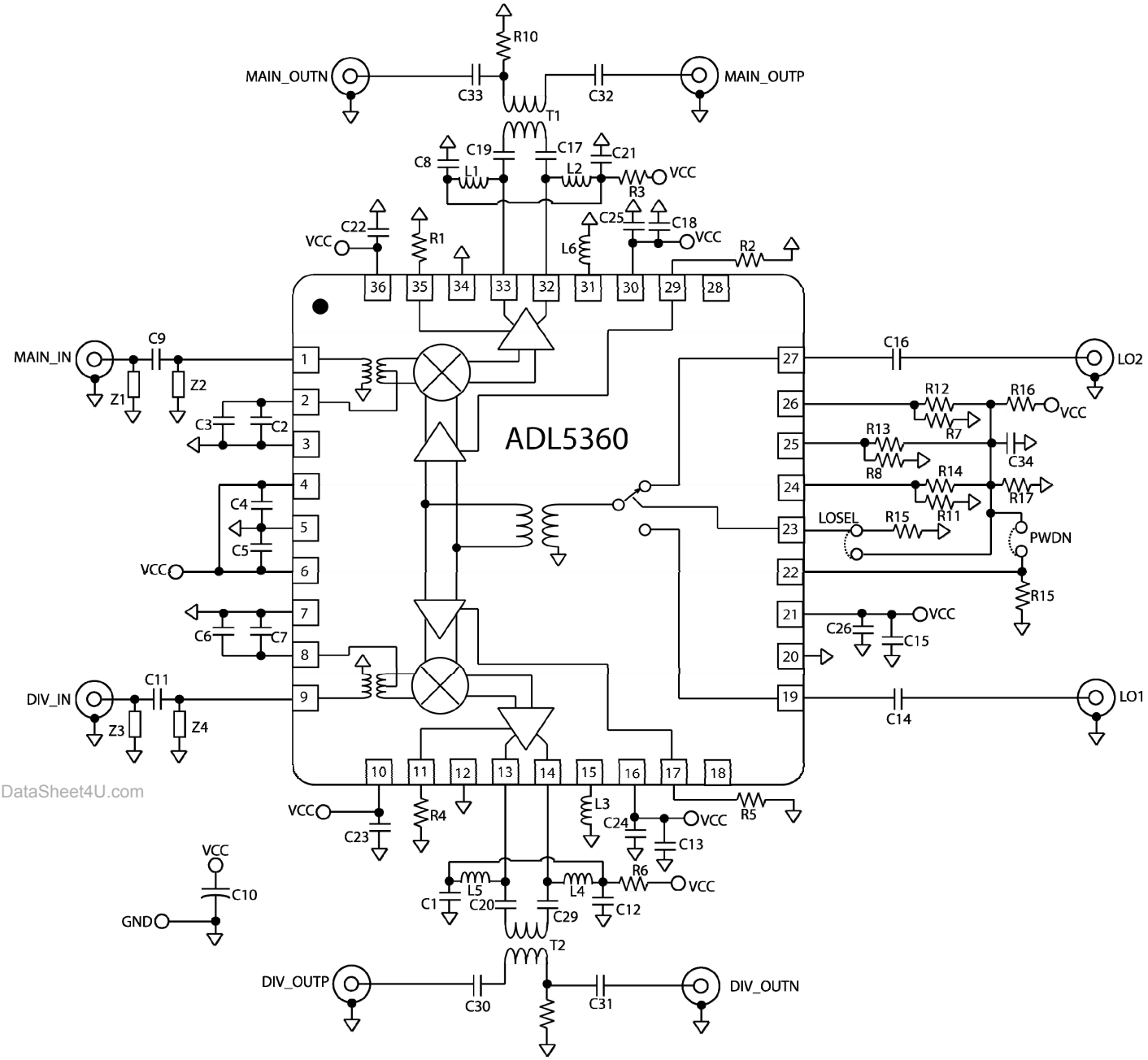

Figure 9. Evaluation Board Schematic.

Table 3. Eval Board Configuration

Components	Function	Default Conditions
C1, C4, C5, C8, C10, C12, C13, C15, C18, C21, C22, C23, C24, C25, C26	Power Supply Decoupling. Nominal supply decoupling consists a 0.01 µF capacitor to ground in parallel with 10pF capacitors to ground positioned as close to the device as possible.	C10 = 4.7 µF (size 3216) C1, C8, C12, C21 = 150pF (size 0402) C4, C5, C22, C23, C24, C25, C26 = 10pF (size 0402) C13, C15, C18 = 0.1 µ (size 0402)
Z1-Z4, C2, C3, C6, C7, C9, C22	RF Main and Diversity Input Interface. Main and Diversity input channels are ac-coupled through C9 and C22. Z1-Z4 provides additional component placement for external matching/filter networks. C2, C3, C6, and C7 provide bypassing for the center taps of the main and diversity on-chip input baluns.	C2, C7 = 10pF (size 0402) C3, C6 = 0.01 µF (size 0402) C9, C22 = 22pF (size 0402) Z1-Z4 = open (size 0402)
T1, T2, C17, C19, C20, C27, C28, C29, C30, C31, C32, C33, L1, L2, L4, L5, R3, R6, R9, R10	IF Main and Diversity Output Interface. The open collector IF output interfaces are biased through pull-up choke inductors L1, L2, L4, and L5, with R3 and R6 available for additional supply bypassing. T1 and T2 are 4:1 impedance transformers used to provide a single ended IF output interface, with C27 and C28 providing center-tap bypassing. C17, C19, C20, C29, C30, C31, C32, and C33 ensure an ac-coupled output interface. R9 and R10 should be removed for balanced output operation.	C17, C19, C20, C29-C33 = 0.001 µF (size 0402) C27, C28 = 150pF (size 0402) T1, T2 = TC4-1T+ (MiniCircuits) L1, L2, L4, L5 = 330 nH (size 0805) R3, R6, R9, R10 = 0 Ω (size 0402)
C14, C16, R15, LOSEL	LO Interface. C14 and C16 provide ac-coupling for the LOI1 and LOI2 local oscillator inputs. LOSEL selects the appropriate LO input for both mixer cores. R15 provides a pull-down to ensure LOI2 is enabled when the LOSEL jumper is removed. Jumper can be removed to allow LOSEL interface to be excercised using external logic generator.	C14, C16 = 10pF (size 0402) R15 = 10kΩ (size 0402) LOSEL = 2-pin shunt
R19, PWDN	PWDN Interface. When the PWDN 2-pin shunt is inserted the ADL5356 is powered down. When open R19 pulls the PWDN logic low and enables the device. Jumper can be removed to allow PWDN interface to be excercised using external logic generator. It is permissible to ground the pwrdn pin for nominal operation.	R19 = 10kΩ (size 0402) PWDN = 2-pin shunt
R1, R2, R4, R5,L3, L6, R7, R8, R11, R12, R13, R14, R16, R17, C34	Bias Control. R16 and R17 form a voltage divider to provide a 3V for logic control, bypassed to ground through C34. R7, R8, R11, R12, R13, and R14 provide resistor programmability of VGS0, VGS1 and VGS2. Typically these nodes can be hard-wired for nominal operation. It is permissible to ground these pins for nominal operation. R2 and R5 set the bias point for the internal LO buffers. R1 and R4 set the bias point for the internal IF amplifiers. L3 and L6 are external inductors used to improve isolation and common mode rejection.	R1, R4 = 1.2kΩ (size 0402) R2, R5 = 390Ω (size 0402) L3, L6 = 10nH (size 0603) R7, R13, R14 = open (size 0402) R8, R11, R12 = 0Ω (size 0402) R16 = 10kΩ (size 0402) R17 = 15kΩ (size 0402) C34 = 1nF (size 0402)

OUTLINE DIMENSIONS

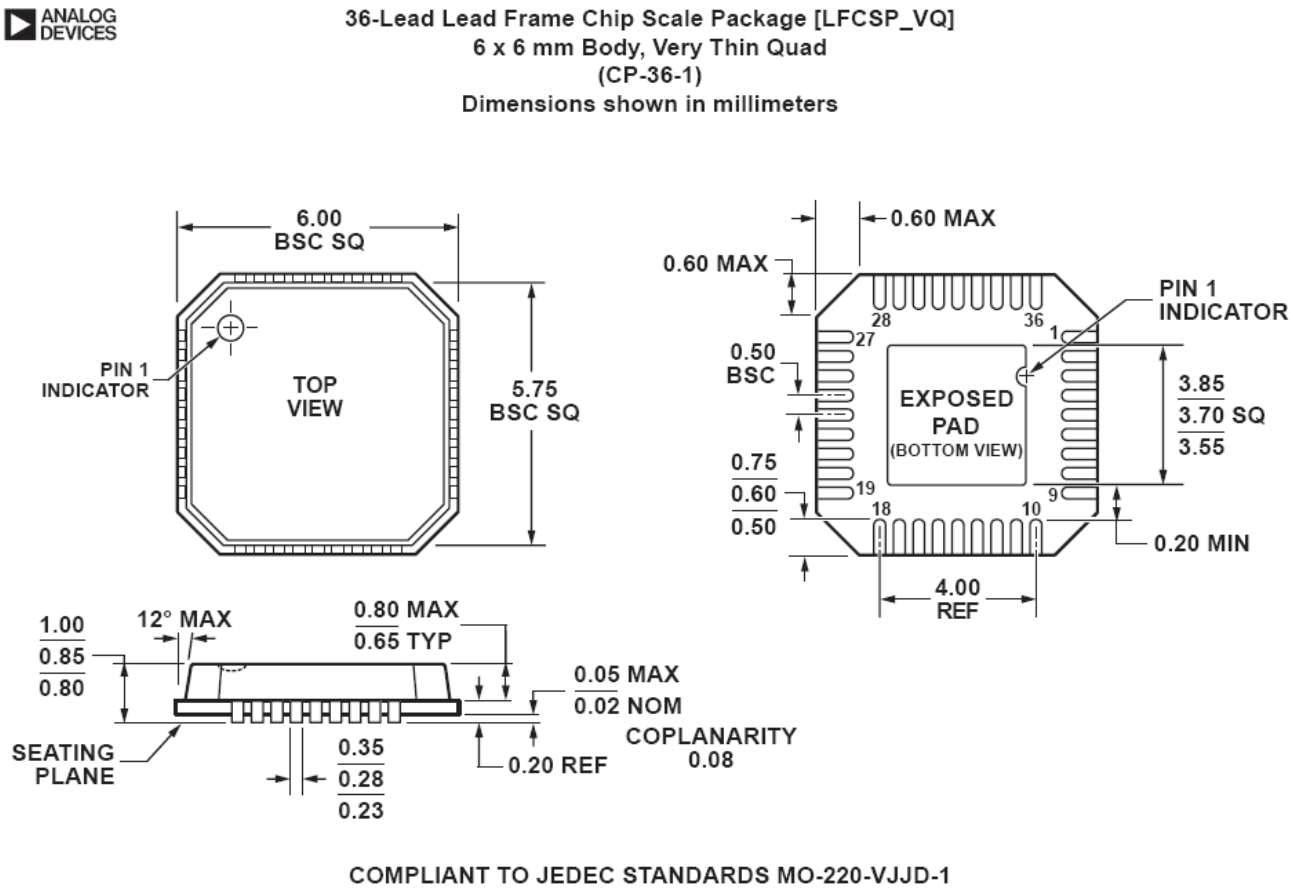

Figure 10. 36-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
6mm × 6 mm Body, Very Thin Quad (CP-36-1))
Dimensions shown in millimeters

ORDERING GUIDE

Models	Temperature Range	Package Description	Package Option	Branding	Transport Media Quantity
ADL5360XCPZ-R7	–40°C to +85°C	36-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-36-1	TBD	TBD, Reel
ADL5360XCPZ-WP	–40°C to +85°C	36-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-36-1	TBD	TBD, Waffle Pack
ADL5360-EVALZ		Evaluation Board			1