6.5 GHz, Ultrahigh Dynamic Range, Differential Amplifier

Data Sheet **ADL5569**

FEATURES

- –3 dB bandwidth: 6.5 GHz typical
- Preset 20 dB voltage gain, can be reduced by adding external resistors
- Differential or single-ended input to differential output
- Internally dc-coupled inputs and outputs
- Low noise input stage: 9.3 dB noise figure at 2 GHz
- Low distortion at 5 V supply and 2 V p-p output with 100 Ω load
  - 500 MHz: –78 dBc (HD2), –71 dBc (HD3), –80 dBc (IMD3)
  - 2 GHz: –64 dBc (HD2), –52 dBc (HD3), –65 dBc (IMD3)
- Input voltage noise (NSD, RTI): 1.0 nV/√Hz at 100 MHz
- Single-supply operation: ac-coupled applications
- Dual-supply operation: dc-coupled applications
- Slew rate: 24 V/ns at 2 V p-p output
- DC power consumption: 86 mA per amplifier at 5 V

APPLICATIONS

- Differential ADC drivers for GSPS ADCs
- High speed data acquisition
- Single-ended to differential conversion
- DAC buffering
- DC coupling and level shifting
- RF/IF gain blocks
- Balun alternative from dc to 4 GHz
- SAW filter interfacing

FUNCTIONAL BLOCK DIAGRAM

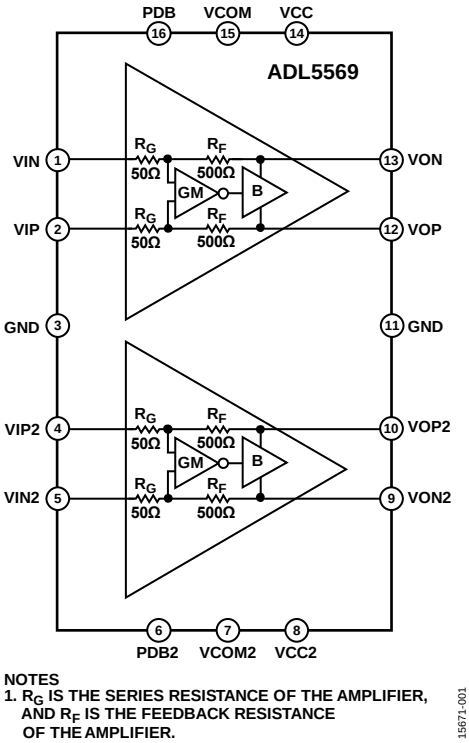

Figure 1.

GENERAL DESCRIPTION

The ADL5569 is a high performance, dual, differential amplifier with 20 dB of voltage gain, optimized for applications spanning from dc to 6.5 GHz. The amplifier is available in a dual format, and it offers a low referred to input (RTI) noise spectral density (NSD) of 1.0 nV/√Hz (at 100 MHz) and excellent distortion performance over a wide frequency range, making it an ideal driver for high speed 12-bit to 16-bit analog-to-digital converters (ADCs). The ADL5569 is ideally suited for use in high performance zero intermediate frequency (IF) and complex IF receiver designs. In addition, this device has excellent low distortion for single-ended input driver applications.

Using two external series resistors for each amplifier expands the gain flexibility of the amplifier and allows any gain selection from 6 dB to 20 dB for a differential input. For a single-ended input, the gain can be adjusted from 6 dB to 17 dB with the addition of some external resistors. This device maintains low distortion through its output common-mode range of 2.0 V to 3.0 V, providing a flexible capability for driving ADCs with ac levels up to 2 V p-p.

Operating from a single 5 V supply, the quiescent current of the ADL5569 is typically 86 mA per amplifier. When disabled, the amplifiers consume only 8 mA per amplifier.

The device is optimized for wideband, low distortion, and low noise operation, giving it unprecedented second harmonic distortion (HD2) and third harmonic distortion (HD3) from dc to 4 GHz. These attributes, together with its adjustable gain capability, make this device the amplifier of choice for driving a wide variety of ADCs, mixers, pin diode attenuators, surface acoustic wave (SAW) filters, and a multitude of discrete radio frequency (RF) devices.

Fabricated on an Analog Devices, Inc., high speed silicon germanium (SiGe) process, the ADL5569 is supplied in a compact 2.5 mm × 3 mm, 16-lead LFCSP package and operates over the –40°C to +85°C temperature range.

Rev. C Document Feedback

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7/2018—Rev. 0 to Rev. A

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Changes to Figure 10, Figure 11, Figure 12, and Figure 13 ... 9
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5/2018—Revision 0: Initial Version

SPECIFICATIONS

Supply voltage (V_S) = 5 V, maximum gain, output common-mode voltage (V_{COM}) = V_S/2, source impedance (R_S) = 100 Ω differential, load impedance (R_L) = 100 Ω differential, output voltage (V_{OUT}) = 2 V p-p composite, frequency = 500 MHz, T_A = 25°C, parameters specified for differential input and differential output, and signal spacing = 2 MHz for two tone measurements, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth[1]	V_{OUT} ≤ 0.5 V p-p		6.5		GHz
Bandwidth, 1.0 dB Flatness	V_{OUT} ≤ 1.0 V p-p		4.8		GHz
Voltage Gain (A_V)					
Differential Input	R_L = open		20		dB
	R_L = 100 Ω differential	6	19		dB
Single-Ended Input	R_L = 100 Ω differential	6	17		dB
Gain Accuracy			±0.15		dB
Gain Supply Sensitivity	V_S ± 5%		8.6		mdB/V
Gain Temperature Sensitivity	T_A = −40°C to +85°C		4		mdB/°C
Slew Rate	Rising, V_{OUT} = 2 V p-p step		24		V/ns
	Falling, V_{OUT} = 2 V p-p step		24		V/ns
Settling Time	2 V step to 1%		500		ps
Overdrive Recovery Time	Differential input voltage step from 2 V to 0 V for V_{OUT} ≤ ±20 mV		6		ns
Reverse Isolation (SDD12)	PDB and PDB2 are high		−34		dB
When Amplifier Disabled	PDB and PDB2 are low		−17.5		dB
INPUT AND OUTPUT CHARACTERISTICS					
Input Common-Mode Range		1.3		3.5	V
Input Resistance					
Differential			100		Ω
Single-Ended			91.7		Ω
Common-Mode Rejection Ratio (CMRR)			47		dB
Output Common-Mode Range	VCOM and VCOM2	2.0		3.0	V
VCOM and VCOM2 Input Impedance			2.5		kΩ
Output, Common Mode	Referenced to V_{COM} (V_S/2)				
Offset		−30	±10	+30	mV
Drift	T_A = −40°C to +85°C		0.15		mV/°C
Output, Differential Offset					
Voltage		−10	±1.5	+10	mV
Drift	T_A = −40°C to +85°C		±6		µV/°C
Output Resistance (Differential)			14.0		Ω
Maximum Output Voltage Swing	1 dB compression point		6.5		V p-p
POWER INTERFACE					
Supply Voltage		4.75	5	5.25	V
Digital Input Voltage	PDB, PDB2				
Logic High (V_{IH})		2.1		3.45	V
Logic Low (V_{IL})		0		1.0	V
PDB Input Current	PDB = 3 V		−7		µA
	PDB = 0 V		−70		µA
Supply Current (I_{SUPPLY})	Each amplifier				
Quiescent, Each Amplifier	PDB is high		86		mA
Disabled (Powered Down), Each Amplifier	PDB is low		8		mA

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE/HARMONIC PERFORMANCE					
100 MHz					
Second Harmonic Distortion (HD2)			−89		dBc
Third Harmonic Distortion (HD3)			−83		dBc
Output Third-Order Intercept (OIP3)			42		dBm
Third-Order Intermodulation Distortion (IMD3)			−82		dBc
Output Second-Order Intercept (OIP2)			74		dBm
Second-Order Intermodulation Distortion (IMD2)			−73		dBc
Output 1 dB Compression Point (OP1dB)			17.4		dBm
Noise Figure[2]			5.4		dB
Noise Spectral Density (NSD), RTI[2]			1.0		nV/√Hz
500 MHz					
HD2			−78		dBc
HD3			−71		dBc
OIP3			41		dBm
IMD3			−80		dBc
OIP2			74		dBm
IMD2			−73		dBc
OP1dB			17.2		dBm
NF[2]			6.3		dB
NSD, RTI[2]			1.2		nV/√Hz
1000 MHz					
HD2			−65		dBc
HD3			−58		dBc
OIP3			39		dBm
IMD3			−76		dBc
OIP2			71		dBm
IMD2			−70		dBc
OP1dB			17.7		dBm
NF[2]			7.0		dB
NSD, RTI[2]			1.3		nV/√Hz
2000 MHz					
HD2			−64		dBc
HD3			−52		dBc
OIP3			34		dBm
IMD3			−65		dBc
OIP2			63		dBm
IMD2			−62		dBc
OP1dB			17.4		dBm
NF[2]			9.3		dB
NSD, RTI[2]			1.8		nV/√Hz
3000 MHz					
HD2			−62		dBc
HD3			−46		dBc
OIP3			30		dBm
IMD3			−58		dBc
OIP2			57		dBm
IMD2			−56		dBc
OP1dB			16.2		dBm
NF[2]			11.1		dB
NSD, RTI[2]			2.2		nV/√Hz

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
4000 MHz					
HD2			−58		dBc
HD3			−48		dBc
OIP3			25		dBm
IMD3			−48		dBc
OIP2			59		dBm
IMD2			−58		dBc
OP1dB			14.3		dBm
NF[2]			12.1		dB
NSD, RTI[2]			2.5		nV/√Hz

[1] S parameters are taken with the device under test (DUT) itself. The printed circuit board (PCB) is not used in the measurement.
[2] NSD RTI is calculated from the noise figure, as follows:

$$NSD\ (RTI) = ½ \times \sqrt{4kT \times (10^{NF/10} - 1) \times R_{IN}}$$

where:
k is Boltzmann's constant, which equals 1.381×10^{-23} J/K.
T is the standard absolute temperature for evaluating noise figure, which equals 290 K.
R_{IN} is the differential input impedance of each amplifier, which equals 100 Ω.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Output Voltage Swing × Bandwidth Product	5 V-GHz
Supply Voltage (V_S) at VCC and VCC2	5.25 V
VIP, VIP2, VIN, and VIN2	V_S + 0.5 V
PDB, PDB2	3.6 V
Maximum Output Current, I_{OUT} (VIP, VIP2, VIN, and VIN2 Pins)	±30 mA
Internal Power Dissipation	1 W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-16-44	90.5	20.9	°C/W

[1] Measured on an Analog Devices evaluation board.
[2] Based on simulation with JEDEC standard JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

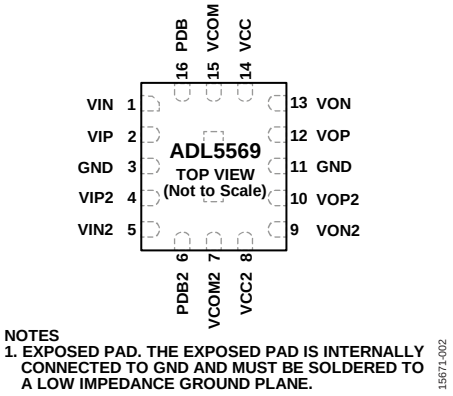

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIN	Negative Side of Balanced Differential Inputs for Amplifier 1. This pin is biased to the VCC voltage (V_{VCC})/2, and is typically ac-coupled.
2	VIP	Positive Side of Balanced Differential Inputs for Amplifier 1. This pin is biased to V_{VCC}/2, and is typically ac-coupled.
3, 11	GND	Ground. Ground reference for the entire chip. These pins must be soldered to a low impedance ground plane.
4	VIP2	Positive Side of Balanced Differential Inputs for Amplifier 2. This pin is biased to the VCC2 voltage (V_{VCC2})/2 and is typically ac-coupled.
5	VIN2	Negative Side of Balanced Differential Inputs for Amplifier 2. This pin is biased to V_{VCC2}/2 and is typically ac-coupled.
6	PDB2	Power-Down Control (Active Low) for Amplifier 2. This pin is internally pulled up to approximately 2.8 V. A logic high on this pin (2.1 V < PDB2 voltage (V_{PDB2}) < 3.3 V) enables the device.
7	VCOM2	Common-Mode Voltage Input for Amplifier 2. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of the amplifier. If left open, the VCOM2 voltage (V_{VCOM2}) = V_{CC2}/2. Decouple this pin to ground with a 0.1 µF capacitor.
8	VCC2	Positive Supply for Amplifier 2.
9	VON2	Negative Side of Balanced Differential Outputs for Amplifier 2. This pin is biased to V_{VCOM2} and is typically ac-coupled.
10	VOP2	Positive Side of Balanced Differential Outputs for Amplifier 2. This pin is biased to V_{VCOM2} and is typically ac-coupled.
12	VOP	Positive Side of Balanced Differential Outputs for Amplifier 1. This pin is biased to V_{VCOM} and is typically ac-coupled.
13	VON	Negative Side of Balanced Differential Outputs for Amplifier 1. This pin is biased to V_{VCOM} and is typically ac-coupled.
14	VCC	Positive Supply for the Amplifier 1.
15	VCOM	Common-Mode Voltage Input for Amplifier 1. A voltage applied to this pin sets the common-mode voltage of the inputs and outputs of the amplifier. If left open, V_{VCOM} = V_{VCC}/2. Decouple this pin to ground with a 0.1 µF capacitor.
16	PDB	Power-Down Control (Active Low) for Amplifier 1. This pin is internally pulled up to approximately 2.8 V. A logic high on this pin (2.1 V < PDB voltage (V_{PDB}) < 3.3 V) enables the device.
	EPAD	Exposed Pad. The exposed pad is internally connected to GND and must be soldered to a low impedance ground plane.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = 5 V, maximum gain, V_{COM} = V_S/2, R_S = 100 Ω differential, R_L = 100 Ω differential, V_{OUT} = 2 V p-p, frequency = 500 MHz, T_A = 25°C, parameters specified for differential input and differential output, and signal spacing = 2 MHz for two-tone measurements, unless otherwise noted.

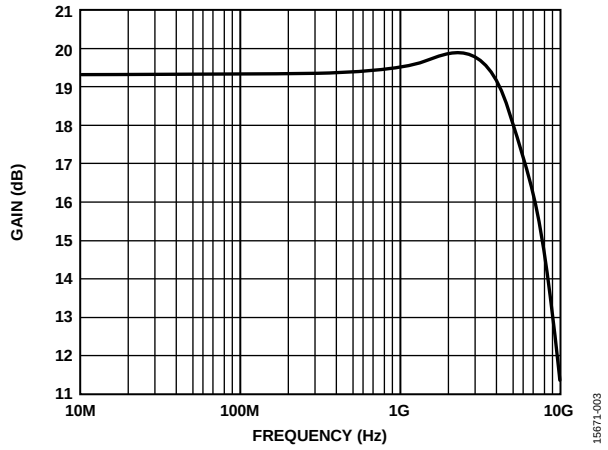

Figure 3. Gain vs. Frequency (S Parameters Taken with DUT, PCB Not Used in Measurement)

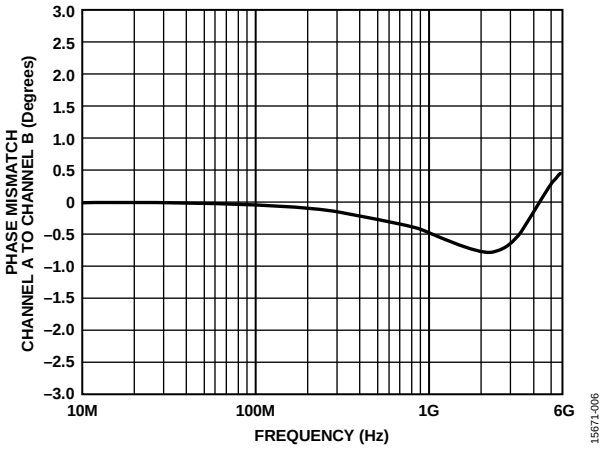

Figure 6. Phase Mismatch (Channel A to Channel B) vs. Frequency

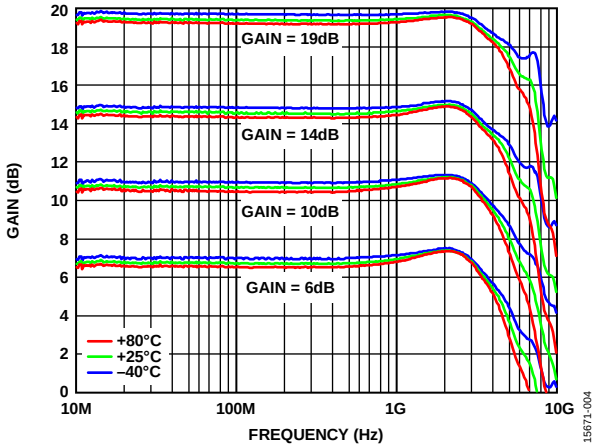

Figure 4. Gain vs. Frequency over Temperature

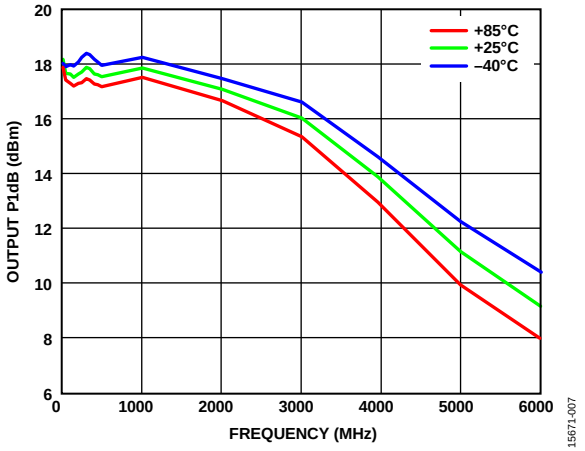

Figure 7. Output P1dB vs. Frequency over Temperature

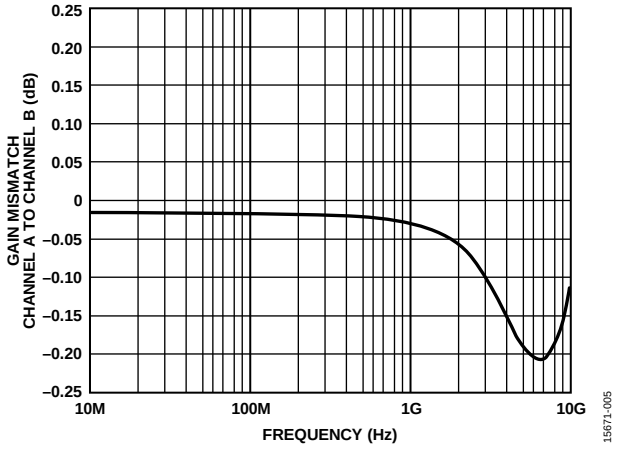

Figure 5. Gain Mismatch (Channel A to Channel B) vs. Frequency

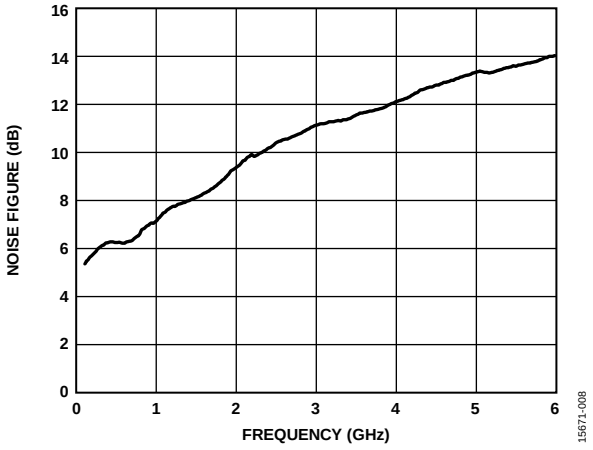

Figure 8. Noise Figure vs. Frequency

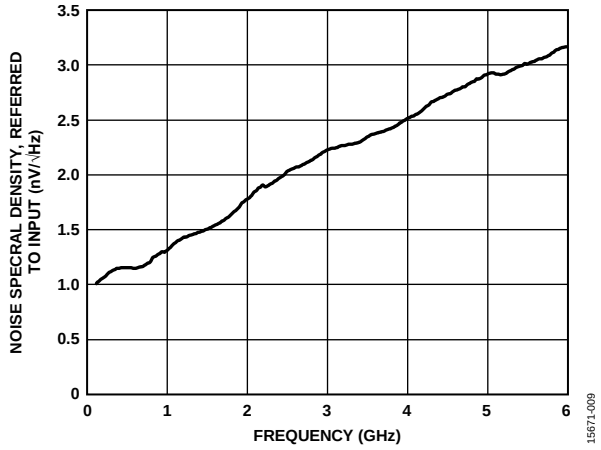

Figure 9. Noise Spectral Density, Referred to Input vs. Frequency

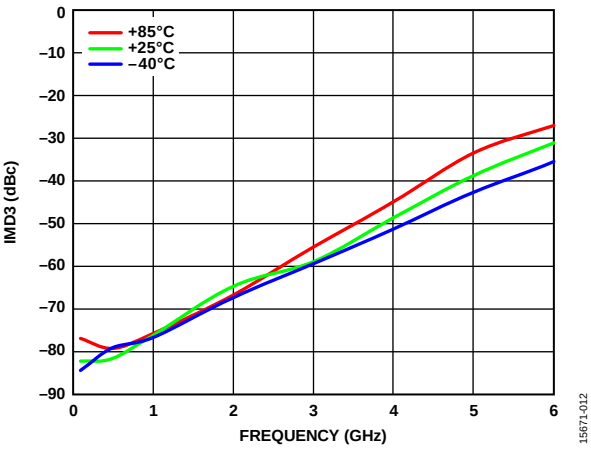

Figure 12. IMD3 vs. Frequency over Temperature

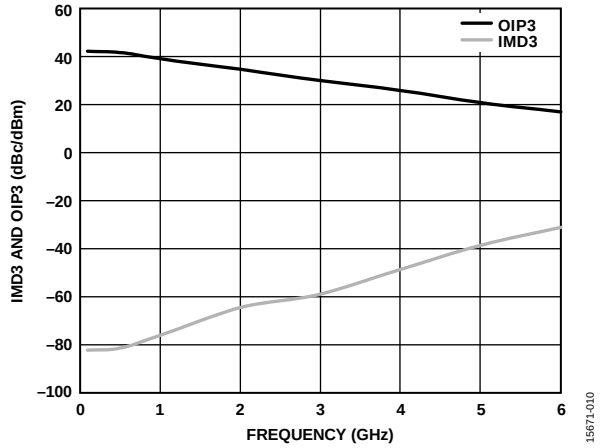

Figure 10. Third-Order Intermodulation Distortion (IMD3) and Output Third-Order Intercept (OIP3) vs. Frequency

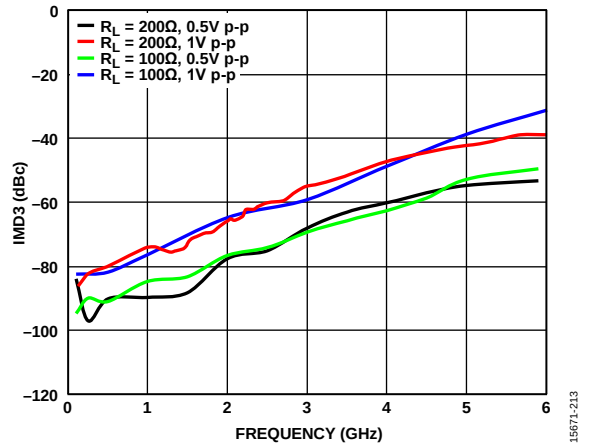

Figure 13. IMD3 vs. Frequency over R_{LOAD} for P_{OUT} per Tone

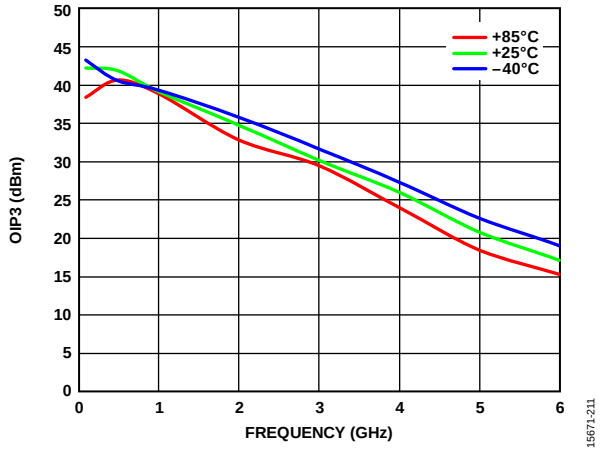

Figure 11. OIP3 vs. Frequency over Temperature

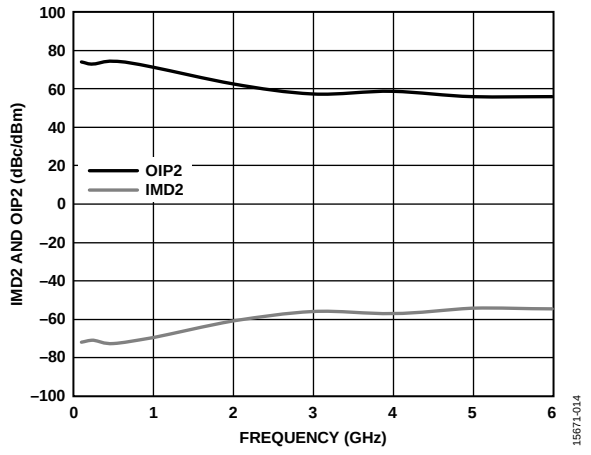

Figure 14. Second-Order Intermodulation Distortion (IMD2) and Output Second-Order Intercept (OIP2) vs. Frequency

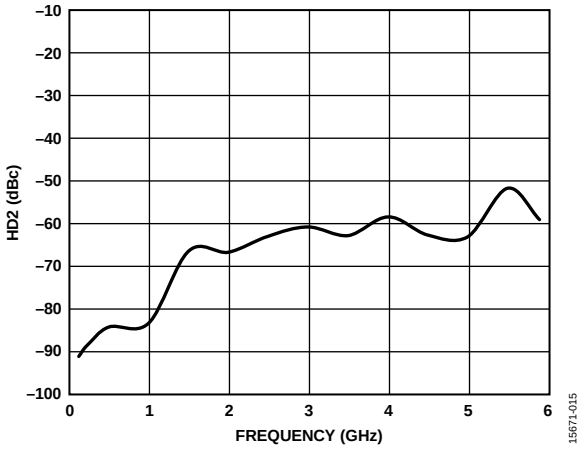

Figure 15. Second Harmonic Distortion (HD2) vs. Frequency

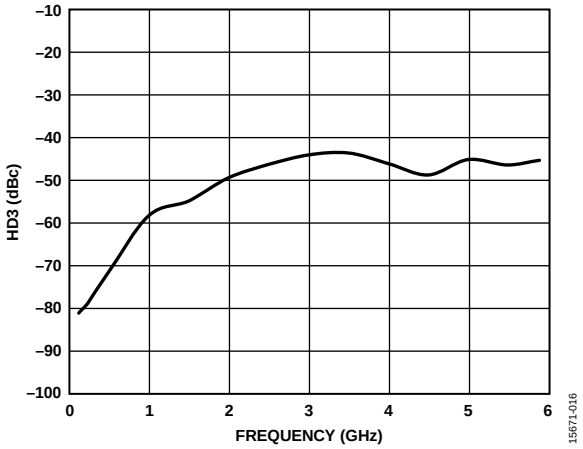

Figure 16. Third Harmonic Distortion (HD3) vs. Frequency

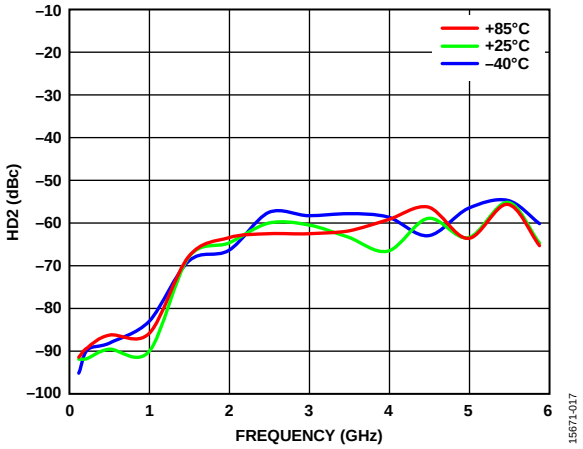

Figure 17. HD2 vs. Frequency over Temperature

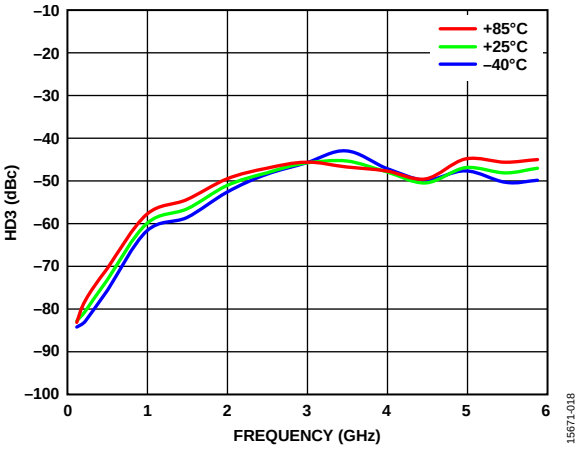

Figure 18. HD3 vs. Frequency over Temperature

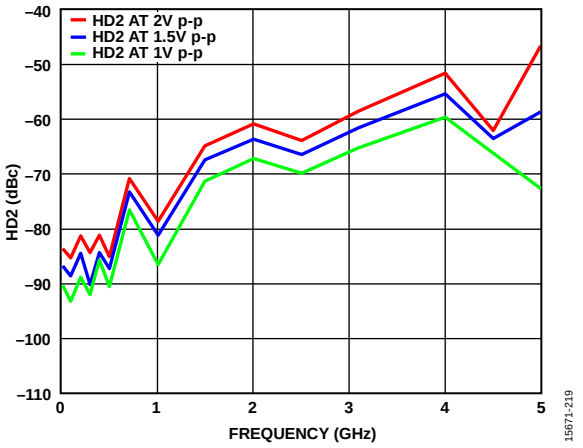

Figure 19. HD2 vs. Frequency for Various Output Voltages Swings

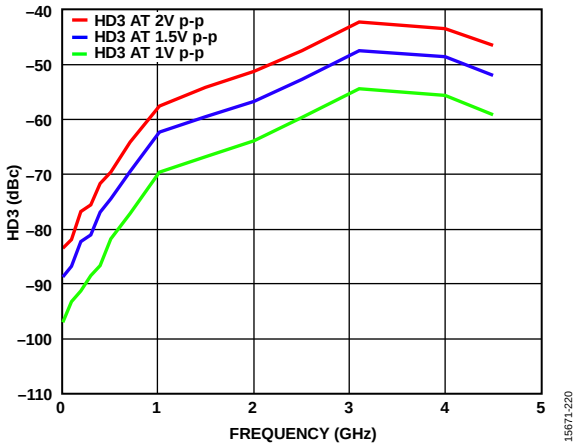

Figure 20. HD3 vs. Frequency for Various Voltages Swings

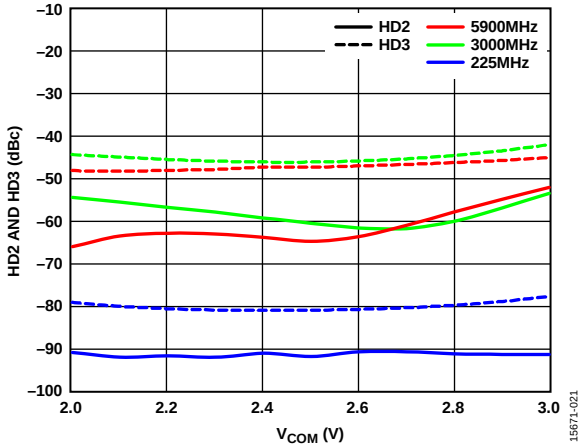

Figure 21. HD2 and HD3 vs. Output Common-Mode Voltage (V_{COM})

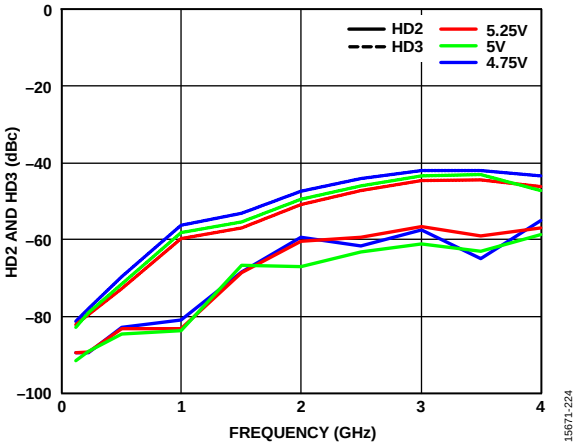

Figure 24. HD2 and HD3 vs. Frequency for Various Supplies

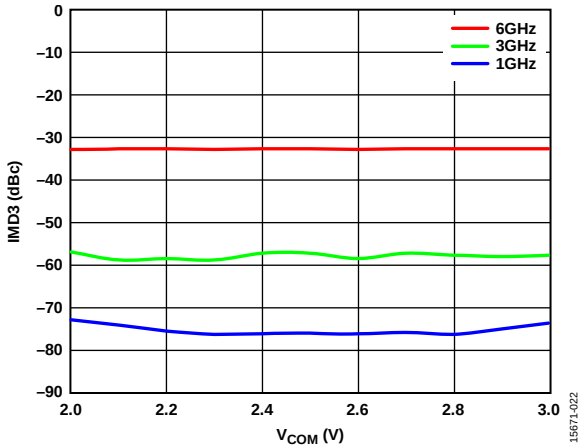

Figure 22. IMD3 vs. V_{COM}

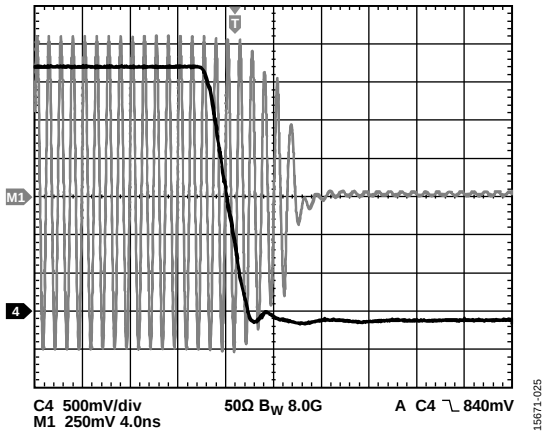

Figure 25. Disable Time Response

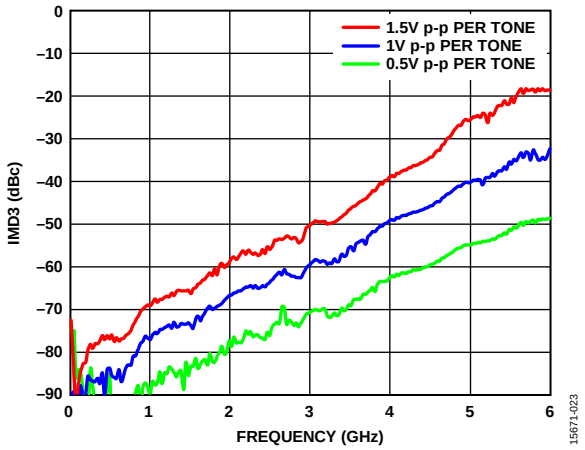

Figure 23. IMD3 vs. Frequency at Various P_{OUT} per Tones

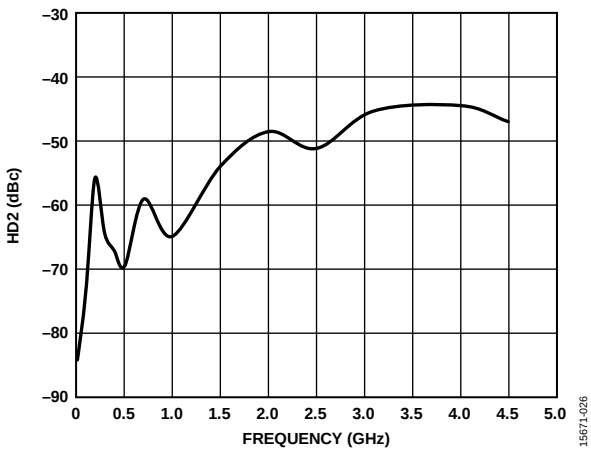

Figure 26. HD2 vs. Frequency for a Single-Ended Input Circuit

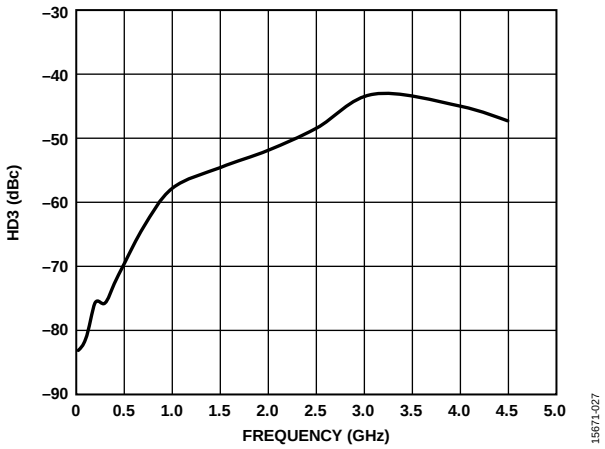

Figure 27. HD3 vs. Frequency for a Single-Ended Input Circuit

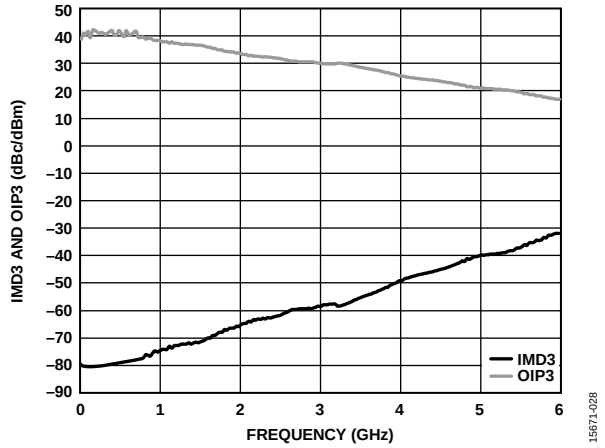

Figure 28. IMD3 and OIP3 vs. Frequency for a Single-Ended Input Circuit

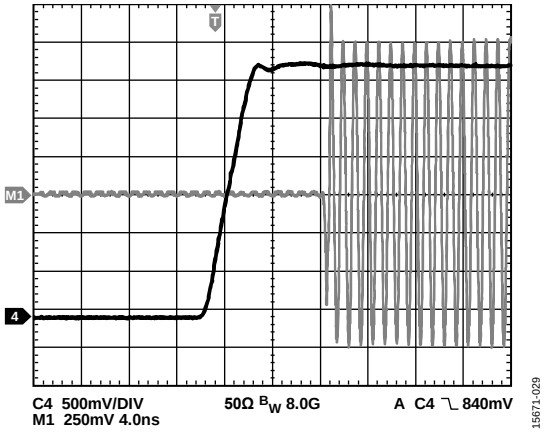

Figure 29. Enable Time Response

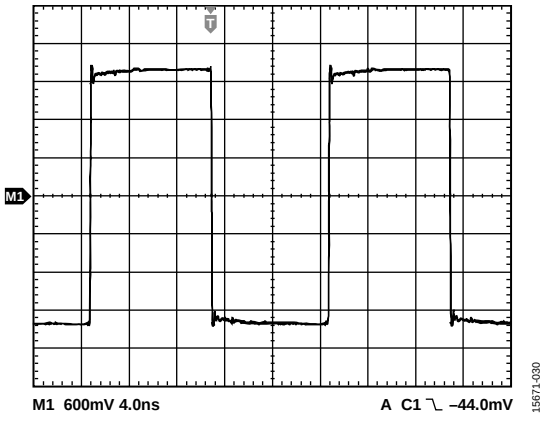

Figure 30. Large Signal Pulse Response, Output Voltage (V_{OUT}) = 4 V p-p

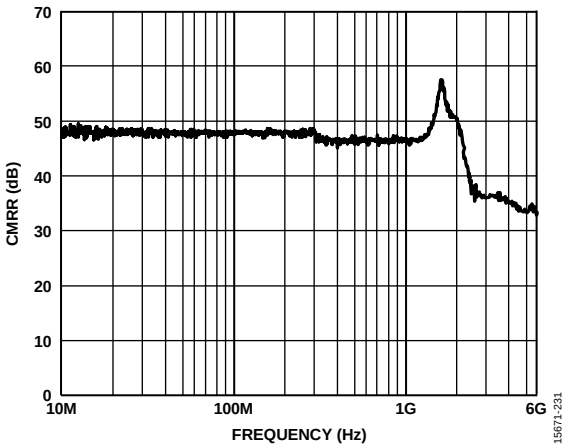

Figure 31. Common-Mode Rejection Ratio (CMRR) vs. Frequency

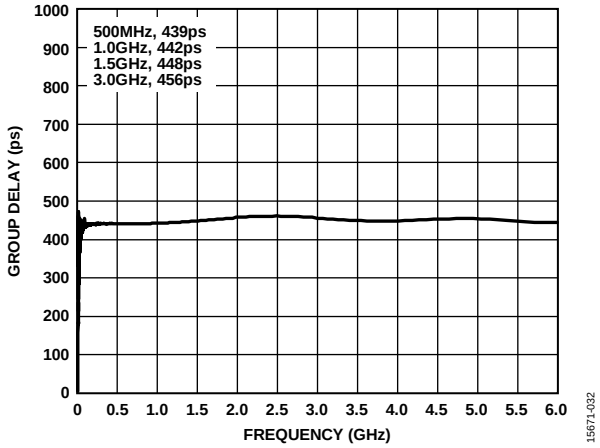

Figure 32. Group Delay vs. Frequency

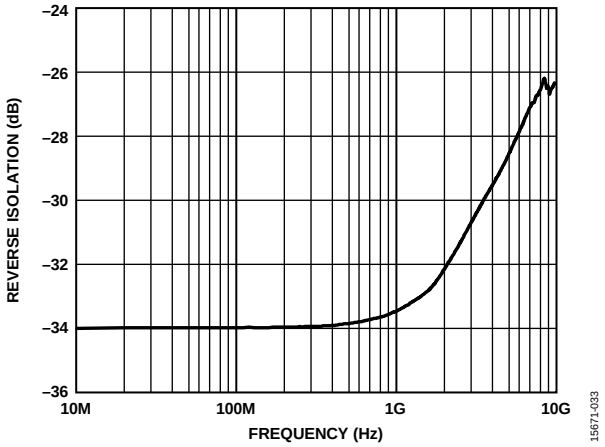

Figure 33. Reverse Isolation (SDD12) vs. Frequency

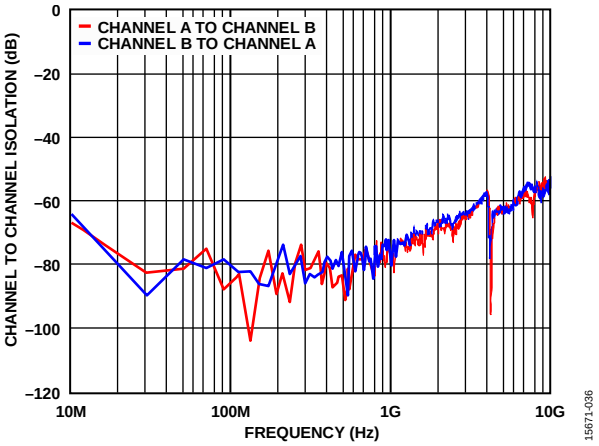

Figure 36. Channel to Channel Isolation vs. Frequency

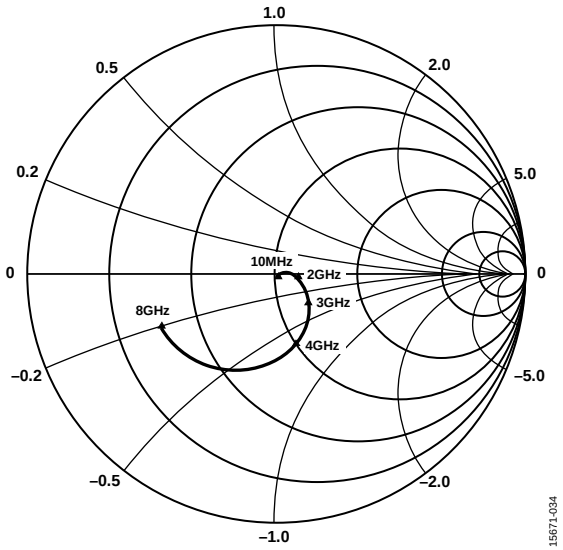

Figure 34. Differential Input Reflection Coefficient (SDD11)

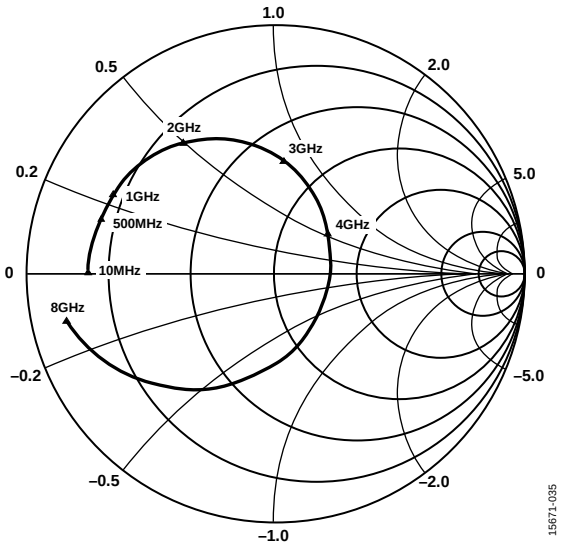

Figure 37. Differential Output Reflection Coefficient (SDD22)

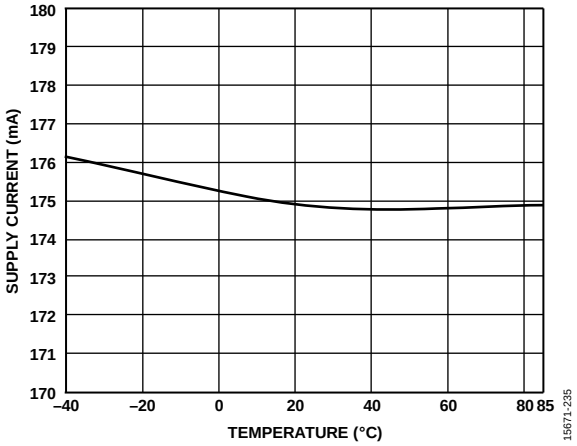

Figure 35. Supply Current vs. Temperature

THEORY OF OPERATION

The ADL5569 is a high gain, fully differential, dual amplifier and ADC driver that operates on a single power supply voltage (V_S) of 5 V. Internal resistors preset the gain to 20 dB, and external resistors can be added to reduce this gain. The −3 dB bandwidth is 6.5 GHz, and the device has a differential input impedance of 100 Ω. The ADL5569 has a differential output impedance of 14 Ω and an operating output common-mode voltage range of 2.0 V to 3.0 V with a 5 V supply.

The ADL5569 is composed of a pair of fully differential amplifiers with on-chip feedback and feedforward resistors. The gain is fixed at 20 dB but can be reduced by adding two resistors in series with the two inputs. The amplifier provides a high differential, open-loop gain and has an output common-mode circuit that enables the user to change the output common-mode voltage by applying a voltage to the VCOM or VCOM2 pin.

Each amplifier provides superior low distortion for frequencies near dc to beyond 2000 MHz, with low noise and low power consumption. This amplifier achieves an IMD3 of −82 dBc at 100 MHz, and −80 dBc IMD3 at 500 MHz for 2 V p-p operation. In addition, the ADL5569 can deliver 5 V p-p operation under heavy loads. The internal gain is set at 20 dB, and the device has a noise figure of 9.3 dB at 2 GHz. When comparing noise figure and distortion performance, this amplifier delivers the best in category spurious-free dynamic range (SFDR).

The ADL5569 features flexible input and output coupling. The device can be ac-coupled or dc-coupled. For dc coupling, the output common-mode voltage can be adjusted (using the VCOM and VCOM2 pins) from 2.5 V to 0.5 V for V_S at 3.3 V and ground at −2.0 V.

The distortion performance as a function of output common-mode voltage is shown in Figure 21. Note that the VCOM and VCOM2 pins set the common-mode voltage at the outputs of the amplifier, the VOP, VOP2, VON, and VON2 pins, when configured for ac-coupled applications.

For ac-coupled applications with series capacitors at the inputs, as shown in Figure 38, the input common-mode level is set to the same as the voltage at VCOM or VCOM2.

Due to the wide input common-mode voltage range, this device can easily be dc-coupled to many types of mixers, demodulators, and amplifiers. If the outputs are ac-coupled, no external VCOM or VCOM2 voltage adjustment is required because the amplifier output common-mode level is set to $V_S/2$.

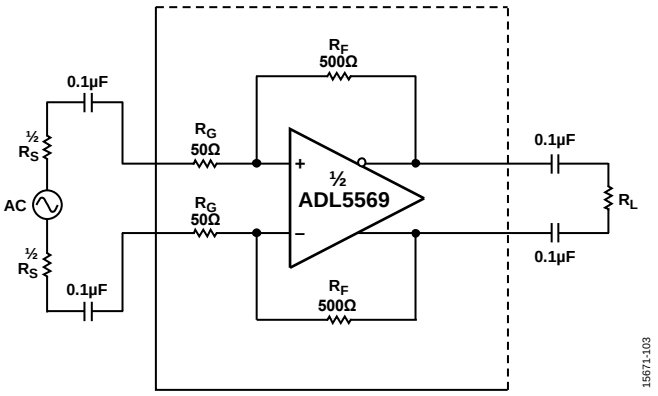

Figure 38. Basic Structure

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 39 shows the basic connections for operating the ADL5569. Apply 5 V to the VCC and VCC2 pins and decouple with 0.1 µF and 10 µF surface-mount ceramic capacitors in parallel to ground.

Decouple the VCOM and VCOM2 pins (Pin 7 and Pin 15) using a 0.1 µF capacitor. The PDB and PDB2 pins (Pin 6 and Pin 16) are tied to logic high, respectively, to enable each amplifier. A differential signal is applied to Amplifier 1 through Pin 1 (VIN) and Pin 2 (VIP) and to Amplifier 2 through Pin 4 (VIP2) and Pin 5 (VIN2). Each amplifier has a gain of 20 dB.

The Amplifier 1 input pins, Pin 1 (VIN) and Pin 2 (VIP), and the output pins, Pin 13 (VON) and Pin 12 (VOP), are biased by applying a voltage to Pin 15 (VCOM). If VCOM is left open, VCOM equals ½ of V_S. The Amplifier 2 input pins, Pin 4 (VIP2) and Pin 5 (VIN2), and the output pins, Pin 9 (VON2) and Pin 10 (VOP2), are biased by applying a voltage to Pin 7 (VCOM2). If VCOM2 is left open, VCOM2 equals ½ of V_S.

The ADL5569 can be ac-coupled, as shown in Figure 39, or it can be dc-coupled if within the specified input and output common-mode voltage ranges. Pulling the PDB and PDB2 pins low puts the ADL5569 in sleep mode, reducing the current consumption to 16 mA at ambient temperature.

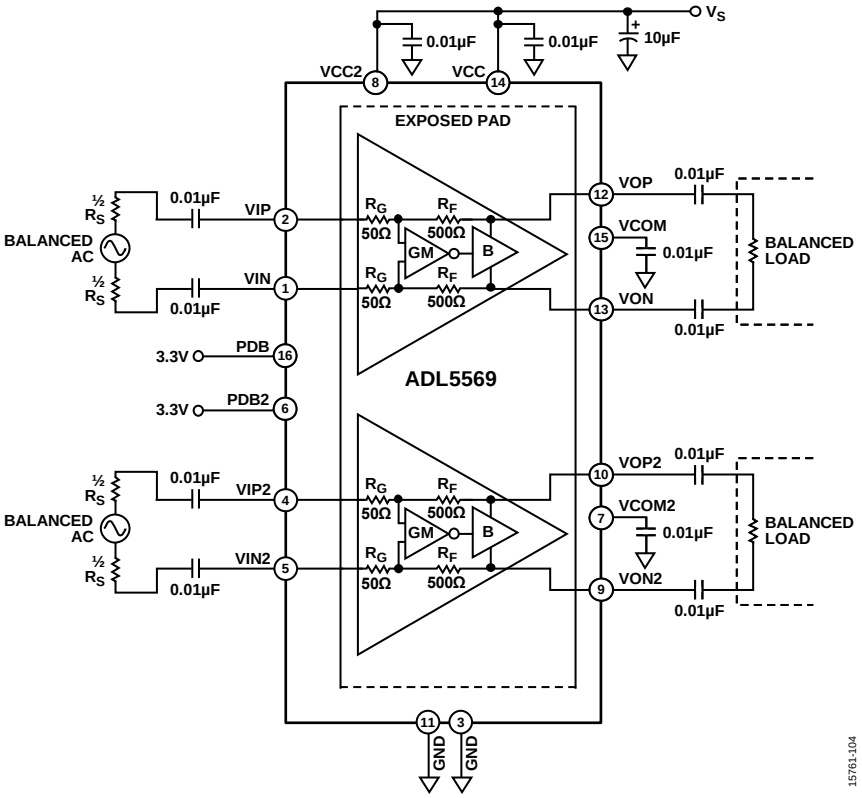

Figure 39. Basic Connections

INPUT AND OUTPUT INTERFACING

The ADL5569 can be configured as a differential input to differential output driver, as shown in Figure 40. The 50 Ω resistors, R1 and R2, combined with the input balun, provide a 50 Ω input match for the 100 Ω input impedance. The input and output 0.1 µF capacitors isolate the V_{VCC}/V_{VCC2} bias from the source and balanced load. The load is 100 Ω to provide the expected ac performance (see the Specifications section).

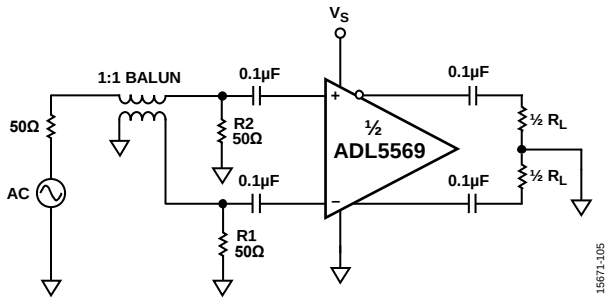

Figure 40. Differential Input to Differential Output Configuration

The differential gain of the ADL5569 is dependent on the source impedance and load, as shown in Figure 41. Determine the differential gain (A_V) by

$$A_V = 500/50 \quad (1)$$

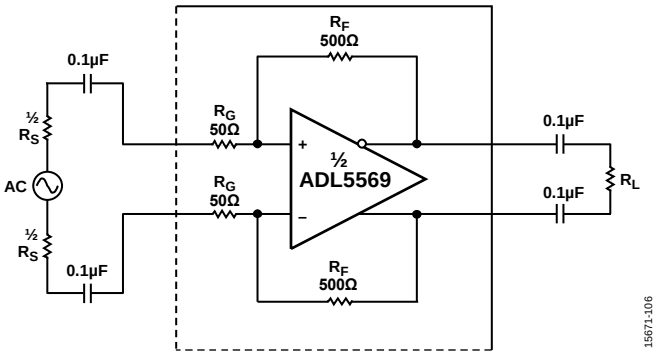

Figure 41. Differential Input Loading Circuit

Single-Ended Input to Differential Output

The ADL5569 can also be configured in a single-ended input to differential output configuration, as shown in Figure 42. In this configuration, the gain of the device is reduced due to the application of the signal to only one side of the amplifier. The input and output 0.1 µF capacitors isolate the V_{VCC}/V_{VCC2} bias from the source and the balanced load.

The single-ended circuit configuration can be accomplished in three steps (see Figure 42), assuming a 50 Ω R_S source. First, calculate the input resistance (R_{IN}) of the amplifier using the following formula:

$$R_{IN} = \frac{R_G}{1 - \left(\frac{R_F}{2 \times (R_G + R_F)} \right)} \quad (2)$$

where:
R_G is the series resistance internal to the amplifier.
R_F is feedback resistance internal to the amplifier.

Thus, R_{IN} = 91.7 Ω.

The next step is to calculate the termination of Resistor R2 (see Figure 42). Because source impedance (R_S) must be equal to the parallel equivalent resistance of R2 and R_{IN},

$$R_S = \frac{R2 \times R_{IN}}{R2 + R_{IN}}$$

Thus,

$$R2 = R_{IN} \times R_S/(R_{IN} - R_S) \quad (3)$$

When R_S = 50 Ω and R_{IN} = 91.7 Ω, R2 = 109 Ω.

The last step is to calculate the gain path rebalancing resistor, R1 (see Figure 42), by using the following formula:

$$R1 = \frac{R_S \times R2}{R_S + R2} \quad (4)$$

Thus, R1 = 34.0 Ω.

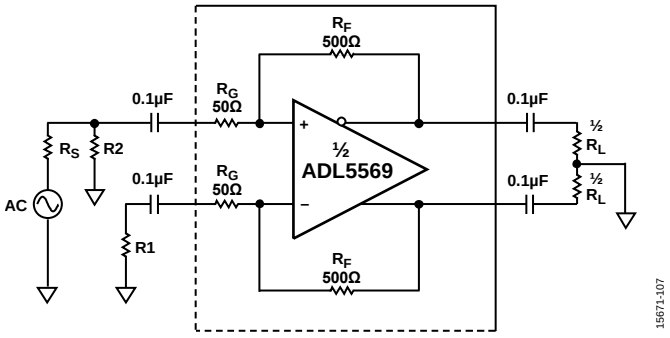

Figure 42. Single-Ended Input to Differential Output Configuration

See the AN-0990 Application Note, *Terminating a Differential Amplifier in Single-Ended Input Applications*, for more information on terminating single-ended inputs. The single-ended gain configuration of the ADL5569 is dependent on the source impedance and load, as shown in Figure 43.

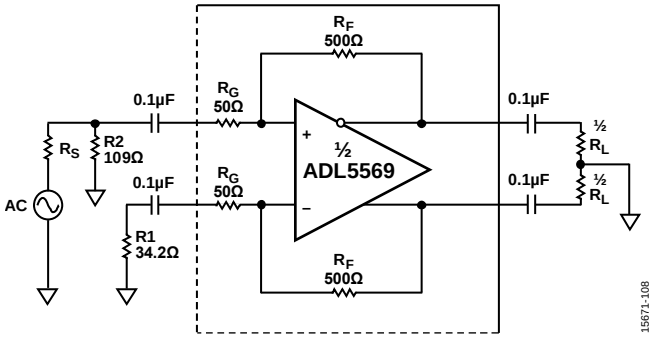

Figure 43. Single-Ended Input Loading Circuit

Determine the single-ended gain (A_{V1}) using the following two equations:

$$R_{MATCH} = \frac{R2 \times R_{IN}}{R2 + R_{IN}} \quad (5)$$

where R_{MATCH} is the input resistance value that matches R_S, which is calculated as follows:

$$A_{V1} = \frac{500}{50 + \left(\frac{R_S \times R2}{R_S + R2}\right)} \times \frac{R2}{R_S + R2} \times \frac{R_{MATCH} + R_S}{R_{MATCH}} \times \frac{R_L}{10 + R_L} \quad (6)$$

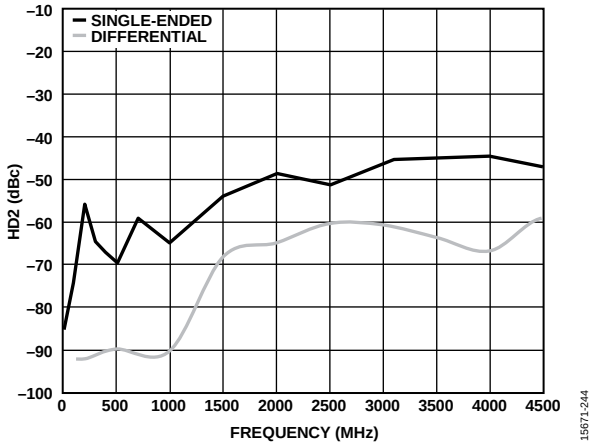

Figure 44. HD2 for Single-Ended and Differential Configurations vs. Frequency, V_{OUT} = 2 V p-p

GAIN ADJUSTMENT AND INTERFACING

The effective gain of the ADL5569 can be reduced by adding two resistors in series with the inputs to reduce the gain.

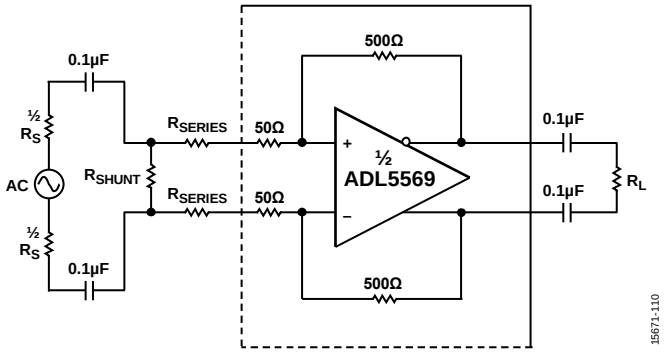

Figure 45. Gain Adjustment Using a Series Resistor

To find series resistor (R_{SERIES}) for a given A_V gain and R_L, use the following equation:

$$R_{SERIES} = (500/A_V) - 50 \quad (7)$$

The necessary shunt component (R_{SHUNT}) to match the source impedance, R_S, is expressed as

$$R_{SHUNT} = \frac{1}{\frac{1}{R_S} - \frac{1}{2 \times R_{SERIES} + 100}} \quad (8)$$

The shunt resistor values for multiple target voltage gains are listed in Table 5. The source resistance and input impedance need careful attention when using Equation 6. Consider the input impedance of the ADL5569 and the reactance of the ac coupling capacitors before assuming that the impedance and reactance of the capacitors make a negligible contribution.

To calculate the A_V for a given R_{SERIES}, use the following equation:

$$A_V = \left(\frac{500}{R_{SERIES} + 50}\right) \quad (9)$$

Note that Equation 9 only gives the absolute gain and does not take into account that the circuit introduces a 180° phase shift. To account for this phase shift, multiply the product of Equation 9 by −1.

Table 5. Differential Gain Adjustment Using Series Resistor

R_S (Ω)	Target Voltage Gain (dB)	R_{SERIES} (Ω)	R_{SHUNT} (Ω)
50	6	169	56.2
50	7	147	57.6
50	8	124	59
50	9	105	59
50	10	88.7	60.4
50	11	73.2	63.4
50	12	60.4	64.9
50	13	48.7	66.5
50	14	37.4	69.8
50	15	28	73.2
50	16	19.6	78.7
50	17	12.1	84.5
50	18	5.23	90.9
100	6	169	130
100	7	147	133
100	8	124	140
100	9	105	147
100	10	88.7	158
100	11	73.2	169
100	12	60.4	182
100	13	48.7	205
100	14	37.4	232
100	15	28	280
100	16	19.6	357
100	17	12.1	511
100	18	5.23	1050

EFFECT OF LOAD CAPACITANCE

Load capacitance, including stray capacitance from PCB traces, affects the bandwidth and flatness of the ADL5569 frequency response, resulting in excessive peaking. It is recommended to add 5 Ω external series resistors to each output to isolate the load capacitance from the outputs and to effectively reduce peaking. Respective frequency responses resulting from the addition of a 0.5 pF to a 2.0 pF differential load capacitance are shown in Figure 46.

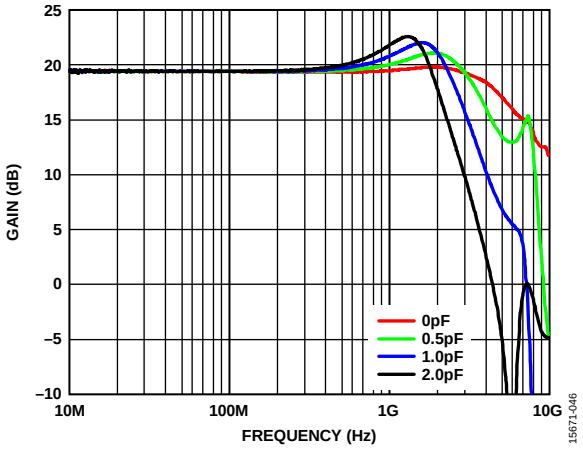

Figure 46. Frequency Response for Various Load Capacitances, R_L = 100 Ω

GSPS ADC INTERFACING

A wideband data acquisition system using the ADL5569 together with the AD9689, a dual 14-bit ADC, was developed and tested as shown in Figure 49 for ac-coupled applications. The amplifier output common-mode voltage is set to AVDD/2 with the voltage divider formed by the two 10 kΩ resistors on the VCOM pin. However, the VCOM pin can be left open (with a decoupling capacitor as described in Table 4), because there is an internal divider to pull the node to VCC/2 in such cases. The resistor capacitor (RC) filter after the amplifier works with the pole formed by the ADC input capacitance to attenuate the broadband noise and out of band harmonics generated by the amplifier. The RC filter also blocks sharp switching pulses, that is, charge injection from the ADC internal sampling circuitry, from reaching the amplifier outputs and creating nonlinear effects. An additional band-pass filter, specific to the system rejection requirements, is also needed in front of the ADL5569 amplifier to prevent unwanted signals from compressing the amplifier as well as from reaching the ADC. This filter is usually added during bench testing.

See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for additional testing information and setups.

The signal-to-noise ratio (SNR) and SFDR with respect to full scale (FS) of the ADC system, is shown in Figure 47 and Figure 48.

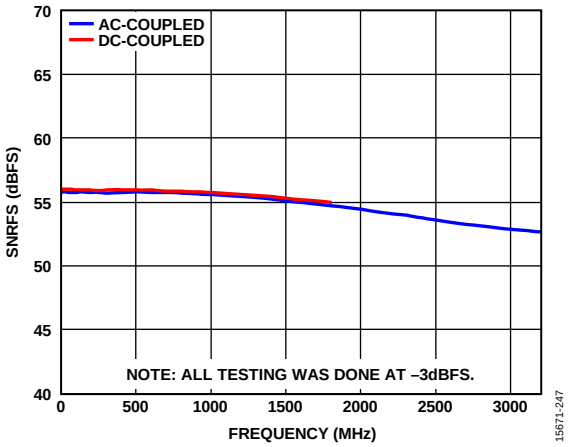

Figure 47. ADC System SNR Referred to Full Scale (SNRFS) vs. Frequency

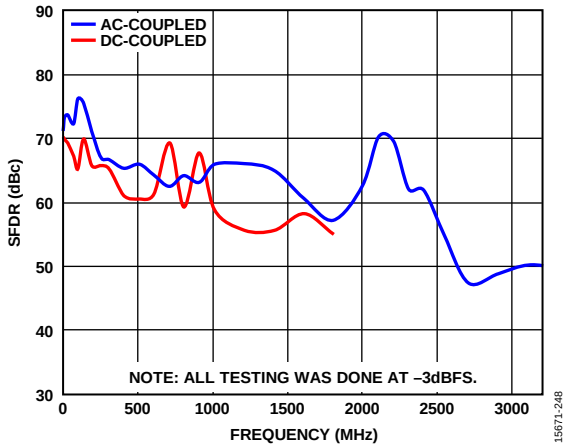

Figure 48. ADC System SFDR vs. Frequency

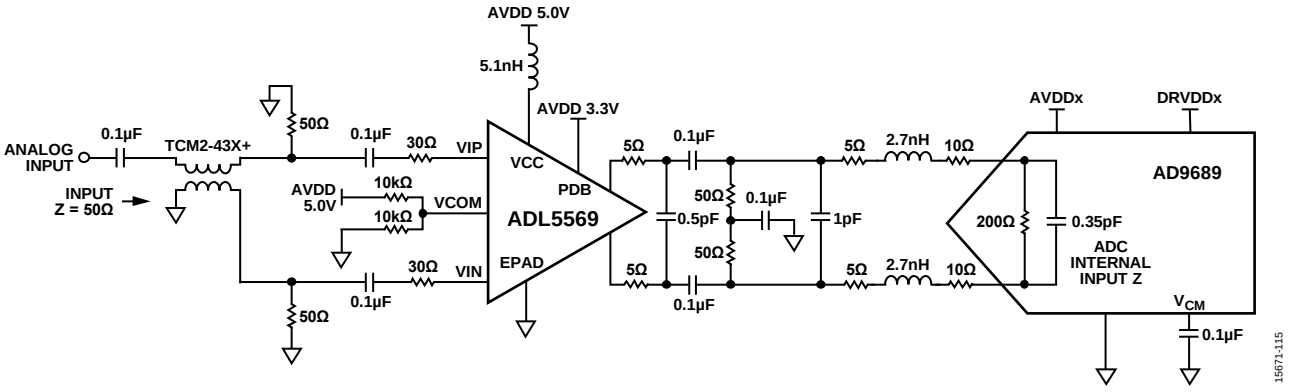

Figure 49. Wideband 3.2 GHz Bandwidth AC-Coupled ADC Interfacing Example: ADL5569 Driving the AD9689

Two tone intermodulation distortion performance (IMD2 and IMD3) is shown in Figure 50. The relative pass-band frequency response for this signal chain with a wideband antialiasing filter is shown in Figure 51.

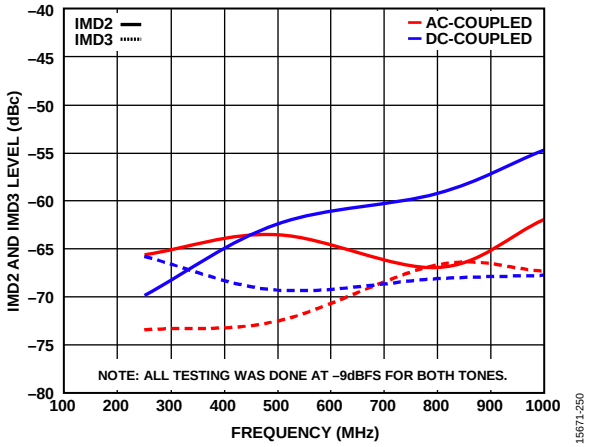

Figure 50. Measured Two Tone IMD2/IMD3 Performance

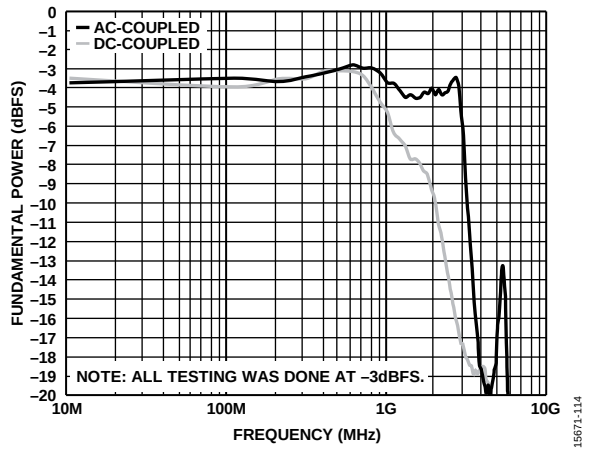

Figure 51. Measured Relative Frequency Response

For dc applications, special requirements must be completed for the ADL5569 to accommodate a dc signal and level shift the amplifier to meet the common-mode voltage requirements of the companion converter. Figure 52 shows a 1.5 GHz design example of the ADL5569 using dual supplies of +3.3 V for the VCC and VCC2 pins and −2.0 V for the ground and exposed pad (EP) pins. By using these dual supplies, the internal logic of the power-down pins of the device (PDB and PDB2) is also level shifted to 1.0 V to enable the device.

The example shown in Figure 52 provides a single-ended input design, with an input common-mode voltage of 0.0 V. The output common-mode voltage is designed to accommodate 1.4 V to interface with the AD9689 analog inputs. The VCOM pin cannot be regarded as high-Z for the purposes of a voltage divider calculation for the 2 kΩ and 15.4 kΩ resistors. The 1.5 GHz bandwidth limitation of this design is not due to any of the passive components, but it is an inherent practical limitation of the ADL5569 and AD9689/AD9208 combination.

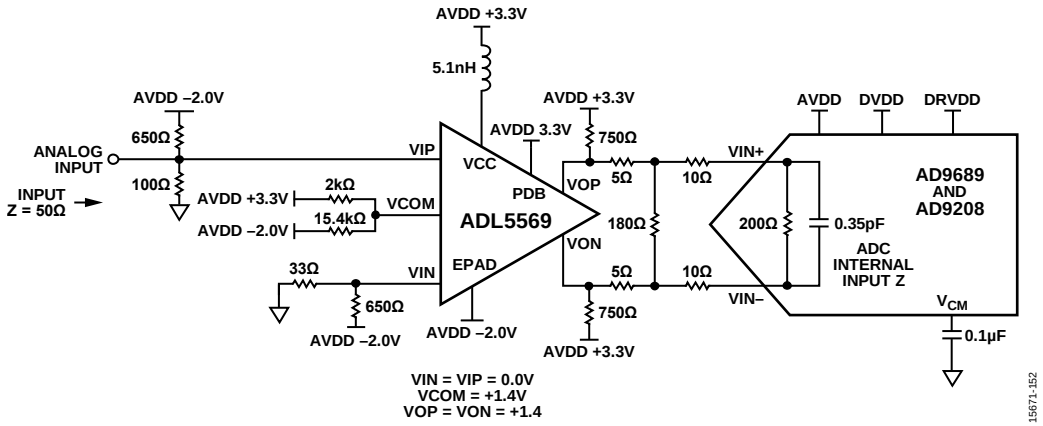

Figure 52. 1.5 GHz Bandwidth, DC-Coupled ADC Interfacing Example: ADL5569 Driving the AD9689 and AD9208

SOLDERING INFORMATION AND RECOMMENDED LAND PATTERN

Figure 53 shows the recommended land pattern for the ADL5569. The ADL5569 is contained in a 2.5 mm × 3 mm LFCSP, which has an exposed ground pad (EPAD). This pad is internally connected to the ground of the chip. To minimize thermal impedance and ensure electrical performance, solder the pad to the low impedance ground plane on the PCB. To further reduce thermal impedance, it is recommended that the ground planes on all layers under the pad be stitched together with vias.

For more information on land pattern design and layout, refer to the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

The land pattern on the ADL5569-EVALZ provides a simulated thermal resistance (θ_{JA}) of 90.5°C/W.

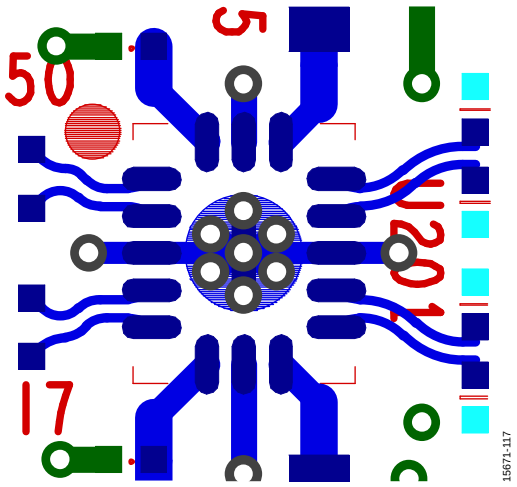

Figure 53. Recommended Land Pattern

EVALUATION BOARD

Figure 54 shows the general block diagram of the ADL5569-EVALZ evaluation board. The schematic of the ADL5569-EVALZ is shown in Figure 55 and has several options. The ADL5569-EVALZ is powered by a single 5 V supply. The power supply is decoupled by 10 µF and 0.1 µF capacitors. On-board regulators provide a 2.5 V common-mode voltage and 3 V logic supply voltage to enable and disable the power-down feature.

Several termination options are also provided to allow the user to terminate unused inputs and outputs of the amplifier for single-ended applications.

For more evaluation board options on the ADL5569, contact the Analog Devices sales.

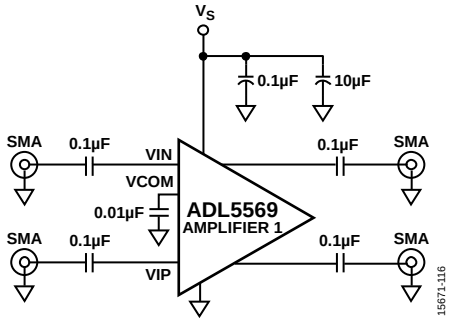

Figure 54. General Block Diagram of the ADL5569-EVALZ Evaluation Board

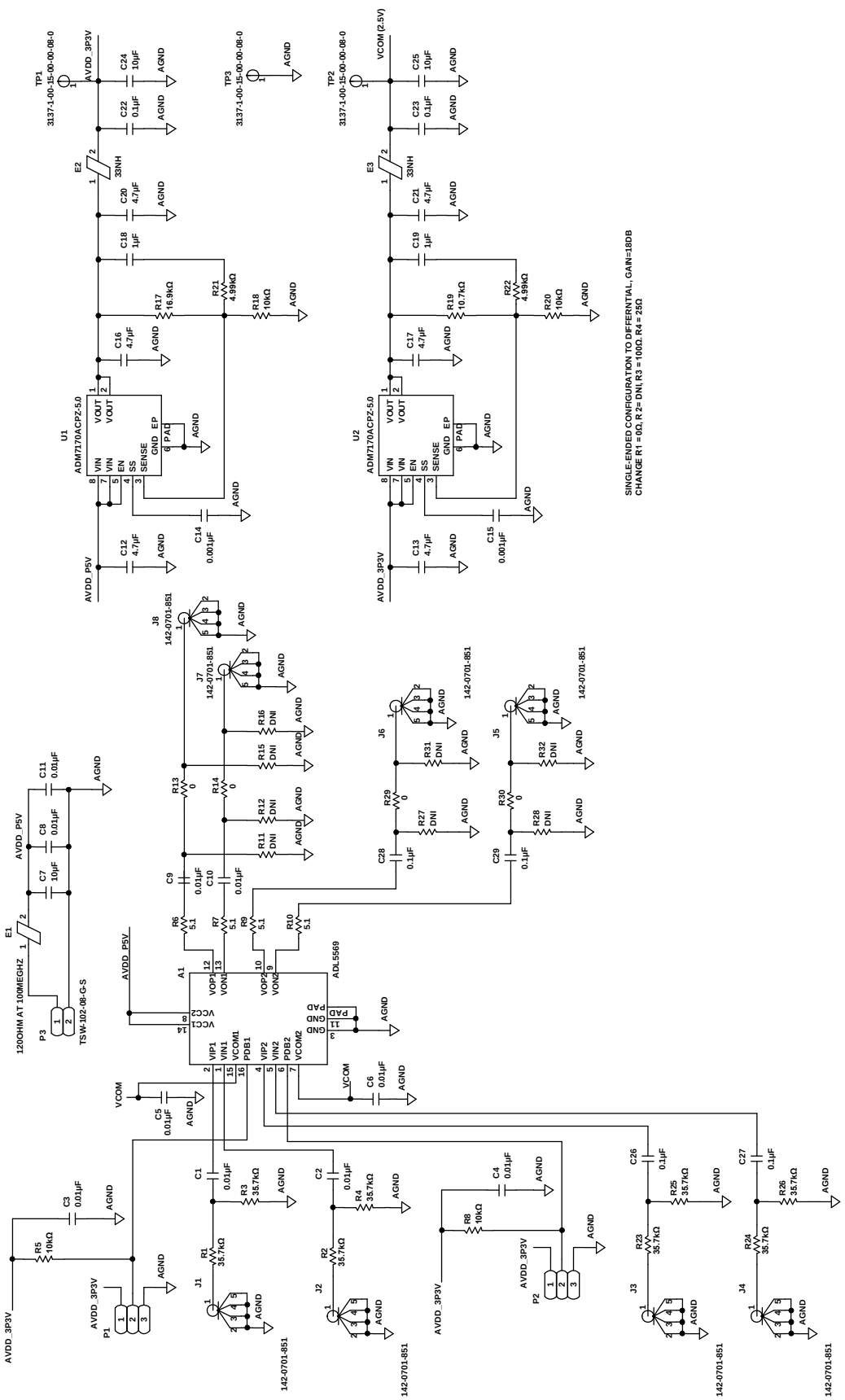

Figure 55. ADL5569-EVALZ Evaluation Board Schematic

Table 6. Bill of Materials

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	A1	IC, dual-channel amplifier	Analog Devices	ADL5569
10	C1 to C6, C8 to C11	0.01 µF capacitors, ceramic, X7R	Murata	GRM033R71A103KA01D
6	C12, C13, C16, C17, C20, C21	4.7 µF capacitors, ceramic, X5R	Murata	GRM155R60J475ME87D
2	C14, C15	0.001 µF capacitors, ceramic, X7R	Murata	GRM033R71E102KA01D
2	C18, C19	1 µF capacitors, ceramic, X5R	Taiyo Yuden	AMK063ABJ105MP-F
6	C22, C23, C26 to C29	0.1 µF capacitors, ceramic, X5R	Murata	GRM033R60J104KE19D
2	C24, C25	10 µF capacitors, ceramic X5R	Taiyo Yuden	AMK105CBJ106MV-F
1	C7	10 µF capacitor ceramic, X5R	Murata	GRM21BR61C106KE15L
1	E1	120 Ω at 100 MHz, ferrite bead, 0.07 Ω, 1.5 A	Murata	BLM18SG121TN1D
2	E2, E3	33 nH, chip inductors, 0.06 Ω, 1.3 A	Coilcraft, Inc.	0402AF-330XJL
8	J1 to J8	PCB SMA connectors, 50 Ω, end launch jack	Cinch Connectivity Solutions	142-0701-851
2	P1, P2	Connector headers, straight, three position	Samtec	TSW-103-08-G-S
1	P3	Connector PCB header, two position	Samtec	TSW-102-08-G-S
8	R1 to R4, R23 to R26	35.7 kΩ resistors, precision thick film chip	Panasonic	ERJ-1GEF3572C
4	R13, R14, R29, R30	0 Ω resistors, 0201	Panasonic	ERJ-1GE0R00C
1	R17	16.9 kΩ resistor, 0201	Panasonic	ERJ-1GEF1692C
1	R19	10.7 kΩ resistor, 0402	Vishay Precision Group	CRCW040210K7FKED
2	R21, R22	4.99 kΩ resistors, 0201	Samsung	RC0603F4991CS
4	R5, R8, R18, R20	10 kΩ resistors, 0201	Panasonic	ERJ-1GNF1002C
4	R6, R7, R9, R10	5.1 Ω resistors, 0201	Yageo	RC0201JR-075R1L
3	TP1, TP2, TP3	Connector PCB pin test points	Mill-Max	3137-1-00-15-00-00-08-0
2	U1, U2	IC ultralow noise, high PSRR, low dropout (LDO) regulators	Analog Devices	ADM7170ACPZ-5.0

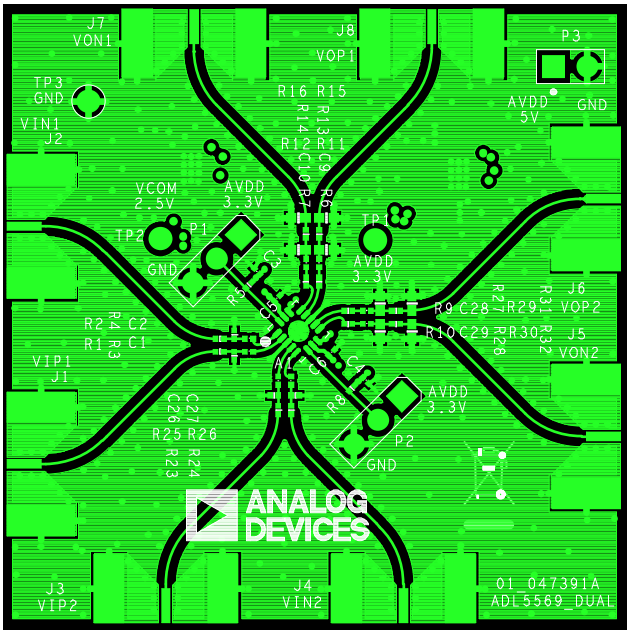

Figure 56. Layout of the ADL5569-EVALZ Evaluation Board, Top Layer

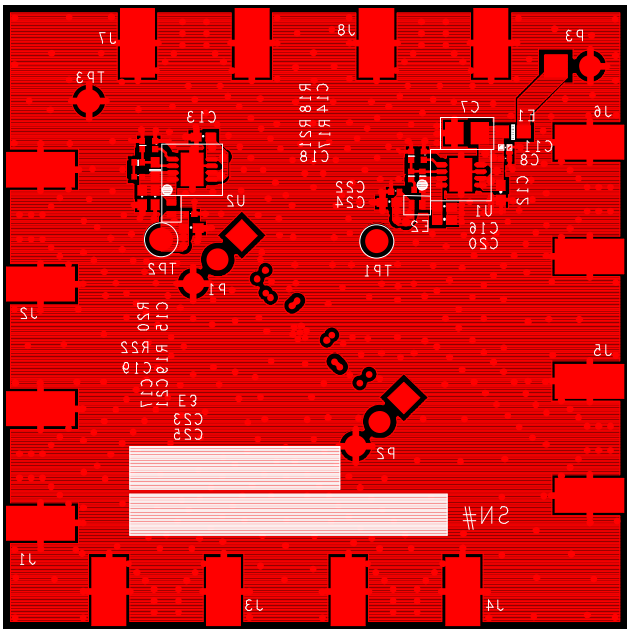

Figure 57. Layout of the ADL5569-EVALZ Evaluation Board, Bottom Layer

OUTLINE DIMENSIONS

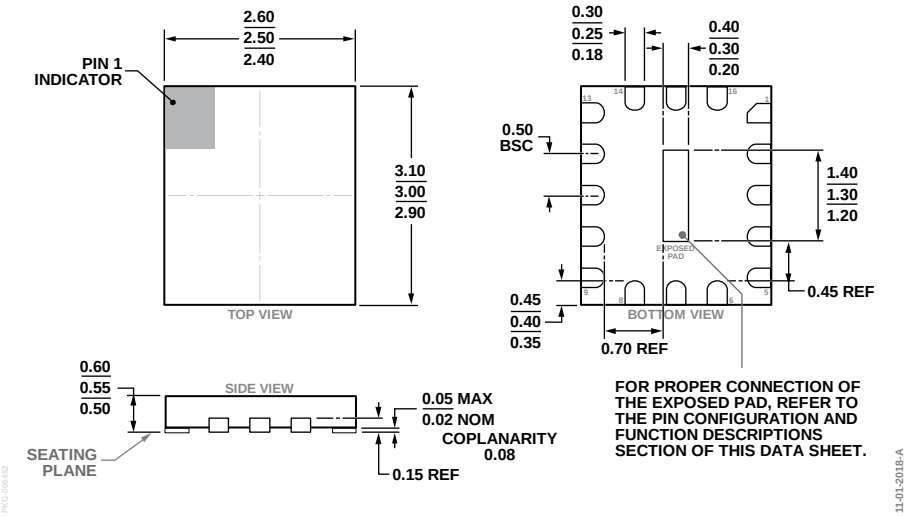

Figure 58. 16-Lead Lead Frame Chip Scale Package [LFCSP]
2.5 mm × 3 mm Body and 0.55 mm Package Height
(CP-16-44)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Marking Code
ADL5569BCPZ	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-44	ET
ADL5569BCPZ-R7	−40°C to +85°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-44	ET
ADL5569-EVALZ		Evaluation Board		

[1] Z = RoHS Compliant Part.