2.3 GHz to 2.4 GHz WiMAX Power Amplifier

Preliminary Technical Data

ADL5570

FEATURES

Fixed gain of 29 dB
Operation from 2.3 GHz to 2.4 GHz
EVM ≤3% with 16 QAM OFDMA
@ P_{OUT} = 25 dBm [3.5V] and
@ P_{OUT} = 27.5 dBm [5V]
Input internally matched to 50 Ω
Power supply: 3.2 V to 5.5 V
Quiescent current
130 mA in high power mode
70 mA in low power mode
PAE: >20%
Multiple operating modes to reduce battery drain
Low power mode: 100 mA (Operating)
Standby mode: 10 mA
Sleep mode: < 1 µA

APPLICATIONS

WiMAX/WiBro Mobile Terminals and CPEs
Good performance from 2.5Ghz to 2.7Ghz - See Page 7

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FUNCTIONAL BLOCK DIAGRAM

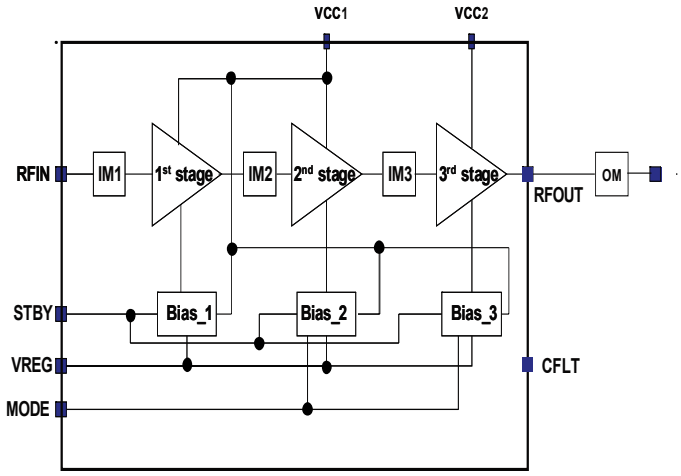

Figure 1.AD5570 Block Diagram

GENERAL DESCRIPTION

The ADL5570 is a high linearity 2.3 GHz to 2.4 GHz power amplifier designed for WiMAX terminals and CPEs using TDD operation at a duty cycle of 50% or lower. With a gain of 29 dB and an output compression point of 31 dBm , it can operate at an output power level up to 26 dBm while maintaining an EVM of ≤3% with a supply voltage of 3.5V. PAE is greater than 20% at P_{OUT} = 25 dBm with a 3.5V supply voltage.

The ADL5570 RF input is matched on chip and provides an input return loss of less than −10 dB. The open-collector output is externally matched with strip-line and external shunt capacitance.

The ADL5570 operates over a supply voltage range from 3.2 V to 5.5 V with a supply current of 400mA Burst RMS when delivering 25 dBm (3.5 V supply). A low power mode is also available for operation at power levels ≤10 dBm with optimized operating and quiescent currents of 100 and 70 mA, respectively. A Standby mode is available which reduces the quiescent current to 10 mA: useful when a TDD terminal is receiving data.

The ADL5570 is fabricated in a GaAs HBT process and is packaged in a 4mm x 4mm 16-Lead Pb-free RoHS compliant LFCSP that uses an exposed paddle for excellent thermal impedance. It operates from −40°C to +85°C.

Rev. PrG
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REVISION HISTORY

3/07—Rev. PrF: Preliminary Version

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TARGET SPECIFICATIONS - VCC = 3.5 V

T = 25°C, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz Channel BW, Z_L = 50 Ω, MODE = 0 V, STBY = 0 V, VREG = 2.85 V, 33% duty cycle, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	**See table 5 for tuning details**	**2.3**		**2.4**	**GHz**
Linear Output Power	MODE = 0 V, EVM ≤ 3%		25		dBm
	MODE = 2.5 V, EVM ≤ 3%		10		dBm
Gain			29		dB
vs. Frequency	±5 MHz		±0.3		dB
vs. Temp	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	3.2 V to 4.2 V		±1		dB
OP1dB	Unmodulated input		31		dBm
EVM	P_{OUT} = 25 dBm		3		% rms
Input Return Loss			10		dB
Spectral Mask @ 25dBm Output Power	±5 MHz carrier offset		35		dBc
	±6 MHz carrier offset		37		dBc
	±10.5 MHz carrier offset		41		dBc
	±20 MHz carrier offset		51		dBc
Harmonic Distortion			36		dBc
Power Supply Interface	VCC = 3.5 V				
Supply Current	P_{OUT} = 25 dBm, MODE= 0 V.		250		mA
	P_{OUT} = 12 dBm, MODE= 2.5 V.		100		mA
PAE	P_{OUT} = 25 dBm, MODE= 0 V		>20		%
Standby Mode	VREG = 2.85 V, STBY = 2.5 V		10		mA
Sleep Mode	VREG = 0 V		10		µA
Turn On/Off Time			1		µs
VSWR Survivability		10:1			

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TARGET SPECIFICATIONS - VCC = 5 V

T = 25°C, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz Channel BW, Z_L = 50 Ω, MODE = 0 V, STBY = 0 V, VREG = 2.85 V, 33% duty cycle, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
Frequency Range	**See table 5 for tuning details**	**2.3**		**2.4**	**GHz**
Linear Output Power	MODE = 0 V, EVM ≤ 3%		27.5		dBm
	MODE = 2.5 V, EVM ≤ 3 %		10		dBm
Gain			28		dB
vs. Frequency	±5 MHz		±0.3		dB
vs. Temp	−40°C ≤ T_A ≤ +85°C		±0.5		dB
vs. Supply	4.5 V to 5.5 V		±1		dB
OP1dB	Unmodulated input		32		dBm
EVM	P_{OUT} = 27.5 dBm		3		% rms
Input Return Loss			10		dB
Spectral Mask @ 25dBm Output Power	±5MHz carrier offset		38		dBc
	±6 MHz carrier offset		39		dBc
	±10.5 MHz carrier offset		43		dBc
	±20 MHz carrier offset		49		dBc
Harmonic Distortion			36		dBc
Power Supply Interface	VCC = 5 V				
Supply Current	P_{OUT} = 27.5 dBm, MODE = 0 V		300		mA
	P_{OUT} = 13 dBm, MODE = 2.5 V		115		mA
PAE	P_{OUT} = 27.5 dBm, MODE = 0 V		16		%
Standby Mode	VREG = 2.85 V, STBY = 2.5 V		10		mA
Sleep Mode	VREG = 0 V		10		µA
Turn On/Off Time			1		µs
VSWR Survivability		10:1			

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PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

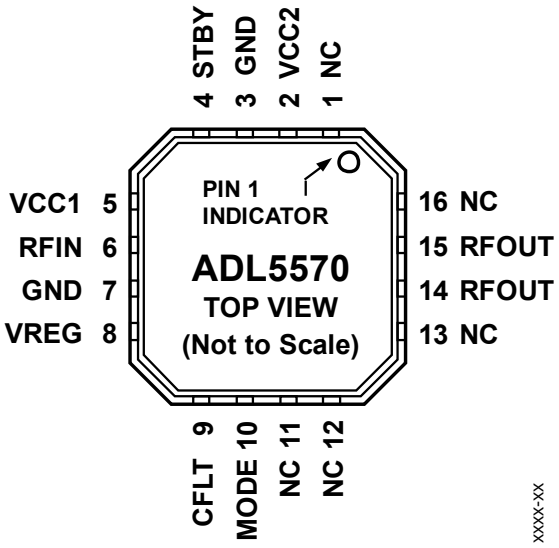

Figure 2. ADL5570 Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
5	VCC1	Connect to Power Supply.
6	RFIN	Matched RF Input.
8	VREG	When VREG is low, the device goes into sleep mode, reducing supply current to 1 uA. When VREG is high (2.85 V), the device operates in its normal transmit mode. When high, VREG draws a bias current of approximately 10 mA.
9	CFLT	A Ground Referenced Capacitor. It should be connected to this node to reduce bias line noise (see figure 8).
10	MODE	Switches Between High Power and Low Power Modes. When MODE is low (0 V), the device operates in high power mode. When MODE is high (2.5 V), the device operates in low power mode.
14, 15	RFOUT	Unmatched RF Output. These parallel outputs can be matched to 50 Ω using strip-line and shunt capacitance. The power supply voltage should be connected to these pins through a choke inductor.
2	VCC2	This power supply pin should be connected to the supply via a choke circuit (see Figure 8).
4	STBY	When STBY is low (0 V), the device operates in transmit mode. When the radio is receiving data, STBY can be taken high (2.5 V), reducing supply current to 10 mA.
1, 11 to 13, 16	N/C	No Connect. Do not connect these pins.
7	GND	Connected to Ground.
	Exposed Paddle	The exposed paddle should be soldered down to a low impedance ground plane (use multiple vias (at least 9) to stitch together the ground planes) for optimum electrical and thermal performance.

Table 4. Operating Modes[1]

Mnemonic	Normal Operation	Low Power Mode, POUT ≤ 10dBm	Standby Mode	Sleep Mode
VREG	High	High	High	Low
MODE	Low	High	X	X
STBY	Low	Low	High	X

[1] X = don't care.

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TYPICAL PERFORMANCE CHARACTERISTICS

T = 25°C, 1024 FFT, 16 QAM OFDMA modulated carrier, 10 MHz Channel BW, Z_L = 50 Ω, MODE = 0 V, STBY = 0 V, VREG = 2.85 V, 33% duty cycle, unless otherwise noted.

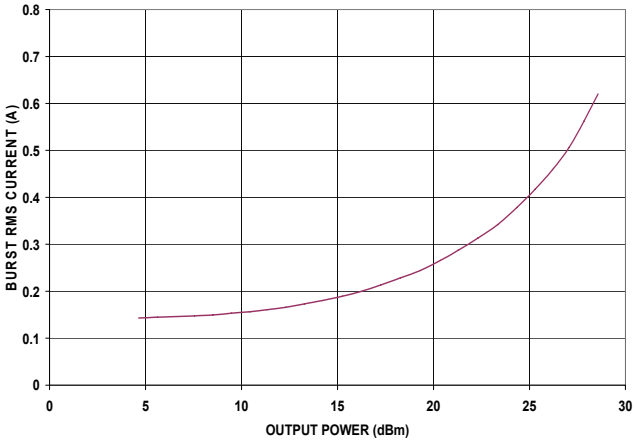

Figure 3.Burst RMS Current vs. $P_{OUT,}$ at 2.35 GHz, Vcc=3.5V

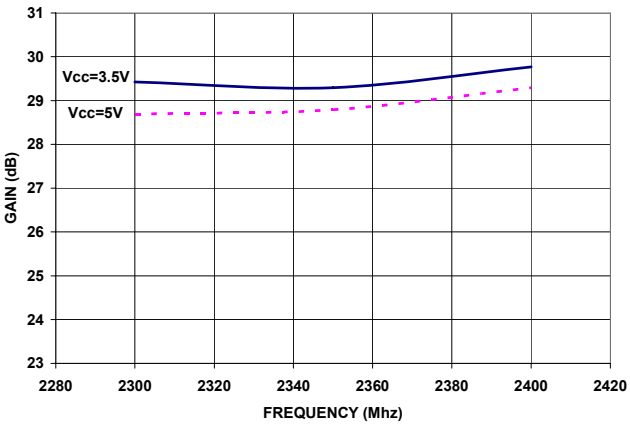

Figure 6. Gain vs. Frequency at P_{IN}= –2 dBm

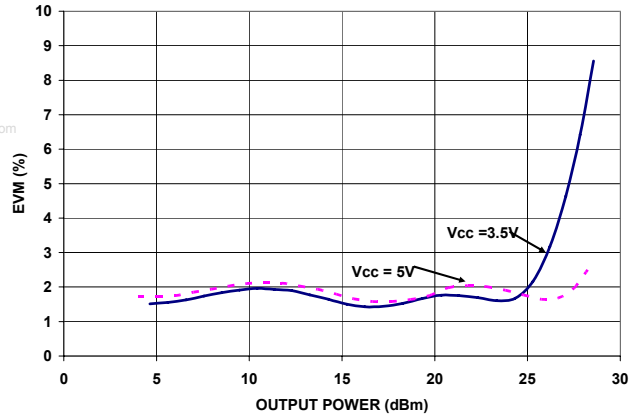

Figure 4. EVM vs. P_{OUT} at 2.35 GHz.

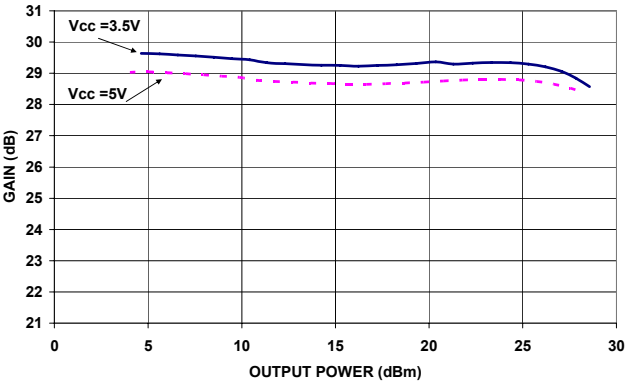

Figure 7. Gain vs Output Power at 2.35 GHz

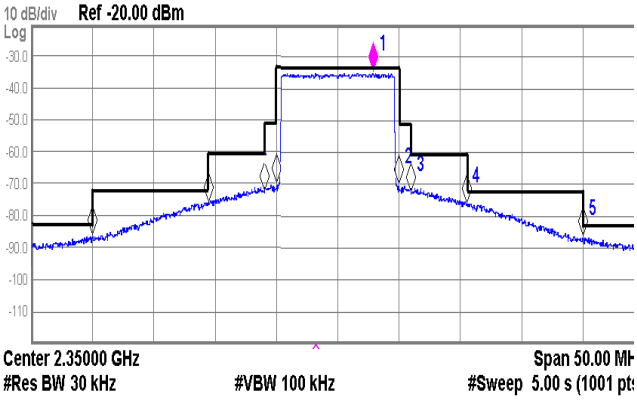

Figure 5. WiMax Spectrum with FCC Spectral Mask limits applied at 2.35Ghz, Vcc=3.5V, Pout=25dBm.

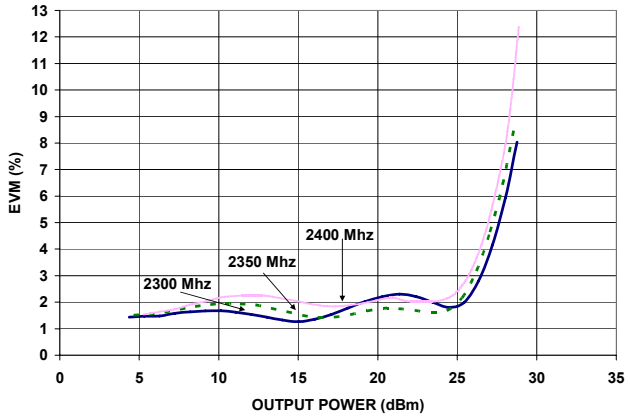

Figure 8.EVM vs. Output Power at Vcc=3.5V

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APPLICATIONS

2.5 GHZ TO 2.7 GHZ PEFORMANCE

The ADL5570 is optimized for superior performance within the 2.3 GHz to 2.4 GHz frequency band. With a change in the external matching capacitor, C3, to 2.4pF, the ADL5570 shows good performance in the 2.5 GHz to 2.7 GHz frequency band. The EVM, Gain and RMS current performance data are shown in Figure 9 and Figure 10.

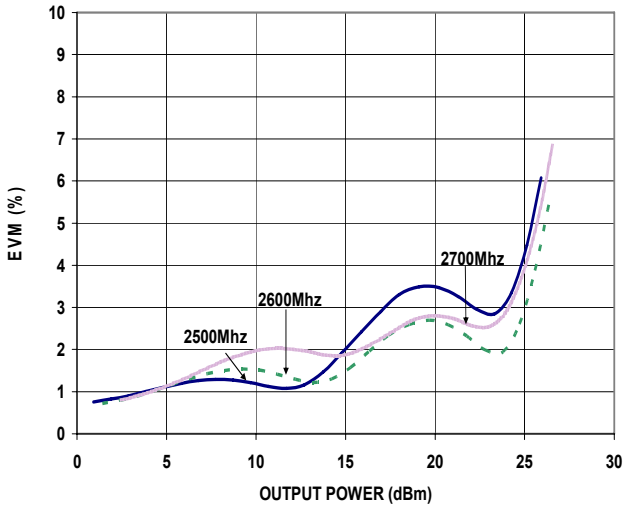

Figure 9. EVM vs Output power Perfomance at Vcc=3.5V and 16QAM OFDMA Signal

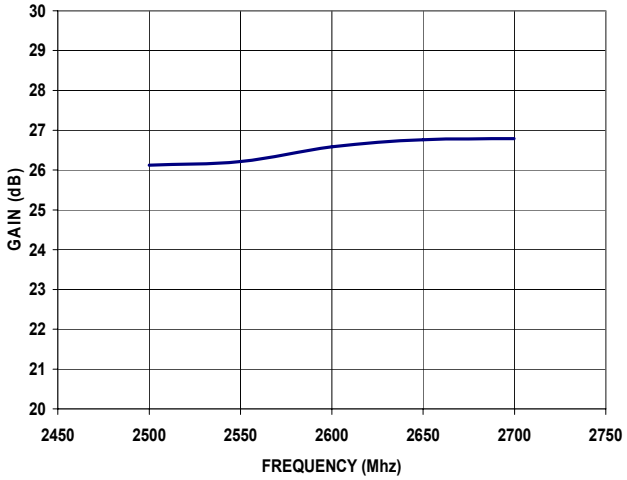

Figure 10. Gain vs Frequency Performance at Vcc=3.5V and 16QAM OFDMA Signal

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EVALUATION BOARD

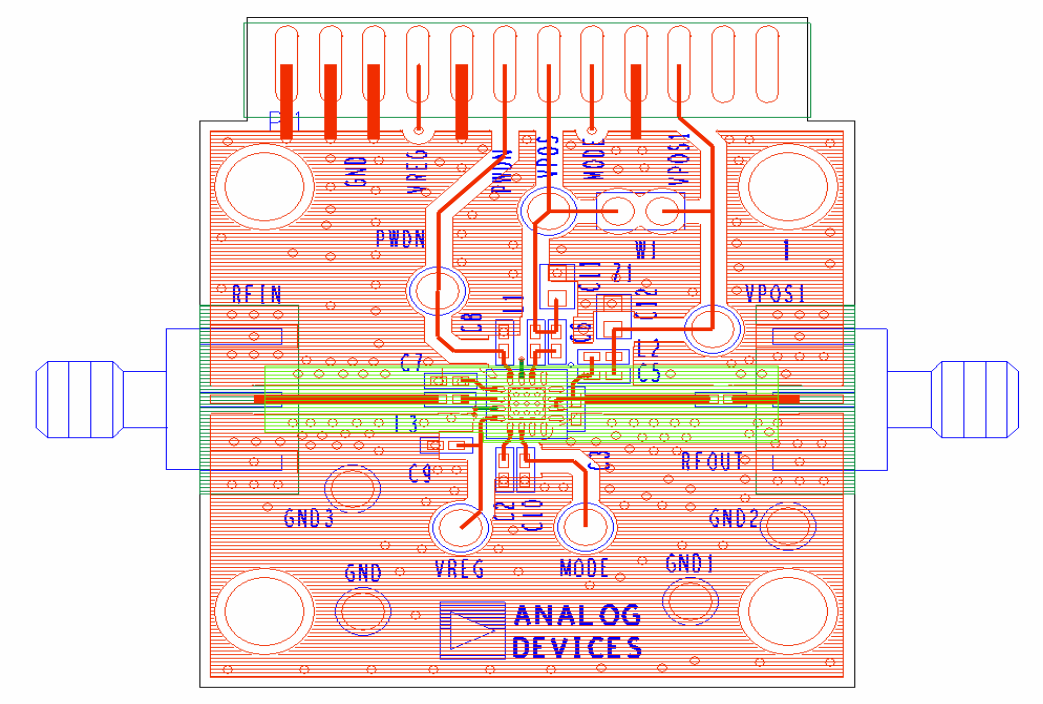

Figure 11. Evaluation Board Layout

The ADL5570 perfomance data were taken on a FR4 board layout. Care should be taken to ensure 50Ω impedance for all RF traces. For optimal performance in linearity, gain and efficiency, the output matching capacitor, C3, should be placed 30 mils from the edge of the package.

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Table 5. Evaluation Board Configuration Options

Component	Function	Default Value
Vpos, Vpos1, GND	Supply and Ground Connections	W1 = Installed
TP1(STBY)	**Transmit/Standby Mode**: When STBY is low (0 V), the device operates in transmit mode. When the radio is receiving data, STBY can be taken high (2.5 V), reducing supply current to 10 mA.	Not Applicable
TP2 (VREG)	**Normal/Sleep Mode**: When VREG is low, the device goes into sleep mode, reducing supply current to 10 uA. When VREG is high (2.85 V), the device operates in its normal transmit mode. When high, VREG draws a bias current of approximately 10 mA	Not Applicable
TP5(MODE)	**High/Low Power Mode**: Switches between High Power and Low Power Modes. When Mode is low (0V), the device operates in High Power Mode. When Mode is high (MODE = 2.5 V), the device operates in Low Power Mode.	Not Applicable
L3,	**Input Interface**: (L3) matches the input to 50 ohms.	L3 = 2.2nH (Size 0402)
C3, C4,	**Output Interface**: C4 provides dc blocking. C3 matches the output to 50 ohms.	C4 = 39pF (Size 0402) C3 = 3.3pF (Size 0402) (C3 value for 2.3 Ghz to 2.4Ghz operation)
C2	**Filter Interface**: A ground referenced capacitor should be connected to this node to reduce bias line noise	C2 = 2.2pF (Size 0402)
C7, C8, C9, C10, C11, C12	**Power Supply Decoupling**: The capacitors, C7, thru C12, are used for power supply decoupling. They should be placed as close as possible to the DUT.	C7 = 0.01µ F (Size 0402) C8 = 0.01µ F (Size 0402) C9 = 0.01µ F (Size 0402) C10 = 0.01µ F (Size 0402) C11 = 1µ F (Size 0402) C12 = 1µ F (Size 0402)
L1, L2, C6, C5	**RF Trap**: L1, C6 and L2, C5 form tank circuits and prevent RF from propagating on the dc supply lines	L1 = 1nH (Size 0402) C6 = 3.6pF (Size 0402) L1 = 11nH (Size 0402) C5 = OPEN

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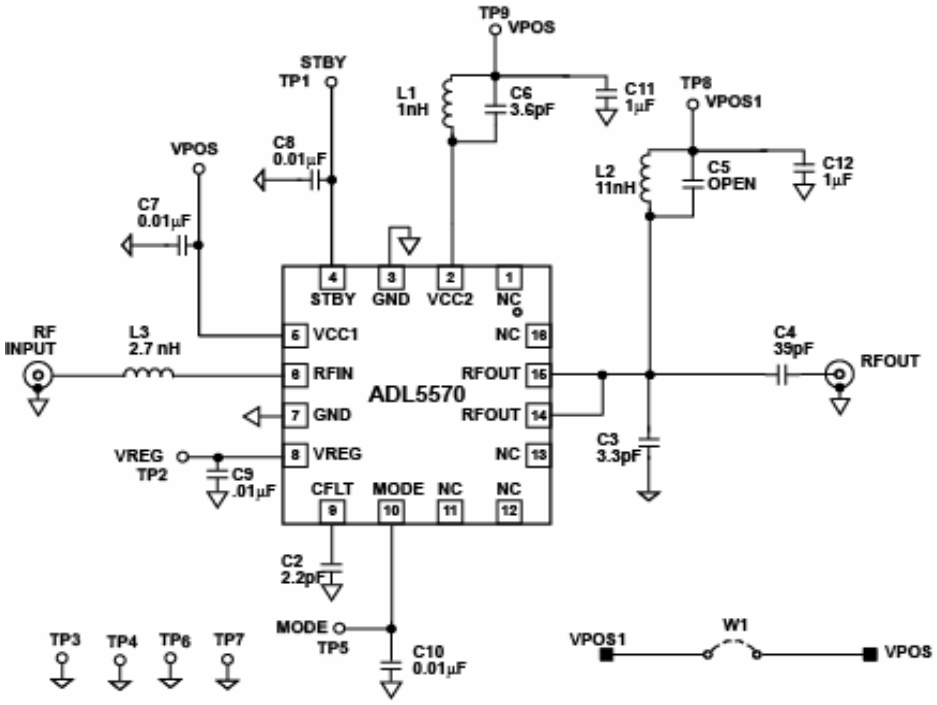

Figure 12. Application Schematic

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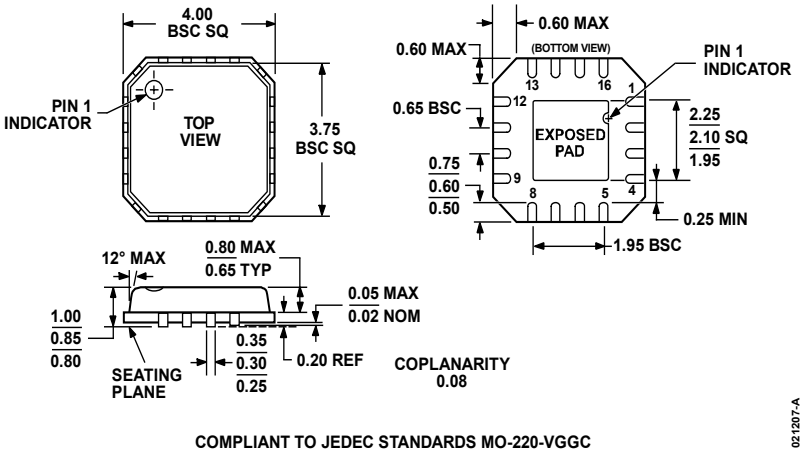
OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 13. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm x 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

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