5.7 kV RMS Signal and Power Isolated RS-485 Transceiver with ±15 kV IEC ESD

Preliminary Technical Data

ADM2867E

FEATURES

- 5.7 kV rms isolated full duplex RS-485/RS-422 transceiver
- Low radiated emissions integrated isolated dc-to-dc converter
- Meets EN55022 Class B radiated emissions requirements on a 2-layer PCB
- Cable invert smart feature
  - Correct reversed cable connection on A, B, Y, and Z bus pins while maintaining full receiver fail-safe feature
- IEC 61000-4-2 ESD protection to ±12 kV contact, ±15 kV air on RS-485 A, B, Y, and Z pins
- High speed 25 Mbps data rate
- Flexible power supplies
  - V_{CC} of 3 V to 5.5 V
  - V_{IO} of 1.7 V to 5.5 V
  - V_{SEL} pin to select V_{ISO} of 3.3 V (V_{CC} > 3 V) or 5 V (V_{CC} > 4.5 V)
- PROFIBUS compliant for 5 V V_{ISO}
- Wide −40°C to +105°C operating temperature range
- High common-mode transient immunity: 250 kV/µs
- Short circuit, open circuit and floating input receiver fail-safe
- Supports 196 bus nodes (72 kΩ receiver input impedance)
- Full hot swap support (glitch free power-up/power-down)
- Safety and regulatory approvals (pending)
- CSA Component Acceptance Notice 5A, DIN V VDE V 0884-11, UL 1577, CQC11-471543-2012, IEC 61010-1
- 28-lead fine pitch SOIC package (10.15 mm × 10.05 mm) with >8.0 mm creepage and clearance

APPLICATIONS

- Heating, ventilation, and air-conditioning (HVAC) networks
- Industrial field buses
- Building automation
- Utility networks

FUNCTIONAL BLOCK DIAGRAM

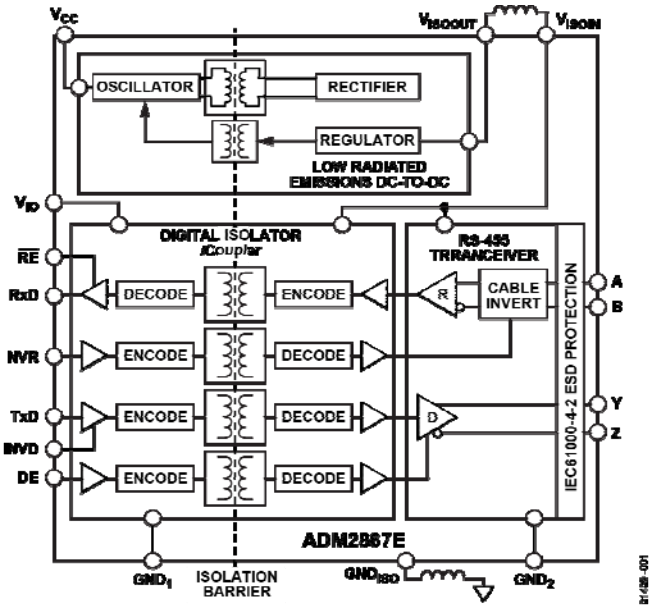

Figure 1. ADM2867E Functional Block Diagram

GENERAL DESCRIPTION

The ADM2867E is a 5.7 kV rms signal and power isolated full duplex RS-485 transceiver which passes radiated emissions testing to the EN55022 Class B standard with margin on a 2-layer PCB using two small external 0402 ferrites on isolated power and ground pins. The isolation barrier provides immunity to system level EMC standards. The ADM2867E has ±12 kV contact, ±15 kV air IEC61000-4-2 ESD protection on RS-485 A, B, Y, and Z pins. The device also features cable invert pins, allowing the user to quickly correct reversed cable connection on A, B, Y, and Z bus pins while maintaining receiver full receiver fail-safe performance. This full duplex device allows for independent cable inversion of the driver and receiver for additional flexibility.

Rev. PrA
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

SPECIFICATIONS

All voltages are relative to their respective ground: 3.0 ≤ V_{CC} ≤ 5.5 V, 1.7 ≤ V_{IO} ≤ 5.5 V, T_{MIN} (−40°C) to T_{MAX} (+105°C). All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{CC} = V_{IO} = 5 V, V_{ISO} = 3.3 V (V_{SEL} = GND_{ISO}) unless otherwise noted. All parameters are characterized with a BLM15HD182SN1 ferrite bead between the V_{ISOOUT} and V_{ISOIN} pins, and between the GND_{ISO} and GND_2 pins.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
NO LOAD SUPPLY CURRENT	I_{CC}		21	46	mA	V_{SEL} = GND_{ISO} (DE = 0 V)
			28	48	mA	V_{CC} ≥ 4.5 V, V_{SEL} = V_{ISO} (DE =0 V)
			20	53	mA	V_{SEL} = GND_{ISO} (DE = V_{IO})
			26	51	mA	V_{CC} ≥ 4.5 V, V_{SEL}= V_{ISO} (DE = V_{IO})
LOGIC SUPPLY CURRENT	I_{IO}		0.65	0.9	mA	DE = 0 V, $\overline{RE}$ = V_{IO}
			5	8	mA	DE = V_{IO}, $\overline{RE}$ = 0 V
ISOLATED SUPPLY VOLTAGE	V_{ISO}					
V_{ISOOUT} and V_{ISOIN}		3	3.3	3.465	V	V_{SEL} = GND_{ISO}, I_{ISOOUT} = 10 mA minimum to 55 mA maximum
		4.5	5.0	5.25	V	V_{CC} ≥ 4.5 V, V_{SEL} = V_{ISO}, I_{ISOOUT} = 10 mA minimum to 90 mA maximum
Start-Up Time	t_{START}		5		ms	DE = GND_1, see the Theory of Operation section
ISOLATED SUPPLY CURRENT						See the Theory of Operation section for description of using surplus I_{ISOOUT} for external circuits
Data Rate = 25 Mbps	I_{ISOIN}		55	75	mA	V_{ISOIN} = 3 V to 3.465 V, 54 Ω between Y and Z
Maximum Current Supply on V_{ISOOUT} Pin	I_{ISOOUT}	90			mA	V_{CC} ≥ 4.5 V, V_{SEL} = V_{ISO}, V_{ISO} > 4.5 V
DRIVER						
Differential Outputs						
Differential Output Voltage, Loaded	$\lvert V_{OD2}\rvert$	2.0	2.4	V_{ISO}	V	V_{CC} ≥ 3.0 V, V_{SEL} = GND_{ISO}, R_L = 100 Ω, see Figure 20
	$\lvert V_{OD2}\rvert$	1.5	2	V_{ISO}	V	V_{CC} ≥ 3.0 V, V_{SEL} = GND_{ISO}, R_L = 54 Ω, see Figure 20
	$\lvert V_{OD2}\rvert$	2.1	3.1	V_{ISO}	V	V_{CC} ≥ 4.5 V, V_{SEL} = V_{ISO}, R_L = 54 Ω, see Figure 20
	$\lvert V_{OD3}\rvert$	1.5	1.9	V_{ISO}	V	V_{CC} ≥ 3.0 V, V_{SEL} = GND_{ISO}, −7 V ≤ V_{CM} ≤ 12 V, see Figure 21
	$\lvert V_{OD3}\rvert$	2.1	3.1	V_{ISO}	V	V_{CC} ≥ 4.5 V, V_{SEL} = V_{ISO}, −7 V ≤ V_{CM} ≤ 12 V, see Figure 21
Δ$\lvert V_{OD2}\rvert$ for Complementary Output States	Δ$\lvert V_{OD2}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 20
Common-Mode Output Voltage	V_{OC}		1.5	3.0	V	R_L = 54 Ω or 100 Ω, see Figure 20
Δ$\lvert V_{OC}\rvert$ for Complementary Output States	Δ$\lvert V_{OC}\rvert$			0.2	V	R_L = 54 Ω or 100 Ω, see Figure 20
Short-Circuit Output Current	I_{OS}	−250		+250	mA	−7 V < V_{OUT} < +12 V
Output Leakage Current (Y, Z)	I_O		1	50	μA	DE = $\overline{RE}$ = 0 V, V_{CC} = 0 V or 5.5 V, V_{IN} = 12 V
		−50	10		μA	DE = $\overline{RE}$ = 0 V, V_{CC} = 0 V or 5.5 V, V_{IN} = −7 V
Digital Logic Inputs						
Input Low Voltage	V_{IL}			0.3 × V_{IO}	V	DE, $\overline{RE}$, TxD, INVR, INVD
Input High Voltage	V_{IH}	0.7 × V_{IO}			V	DE, $\overline{RE}$, TxD, INVR, INVD
Input Current	I_I	−1	0.1	2	μA	DE, $\overline{RE}$, TxD, V_{IN} = 0 V or V_{IO}
		−1	10	30	μA	INVR, INVD, V_{IN} = 0 V or V_{IO}
Pin Capacitance						
Y, Z Pins	C_{IN}		28		pF	Input voltage (V_{IN}) = 0.4sin(10πt × 10^6)
A, B Pins			4		pF	V_{IN} = 0.4sin(10πt × 10^6)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
RECEIVER						
Differential Inputs						
Differential Input Threshold Voltage	V_{TH}	−200	−125	−30	mV	−7 V < common-mode voltage (V_{CM}) < +12 V, INVR = 0 V
		30	125	200	mV	−7 V < V_{CM} < +12 V, INVR = V_{IO}
Input Voltage Hysteresis	V_{HYS}		25		mV	−7 V < V_{CM} < +12 V
Input Current (A, B)	I_I			167	µA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = +12 V
		−133			µA	DE = 0 V, V_{CC} = powered/unpowered, V_{IN} = −7 V
Logic Outputs						
Output Voltage Low	V_{OL}			0.4	V	V_{IO} = 3.6 V, I_{OUT} = 2.0 mA, $V_A - V_B \leq -0.2$ V, INVR = 0
				0.4	V	V_{IO} = 2.7 V, I_{OUT} = 1.0 mA, $V_A - V_B \leq -0.2$ V, INVR = 0
				0.2	V	V_{IO} = 1.95 V, I_{OUT} = 500 µA, $V_A - V_B \leq -0.2$ V, INVR = 0
Output Voltage High	V_{OH}	2.4			V	V_{IO} = 3.0 V, I_{OUT} = −2.0 mA, $V_A - V_B \geq -0.03$ V, INVR = 0
		2.0			V	V_{IO} = 2.3 V, I_{OUT} = −1.0 mA, $V_A - V_B \geq -0.03$ V, INVR = 0
		V_{IO} − 0.2			V	V_{IO} = 1.7 V, I_{OUT} = −500 µA, $V_A - V_B \geq -0.03$ V, INVR = 0
Short-Circuit Current				100	mA	V_{OUT} = 0 V or V_{IO}, $\overline{RE}$ = 0 V
Three-State Output Leakage Current	I_{OZR}	−1	0.01	+1	µA	$\overline{RE}$ = V_{IO}, RxD = 0 V or V_{IO}
COMMON-MODE TRANSIENT IMMUNITY[1]	CMTI	250			kV/µs	$V_{CM} \geq \pm 1$ kV, transient magnitude measured at between 20% and 80% of V_{CM}, see Figure 32

[1] CMTI is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation. V_{CM} is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common-mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

TIMING SPECIFICATIONS

All minimum/maximum specifications apply over the entire recommended operation range, V_{CC} = 3.0 V to 5.5 V, V_{IO} = 1.7 V to 5.5 V, T_A = T_{MIN} (−40°C) to T_{MAX} (+105°C). All typical specifications are at T_A = 25°C, V_{CC} = V_{IO} = 5 V, V_{ISO} = 3.3 V (V_{SEL} = GND_{ISO}). All parameters are characterized with a BLM15HD182SN1 ferrite bead between the V_{ISOOUT} and V_{ISOIN} pins, and between the GND_{ISO} and GND_2 pins.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DRIVER						
Maximum Data Rate		25			Mbps	
Propagation Delay	t_{DPLH}, t_{DPHL}		18	25	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 22 and Figure 26
Output Skew	t_{SKEW}		1.5	5	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 22 and Figure 26
Rise Time/Fall Time	t_{DR}, t_{DF}		4.5	10	ns	R_L = 54 Ω, C_{L1} = C_{L2} = 100 pF, see Figure 22 and Figure 26
Enable Time	t_{ZL}, t_{ZH}		25	40	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 23 and Figure 28
Disable Time	t_{LZ}, t_{HZ}		20	40	ns	R_L = 110 Ω, C_L = 50 pF, see Figure 23 and Figure 28
RECEIVER						
Propagation Delay	t_{RPLH}, t_{RPHL}		32	50	ns	C_L = 15 pF, see Figure 24 and Figure 27
Output Skew	t_{SKEW}		2	6	ns	C_L = 15 pF, see Figure 24 and Figure 27
Enable Time	t_{ZL}, t_{ZH}		4	25	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 25 and Figure 29
Disable Time	t_{LZ}, t_{HZ}		8	25	ns	R_L = 1 kΩ, C_L = 15 pF, see Figure 25 and Figure 29
RECEIVER CABLE INVERT, INVR						
Propagation Delay, High to Low	$t_{INVRPHL}$		25	35	ns	Differential input voltage (V_{ID}) ≥ +200 mV or V_{ID} ≤ −200 mV, see Figure 30
Propagation Delay, Low to High	$t_{INVRPLH}$		25	35	ns	V_{ID} ≥ +200 mV or V_{ID} ≤ −200 mV, see Figure 30
DRIVER CABLE INVERT, INVD						
Propagation Delay, High to Low	$t_{INVDPHL}$		18	25	ns	TxD = 0 V or TxD = V_{IO}, see Figure 31
Propagation Delay, Low to High	$t_{INVDPLH}$		18	25	ns	TxD = 0 V or TxD = V_{IO}, see Figure 31

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input to Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input to Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		3.0		pF	Input capacitance

[1] Device considered a 2-terminal device: short together Pin 1 to Pin 14 and short together Pin 15 to Pin 28.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

Table 4. ADM2867E Approvals

Organization	Approval Type	Notes
UL	To be recognized under UL 1577 component recognition program	Single protection, 5700 V rms isolation voltage; in accordance with UL 1577, each ADM2867E is proof tested by applying an insulation test voltage ≥ 6840 V rms for 1 sec
VDE	To be certified according to DIN V VDE V 0884-11	Basic insulation, V_{IOWM} = 400 V rms, V_{IORM} = 560 V peak, V_{IOSM} = 10000 V peak Reinforced insulation, V_{IOWM} = 400 V rms, V_{IORM} = 560 V peak, V_{IOSM} = 6250 V peak In accordance with DIN V VDE 0884-11, each ADM2867E is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 sec (partial discharge detection limit = 5 pC)

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 5. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		5700	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.3	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.3	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L (PCB)	8.1	mm	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		22	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>600	V	DIN IEC 112/VDE 0303 Part 1
Material Group		I		Material Group (DIN VDE 0110: 1989-01, Table 1)

DIN V VDE 0884-11 (VDE 0884-11) INSULATION CHARACTERISTICS (PENDING)

This isolator is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data must be ensured by means of protective circuits.

Table 6.

Description	Test Conditions	Symbol	Characteristic	Unit
CLASSIFICATIONS				
Installation Classification per DIN VDE 0110 for Rated Mains Voltage				
≤150 V rms			I to IV	
≤300 V rms			I to IV	
≤600 V rms			I to IV	
Climatic Classification			40/105/21	
Pollution Degree	Per DIN VDE 0110, Table 1		2	
VOLTAGE				
Maximum Working Insulation Voltage		V_{IOWM}	400	V rms
Maximum Repetitive Peak Insulation Voltage		V_{IORM}	560	V peak
Input to Output Test Voltage		V_{PR}		
Method b1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production tested, t_m = 1 sec, partial discharge < 5 pC		1050	V peak
Method a				
After Environmental Tests, Subgroup 1	$V_{IORM} \times 1.5 = V_{pd}(m)$, t_{ini} = 60 sec, t_m= 10 sec, partial discharge < 5 pC		840	V peak
After Input and/or Safety Test, Subgroup 2/Subgroup 3	$V_{IORM} \times 1.2 = V_{pd}(m)$, t_{ini} = 60 sec, t_m= 10 sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{IOTM}	8000	V peak
Surge Isolation Voltage, Basic	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	10,000	V peak
Surge Isolation Voltage, Reinforced	V_{PEAK} = 10 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	6250	V peak
SAFETY LIMITING VALUES	Maximum value allowed in the event of a failure			
Case Temperature		T_S	150	°C
Total power dissipation at 25C		P_S	2.77	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

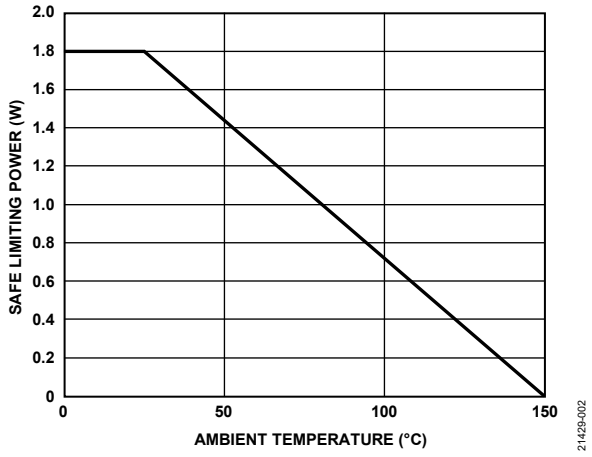

Figure 2. Thermal Derating Curve for 28-Lead Standard Small Outline, Wide Body, with Finer Pitch (SOIC_W_FP), Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. All voltages are relative to their respective ground.

Table 7.

Parameter	Rating
V_{CC} to GND_1	6 V
V_{IO} to GND_1	−0.5 V to +7.0 V
Digital Input Voltage (DE, $\overline{RE}$, TxD, INV, INVR, INVD) to GND_1	−0.3 V to V_{IO} +0.3 V
Digital Output Voltage (RxD) to GND_1	−0.3 V to V_{IO} +0.3 V
Driver Output/Receiver Input Voltage to GND_2	−9 V to +14 V
Operating Temperature Range	−40°C to +105°C
Storage Temperature Range	−55°C to +150°C
ESD on the Bus Pins (A, B, Y, Z to GND_2)	
IEC 61000-4-2 Contact Discharge	±12 kV
IEC 61000-4-2 Air Discharge	±15 kV
IEC 61000-4-2 ESD Across Isolation Barrier (A, B, Y, Z to GND_1)	±8 kV
ESD (Human Body Model) on Other Pins	±4 kV
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one -cubic foot sealed enclosure.

Table 8. Thermal Resistance

Package Type	θ_{JA}	Unit
RN-28-1[1]	43.45	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

Table 9. Maximum Continuous Working Voltage[1, 2]

Parameter	Max	Unit	Reference Standard
AC Voltage			
Bipolar Waveform			
Basic Insulation	565	V peak	50-year minimum lifetime
Reinforced Insulation	565	V peak	50-year minimum lifetime
Unipolar Waveform			
Basic Insulation	1131	V peak	50-year minimum lifetime
Reinforced Insulation	1131	V peak	50-year minimum lifetime
DC Voltage			
Basic Insulation	565	V DC	50-year minimum lifetime
Reinforced Insulation	565	V DC	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.
[2] Values quoted for Material Group I, Pollution Degree II.
[1] Thermocouple located at center of package underside.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

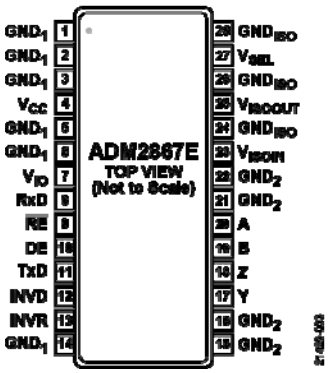

Figure 3. ADM2867E Pin Configuration

Table 10. Pin Function Description

Pin No.	Mnemonic	Description
1, 2, 3, 5, 6, 14	GND_1	Ground 1, Logic Side.
4	V_{CC}	3.0 V to 3.6 V, or 4.5 V to 5.5 V Logic Side Power Supply. It is recommended that a 10 µF and a 0.1 µF decoupling capacitor be connected between V_{CC} and GND_1 (Pin 1, Pin 2, and Pin 3).
7	V_{IO}	1.7 V to 5.5 V Flexible Logic Interface Supply. It is recommended that a 0.1 µF decoupling capacitor be connected between V_{IO} and GND_1 (Pin 5 and Pin 6).
8	RxD	Receiver Output Data. When the INVR pin is logic low, this output is high when (A − B) > −30 mV and low when (A − B) < −200 mV. When the INVR pin is high, this output is high when (A − B) < +30 mV and low when (A − B) > +200 mV. This output is tristated when the receiver is disabled by driving the $\overline{RE}$ pin low.
9	$\overline{RE}$	Receiver Enable Input. This pin is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver.
10	DE	Driver Output Enable. A high level on this pin enables the driver differential outputs, Y and Z. A low level places them into a high impedance state.
11	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input. When the INVD pin is logic high, the data applied to this input is inverted.
12	INVD	Driver Inversion Enable. This pin is active high input. Driving this pin high inverts the TxD signal applied.
13	INVR	Receiver Inversion Enable. This pin is active high input. Driving this pin high inverts the A and B inputs.
15, 16, 21, 22	GND_2	Isolated Ground 2 for the integrated RS-485 transceiver, Bus Side.
17	Y	Driver Noninverting Output.
18	Z	Driver Inverting Output.
19	B	Receiver Inverting Input.
20	A	Receiver Noninverting Input.
23	V_{ISOIN}	Isolated Power Supply Input. This pin must be connected externally to V_{ISOOUT} (Pin 25) through one BLM15HD182SN1 ferrite. It is recommended that a reservoir capacitor of 10 µF and two decoupling capacitors of 0.1 µF be connected between V_{ISOIN} (Pin 23) and GND_2 (Pin 21).
24, 26	GND_{ISO}	Isolated Power Supply ground. These pins must be connected externally to Pin 28.
25	V_{ISOOUT}	Isolated Power Supply Output. This pin must be connected externally to V_{ISOIN} (Pin 23) through one BLM15HD182SN1 ferrite. It is recommended that a decoupling capacitor of 0.1 µF be connected between V_{ISOOUT} and GND_{ISO} (Pin 28).
27	V_{SEL}	Output Voltage Selection. When $V_{SEL} = V_{ISO}$, the V_{ISO} set point is 5.0 V. When $V_{SEL} = GND_{ISO}$, the V_{ISO} set point is 3.3 V.
28	GND_{ISO}	Isolated Power Supply ground. This pin must be connected externally to GND_2 (Pin 22) through one BLM15HD182SN1 ferrite.

TYPICAL PERFORMANCE CHARACTERISTICS

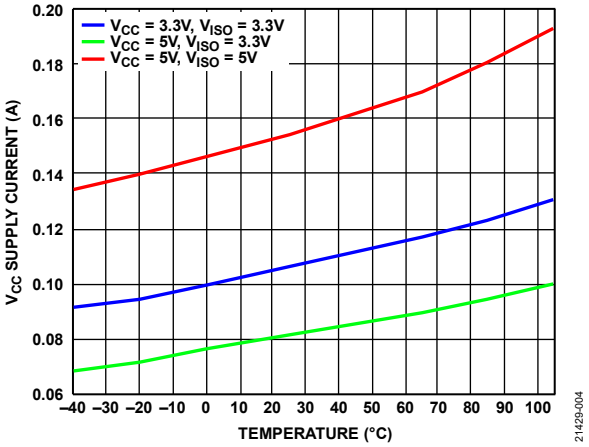

Figure 4. V_{CC} Supply Current vs. Temperature at 25 Mbps, No Load

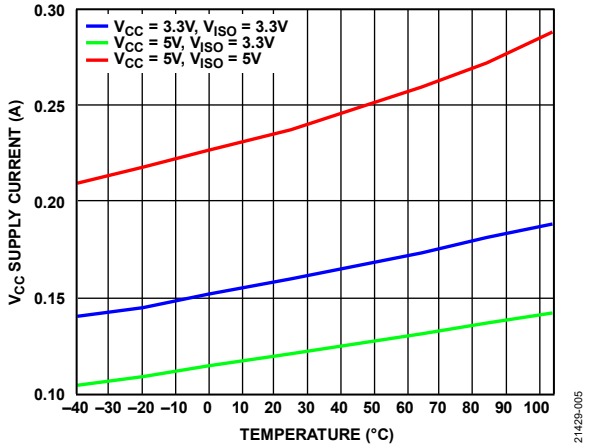

Figure 5. V_{CC} Supply Current vs. Temperature at 25 Mbps, 120 Ω Load

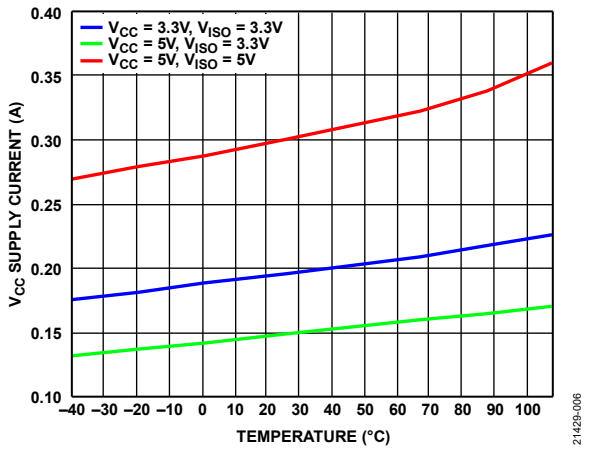

Figure 6. V_{CC} Supply Current vs. Temperature at 25 Mbps, 54 Ω Load

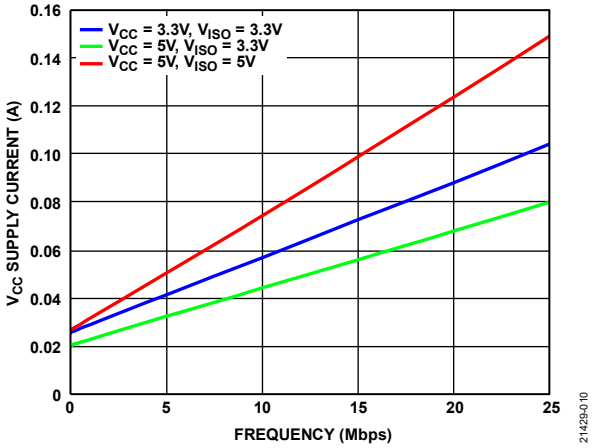

Figure 7. V_{CC} Supply Current vs. Frequency, T_A = 25°C, No Load

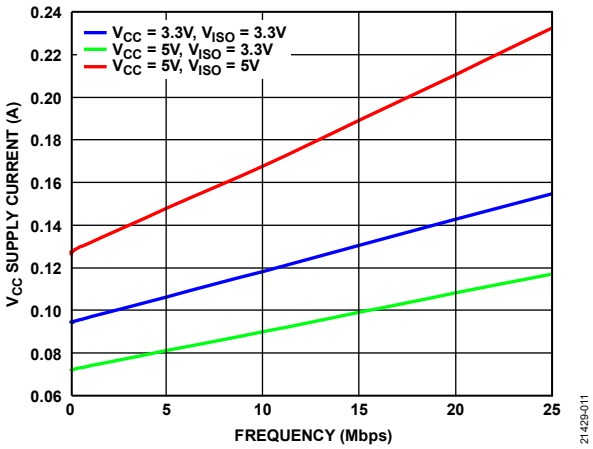

Figure 8. V_{CC} Supply Current vs. Frequency, T_A = 25°C, 120 Ω Load

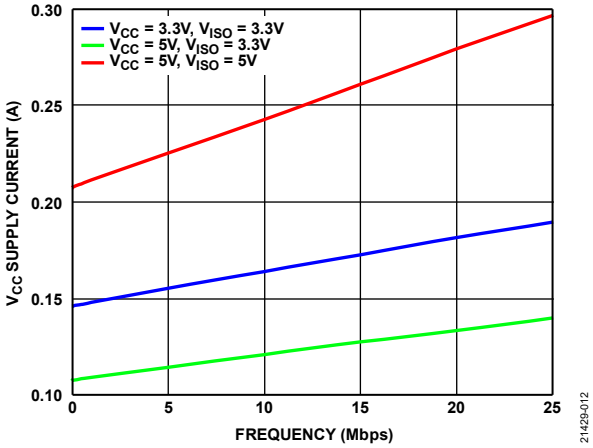

Figure 9. V_{CC} Supply Current vs. Frequency, T_A = 25°C, 54 Ω Load

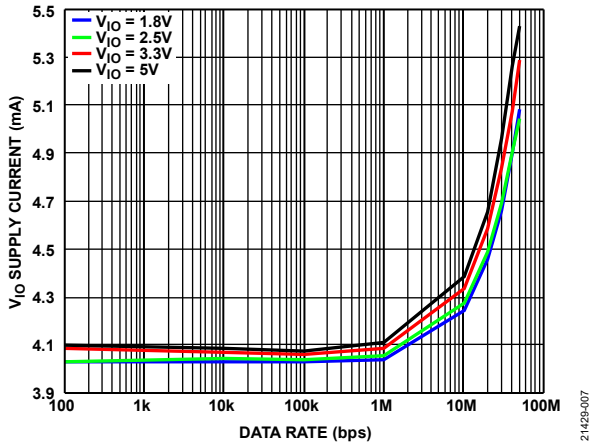

Figure 10. V_{IO} Supply Current vs. Data Rate

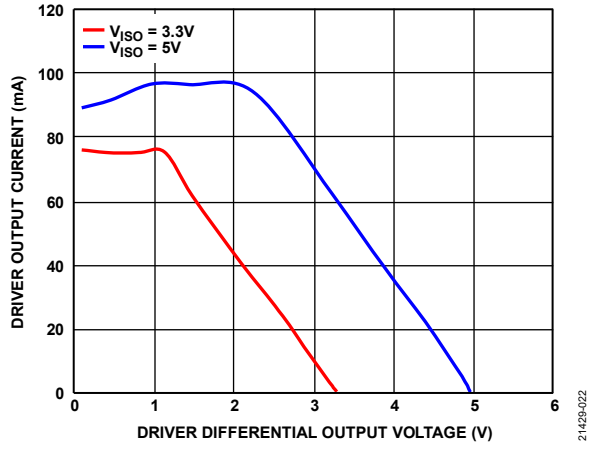

Figure 11. Driver Output Current vs. Driver Differential Output Voltage

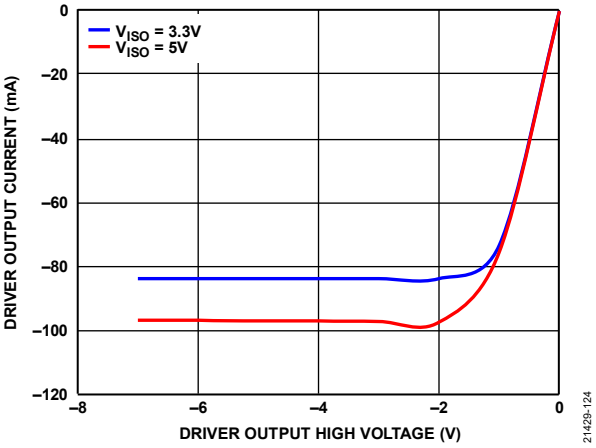

Figure 12. Driver Output Current vs. Driver Output High Voltage

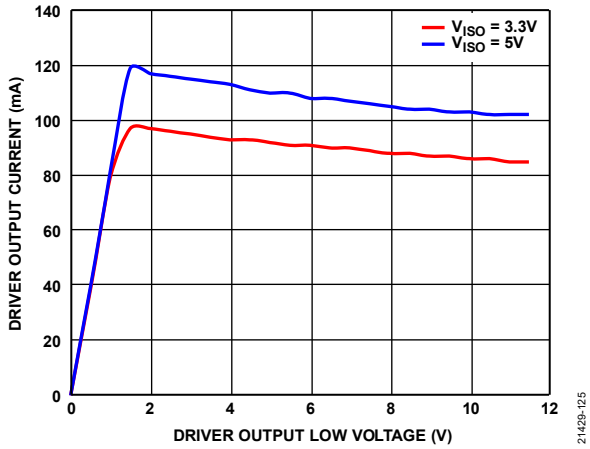

Figure 13. Driver Output Current vs. Driver Output Low Voltage

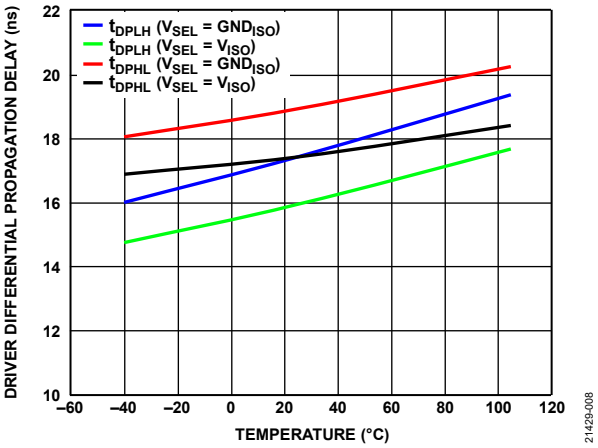

Figure 14. Driver Differential Propagation Delay vs. Temperature

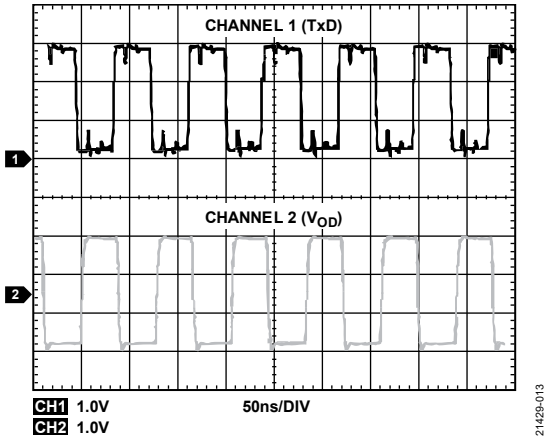

Figure 15. Transmitter Switching at 25 Mbps

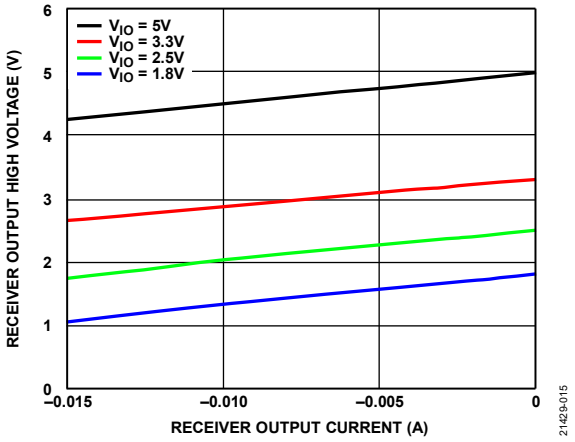

Figure 16. Receiver Output High Voltage vs. Receiver Output Current

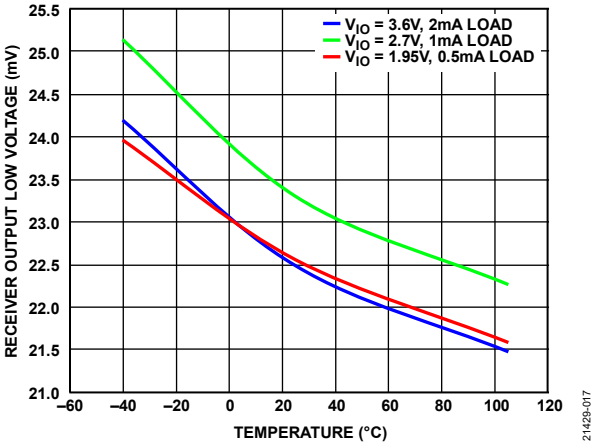

Figure 18. Receiver Output Low Voltage vs. Temperature

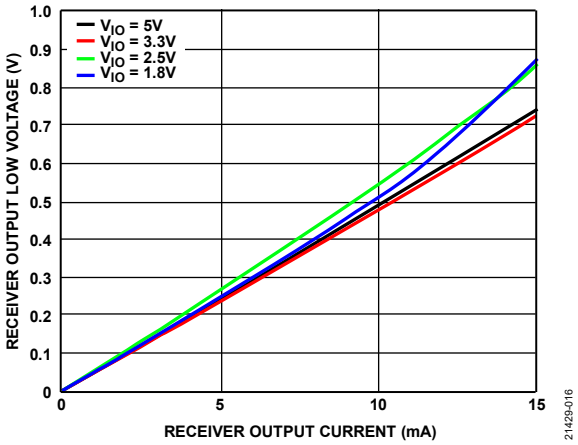

Figure 17. Receiver Output Low Voltage vs. Receiver Output Current

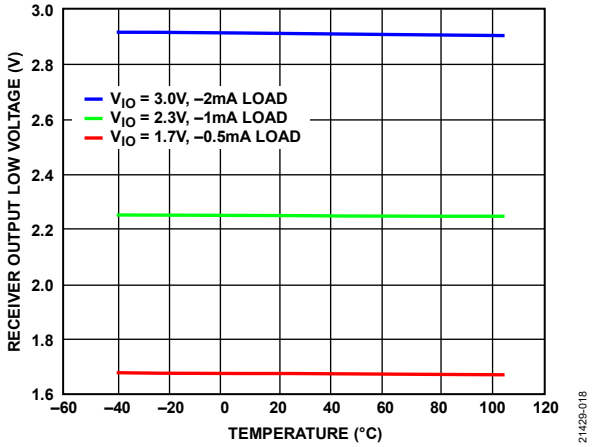

Figure 19. Receiver Output Low Voltage vs. Temperature

TEST CIRCUITS AND SWITCHING CHARACTERISTICS

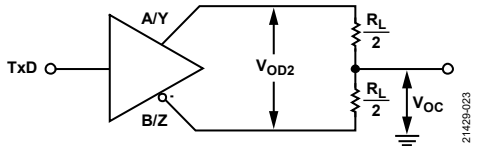

Figure 20. Driver Voltage Measurement

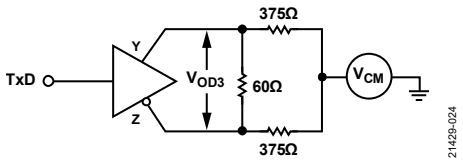

Figure 21. Driver Voltage Measurement over Common Mode Range

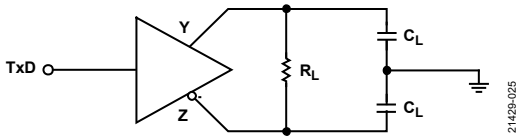

Figure 22. Driver Propagation Delay Measurement

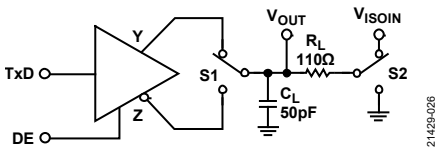

Figure 23. Driver Enable or Disable Time Measurement

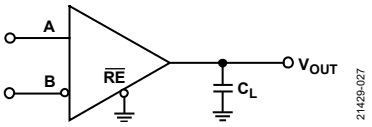

Figure 24. Receiver Propagation Delay Time Measurement

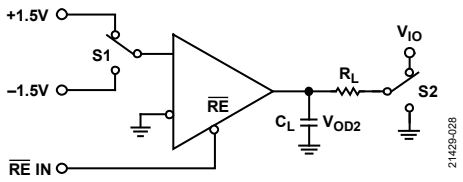

Figure 25. Receiver Enable or Disable Time Measurement

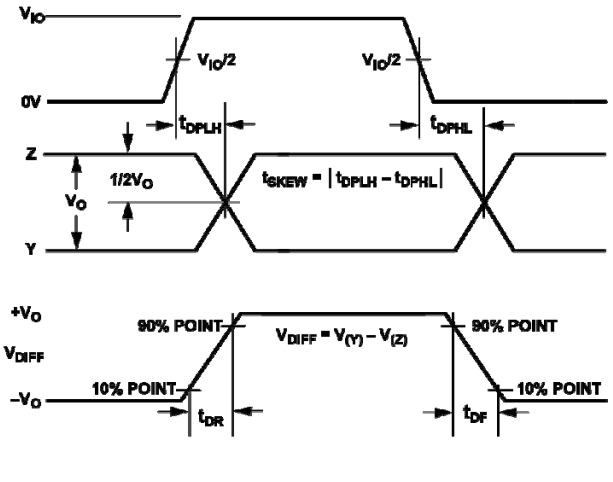

Figure 26. Driver Propagation Delay, Rise/Fall Timing

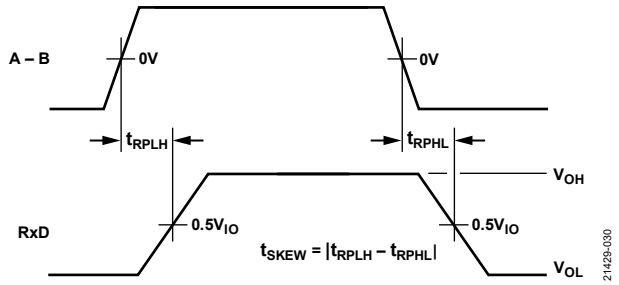

Figure 27. Receiver Propagation Delay

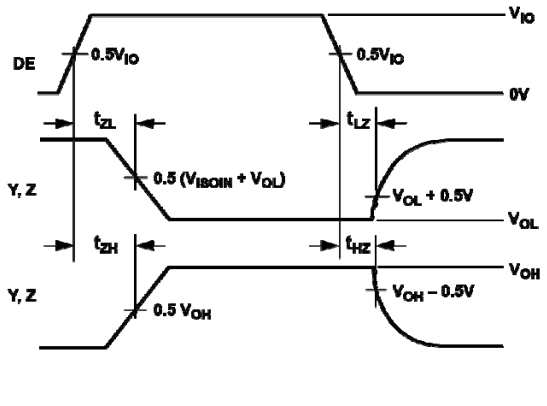

Figure 28. Driver Enable or Disable Timing

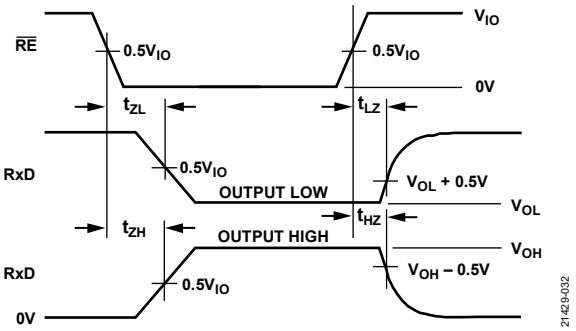

Figure 29. Receiver Enable or Disable Timing

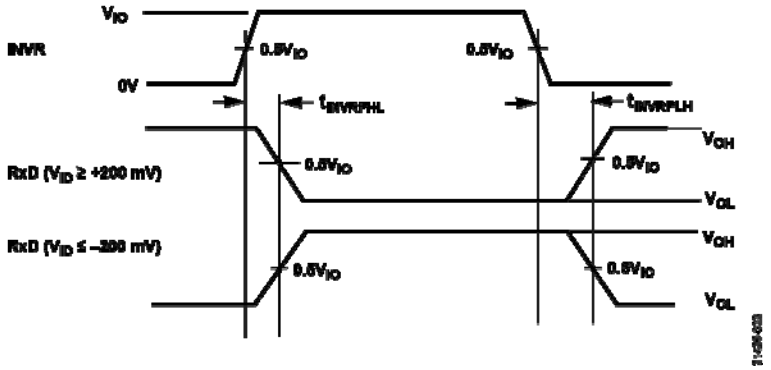

Figure 30. Receiver INVR Cable Invert Timing

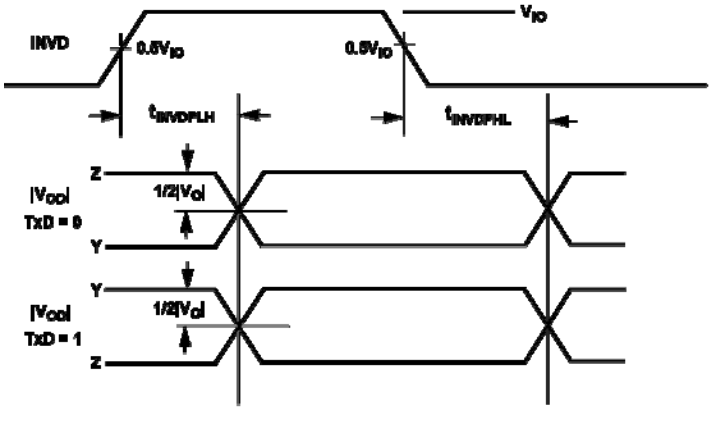

Figure 31. Driver INVD Cable Invert Timing

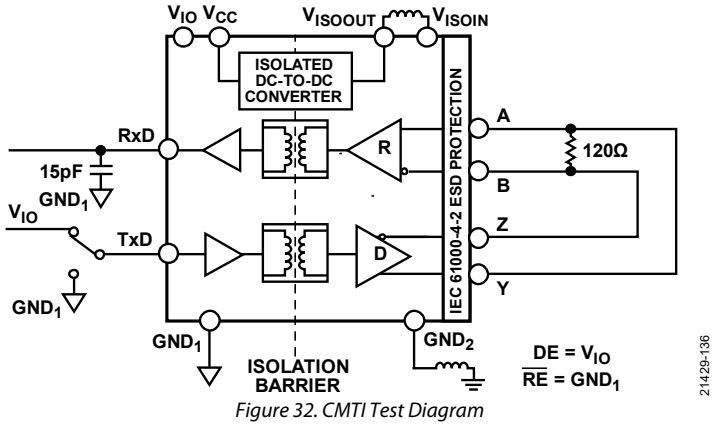

Figure 32. CMTI Test Diagram

THEORY OF OPERATION

LOW EMI INTEGRATED DC-TO-DC CONVERTER

The ADM2867E includes a flexible integrated dc-to-dc converter optimized for low radiated emissions (EMI). The isolated dc-to-dc converter is constructed of a set of chip scale coplanar coils that are separated by an insulating material. By exciting the upper coil with an ac signal, power is magnetically coupled across the isolation barrier where it is rectified and regulated. Because no direct electrical connection exists between the top and bottom coil, the primary and secondary side of the device remain galvanically isolated.

This isolated dc-to-dc converter features a regulated output of either 3.3 V or 5 V, selectable via the V_{SEL} logic pin, which allows the user to optimize the supply rail of the RS-485 transceiver for their application. For lower power applications, a 3.3 V supply can be chosen. For applications requiring a large differential output voltage, such as PROFIBUS®, the isolated dc-to-dc converter can be operated with a 5 V output. Table 11 shows the supported supply configurations for the isolated dc-to-dc converter

Table 11. Isolated DC-to-DC Converter Supply Configuration

V_{SEL} Pin	V_{ISO} Output Supply Voltage	V_{CC} Input Supply Voltage
Connected to GND_{ISO}	3.3 V	3 V to 5.5 V
Connected to V_{ISOOUT}	5 V	4.5 V to 5.5 V

The integrated dc-to-dc converter is optimized to minimize radiated electromagnetic interference (EMI), and allows designers to meet the CISPR22/EN55022 Class B requirements on a 2-layer PCB with the addition of two low cost surface-mount device (SMD) ferrites. Care should be taken when designing PCB layouts to minimize these emissions. See the PCB Layout and Electromagnetic Interference (EMI) section for more details.

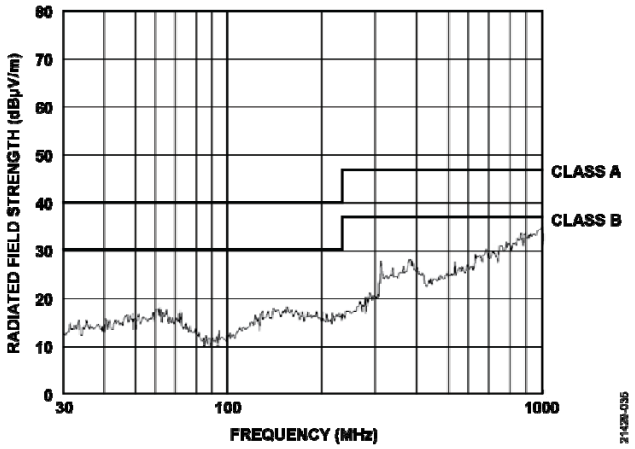

Figure 33. Low Radiated Emissions DC-to-DC Converter Meets EN55022 Class B with Margin on a 2-Layer PCB

ROBUST LOW POWER DIGITAL ISOLATOR

The ADM2867E features a low power digital isolator block to galvanically isolate the primary and secondary side of the device. The use of coplanar transformer coils with an on and off keying modulation scheme allows high data throughput across the isolation barrier while minimizing radiation emissions. This architecture provides a robust digital isolator with immunity to common-mode transients of greater than 250 kV/µs across the full temperature and supply range of the device.

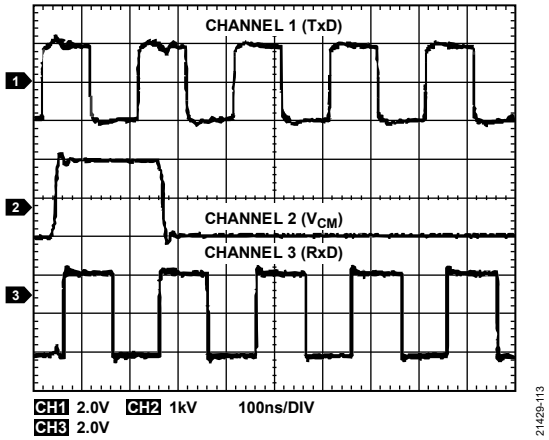

Figure 34. Switching Correctly in the Presence of >250 kV/µs Common-Mode Transients

HIGH DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM2867E features a proprietary transmitter architecture with a low driver output impedance, resulting in an increased differential output voltage. This architecture is particularly useful when operating the device at lower data rates over long cable runs, where the dc resistance of the transmission line dominates signal attenuation. In these applications, the increased differential voltage extends the reach of the device to longer cable lengths. In addition, when operated as a 5 V transceiver (V_{SEL} = V_{ISO}), the ADM2867E meets or exceeds the PROFIBUS requirement of a minimum 2.1 V differential output voltage.

IEC61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. ESD has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT. A number of factors affect

the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT. Air discharge testing is a more accurate representation of an actual ESD event but is not as repeatable. Therefore, contact discharge is the preferred test method. During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment. Figure 35 shows the 8 kV contact discharge current waveform as described in the IEC 61000-4-2 specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns.

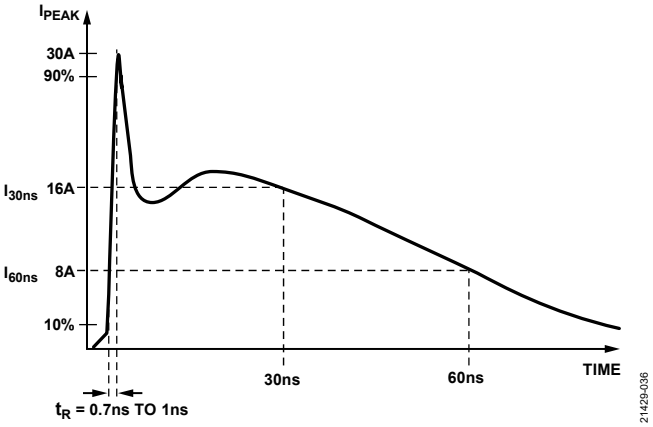

Figure 35. IEC61000-4-2 ESD Waveform (8 kV)

Figure 36 shows the 8 kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the HBM ESD 8 kV waveform. Figure 36 shows that the two standards specify a different waveform shape and peak current. The peak current associated with an IEC 61000-4-2 8 kV pulse is 30 A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33 A. The other difference is the rise time of the initial voltage spike, with the IEC 61000-4-2 ESD waveform having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to three positive and three negative discharges, whereas in comparison, the IEC ESD standard requires 10 positive and 10 negative discharge tests.

The ADM2867E with IEC 61000-4-2 ESD ratings is better suited for operation in harsh environments compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

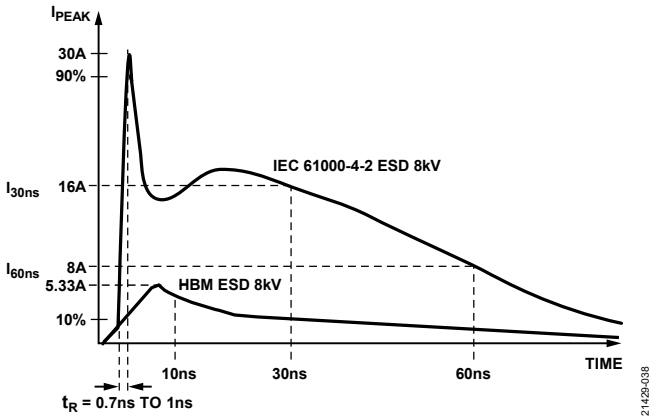

Figure 36. IEC61000-4-2 ESD Waveform 8 kV compared to HBM ESD Waveform 8 kV

TRUTH TABLES

Table 13 and Table 14 use the abbreviations shown in Table 12. V_{IO} supplies the DE, TxD, $\overline{RE}$, RxD, INVR, INVD pins only.

Table 12. Truth Table Abbreviations

Letter	Description
H	High level
I	Indeterminate
L	Low level
X	Any state
Z	High impedance (off)

Table 13. Transmitting Truth Table

Supply Status		Inputs			Outputs	
V_{CC}	V_{IO}	DE	TxD	INVD	Y	Z
On	On	H	H	L	H	L
On	On	H	H	H	L	H
On	On	H	L	L	L	H
On	On	H	L	H	H	L
On	On	L	X	X	Z	Z
On	Off	X	X	X	Z	Z
Off	X	X	X	X	Z	Z

Table 14. Receiving Truth Table

Supply Status		Inputs			Outputs
V_{CC}	V_{IO}	A – B	INVR	$\overline{RE}$	RxD
On	On	≥−0.03 V	L	L	H
On	On	≤0.03 V	H	L	H
On	On	≤−0.2 V	L	L	L
On	On	≥0.2 V	H	L	L
On	On	−0.2 V < A – B < −0.03 V	L	L	I
On	On	0.03 V < A – B < 0.2 V	H	L	I
On	On	Inputs open/shorted	X	L	H
X	On	X	X	H	Z
X	Off	X	X	X	I
Off	On	X	X	L	I

RECEIVER FAIL-SAFE

The ADM2867E guarantees a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled. When the receiver inversion feature is disabled (INVR = 0 V), a fail-safe logic high output is achieved by setting the receiver input threshold between −30 mV and −200 mV. If the differential receiver input voltage (A − B) is greater than or equal to −30 mV, the RxD pin is logic high. If the A − B input is less than or equal to −200 mV, RxD is logic low. Fail-safe is preserved when the receiver inversion feature is enabled (INVR = V_{IO}) by setting the inverted receiver input threshold between 30 mV and 200 mV. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0 V by the termination resistor, resulting in a logic high with a 30 mV minimum noise margin. This feature eliminates the need for external biasing components usually required to implement fail-safe.

The feature is fully compatible with external fail-safe biasing configurations, which must be used in applications that require support for legacy nonfail-safe devices, or in applications where additional noise margin is desired.

DRIVER AND RECEIVER CABLE INVERSION

The ADM2867E features cable inversion functionality to correct for errors during installation. This correction can be implemented in software on the controller driving the RS485 transceiver and helps avoid additional installation costs to fix wiring errors. The ADM2867E features separate digital logic pins, INVD and INVR, to correct cases where the driver and/or receiver are wired incorrectly. Use the INVD pin to correct driver functionality when Y and Z are wired incorrectly. Use the INVR pin to correct receiver functionality when A and B are wired incorrectly. When the receiver is inverted, the device maintains a Logic 1 receiver output with a 30 mV noise margin when inputs are shorted together or open circuit. Figure 37 shows the receiver output in both inverted and noninverted cases.

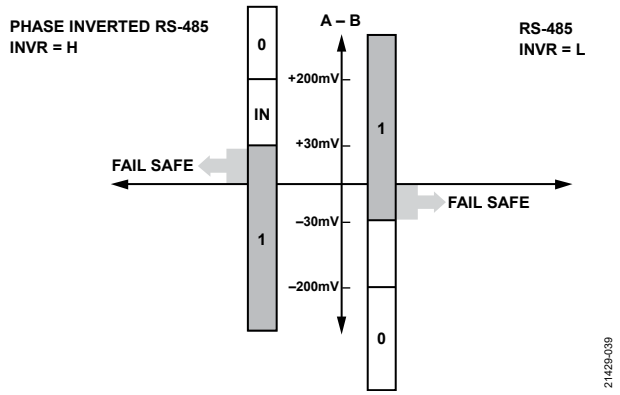

Figure 37. RS-485 and Phase Inverted RS-485 Comparison

HOT SWAP INPUTS

When a circuit board is inserted into a powered (or hot) backplane, parasitic coupling from supply and ground rails to digital inputs can occur. In addition, because the ADM2867E has both a low voltage logic supply, V_{IO}, and a V_{CC} power supply pin, a number of different power supply sequences and conditions can occur.

The ADM2867E contains circuitry to ensure the Y and Z outputs remain in a high impedance state during power-up, and then default to the correct states. For example, when V_{IO} and V_{CC} power up at the same time and the $\overline{RE}$ pin is pulled low, with the DE and TxD pins pulled high, the Y and Z outputs remain in high impedance until settling at an expected default high for the Y pin and expected default low for the Z pin.

196 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12 kΩ (1 unit load), and the standard driver can drive up to 32 unit loads. The ADM2867E transceiver has a 1/6 unit load receiver input impedance (72 kΩ), allowing up to 196 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

DRIVER OUTPUT PROTECTION

The ADM2867E features two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current-limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are reenabled at a temperature of 140°C.

1.7 V TO 5.5 V V_{IO} LOGIC SUPPLY

The ADM2867E features a V_{IO} logic supply pin to allow a flexible digital interface operational to voltages as low as 1.7 V. The V_{IO} pin powers the primary side of the signal isolation, the logic inputs, and the RxD output. These input and output pins interface with logic devices such as universal asynchronous receiver/transmitters (UARTs), application specific integrated circuits (ASICs), and microcontrollers. For applications where these devices use an input/output (I/O) operating at power supplies other than the ADM2867E V_{CC} supply voltage, the V_{IO} supply can be powered from the supply rail as the logic device. The V_{IO} supply accepts a supply voltage between 1.7 V and 5.5 V, allowing communication with 1.8 V, 2.5 V, 3.3 V, and 5 V devices.

APPLICATIONS INFORMATION

PCB LAYOUT AND ELECTROMAGNETIC INTERFERENCE (EMI)

The ADM2867E meets EN 55022 Class B/CISPR 22 radiated emissions requirements. Two external SMT ferrite beads are used to pass the Class B limits with margin. No additional mitigation techniques such as stitching capacitance are needed, allowing system designers to create a compliant design on a 2-layer PCB, without the need for complex techniques such as stitching capacitance.

The ADM2867E features an internal split paddle lead frame on the bus side. For optimal noise suppression, filter the V_{ISOOUT} signal (Pin 25) and GND_{ISO} signal (Pin 24, Pin 26, and Pin 28) for high frequency currents before routing power to the RS-485 transceiver or to other circuitry. Two SMT ferrite beads, L1 and L2, are recommended to achieve this filtering. The size of the V_{ISOOUT} and GND_{ISO} net must also be kept to a minimum. See Figure 38 for the recommended PCB layout.

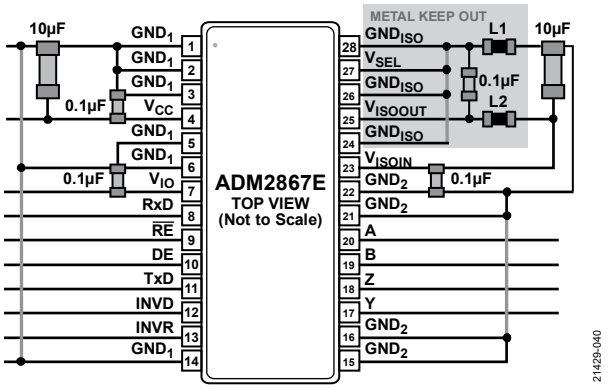

Figure 38. Recommended PCB Layout

The *iso*Power® integrated dc-to-dc converter contains switching frequencies between 180 MHz and 400 MHz. To effectively filter these frequencies, the impedance of the ferrite bead is chosen to be about 2 kΩ between the 100 MHz and 1 GHz frequency range. Some recommended SMT ferrites are shown in Table 15. Although these ferrite beads are required to achieve compliance to EN 55022 Class B, they are not needed for system functionality. The ADM2867E has been fully characterized with the recommended BLM15HD182SN1 ferrite beads.

Table 15. Surface-Mount Ferrite Beads Example

Manufacturer	Part No.
Murata Electronics	BLM15HD182SN1
Taiyo Yuden	BKH1005LM182-T

Because it is not possible to apply a heat sink to an isolation device, the devices primarily depend on heat dissipation into the PCB through the GND pins. If the devices are used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane. The use of a solid GND_1 and GND_2 plane is recommended. Implementing a low thermal impedance between the top ground layers and internal ground layers reduce the temperature inside the chip significantly.

POWER UP SEQUENCING

The integrated *iso*Power isolated dc-to-dc converter requires up to 10 ms to power up to its set point of 3.3 V or 5 V. During this start-up time, it is not recommended to assert the DE driver enable signal.

In applications where the isolated dc-to-dc converter is operated with a 3.3 V output voltage (V_{SEL} pin connected to GND_{ISO}), the V_{CC} supply rail must be greater than 3.135 V during the power-up sequence. After the 10 ms power-up duration, the V_{CC} supply rail can operate across the full 3 V to 5.5 V range.

EMC/EFT/SURGE

In applications where additional levels of protection against IEC61000-4-5 EFT or IEC61000-4-4 surge events are required, external protection circuits can be added to further enhance the EMC robustness of these devices. See Figure 39 for a recommended protection circuit, which uses a series of SM712 transient voltage suppressor (TVS) and 10 Ω pulse proof resistors to achieve in excess of Level 4 IEC61000-4-2 ESD and IEC61000-4-4 EFT protection, and Level 2 IEC61000-4-5 surge protection. Table 16 details the protection levels and recommended protection components.

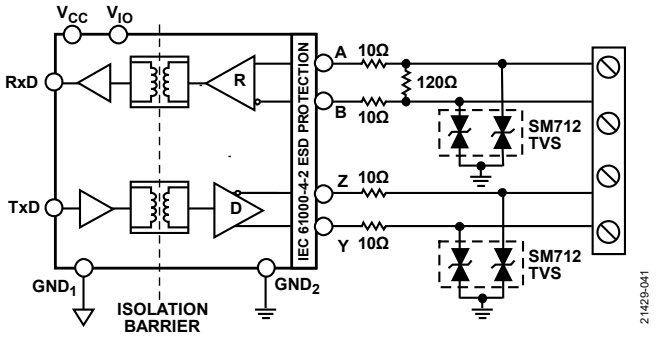

Figure 39. Isolated RS-485 Solution with ESD, EFT, and Surge Protection

Table 16. Recommended Components for ESD, EFT, and Surge Protection

Recommended Components	Part Number
TVS	CDSOT23-SM712
10 Ω Pulse Proof Resistors	CRCW060310R0FKEAHP

Table 17. Protection Levels with Recommended Circuit

EMC Standard	Protection Level
ESD—Contact (IEC61000-4-2)	≥ ±30kV – Exceeds Level 4
ESD—Air (IEC61000-4-2)	≥ ±30kV – Exceeds Level 4
EFT (IEC61000-4-4)	≥ ±4kV – Exceeds Level 4
Surge (IEC61000-4-5)	≥ ±1kV – Level 2

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period of time. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation as well as on the materials and material interfaces.

The two types of insulation degradation of primary interest are breakdown along surfaces exposed to the air and insulation wear out. Surface breakdown is the phenomenon of surface tracking and is the primary determinant of surface creepage requirements in system level standards. Insulation wear out is the phenomenon where charge injection or displacement currents inside the insulation material cause long-term insulation degradation.

Surface Tracking

Surface tracking is addressed in electrical safety standards by setting a minimum surface creepage based on the working voltage, the environmental conditions, and the properties of the insulation material. Safety agencies perform characterization testing on the surface insulation of components, allowing the components to be categorized in different material groups. Lower material group ratings are more resistant to surface tracking and can therefore provide adequate lifetime with smaller creepage. The minimum creepage for a given working voltage and material group is in each system level standard and is based on the total rms voltage across the isolation, pollution degree, and material group. See Table 5 for the material group and creepage information for the ADM2867E isolated RS-485 transceiver.

Insulation Wear Out

The lifetime of insulation caused by wear out is determined by the thickness, material properties, and the voltage stress applied across the insulation. It is important to verify that the product lifetime is adequate at the application working voltage. The working voltage supported by an isolator for wear out may not be the same as the working voltage supported for tracking. The working voltage applicable to tracking is specified in most standards.

Testing and modeling show that the primary driver of long-term degradation is displacement current in the polyimide insulation, causing incremental damage. The stress on the insulation can be divided into broad categories, such as dc stress and ac component, time varying voltage stress. DC stress causes little wear out because there is no displacement current, whereas ac component time varying voltage stress causes wear out.

The ratings in certification documents are typically based on 60 Hz sinusoidal stress to reflect isolation from the line voltage. However, many practical applications have combinations of 60 Hz ac and dc across the barrier, as shown in Equation 1. Because only the ac portion of the stress causes wear out, the equation can be rearranged to solve for the ac rms voltage, as shown in Equation 2. For insulation wear out with the polyimide materials used in these products, the ac rms voltage determines the product lifetime.

$$V_{RMS} = \sqrt{V_{AC\,RMS}{}^2 + V_{DC}{}^2} \quad (1)$$

or

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2} \quad (2)$$

where:
$V_{AC\,RMS}$ is the time varying portion of the working voltage.
V_{RMS} is the total rms working voltage.
V_{DC} is the dc offset of the working voltage.

Calculation and Use of Parameters Example

The following example frequently arises in power conversion applications. Assume that the line voltage on one side of the isolation is 240 V ac rms and a 400 V dc bus voltage is present on the other side of the isolation barrier. The isolator material is polyimide. To establish the critical voltages in determining the creepage, clearance, and lifetime of a device, see Figure 40 and the following equations.

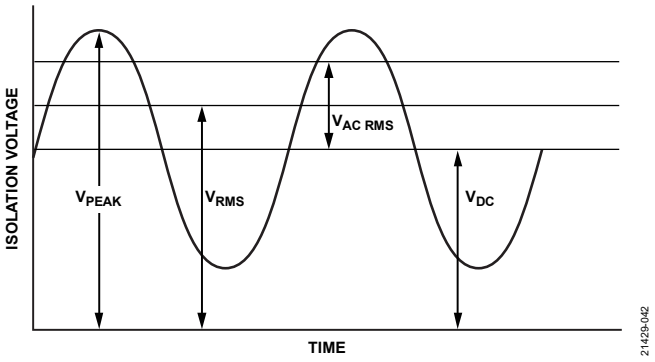

Figure 40. Critical Voltage Example

The working voltage across the barrier from Equation 1 is

$$V_{RMS} = \sqrt{V_{AC\,RMS}{}^2 + V_{DC}{}^2}$$

$$V_{RMS} = \sqrt{240^2 + 400^2}$$

V_{RMS} = 466 V

This V_{RMS} value is the working voltage used together with the material group and pollution degree when looking up the creepage required by a system standard.

To determine if the lifetime is adequate, obtain the time varying portion of the working voltage. To obtain the ac rms voltage, use Equation 2.

$$V_{AC\,RMS} = \sqrt{V_{RMS}{}^2 - V_{DC}{}^2}$$

$$V_{AC\,RMS} = \sqrt{466^2 - 400^2}$$

$V_{AC\,RMS}$ = 240 V rms

In this case, the ac rms voltage is simply the line voltage of 240 V rms. This calculation is more relevant when the waveform is

not sinusoidal. The value is compared to the limits for working voltage in Table 9 for the expected lifetime, which is less than a 60 Hz sine wave, and it is well within the limit for a 50-year service life.

Note that the dc working voltage limit is set by the creepage of the package as specified in IEC 60664-1. This value can differ for specific system level standards.

TYPICAL APPLICATIONS

An example circuit using the ADM2867E as a full duplex RS-485 node is shown below in Figure 41. Placement of the termination resistor R_T is dependent on the location of the node and the network topology. Refer to the AN-960 Application Note, *RS-485/RS-422 Circuit Implementation Guide*, for guidance on termination. Up to 192 transceivers can be connected to the bus. To minimize reflections, terminate the line at the receiving end in its characteristic impedance and keep stub lengths off the main line as short as possible. For half-duplex operation, this means that both ends of the line must be terminated because either end can be the receiving end.

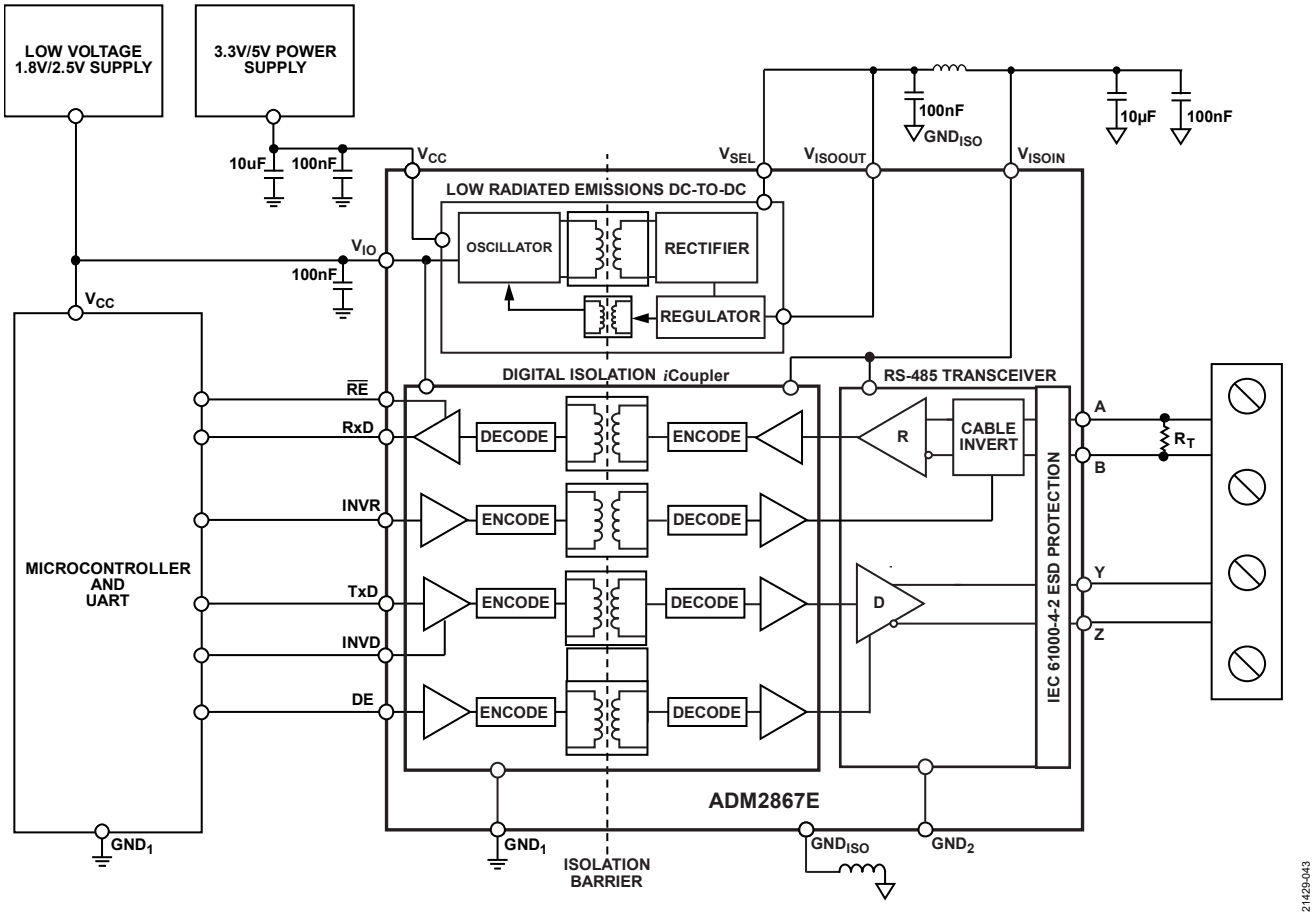

Figure 41. Example Circuit Diagram Using the ADM2867E

OUTLINE DIMENSIONS

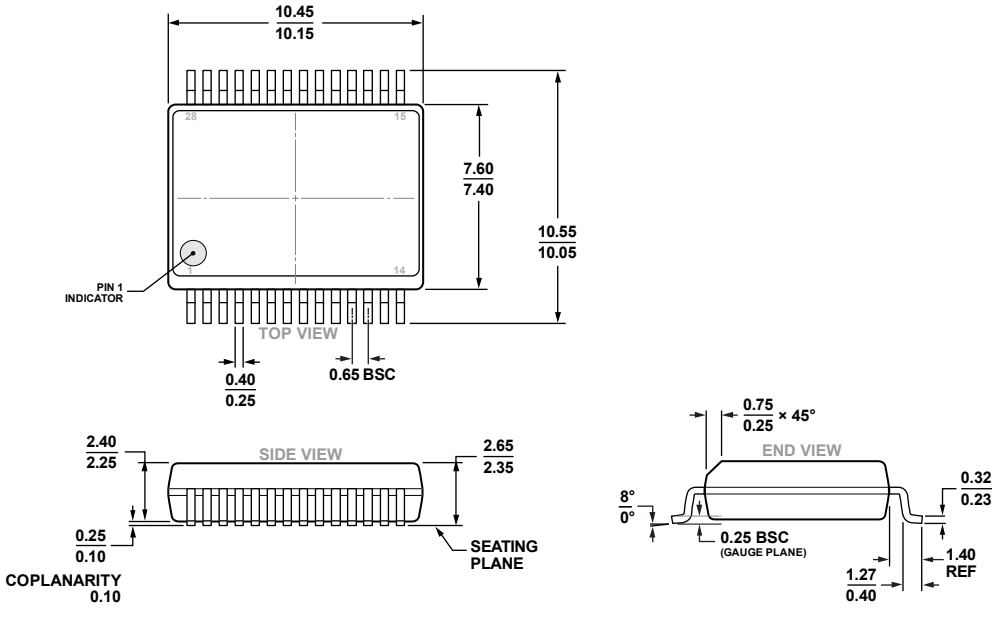

Figure 42. 28-Lead Standard Small Outline, Wide Body, with Finer Pitch [SOIC_W_FP]
(RN-28-1)
Dimensions shown in millimeters

PR21429-0-11/19(PrA)