An Infineon Technologies Company

ADM7001
Single Ethernet 10/100M PHY

Datasheet
Version 1.07

Infineon-ADMtek Co Ltd

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About this Manual

Intended Audience

Structure

This Data sheet contains 6 chapters

Chapter 1. Product Overview

Chapter 2. Interface Description

Chapter 3. Function Description

Chapter 4. Register Description

Chapter 5. Electrical Specification

Chapter 6. Packaging

Revision History

Date	Version	Change
05 March 2003	1.0	First release of ADM7001
08 April 2003	1.01	Register Modifications and Pin updates.
24 July 2003	1.02	The following sections were updated: 1.2, 1.3, 2.1, 2.2.1, 2.2.5, 2.2.7, 2.2.8, 2.2.8, 4.1, 4.2.3-4, 4.2.11-12, 4.3.4, 4.3.9, 4.3.11, 4.3.12, & 4.3.16
30 July 2003	1.03	Updated section 6.2
15 September 2003	1.04	Updated Section 2.2.5, 2.2.8, & 4.2.11
19 February 2004	1.05	Updated table 5.3
16 April 2004	1.06	Removed TQFP packaging
28 April 2004	1.07	Updated Infineon-Infineon-ADMtek Co Ltd logo

Detailed revision information is available on request.

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Chapter 1 Product Overview

1.1 Overview

ADM7001, is a single chip one port 10/100M PHY, designed for today's low cost and low power dual speed application. It supports auto sensing 10/100 Mbps ports with on-chip clock recovery and base line wander correction including integrated MLT-3 functionality for 100 Mbps operation and also supports Manchester Code Converter with on chip clock recovery circuitry for 10 Mbps functionality. Meanwhile, it provides Medium Independent Interface (MII), Reduced Medium Independent Interface (RMII) and General Purpose Serial Interface (GPSI), three different interfaces different application.

For today's IA (Information Application), ADM7001 supports "Auto Cross Over Detection" function to eliminate the technical barrier between networking and end user. With the aid of this auto cross over detection function, Plug-n-Play feature can be easily applied to IA relative products.

The major design target for ADM7001 is to reduce the power consumption and system radiation for the whole system. With the aid of this low power consumption and low radiation chip, the fan and on-system power supply can be removed to save the total manufacture cost and make SOHO application achievable.

1.1.1 Product Order Information

The ADM7001 comes in two packaging formats as follows:

6.1 ADM7001 Low Profile Quad Flat Package (LQFP)

1.2 Features

- IEEE 802.3 compatible 10BASE-T and 100BASE-T physical layer interface and ANSI X3.263 TP-PMD compatible transceiver
- Single chip, integrated physical layer and transceivers for 10BASE-T and 100BASE-TX function.
- Medium Independent Interface (MII), Reduced MII (RMII) and General Purpose Serial Interface (GPSI) for high port count switch
- Built-in 10Mbit transmit filter
- 10Mbit PLL, exceeding tolerances for both preamble and data jitter
- 100Mbit PLL, combined with the digital adaptive equalizer and performance up to 120 meters for UTP 5.
- 125MHz Clock Generator and Timing Recovery
- Integrated Base Line Wander Correction
- Carrier Integrity Monitor function supported
- Support FEFI when Auto Negotiation disabled
- Support Auto MDIX function for Plug-and-Play

- IEEE 802.3u Clause 28 compliant auto negotiation for full 10 Mbps and 100 Mbps control.
- Supports programmable LED For different Switch Application and Power On LED Self Test
- Supports Cable Length Indication both in MII Register and LED (Programmable)
- Supports PECL interface for fiber connection
- Supports TP vs. FX Medium Converter function
- Supports Fault Propagation function for medium converter
- Supports 10K Bytes Jumbo Packet with Clock Skew 150 ppm
- Built-in Clock Generator and Power On Reset Signal to save system cost
- 48 LQFP without regulator
- Support Power saving function
- Support Parallel LED output

1.3 Block Diagram

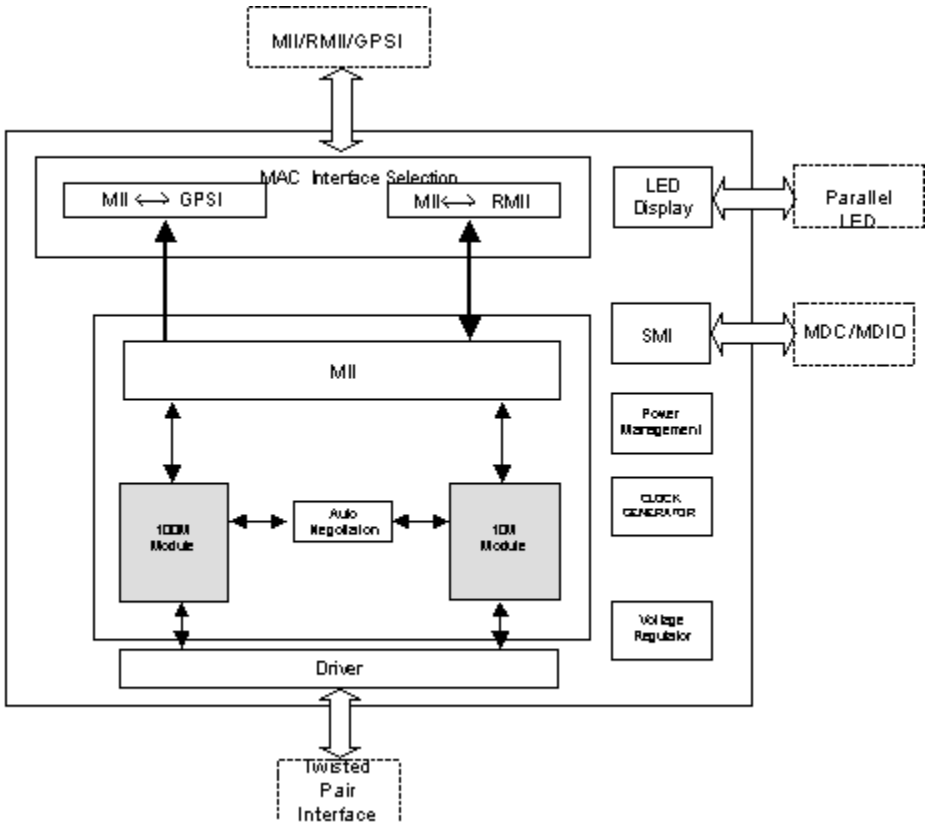


Figure 1-1 ADM7001 Block Diagram

1.4 Abbreviations and Acronyms

ANSI	American National Standards Institute
BER	Bit Error Rate
COL	Collision
CRS	Carrier Sense
CRSDV	Carrier Sense and Data Valid
CTL	Crystal
DSP	Digital Signal Processor
DUPCOL	Duplex and Collision
ESD	End of Stream Delimiter
FEFI	Far End Fault Indication
FIFO	First In First Out
FLP	Fast Link Pulse
FX	Fiber
GPSI	General Purpose Serial Interface
TP	Twisted Pair
TX	Transmit
RX	Receive
IA	Information Application
LFSR	Linear Feedback Shifter Register
LNKACT	Link and Activity
LQFP	Low Profile Quad Flat Package
LVTTL	Low Voltage TTL Level
MAC	Media Access Controller
MD	Medium Detect
MDC	Management Data Clock
MDIO	Management Data Input/Output
NRZ	None Return to Zero
NRZI	None Return to Zero Inverter
OP	Operation Code
PCS	Physical Coding Sub-layer
PECL	Pseudo Emitter Couple Logic
PHY	Physical Layer
PHYADDR	PHY Address
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
PNP	A type of Transistor
PQFP	Plastic Quad Flat Pack
REFCLK	Reference Clock
RF	Remote Fault
MII	Media Independent Interface
RMII	Reduced Media Independent Interface
RXCLK	Receive Clock
RXD	Receive Data
RXDV	Receive Data Valid

RXER	Receive Data Error
RXN	Receive Negative (Analog receive differential signal)
RXP	Receive Positive (Analog receive differential signal)
SDN	Signal Detect Negative (Fiber signal detect)
SDP	Signal Detect Positive (Fiber signal detect)
SELFX	Select Fiber
SMI	Serial Management Interface
SOHO	Small Office and Home Office
SQE	Signal Quality Error
SSD	Start of Stream Delimiter
GPSI	General Purpose Serial Interface
TA	Turn Around
TDR	Time Domain Reflectometry
TP-PMD	Twisted Pair Physical Medium Dependent
TTL	Transistor Transistor Logic
TXCLK	MII Transmission Clock
TXD	Transmission Data
TXEN	Transmission Enable
TXER	Transmission Error
TXN	Transmission Negative
TXP	Transmission Positive
/J/K	5B signal to detect the start of a frame
/T/R	5B signal to detect the end of a frame
PHYDIG	Internal Digital Block to Handle PHY relative functions
TRXANA	Internal Analog Block contains both TX and RX Function

1.5 Conventions

1.5.1 Data Lengths

qword	64-bits
dword	32-bits
word	16-bits
byte	8 bits
nibble	4 bits

1.5.2 Register Type Descriptions

Register Type	*Description*
RO	Read Only
R/W	Read and Write capable
SC	Self-clearing
LL	Latching low, unlatch on read
LH	Latching high, unlatch on read
COR	Clear On Read

1.5.3 Pin Type Descriptions

Pin Type	*Description*
I:	Input
O:	Output
I/O:	Bi-directional
OD:	Open drain
SCHE:	Schmitt Trigger
PU:	Pull Up
PD:	Pull Down

Chapter 2 Interface Description

2.1 Pin Diagram

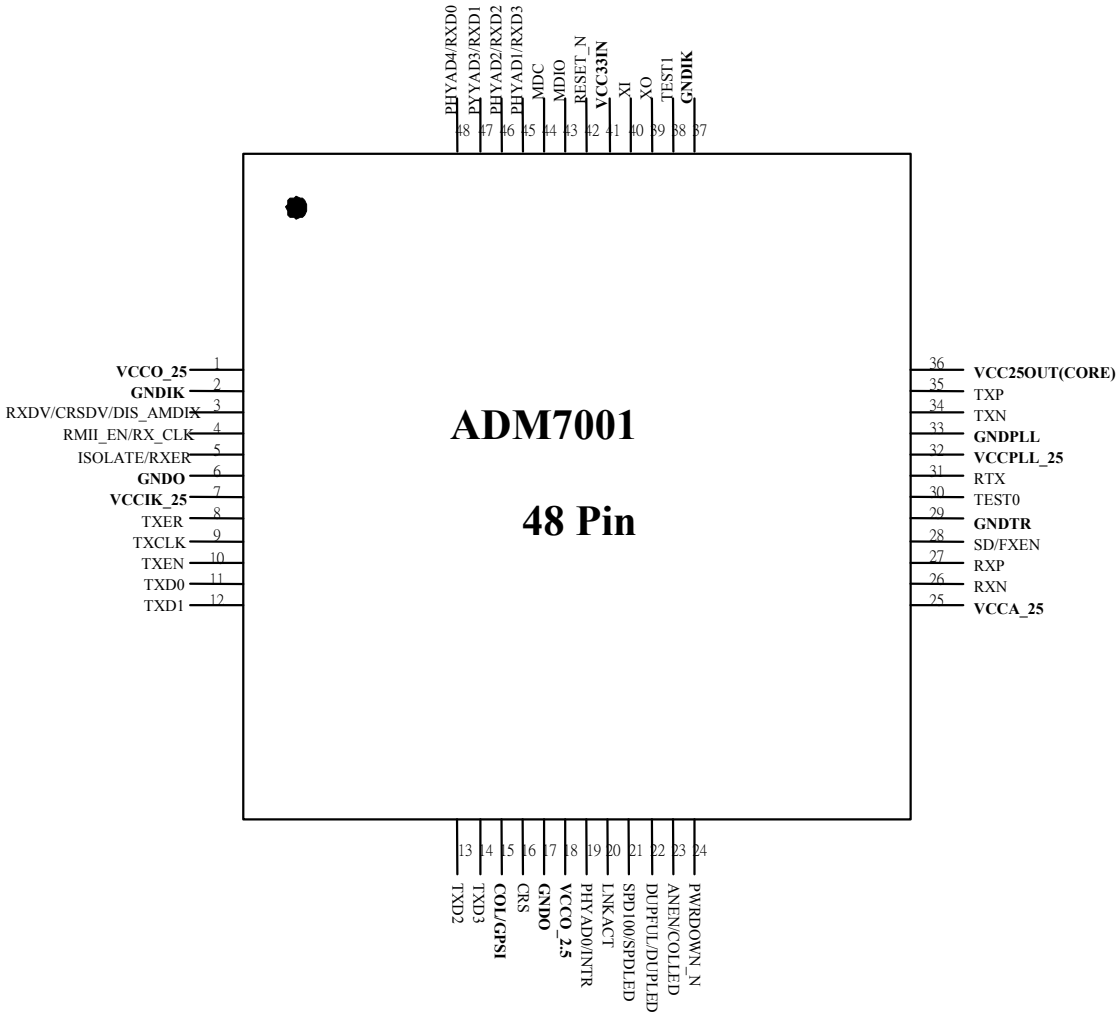


Figure 2-1 ADM7001 48 Pin Diagram

2.2 Pin Description

Note:
For those pins, which have multiple functions, pin name is separated by slash ("/").
If not specified, all signals are default to digital signals.
Please refer to section '1.5.3 Pin Type Descriptions' for an explanation of pin abbreviations.

2.2.1 Twisted Pair Interface, 5 pins

Pin #	Pin Name	Type	Description
35	TXP	I/O, Analog	Twisted Pair Transmit Output Positive.
34	TXN	I/O, Analog	Twisted Pair Transmit Output Negative.
27	RXP	I/O, Analog	Twisted Pair Receive Input Positive.
26	RXN	I/O, Analog	Twisted Pair Receive Input Negative.
28	Power On Setting FXEN Fiber Mode SDP	I, Analog	**Fiber Enable.** Value on this pin will be latched by ADM7001 during power on reset as fiber select signal. 0: Twisted Pair Mode 1: Fiber Optic Mode **100BASE-FX Signal Detect.** After power on reset stage, this pin acts as signal detect signal from external fiber optic transceiver in case FXEN is detected as high during power on reset. 0: No signal detected 1: Signal

2.2.2 Digital Power/Ground, 7 pins

Pin #	Pin Name	Type	Pin Description
6, 17	GNDO	Digital Ground	Ground used by 3.3V I/O.
2, 37	GNDIK	Digital Ground	Ground used by Core.
1, 18	VCCO_25	Digital Power	2.5V Power Used by Digital I/O Pad.
7	VCCIK_25	Digital Power	2.5V Power used by Core

2.2.3 Ground and Power, 5 pins

Pin #	Pin Name	Type	Description
41	VCC3IN	Analog Power	3.3V Power input to ADM7001 and used by built-in 3.3V to 2.5V regulator.
36	VCC25OUT	Analog Power	2.5V Power output by ADM7001. Maximum Supply current from this pin is 200 mA.
29	GNDTR	Analog Ground	Analog Ground Pad
25	VCCA_25	Analog Power	Analog 2.5V Power

32	VCCPLL_25	Analog Power	Analog 2.5V Power used by Clock Generator module

2.2.4 Clock Input, 2 pins

Pin #	Pin Name	Type	Pin Description
40	XI/OSCI	I, CTL	**Crystal/Oscillator input.** 25M Crystal/Oscillator Input in MII mode and 50M Clock input in RMII mode (Also called REFCLK in RMII Mode)
39	XO	O, CTL	**Crystal output.** When 25M Oscillator is used, this pin should left unconnected. Capable of driving one XI input for multiple port application.

2.2.5 MII/RMII/GPSI Interface, 16 pins

Pin #	Pin Name	Type	Pin Description
9	MII Mode TXCLK	O, 16mA	**MII Transmit Clock.** 25M Clock output in 100BASE-X mode and 2.5M Clock output for 10BASE-T mode. This clock is continuously driven output and generated from XI. Before Speed is recognized, this pin drives out continuous 25M clock.
	RMII Mode TXCLK		N/A.
	GPSI Mode TXCLK		**GPSI Transmit Clock**. 10M Clock output in 10BASE-T mode.
14, 13, 12, 11	MII Mode TXD[3:0]	I, TTL, PD	**Transmit Data.** Nibble-wide transmit data stream in MII mode. These four bits are synchronous to the rising edge of TXCLK and TXD[3] is the most significant bit.
	RMII Mode TXD[1:0]		**Di-bits Transmit Data.** TXD0 and TXD1 for the di-bits that are transmitted and are driven synchronously to REFCLK. TXD[1] is the MSB. Note that in 100Mb/s mode, TXD can change once per REFCLK cycle, whereas in 10Mb/s mode, TXD must be held steady for 10 consecutive REFCLK cycles. TXD[3] and TXD[2] are not used in RMII Mode, left unconnected or pull down externally for normal operation.
	GPSI Mode TXD		**Serial Transmit Data.** TXD0 for the designated port inputs the data that is transmitted and is driven synchronously to TXCLK in 10Mb/s mode. When ADM7001 is programmed into GPSI mode, TXD[3:1] should be left unconnected or pull down externally for normal operation.
10	MII Mode TXEN	I, TTL, PD	**Transmit Enable.** Transmit Enable to indicate that the data on TXD[3:0] is valid.
	RMII Mode TXEN		**Transmit Enable.** TXEN indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	GPSI Mode TXEN		**Transmit Enable.** Transmit Enable to indicate that the data on TXD0 is valid.
8	MII Mode TXER	I, TTL, PD	**Transmit Error.** Active high signal to indicate that there is error condition requested by MAC.
	RMII Mode TXER		**Transmit Error.** Active high signal to indicate that there is error condition requested by MAC.

Pin #	Pin Name	Type	Pin Description
	GPSI Mode LOW		Keep Low in GPSI Mode.
4	Power On Setting RMII_EN	I, LVTTL, PD	**RMII Enable.** Used to select MII or RMII operation. The default value during power on reset is 0 (Before RMII_EN and GPSI value is determined) 0: MII mode 1: RMII Mode
	MII Mode RX_CLK	O, 16mA	**MII Receive Clock.** 25M Clock output in 100BASE-X mode, 2.5M Clock output for 10BASE-T MII mode. This clock is recovered from the received data on the cable input. Due to recovered from incoming receive data, it is possible that RXCLK starts running yet RXDV keeps low for a while. During power on reset, there is no receiving clock driven by ADM7001.
	RMII Mode CLKO50		**RMII 50M Clock Output.** This pin outputs continuous 50M clock in RMII mode. To reduce the BOM cost for system application, user can connect this pin directly to REFCLK to proper RMII operation.
	GPSI Mode RX_CLK		**GPSI Receive Clock.** 10M clock for 10BASE-T GPSI mode. This clock is recovered from the received data on the cable input. Due to recovered from incoming receive data, it is possible that RXCLK starts running yet CRS keeps low for a while. During power on reset, there is no receiving clock driven by ADM7001. ***Note:*** that clock on this pin will not be active during power on reset due to power on setting.
3	Power On Setting DIS_AMDIX_EN	I, LVTTL, PD	**Disable Auto Crossover Function.** Value on this pin will be latched by ADM7001 to select Auto Cross-Over Function. 0: Enable Auto Crossover. 1: Disable Auto Crossover.
	MII Mode RXDV	O, 8mA	**MII Receive Data Valid.** Active high signal to indicate that the data on RXD[3:0] is valid. Synchronous to the rising edge of RXCLK in MII mode.
	RMII Mode CRSDV	O, 8mA	**RMII Carrier Sense/Receive Data Value.** Represents Receive Carrier Sense and Data Valid in RMII mode. CRSDV asserts when the receive medium is non-idle. The assertion of CRSDV is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV is asserted synchronously to REFCLK. The toggling of CRSDV_P on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV is asserted for the duration of carrier activity for a false carrier event.
	GPSI Mode LOW		**Keep Low in GPSI Mode.**

Pin #	Pin Name	Type	Pin Description
45, 46, 47, 48	Power On Setting PHYAD[1:4]	I, TTL, PD	**PHY Address Select.** Value on these 4 pins combined with PHYAD0 will be stored into ADM7001 as PHY physical address during power on reset. After power on reset, these 4 pins are output.
	MII Mode RXD[3:0]	O, 8mA	**MII Receive Data.** Nibble-wide receive data stream in MII mode. These four bits are synchronous to the rising edge of RX_CLK and RXD[3] is the most significant bit.
	RMII Mode RXD[1:0]	O, 8mA	**RMII Receive Data.** RXD0 and RXD1 for the di-bits that are received and are driven synchronously to REFCLK. RXD[1] is the MSB. Note that in 100Mb/s mode, RXD can change once per REFCLK cycle, whereas in 10Mb/s mode, RXD must be held steady for 10 consecutive REFCLK cycles. RXD[3:2] have not used in this mode.
	GPSI Mode RXD	O, 8mA	**GPSI Receive Data.** RXD0 for the designated port inputs the data that is transmitted and is driven synchronously to RX_CLK in 10Mb/s mode. RXD[3:1] have not used in this mode.
5	Power On Setting ISOLATE	I, TTL PD	**ISOLATE.** Value on this pin will be latched by ADM7001 during power on reset. 0: Normal Operation 1: All MII outputs are tri-stated. All MII Inputs(TXD, TXEN, TXER) are ignored .
	MII Mode RXER	O, 4mA	**MII Receive Error.** Active high signal to indicate that there is error condition detected by ADM7001. When error is detected, RXER will be high and maintains high until RXDV is de-asserted.
	RMII Mode, RXER	O, 4mA	**RMII Receive Error.** Active high signal to indicate that there is error condition detected by ADM7001. When error is detected, RXER will be high and maintains high until CRSDV is de-asserted.
	GPSI Mode, N/A		**No operation in GPSI Mode.**
15	Power On Setting GPSI	I PD	**GPSI Mode Select.** Value on this pin will be sampled by ADM7001 during power on reset to form GPSI internal control signal. Together with RMII_EN, these two pins form three possible internal supported by ADM7001 RMII_EN GPSI Interface 0 0 MII 0 1 GPSI (1M8) 1 x RMII
	GPSI/MII Mode COL	O, 8mA	**GPSI/MII Collision.** In half duplex mode, active high to indicate that there is collision on the medium. In full duplex mode, this pin will keep low all the time.
	RMII Mode N/A		Not Available.
16	Power On Setting	I, LVTTL,	**Repeater Mode.** Value on this pin will be latched by ADM7001 during power on reset as repeater mode

Pin #	Pin Name	Type	Pin Description
	REPEATER	PD	0: SW/NIC mode, CRS will be asserted according to RX/TX in half duplex mode 1: REPEATER mode. CRS will be asserted only in RX mode in half duplex operation.
	MII Mode CRS	O, 8mA	**MII Carrier Sense.** This bit indicates that there is carrier sense presented on the medium. Note that in half duplex mode, this pin will also be asserted high by ADM7001 under transmit condition. This pin is asynchronous to RX_CLK.
	RMII Mode N/A		Not Available
	GPSI Mode CRS		**GPSI Carrier Sense.** This bit indicates that there is carrier sense presented on the medium. Note that in half duplex mode, this pin will also be asserted high by ADM7001 under transmit condition. This pin is asynchronous to RX_CLK.

2.2.6 Reset Pin

Pin #	Pin Name	Type	Description
42	RESET#	I, SCHE	**Reset Signal.** Active low to bring ADM7001 into reset condition. Recommend keeping low for at least 200 ms to ensure the stability of the system after power on reset.

2.2.7 Control Signals, 6 pins

Pin #	Pin Name	Type	Pin Description
43	MDIO	I/O, LVTTL, PU	**Management Data.** MDIO transfers management data in and out of the device synchronous to MDC.
44	MDC	I, LVTTL	**Management Data Reference Clock.** A non-continuous clock input for management usage. ADM7001 will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock.
19	Power On Setting PHYAD0 MII/RMII/GPSI Mode INTR#	I, LVTTL, PU	**PHY Address bit 0.** See RXD[3:0] description. **Interrupt.** Default active low signal to indicate that there is interrupt event in SMI register. Active value of interrupt signal can be configured by register 18.1. Only available when interrupt mode is selected.
24	PWRDOWN#	I, LVTTL, PU	**Low Power Operation.** 0: ADM7001 in low power mode operation. All blocks except the energy detection and crystal oscillator are de-activated. 1: ADM7001 in normal mode operation. Note: When RESET# is reset to 0 and PWRDOWN# is set to 0, whole ADM7001 blocks will be disabled.
38, 30	TEST[1:0]	I, LVTTL, PD	**Industrial Test Pin.** Keeps low for normal operation.

2.2.8 LED Interface, 4 pins

Pin #	Pin Name	Type	Pin Description
20	Reserved	I, TTL, PU	Reserved
	LNKACT	O, 8mA	**Link/Activity LED.** Active low (Note) 100ms (blink 100ms) to indicate that there is transmit or receive activity after Link Up. Keeps high all the time when link is failed.
21	Power On Setting SPD100	I, TTL PU,	**Recommend 100M Operation.** This bit is only available in TP mode. Together with ANEN to form speed mode select for ADM7001: ANEN SPD100 Mode 0 0 Force 10BASE-T Mode 0 1 Force 100BASE-TX Mode 1 0 10M Capability 1 1 10/100M Capability
	Normal Mode SPDLED	O, 8mA	**Speed LED.** (Note) 0: 100M 1: 10M **Cable Length LED.** When FXEN is low and MII register 18.2 DIS_CABLEN_LED is set to 0, this pin together with COLLED and LNKACTLED form cable length information on twisted pair. ***NOTE:*** That the following indication assume recommend value on SPDLED, COLLED and LNKACTLED is high, when corresponding bit's power on setting bit is 0, polarity of corresponding bit will be inverted. SPDLED COLLED LNKACTLED Cable Length 110 > 140 meters or Link Failed 110 0 – 40 meters 100 40 – 80 meters 000 80 – 120 meters *** (FLASHED) Reserved ***Note:*** When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high.
22	Power On Setting DUPFUL	I, TTL PU,	**Duplex Control.** This pin is only available when auto negotiation is disabled. ANEN DUPFUL Mode 0 0 Force to Half Duplex Mode 0 1 Force to Full Duplex Mode 1 0 Half Duplex Capability 1 1 Full/Half Duplex Capability
	Normal Mode DUPLED	O, 8mA	**Duplex LED. (Note)** 0: Full Duplex 1: Half Duplex ***Note*:** When recommend value during power on is high, then

Pin #	Pin Name	Type	Pin Description
			this signal is active low; if the recommend value is low, then this signal is active high. This rule also applies to Cable Length indication
23	Power On Setting ANEN	I, TTL PU,	**Auto Negotiation Enable.** This bit is only available in TP mode. 0: Disable Auto Negotiation 1: Enable Auto Negotiation
	Normal Mode COLLED	O, 8mA	**Collision LED.** Keep high (Note) when ADM7001 is in full duplex mode and will blink 100 ms when collision condition is detected in half duplex mode. ***Note:*** When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high.

2.2.9 Regulator Control

Pin #	Pin Name	Type	Description
31	RTX	I, Analog	Constant Voltage Reference. External 1.1kΩ1% resistor connection to ground.

Chapter 3 Function Description

ADM7001 integrates 100Base-X physical sub layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, and complete 10Base-T modules into a single chip for both 10 Mbps and 100 Mbps Ethernet operations. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either full-duplex mode or half-duplex mode in either 10 Mbps or 100 Mbps operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The 10Base-T section of the device consists of the 10 Mbps transceiver module with filters and a Manchester ENDEC module.

ADM7001 consists of seven kinds of major blocks:

- 10/100M PHY Blocks
- MAC Interface
- LED Display
- SMI
- Power Management
- Clock Generator
- Voltage Regulator

Each 10/100M PHY block contains:

- 10M PHY block
- 100M PHY block
- Auto-negotiation
- Other Digital Control Blocks

3.1 10/100M PHY Block

The 100Base-X section of the device implements he following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair PMD (TP-PMD) transceiver

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interfaces used for communication between PHY block and switch core is MII interface.

3.1.1 100Base-X Module

ADM7001 implements 100Base-X compliant PCS and PMA and 100Base-TX compliant TP-PMD as illustrated in Figure 3-1. Bypass options for each of the major functional

blocks within the 100Base-X PCS provides flexibility for various applications. 100 Mbps PHY loop back is included for diagnostic purpose.

3.1.2 100Base-TX Receiver

For 100Base-TX operation, the on-chip twisted pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits detects the incoming signal.

ADM7001 uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.
The 100Base-X receiver consists of functional blocks required to recover and condition the 125 Mbps receive data stream. The ADM7001 implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125 Mbps receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

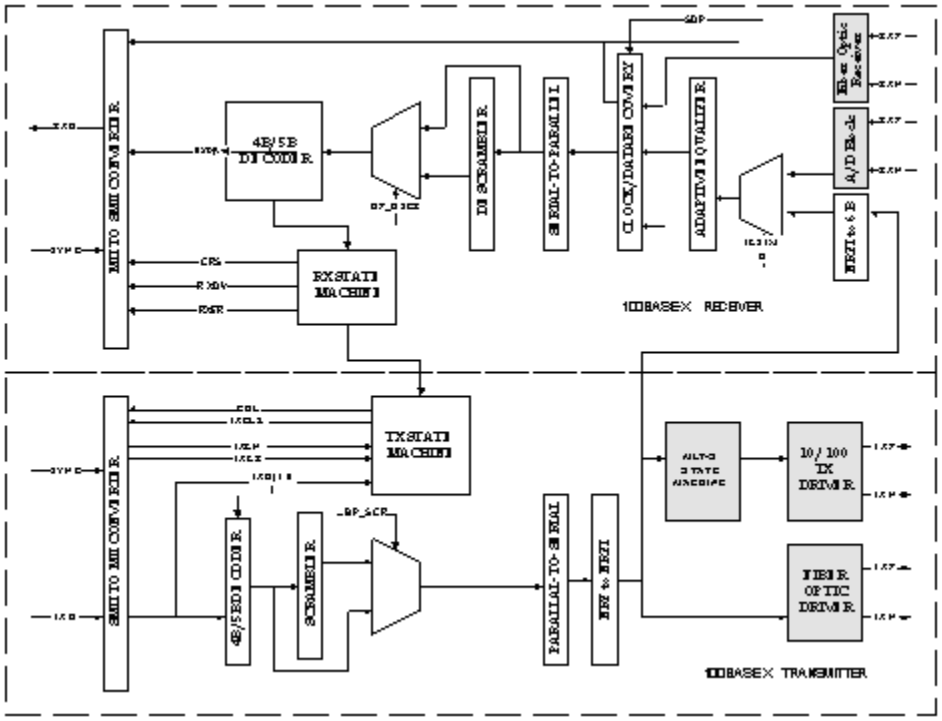


Figure 3-1 100Base-X Block Diagram and Data Path

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and Timing Recovery Module
- NRZI/NRZ and Serial/Parallel Decoder
- De-scrambler
- Symbol Alignment Block

- Symbol Decoder
- Collision Detect Block
- Carrier Sense Block
- Stream Decoder Block

A/D Converter

High performance A/D converter with 125M sampling rate converts signals received on RXP/RXN pins to 6 bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

Adaptive Equalizer and timing Recovery Module

All digital design is especial immune from noise environments and achieves better correlations between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed forward and Decision Feedback techniques meet the requirement of BER less than 10-12 for transmission on CAT5 twisted pair cable ranging from 0 to 140 meters.

NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

Data De-scrambling

The de-scrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and de-scrambled.

In order to maintain synchronization, the de-scrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the de-scrambler the hold timer starts a 722 us countdown. Upon detection of at least 6 idle symbols (30 consecutive "1") within the 722 us period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely given a properly operating network connection with good signal integrity. If the link state monitor does not recognize at least 6 unscrambled idle symbols within 722 us period, the de-scrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

Symbol Alignment

The symbol alignment circuit in the ADM7001 determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the de-scrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is

aligned on a fixed boundary.

Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in Table 3-1.

The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

PCS code-group [4:0]	Name	MII (TXD/RXD) <3:0>	Interpretation
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F
11111	I	Undefined	IDLE used as inter-stream fill code
11000	J	0101	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
10001	K	0101	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
01101	T	Undefined	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0111	R	Undefined	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
00100	H	Undefined	Transmit Error; used to force signaling errors

PCS code-group [4:0]	Name	MII (TXD/RXD) <3:0>	Interpretation
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

Table 3-1 Look-up Table for translating 5B Symbols into 4B Nibbles.

Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are being presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is de-asserted.

Receive Errors

The RXER signal is used to communicate receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word that does not map to a valid code-group.

100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is being received. Without reliable data reception, the link monitor will halt both transmit and receive operations until such time that a valid link is detected.

The ADM7001 performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10 Mbps link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 us, and waits for an enable from the auto negotiation module. When receive, the link-up state is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

Carrier Sense

Carrier sense (CRS) for 100 Mbps operation is asserted upon the detection of two noncontiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is disserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, then the ADM7001 will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles hat correspond to received 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become de-asserted.

Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will be receiving valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by bit 3 of register 11h. It is initialized to 1 (encoded) if the SELFX pin is at logic high level during power on reset. If the FEFI function is enabled the ADM7001 will halt all current operations and transmit the FEFI idle pattern when FOSD signal is de-asserted following a good link indication from the link integrity monitor. FOSD signal is generated internally from the internal signal detect circuit. Transmission of the FEFI idle pattern will continue until link up signal is asserted. If three or more FEFI idle patterns are detected by the ADM7001, then bit 4 of the Basic mode status register (address 1h) is set to one until read by management. Additionally, upon detection of far end fault, all receive and transmit MII activity is disabled/ignored.

3.1.3 100Base-TX Transmitter

ADM7001 implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetics for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

ADM7001 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.1.4 100Base-FX Receiver

Signal is received through PECL receiver inputs from fiber transceiver, and directly passed to clock recovery circuit for data/clock recovery. Scrambler/de-scrambler is bypassed in 100Base-FX.

Automatic "Signal_Detect" Function Block

When DIS_ANASDEN_N in register 18 is set to 0, ADM7001 doesn't support SDP detection in fiber mode, which is used to connect to fiber transceiver to indicate there is signal on the fiber. Instead, ADM7001 use the data on RXP/RXN to detect consecutive 65 "1" on the receive data (Recovered from RXP/RXN) to determine whether "Signal" is detected or not. When the detect condition is true (Consecutive 65 bits "1"), internal signal detect signal will be asserted to inform receive relative blocks to be ready for coming receive activities.

3.1.5 100Base-FX Transmitter

In 100Base FX transmit, the serial data stream is driven out as NRZI PECL signals, which enters fiber transceiver in differential-pairs form. Fiber transceiver should be available working at 3.3V environment.

3.1.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loop-back, jabber, wave-shaper, and link integrity functions, as defined in the standard. Figure 5 provides an overview for the 10Base-T module.

The ADM7001 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.1.7 Operation Modes

The ADM7001 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM7001 functions as an IEEE 802.3

compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmit and receive. In full duplex mode the ADM7001 can simultaneously transmit and receive data.

3.1.8 Manchester Encoder/Decoder

Data encoding and transmission begins when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is a 1, or at the boundary of the bit cell if the last bit is 0.

A differential input receiver circuit accomplishes decoding and a phase-locked loop that separate the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid-bit transitions are detected. Within one and half bit times after the last bit, carrier sense is disserted.

3.1.9 Transmit Driver and Receiver

The ADM7001 integrates the entire required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.1.10 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receives. The ADM7001 implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The “analog squelch circuit” checks the signal at the start of the packet and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

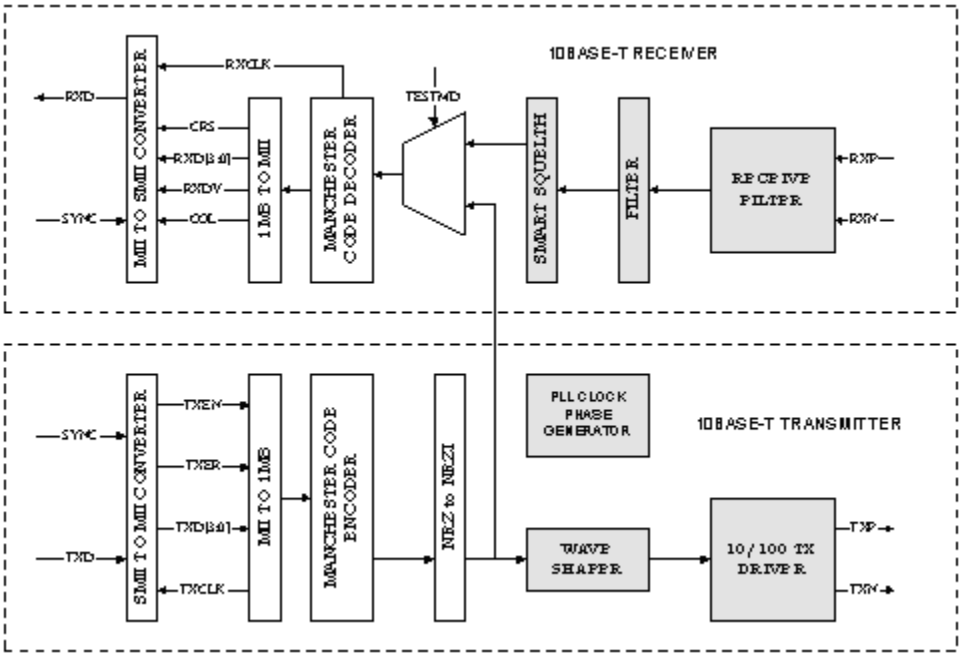


Figure 3-2 10Base-T Block Diagram and Data Path

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 7 of register address 10h.

3.1.11 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbps half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbps full duplex and repeater mode operations, the CRS is asserted only due to receive activity.85

3.1.12 Collision Detection

Collision is detected internal to the MAC, which is generated by an AND function of TXEN and RXDV derived from internal timing recovery circuitry. Note should be taken that due to TXEN and RXDV are asynchronous to each other, COL signal outputted by ADM7001 is irrelevant to either TXCLK or RXCLK.

3.1.13 Jabber Function

The jabber function monitors the ADM7001 output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disabled for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 408 ms (The un-jab time) before the jabber

function re-enables the transmit outputs. The jabber function can be disabled by programming bit 0 of register address 10h to high.

3.1.14 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.
The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100ns in duration and is transmitted every 16 ms, in the absence of transmit data. Setting bit 10 of register 10h to high can disable link pulse check function.

3.1.15 Automatic Link Polarity Detection

ADM7001's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 13 of register 11h.

3.1.16 Clock Synthesizer

The ADM7001 implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz +/- 50ppm.

3.1.17 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provide the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM7001 supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the ADM7001 can be controlled either by internal register access or by the use of configuration pins are sampled. If disabled, auto negotiation will not occur until software enables bit 12 in register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the ADM7001 transmits the abilities programmed into the auto negotiation advertisement register at address 04h via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiation, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05h.

The contents of the "auto negotiation link partner ability register" are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation by comparing the contents of register 04h and 05h and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.

1. 100Base-TX full duplex (highest priority)
2. 100Base-TX half duplex
3. 10Base-T full duplex
4. 10Base-T half duplex (lowest priority)

The basic mode control register at address 0h provides control of enabling, disabling, and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto negotiation enable bit (bit 12) is set.

The basic mode status register (BMSR) at address 1h indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the ADM7001. The BMSR also provides status on :
1.Whether auto negotiation is complete (bit 5)
2.Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
3.Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4h indicates the auto negotiation abilities to be advertised by the ADM7001. All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05h indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bits (bit 5, register address 1h and bit 4, register 17h) is set.

3.1.18 Auto Negotiation and Speed Configuration

The twelve sets of four pins listed in Table 3-2 Channel Configuration. Configure the speed capability of each channel of ADM7001. The logic state of these pins is latched into the advertisement register (register address 4h) for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0h) according to Table 3-2 Channel Configuration.

3.2 MAC Interface

The ADM7001 interfaces to 10/100 Media Access Controllers (MAC) via the RMII, MII, or GPSI Interface.

3.2.1 Reduced Media Independent Interface (RMII)

The reduced media Independent interface (RMII) is compliant to the RMII consortium's RMII Rev. 1.2 specification. The XI/OSCI pin that supplies the 50 MHz reference clock to the ADM7001 is used as the RMII REFCLK signal. All RMII signals with the exception of the assertion of CRSDV_P are synchronous to REFCLK.

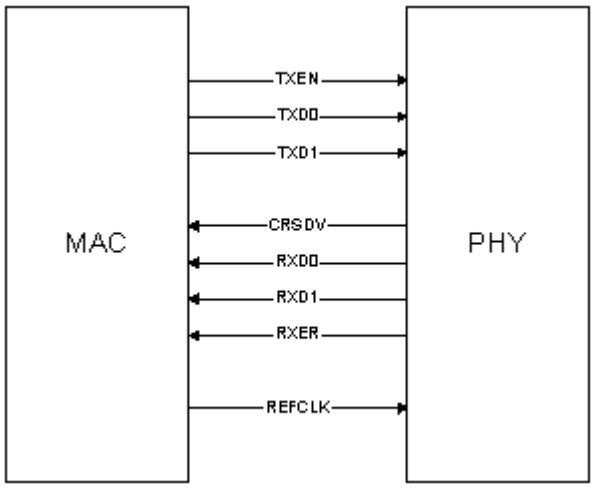


Figure 3-3 RMII Signal Diagram

3.2.2 Receive Path for 100M

Figure 3-4 shows the relationship among REFCLK, CRSDV, RXD and RXER while receiving a valid packet. Carrier sense is detected, which causes CRSDV to assert asynchronously to REFCLK. The received data is then placed into the FIFO for resynchronization. After a minimum of 12 bits are placed into the FIFO, the received data is presented onto RXD[1:0] synchronously to REFCLK. Note that while the FIFO is filling up RXD[1:0] is set to 00 until the first received di-bit of preamble (01) is presented onto RXD[1:0]. When carrier sense is de-asserted at the end of a packet, CRSDV is de-asserted when the first di-bit of a nibble is presented onto RXD[1:0] synchronously to REFCLK. If there is still data in the FIFO that has not yet been presented onto RXD[1:0], then on the second di-bit of a nibble, CRSDV reasserts. This pattern of assertion and de-assertion continues until all received data in the FIFO has been presented onto RXD[1:0]. RXER is inactive for the duration of the received valid packet.

Figure 3-5 shows the relationship among REFCLK, CRSDV and RXD[1:0] during a received false carrier event. CRSDV is asserted asynchronously to REFCLK as in the valid receive case shown in . However, once false carrier is detected, RXD[1:0] is changed to (10) (11) (Value 1110 in MII) and RXER is asserted. Both RXD[1:0] and RXER transition synchronously to REFCLK. After carrier sense is de-asserted, CRSDV is de-asserted synchronously to REFCLK.

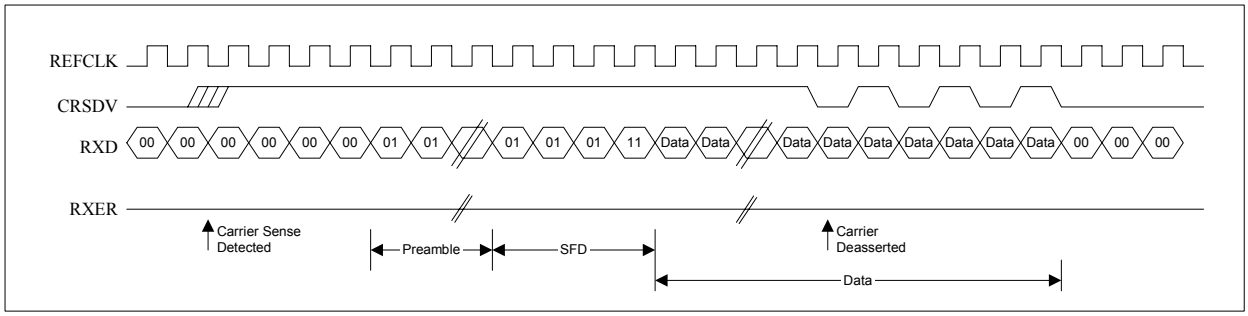


Figure 3-4 RMII Reception Without Error

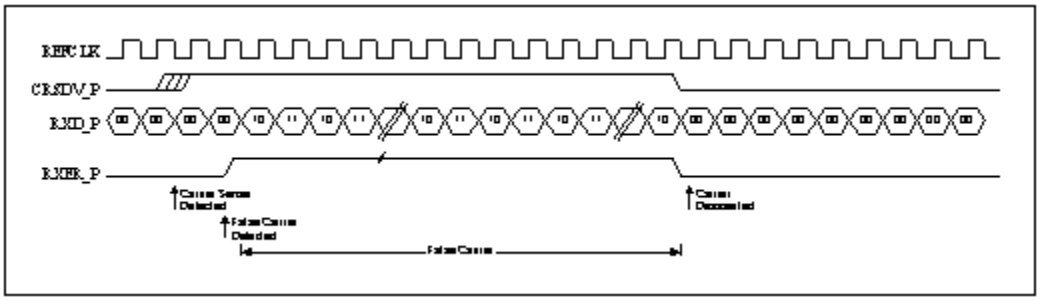


Figure 3-5 RMII Reception with False Carrier (100M Only)

A receive symbol error event is shown in figure 3-6. The packet with the symbol error is treated as if it were a valid packet with the exception that all di-bits are substituted with the (01) pattern.

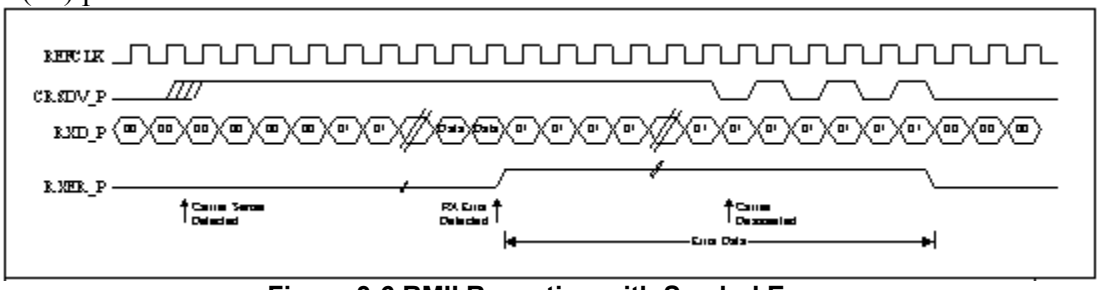


Figure 3-6 RMII Reception with Symbol Error

3.2.3 Receive Path for 10M

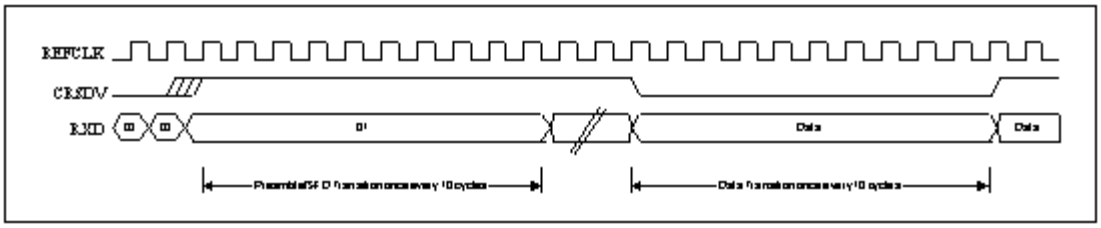


Figure 3-7 10M RMII Receive Diagram

In 10M Mode, RXER will maintain low all the time due to False Carrier and symbol error is not supported by 10M Mode. Different from 100M mode, RXD and CRSDV can

transition once per 10 REFCLK cycles. After carrier sense is de-asserted yet the FIFO data is not fully presented onto RXD, the CRSDV de-assertion and re-assertion also follows this rule.

3.2.4 Transmit Path for 100M

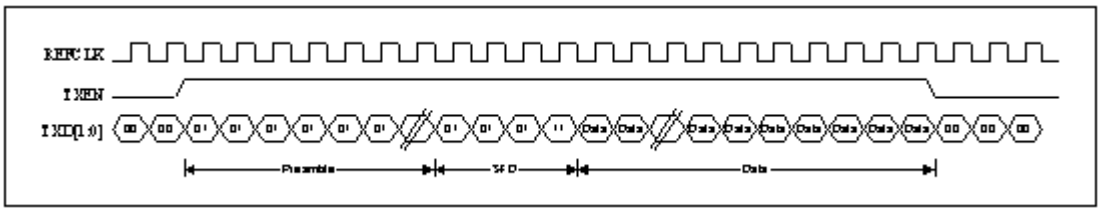


Figure 3-8 100M RMII Transmit Diagram

Figure 3-8 shows the relationship among REFCLK, TXEN and TXD[1:0] during a transmit event. TXEN and TXD[1:0] are synchronous to REFCLK. When TXEN is asserted, it indicates that TXD[1:0] contains valid data to be transmitted. When TXEN is de-asserted, value on TXD[1:0] should be ignored. If an odd number of di-bits are presented onto TXD[1:0] and TXEN, the final di-bit will be discarded by ADM7001.

3.2.5 Transmit Path for 10M

In 10MBSE-T mode, each di-bit must be repeated 10 times by the MAC, TXEN and TXD[1:0] should be synchronous to REFCLK. When TXEN is asserted, it indicates that data on TXD[1:0] is valid for transmission.

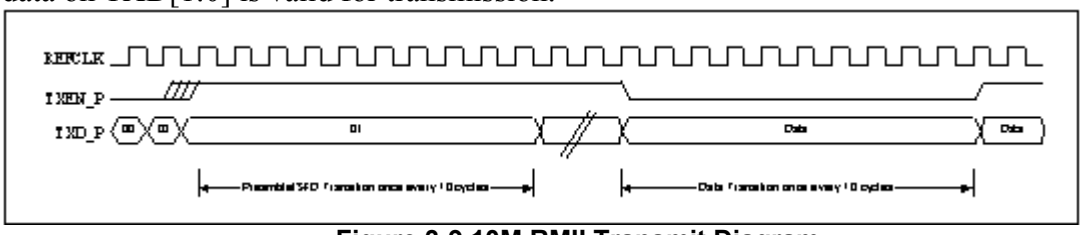


Figure 3-9 10M RMII Transmit Diagram

In 10BASE-T mode, it is possible that the number of preamble bits and the number of frame bits received are not integer nibbles. The preamble is always padded up such that the SFD appears on the RMII aligned to the nibble boundary. Extra bits at the end of the frame that do not complete a nibble are truncated by ADM7001. Figure 3□9 shows the timing diagram for 10M Transmission.

Table 3-2 Channel Configuration

3.2.6 Media Independent Interface (MII)

Signal Diagram for MII interface is shown in Figure 3-10.

Recommend Value			Auto Negotiation		Capability			
ANEN	SPD100	DUPFUL	Enable	Disable	100 Full	100 Half	10 Full	10 Half
1	1	1	✓		✓	✓	✓	✓
1	1	0	✓			✓		✓
1	0	1	✓				✓	✓
1	0	0	✓					✓
0	1	1		✓	✓			
0	1	0		✓		✓		
0	0	1		✓			✓	
0	0	0		✓				✓

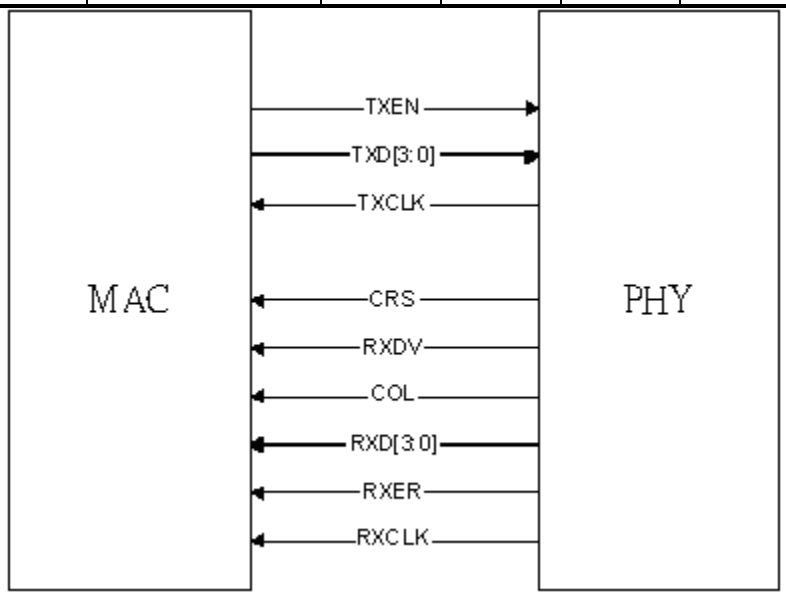


Figure 3-10 MII Signal Diagram

3.2.7 Receive Path for MII

Figure 3-11 shows the relationship among RXCLK, RXDV, RXD and CRS during a reception of valid packet. Carrier sense is detected and asserted asynchronously to RXCLK by ADM7001. When ADM7001 detects there is valid data, RXDV and the

received data is presented onto RXD[3:0] synchronously to RX_CLK. Whenever received data is not valid anymore, RXDV will be de-asserted by ADM7001 and "0" will be put on RXD[3:0].

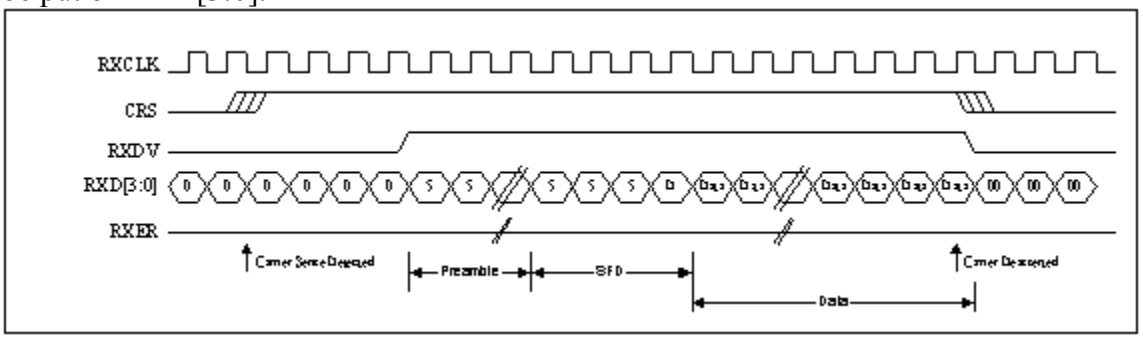


Figure 3-11 MII Receive Without Error

Figure 3-12 shows the relationship among RXCLK, RXDV and RXD[3:0] during a received false carrier event. CRS is asserted asynchronously to RXCLK as in the valid receive case shown in Figure 3-13. However, once false carrier is detected, RXD[3:0] is changed to (1110) and RXER is asserted. Both RXD[3:0] and RXER transition synchronously to RXCLK.

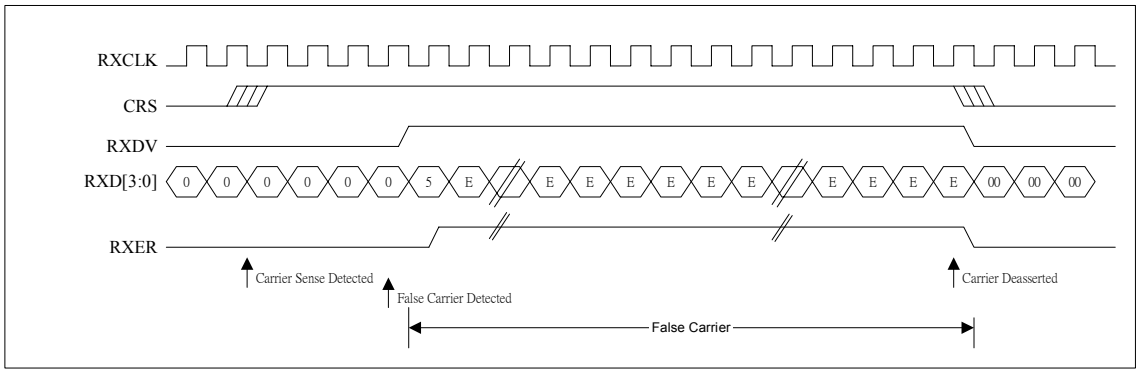


Figure 3-12 MII Receive With False Carrier

A receive symbol error event is shown in Figure 3-13. The packet with the symbol error is treated as if it were a valid packet with the exception that all bits are substituted with the (0101) pattern. RXER will keep low in 10M Operation.

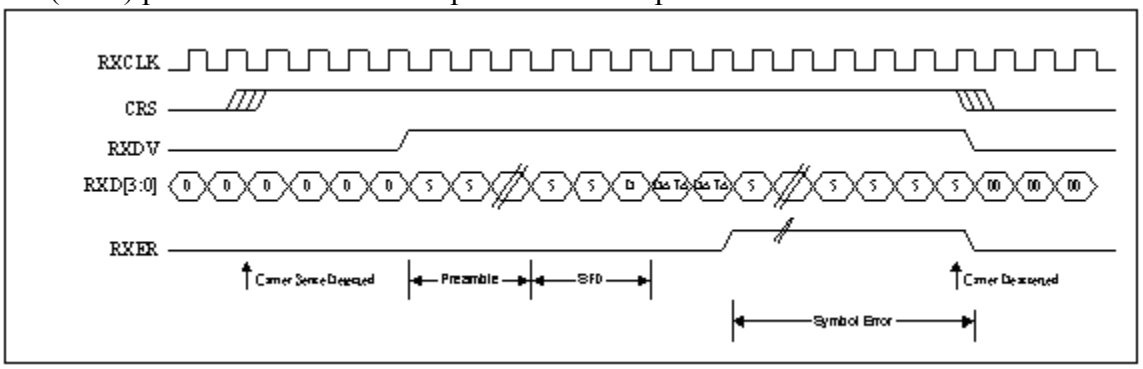


Figure 3-13 MII Receive With Symbol Error (100M Only)

3.2.8 Transmit Path For MII

Figure 3□14 shows the relationship among TXCLK, TXEN and TXD[3:0] during a transmit event. TXEN and TXD[3:0] are synchronous to TXCLK, which is generated by MAC. TXCLK is running at 25M in 100M mode and 2.5M in 10M mode. When TXEN is asserted, it indicates that TXD[3:0] contains valid data to be transmitted. When TXEN is de-asserted, value on TXD[1:0] should be ignored.

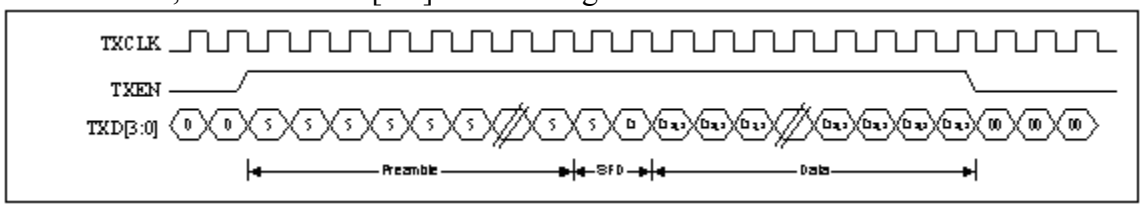


Figure 3-14 MII Transmission

When ADM7001 operates in half duplex mode, either 10M or 100M, it will assert COL signal whenever it detects there is collision on the medium. Figure 3-15 shows the timing diagram for MII Collision.

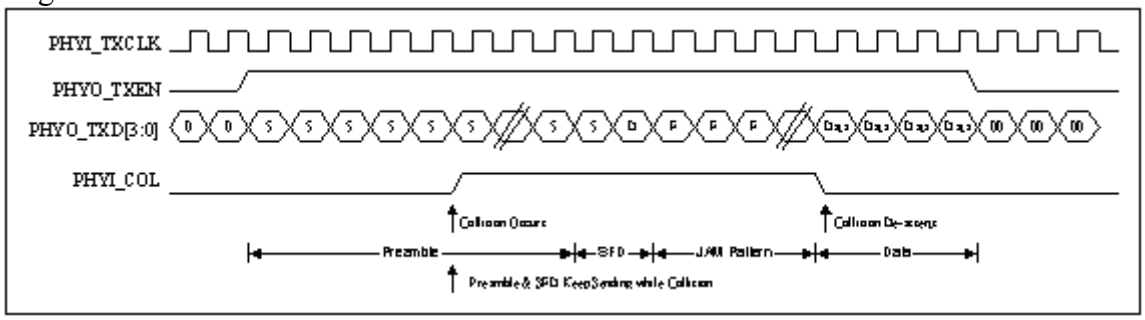


Figure 3-15 MII Transmit with Collision (Half Duplex Only)

3.2.9 General Purpose Serial Interface (GPSI)

Signal Diagram for MII interface is shown in Figure 3-16.

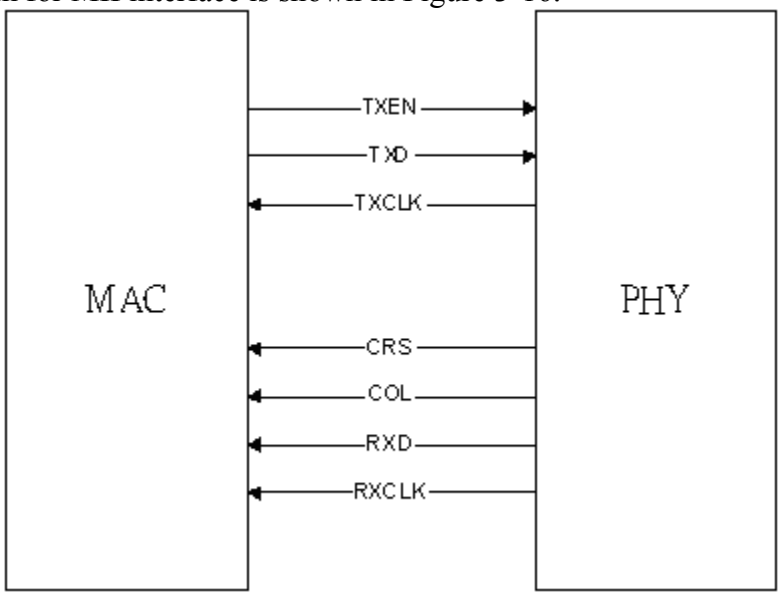


Figure 3-16 GPSI Signal Diagram

3.2.10 Receive Path for GPSI

Figure 3-17 shows the relationship among RXCLK, RXD and CRS during a receive of valid packet. Carrier sense is detected and asserted asynchronously to RXCLK by ADM7001. When ADM7001 detects there is valid data, received data is presented onto RXD synchronously to RXCLK. Whenever received data is not valid anymore, CRS will be de-asserted by ADM7001 and "0" will be put on RXD.

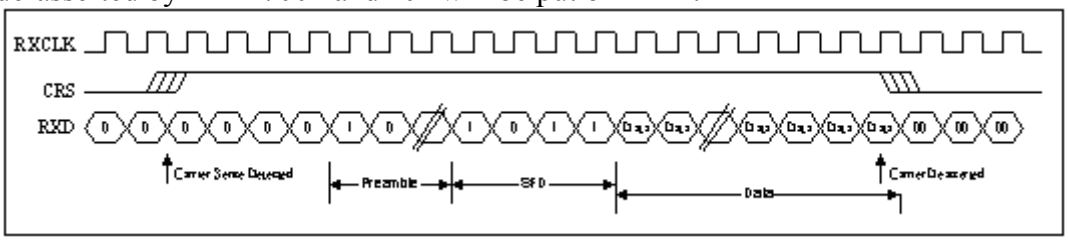


Figure 3-17 GPSI Receive Diagram

3.2.11 Transmit Path for GPSI

Figure 3-18 shows the relationship among TXCLK, TXEN and TXD during a transmit event. TXEN and TXD are synchronous to TXCLK, which is generated by MAC. TXCLK is running at 10M in 10M mode. When TXEN is asserted, it indicates that TXD contains valid data to be transmitted. When TXEN is de-asserted, value on TXD should be ignored.

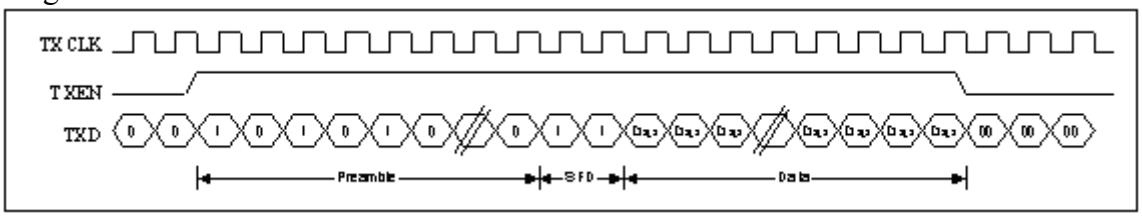


Figure 3-18 GPSI Transmit Diagram

3.3 LED Display

Register 19 is used for different mode led display. ADM7001 provides power on LED self test to minimize and ease the system test cost.

All LEDs will be Off during power on reset (Output value same as recommend value on LED pins). After power on reset, all internal parallel LEDs will be On for 2 seconds to ease manufacture overhead

There are three types of LED supported by ADM7001 internally. The first is LNKACT, which represents the status of Link and Transmit/Receive Activity; the second is LDSPD, which indicates the speed status and the last is DUPCOL, which shows pure duplex status in full duplex and duplex/collision combined status in half duplex. All these three LED can be controlled by Register 19 to change display contents.

After LED self test, Table 3-4, 3-5 and 3-6 show the On/Off polarity according to different recommended value setting for LDSPD, DUPCOL and LNKACT. When the

recommend value is high, ADM7001 will drive LED LOW; ADM7001 will drive the LED HIGH when the recommend value is low, instead.

SPEED	LDSPD
10M	0
100M	1
LINK FAIL	1

Table 3-3 Speed LED Display

DUPLEX	DUPCOL	
	HALF	FULL
LINK UP	Blink (HIGH) When Collision	LOW All the Time
LINK FAIL	HIGH All the Time	HIGH All the Time

Table 3-4 Duplex LED Display

SPEED	Link/Activity	
	Link	Activity
LINK UP	LOW	Blink (HIGH) When RX/TX
LINK FAIL	HIGH All the Time	HIGH All the Time

Table 3-5 Activity/Link LED Display

Besides duplex, speed, link and activity status, ADM7001 also provides cable information that can be shown on LEDs when register 19 is programmed to distance LED display (see Table 3-6).

LNKACT	DUPCOL	LEDSPD	Cable Distance
1	1	0	0 to 40 meters
1	0	0	40 to 80 meters
0	0	0	80 to 120 meters
1	1	1	Reserved

Table 3-6 Cable Distance LED Display

3.4 Management Register Access

The SMI consists of two pins, management data clock (MDC) and management data input/output (MDIO). The ADM7001 is designed to support an MDC frequency specified in the IEEE specification of up to 2.5 MHz. The MDIO line is bi-directional and may be shared by up to 32 devices.

The MDIO pin requires a 1.5 KΩ pull-up which, during idle and turnaround periods, will pull MDIO to a logic one state. Each MII management data frame is 64 bits long. The first 32 bits are preamble consisting of 32 contiguous logic one bits on MDIO and 32

corresponding cycles on MDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP) : <10> indicates read from MII management register operation, and <01> indicates write to MII management register operation. The next two fields are PHY device address and MII management register address. Both of them are 5 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the MDIO to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the MII management registers of the ADM7001.

3.4.1 Preamble Suppression

The ADM7001 supports a preamble suppression mode as indicated by an 1 in bit 6 of the basic mode status register (Register 1h). If the station management entity (i.e. MAC or other management controller) determines that all PHYs in the system support preamble suppression by reading a 1 in this bit, then the station management entity needs not generate preamble for each management transaction. The ADM7001 requires a single initialization sequence of 32 bits of preamble following powerup/hardware reset. This requirement is generally met by pulling-up the resistor of MDIO. While the ADM7001 will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required as specified in IEEE 802.3u.

When ADM7001 detects that there is physical address match, then it will enable Read/Write capability for external access. When neither physical address nor register address is matched, then ADM7001 will tri-state the MDIO pin.

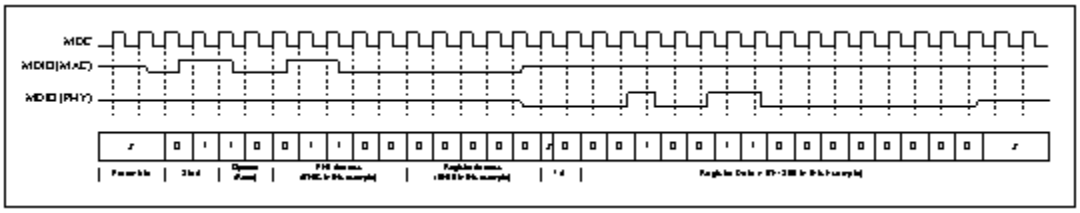


Figure 3-19 SMI Read Operation

3.4.2 Reset Operation

The ADM7001 can be reset either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with duration of at least 200 ms to the RC pin of the ADM7001 during normal operation to guarantee internal Power On Reset Circuit is reset well. Setting the reset bit in the Basic Mode Control activates software reset Register (bit 15, register 0h). This bit is self-clearing and, when set, will return a value of 1 until the software reset operation has completed, please note that internal SRAM will not be reset during software reset.

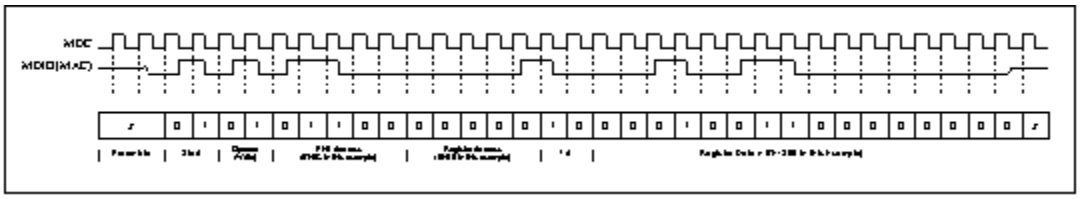


Figure 3-20 SMI Write Operation

Hardware reset operation samples the pins and initializes all registers to their default values. This process includes re-evaluation of all hardware configurable registers.

A software reset will reset an individual PHY and it does not latch the external pins nor reset the registers to their respective default value.

Logic levels on several I/O pins are detected during a hardware reset to determine the initial functionality of ADM7001. Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to VCC or Ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled up or weakly pulled down through resistors.

3.5 Power Management

An analog block is designed for carrier sense detecting. When there is no carrier sense presented on medium (cable not attached), then "SIGNAL DETECT" will not be ON. Whenever cable is attached to ADM7001 and the voltage threshold is above +/- 50mV, then SD will be asserted HIGH to indicate that there is cable attached to ADM7001. All internal blocks except Management block will be disabled (reset) before SD is asserted.

When SD is asserted, internal Auto Negotiation block will be turned on and the 10M transmit driver will also be turned on for auto negotiation process. Auto negotiation will issue control signals to control 10M receive and 100M A/D block according to different state in arbitration block diagram. During auto negotiation, all digital blocks except management and link monitor blocks will be disabled to reduce power consumption.

Whenever operating speed is determined (Either auto negotiation is On or Off), the non-active speed relative circuit will be disabled all the time to save more power. For example, when corresponding port is operating on 10M, then 100M relative blocks will be disabled and 10M relative blocks will be disabled whenever corresponding port is in 100M mode. Auto negotiation block will be reset when SD signal goes from high to low. See figure 3-21 for the state diagram for this algorithm.

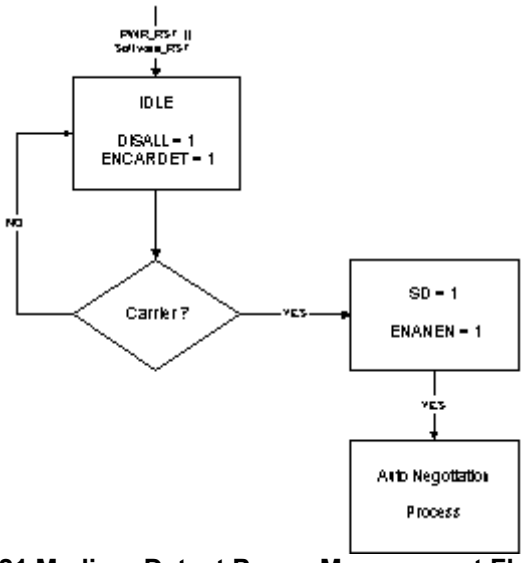


Figure 3-21 Medium Detect Power Management Flow Chart

Another way to reduce instant power is to separate the LED display period. All 4 LEDs will be divided into 4 time frame and each time frame occupies 1 us. One and only one LED will be driven at each time frame to reduce instant current consumed from LED.

3.6 Voltage Regulator

ADM7001 requires two different levels, 3.3V and 2.5V, of voltage supply to provide the power to different parts of circuitry inside the chip. ADM7001 has a build-in voltage regulator circuitry to generate the 2.5V voltage (VCC25OUT) from 3.3V power source (VCC3IN). External Application Circuitry is shown in 3-22.

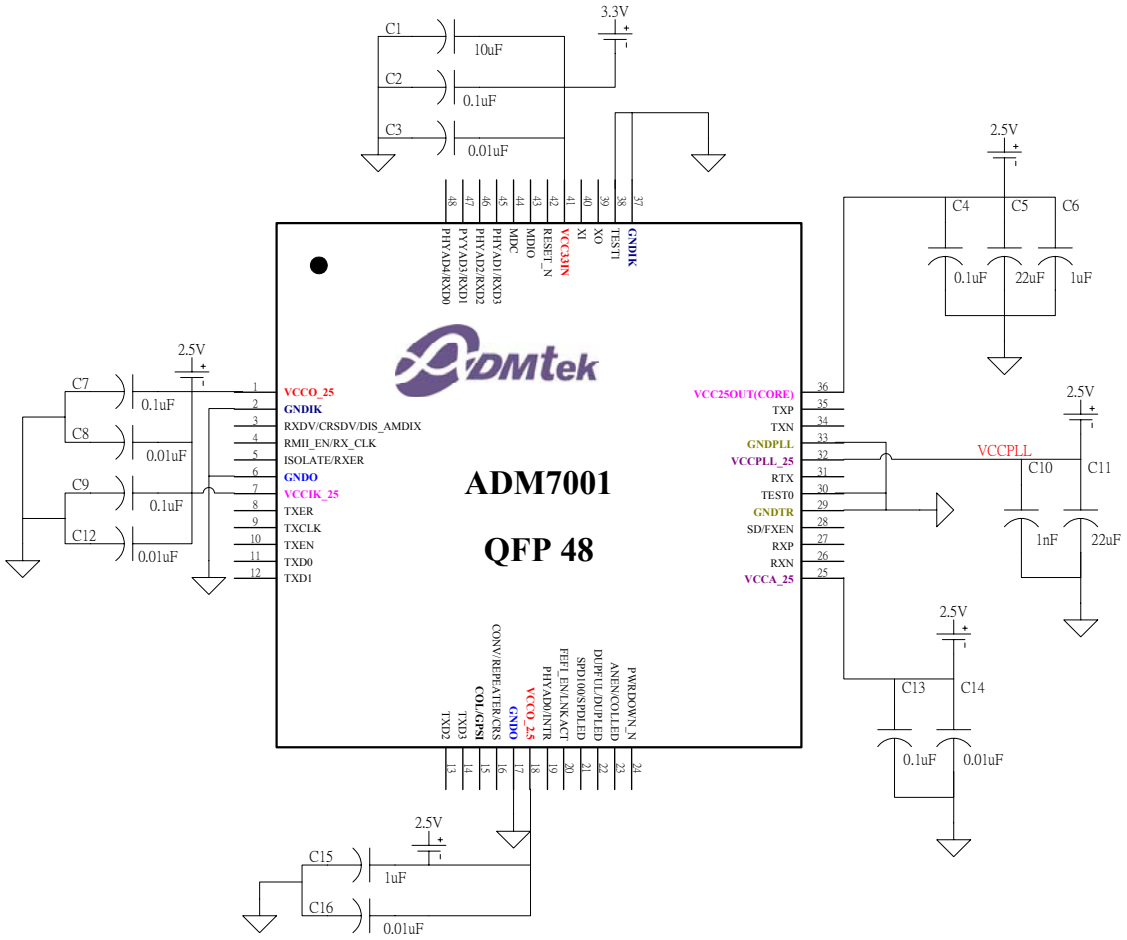


Figure 3-22 Power and Ground Filtering

Note: Place all capacitors as close as possible to each power pin.

Chapter 4 Register Description

Note:
Please refer to section '*1.5.2 Register Type Descriptions*' for an explanation of pin abbreviations.

4.1 Register Mapping

Address	Register Name	Default
0h	Control Register	3000
1h	Status Register	7849
2h – 3h	PHY Identifier Register	002E_CC62
4h	Auto Negotiation Advertisement Register	01E1
5h	Auto Negotiation Link Partner Ability Register	01E1
6h	Auto Negotiation Expansion Register	0000
7h - Fh	Reserved	Reserved
10h	PHY Control Register	1000
11h	PHY 10M Configuration Register	0008
12h	PHY 100M Configuration Register	0022
13h	LED Configuration Register	0A34
14h	Interrupt Enable Register	03FF
16h	PHY Generic Status Register	0000
17h	PHY Specific Status Register	0060
18h	Recommend Value Storage Register	0000
19h	Global Interrupt Status Register	0000
1Dh	Receive Error Counter	0000
1Eh	Reserved	1000
1Fh	Chip ID Register	8125

4.2 Register Bit Mapping

4.2.1 Register #0h -- Control Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST	LPBK	SPD_L	ANEN	PDN	ISO	RSTAR	DPLX	COLTST	SPDMSB	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	PIN	R/W	R/W	RO	RO	RO	RO	RO	RO

4.2.2 Register #1h – Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CAPT4	TXFUL	TXHALF	TFUL	THALF	CAPT2	0	0	0	MFSUP	ANCOMP	RMFLT	ANEN	LINK	JAB	EXTCAP
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.3 Register #2h – PHY ID Register (002E)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.4 Register #3h – PHY ID Register (CC62)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID5	ID4	ID3	ID2	ID1	ID0	MOD5	MOD4	MOD3	MOD2	MOD1	MOD0	REV3	REV2	REV1	REV0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.5 Register #4h – Advertisement Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPAGE	0	RF	0	ASM_DIR	PAUSE	T4	FDX100	HDX100	FDX10	HDX10	0	0	0	0	1
R/W	RO	R/W	RO	R/W	R/W	RO	R/W	R/W	R/W	R/W	RO	RO	RO	RO	RO

4.2.6 Register #5h – Link Partner Ability Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPAGE	ACK	RF	0	LP_DIR	LP_PAU	LP_T4	LP_FDX	LP_HDX	LP_F10	LP_H10	0	0	0	0	1
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.7 Register #6h – Auto Negotiation Expansion Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	PDFLT	LPNPAB	NPABLE	PGRCV	LPANAB
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.8 Register #7h – # Fh Reserved

4.2.9 Register #10h – PHY Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IFSEL1	IFSEL0	LBKMD1	LBKMD0	0	0	FLTLED	CONV	0	0	0	XOVEN	0	0	0	DISPMG
RO	RO	R/W	R/W	RO	RO	R/W	R/W	RO	RO	RO	R/W	R/W	R/W	RO	R/W

4.2.10 Register #11h – 10M Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SERIAL	1	0	0	INTCHKEN	1	1	0	1	0	APDIS	ENRJAB	DISTJAB	NTH	FGDLNK
RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

4.2.11 Register #12h – 100M Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	SELFX	0	1	DISSCR	ENFEFI	DIS_CABL EN_LED	INTR_AC TIVE	0
RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	RO

4.2.12 Register #13h – LED Configuration Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Reserved	Reserved	LNKC3	LNKC2	LNKC1	LNKC0	COLC3	COLC2	COLC1	COLC0	SPDC3	SPDC2	SPDC1	SPDC0
RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

4.2.13 Register #14h – Interrupt Enable Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	XOVCHG	SPDCHG	DUPCHG	PGRCHG	LNKCHG	SYMERR	FCAR	FOURUN	TJABINT	RJABINT
RO	RO	RO	RO	RO	RO	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

4.2.14 Register #16h – PHY Generic Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	Reserved	Reserved	Reserved	MD	FXEN	XOVER	CBLEN7	CBLEN6	CBLEN5	CBLEN4	CBLEN3	CBLEN2	CBLEN1	CBLEN0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.15 Register #17h – PHY Specific Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	JABRX	JABTX	POLAR	PAUOUT	PAUIN	DUPLEX	SPEED	LINK	RECPAU	RECDUP	RECSPD	RECAN
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.16 Register #18h – Recommend Value Storage Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RECAN	SELFX	REC100	RECFUL	PAUREC	DISFEFI	XOVEN	XOVER	RMII_SMII	REPEATER	PHYA4	PHYA3	PHYA2	PHYA1	PHYA0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.17 Register #19h – Interrupt Status Register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	XOVCHG	SPDCHG	DUPCHG	PGRCHG	LNKCHG	SYMERR	FCAR	FOURUN	TJABINT	RJABINT
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.18 Register #1dh – Receive Error Counter

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERB15	ERB14	ERB13	ERB12	ERB11	ERB10	ERB9	ERB8	ERB7	ERB6	ERB5	ERB4	ERB3	ERB2	ERB1	ERB0
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.2.19 Register #1fh – Chip ID (8125)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CID33	CID32	CID31	CID30	CID23	CID22	CID21	CID20	CID13	CID12	CID11	CID10	CID03	CID02	CID01	CID00
RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO

4.3 Register Description

4.3.1 Control (Register 0h)

Bit #	Name	Description	Type	Default	Interface
15	RST	*RESET* 1: PHY Reset 0: Normal operation Setting this bit initiates the software reset function that resets the selected port, except for the phase-locked loop circuit. It will re-latch in all hardware configuration pin values. The software reset process takes 25us to complete. This bit, which is self-clearing, returns a value of 1 until the reset process is complete.	R/W SC	0h	1.Updated by MDC/MDIO. 2.Connect to Central Control Block to Generate Reset Signal.
14	LPBK	*Back Enable* 1:Enable loop back mode 0: Disable Loop back mode This bit controls the PHY loop back operation that isolates the network transmitter outputs (TXP and TXN) and routes the MII transmit data to the MII receive data path. This function should only be used when auto negotiation is disabled (bit12 = 0). The specific PHY (10Base-T or 100Base-X) used for this operation is determined by bits 12 and 13.	R/W	0h	1.Updated by MDC/MDIO Only. Control the Wire connection in Driver
13	SPEED_LSB	*Speed Selection LSB* 0.60.13 0 0 10 Mbps 0 1 100 Mbps 1 0 1000 Mbps 1 1 Reserved Link speed is selected by this bit or by auto negotiation if bit 12 of this register	R/W	1h	When Auto Negotiation is enable, this pin has no effect.

Bit #	Name	Description	Type	Default	Interface
		is set (in which case, the value of this bit is ignored).			
12	ANEN	*Auto Negotiation Enable* 1: Enable auto negotiation process 0: Disable Auto negotiation process This bit determines whether the link speed should set up by the auto negotiation process or not. It is set at power up or reset if the PI_RECANEN pin detects a logic 1 input level in Twisted-Pair Mode.	R/W	1h	
11	PDN	*Power Down Enable* 1: Power Down 0: Normal Operation Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY841F into power down mode. During the power down mode, TXP/TXN and all LED outputs are tri-stated and the MII/RMII interfaces are isolated.	R/W	0h	1.Only Access through MDC/MDIO
10	ISO	*Isolate PHY841F from Network* 1: Isolate PHY from MII/RMII 0: Normal Operation Setting this control bit isolates the part from the RMII/MII, with the exception of the serial management interface. When this bit is asserted, the PHY841F does not respond to TXD, TXEN and TXER inputs, and it presents a high impedence on its TXC, RXC, CRSDV, RXER, RXD, COL and CRS outputs.	R/W	0h	1.Only Access through MDC/MDIO 2.Used to reset corresponding port.
9	ANEN_RST	*Restart Auto Negotiation* 1: Restart Auto Negotiation Process 0: Normal Operation Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced.	R/W SC	0h	
8	DPLX	*Duplex Mode* 1: Full Duplex mode 0: Half Duplex mode If auto negotiation is disabled, this bit	R/W	0h	

Bit #	Name	Description	Type	Default	Interface
		determines the duplex mode for the link.			
7	COLTST	*Collision Test* 1: Enable COL signal test 0: Disable COL signal test When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN.	R/W	0h	
6	SPEED_MSB	*Speed Selection MSB* Set to 0 all the time indicate that the PHY841F does not support 1000 Mbps function.	RO	0h	Always 0.
5:0	Reserved	Not Applicable	RO	00h	Always 0.

4.3.2 Status (Register 1h)

Bit #	Name	Description	Type	Default	Interface
15	CAP_T4	*100Base-T4 Capable* Set to 0 all the time to indicate that the PHY841F does not support 100Base-T4	RO	0h	
14	CAP_TXF	*100Base-X Full Duplex Capable* Set to 1 all the time to indicate that the PHY841F does support Full Duplex mode	RO	1h	
13	CAP_TXH	*100Base-X Half Duplex Capable* Set to 1 all the time to indicate that the PHY841F does support Half Duplex mode	RO	1h	
12	CAP_TF	*10M Full Duplex Capable* TP : Set to 1 all the time to indicate that the PHY841F does support 10M Full Duplex mode FX : Set to 0 all the time to indicate that the PHY841F does not support 10M Full Duplex mode	RO	1h	
11	CAP_TH	*10M Half Duplex Capable* TP : Set to 1 all the time to indicate that the PHY841F does support 10M Half Duplex mode FX : Set to 0 all the time to indicate that the PHY841F does not support 10M Half Duplex mode	RO	1h	
10	CAP_T2	*100Base-T2 Capable* Set to 0 all the time to indicate that the PHY841F does not support 100Base-T2	RO	0h	
9:7	Reserved	Not Applicable	RO	0h	

Bit #	Name	Description	Type	Default	Interface
6	CAP_SUPR	*MF Preamble Suppression Capable* This bit is hardwired to 1 indicating that the PHY841F accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification.	RO	1h	Use to Control MDC/MDIO State Machine.
5	AN_COMP	*Auto Negotiation Complete* 1: Auto Negotiation process completed 0: Auto Negotiation process not completed If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected.	RO	0h	Status Updated by Auto Negotiation Control Block.
4	REM_FLT	*Remote Fault Detect* 1: Remote Fault detected 0: Remote Fault not detected This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05h) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read.	RO	0h	Status Updated by Auto Negotiation Control Block
3	CAP_ANEG	*Auto Negotiation Ability* 1: Capable of auto negotiation 0: Not capable of auto negotiation TP : This bit is set to 1 all the time, indicating that PHY841F is capable of auto negotiation. FX : This bit is set to 0 all the time, indicating that PHY841F is not capable of auto negotiation in Fiber Mode.	RO	1h	
2	LINK	*Link Status* 1: Link is up 0: Link is down This bit reflects the current state of the link -test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface.	RO, LL	0h	Updated By Per port Link Monitor

Bit #	Name	Description	Type	Default	Interface
		Whenever Linkup, this bit should be read twice to get link up status			
1	JAB	*Jabber Detect* 1: Jabber condition detected 0: Jabber condition not detected	RO, LH	0h	Updated by Per port Jabber Detector
0	EXTREG	*Extended Capability* 1: Extended register set 0: No extended register set This bit defaults to 1, indicating that the PHY841F implements extended registers.	RO	1h	

4.3.3 PHY Identifier Register (Register 2h)

Bit #	Name	Description	Type	Default	Interface
15:0	PHY-ID[15:0]	IEEE Address	RO	002E	

4.3.4 PHY Identifier Register (Register 3h)

Bit #	Name	Description	Type	Default	Interface
15:10	PHY-ID[15:0]	IEEE Address/Model No./Rev. No.	RO	CC10	
9:4	MODEL[5:0]	INFINEON-ADMTEK CO LTD PHY Model ID.	RO	CC10	
3:0	REV-ID[3:0]	INFINEON-ADMTEK CO LTD PHY Revision ID.	RO	2h	

4.3.5 Advertisement (Register 4h)

Bit #	Name	Description	Type	Default	Interface
15	NP	Ne*xt Page* This bit is defaults to 1, indicating that PHY841F is next page capable.	R/W	0h	
14	Reserved	Not Applicable	RO	0h	
13	RF	*Remote Fault* 1 □ Remote Fault has been detected 0 □ No remote fault has been detected This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner.	R/W	0h	S/W should read status from Register 1 (bit 1.4) and fill out this bit during Auto Negotiation in case Remote Fault is detected.
12	Reserved	Not Applicable	RO	0h	
11	ASM_DIR	*Asymmetric Pause Direction* Bit[11:10] Capability	R/W	0h	

Bit #	Name	Description	Type	Default	Interface
		00 No Pause 01 Symmetric PAUSE 10 Asymmetric PAUSE toward Link Partner 11 Both Symmetric PAUSE and Asymmetric PAUSE toward local device			
10	PAUSE	*Pause Operation for Full Duplex* Value on PAUREC will be stored in this bit during power on reset.	R/W	pin	
9	T4	*Technology Ability for 100Base-T4* Defaults to 0.	RO	0h	
8	TX_FDX	100Base-TX Full Duplex 1: Capable of 100M Full duplex operation 0: Not capable of 100M Full duplex operation	R/W	1h	Used by Auto Negotiation Block
7	TX_HDX	*100Base-TX Half Duplex* 1: Capable of 100M operation 0: Not capable of 100M operation	R/W	1h	Used By Auto Negotiation Block
6	10_FDX	*10BASE-T Full Duplex* 1: Capable of 10M Full Duplex operation 0: Not capable of 10M full duplex operation	R/W	1h	Used By Auto Negotiation Block
5	10_HDX	*10Base-T Half Duplex* 1: Capable of 10M operation 0: Not capable of 10M operation	R/W	1h	Used By Auto Negotiation Block ***Note:*** that bit 8:5 should be combined with SPD100, DUPFUL pin input to determine the finalized speed and duplex mode.
4:0	Selector Field	These 5 bits are hardwired to 00001b, indicating that the PHY841F supports IEEE 802.3 CSMA/CD.	RO	01h	Used by Auto Negotiation Block.

4.3.6 Auto Negotiation Link Partner Ability (Register 5h)

Bit #	Name	Description	Type	Default	Interface

Bit #	Name	Description	Type	Default	Interface
15	NPAGE	*Next Page* 1: Capable of next page function 0: Not capable of next page function	RO	0h	Updated by Auto Negotiation Block
14	ACK	*Acknowledge* 1: Link Partner acknowledges reception of the ability data word 0: Not acknowledged	RO	0h	Updated by Auto Negotiation Block
13	RF	*Remote Fault* 1: Remote Fault has been detected 0: No remote fault has been detected	RO	0h	Updated by Auto Negotiation Block
12	Reserved	Not Applicable	RO	0h	
11	LP_DIR	*Link Partner Asymmetric Pause Direction.*	RO	0h	Updated by Auto Negotiation Block
10	LP_PAU	*Link Partner Pause Capability* Value on PAUREC will be stored in this bit during power on reset.	RO	0h	Updated by Auto Negotiation Block
9	LP_T4	*Link Partner Technology Ability for 100Base-T4* Defaults to 0.	RO	0h	Updated by Auto Negotiation Block
8	LP_FDX	*100Base-TX Full Duplex* 1: Capable of 100M Full duplex operation 0: Not capable of 100M Full duplex operation	RO	1h	Used by Auto Negotiation Block
7	LP_HDX	*100Base-TX Half Duplex* 1: Capable of 100M operation 0: Not capable of 100M operation	RO	1h	Used By Auto Negotiation Block
6	LP_F10	*10BASE-T Full Duplex* 1: Capable of 10M Full Duplex operation 0: Not capable of 10M full duplex operation	RO	1h	Used By Auto Negotiation Block
5	LP_H10	*10Base-T Half Duplex* 1: Capable of 10M operation 0: Not capable of 10M operation	RO	1h	Used By Auto Negotiation Block
4:0	Selector Field	*Encoding Definitions.*	RO	01h	Updated By Auto Negotiation Block.

4.3.7 Auto Negotiation Expansion Register (Register 6h)

Bit #	Name	Description	Type	Default	Interface
15:5	Reserved	Not Applicable	RO	000h	000h
4	PFAULT	*Parallel Detection Fault*	RO,	0h	Updated by Auto

Bit #	Name	Description	Type	Default	Interface
		1: Fault has been detected 0: No Fault Detect	LH		Negotiation Block
3	LPNPABLE	Link Partner Next Page Able 1: Link Partner is next page capable 0: Link Partner is not next page capable	RO	0h	Updated By Auto Negotiation Block
2	NPABLE	*Next Page Able* 0: Next page Disable 1: Next page Enable.	RO	0h	
1	PGRCV	*Page Received* 1: A new page has been received 0: No new page has been received	RO, LH	0h	Updated By Auto Negotiation Block
0	LPANABLE	*Link Partner Auto Negotiation Able* 1: Link Partner is auto negotiable 0: Link Partner is not auto negotiable	RO	0h	Updated By Auto Negotiation Block

4.3.8 Register Reserved (Register 7h-Fh)

Bit #	Name	Description	Type	Default	Interface
15:0	Reserved				

4.3.9 Generic PHY Configuration Register (Register 10h)

Note: PHY Control/Configuration Registers start from address 16 to 21.

Bit #	Name	Description	Type	Default	Interface
15:14	IFSEL[1:0]	Interface Select. Value on RMII_EN and GPSI will be stored in IFSEL[1] and IFSEL[0], respectively. 00: MII 01: GPSI 1x : RMII	RO	1h	
13:12	LBKMD[1:0]	Loop Back Mode Select. When 0.14 LPBK is set to 1, these two bits are set to 01 by default. Value on these two bits can be modified through MDC/MDIO. When 0.14 LPBK is set to 0, these two bits are reset to 00 and can't be updated by MDC/MDIO. 00 : Disable Loop back 01 : PCS Layer Loop back mode 10 : PMA Layer Loop back mode 11 : PMD layer loop back mode Note : Both 10M and 100M loopback should be	R/W	0h	

Bit #	Name	Description	Type	Default	Interface
		covered by AD2106.			
11:10	Reserved	Not Applicable	RO	0h	
9	FLTLED	Enable colled output remote fault status 0: Disable 1: Enable.	R/W	0h	
8	CONV	Converter mode (only valid in rmii mode) 0:normal mode 1:converter mode	R/W	0h	
7:5	Reserved	Not Applicable	RO	0h	
4	XOVEN	*Cross Over Auto Detect Enable.* 0: Disable 1: Enable	R/W	pin	~DIS_AMDIX
3:2	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.	R/W	0h	
1	ENREG8	Enable Register 8 to Store Next Page Information. 1 – Store Next Page in Register 8 0 – Store Next Page in Register 5	R/W	1h	Only Available when Auto Negotiation Enabled.
0	DISPMG	*Disable Power Management Feature.* 0: Enable. Enable Medium Detect Function. 1: Disable. Medium_On is high all the time.	R/W	0h	

4.3.10 PHY 10M Module Configuration Register (Register 11h)

Bit #	Name	Description	Type	Default	Interface
15	Reserved		RO	0h	
14	SERIAL	*10BASE-T Serial Mode Select. Only available when AD2106 works in 10M mode.* 0 : 10M MII or RMII mode (According to RMII_EN) 1 : 10M Serial Mode (Seven Wire Mode)	R/W	0h	GPSI Recommend Value
13	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 1 to this bit may cause abnormal operation.	R/W	1h	
12:11	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.	R/W	0h	
10	INTCHKEN	Polarity Interval Timer Check Enable. 1 = Enable 0 = Disable	R/W	1h	
9	Reserved	Infineon-ADMtek Co Ltd reserved bits.	R/W	1h	

Bit #	Name	Description	Type	Default	Interface
		Writing value other than 1 to this bit may cause abnormal operation.			
8:6	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 5 to these three bits may cause abnormal operation.	R/W	5h	
5	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 1 to this bit may cause abnormal operation.	R/W	0h	
4	APDIS	*Auto Polarity Disable* 1: Auto Polarity Function Disabled 0: Normal	R/W	0h	
3	ENRJAB	*Enable Receive Jabber Monitor.* 0: Disable 1: Enable	R/W	1h	
2	DISTJAB	*Disable Transmit Jabber* 1: Disable Transmit Jabber Function 0: Enable Transmit Jabber Function	R/W	0h	
1	NTH	*Normal Threshold* 0: Lower 10BASE-T Receive threshold 1: Normal 10BASE-T Receive threshold	R/W	0h	
0	FGDLNK	*Force 10M Receive Good Link* 1: Force Good Link 0: Normal Operation	R/W	0h	

4.3.11 PHY 100M Module Control Register (Register 12h)

Bit #	Name	Description	Type	Default	Interface
15:12	Reserved		RO	0h	
11:10	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.	R/W	0h	
9:8	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.	R/W	00h	
7	SELFX	*Fiber Select* 1: Fiber Mode 0: TP Mode	R/W	pin	FXEN
6:5	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.	R/W	1h	
4	DISSCR	*Disable Scrambler* 1: Disable Scrambler 0: Enable Scrambler When set to fiber mode, this bit will be	R/W	pin	When programmed to fiber mode, set to 1 automatically

Bit #	Name	Description	Type	Default	Interface
		forced to 1 automatically. Write 0 to this bit in Fiber Mode has no effect.			
3	ENFEFI	*Enable FEFI* 1: Enable FEFI 0: Disable FEFI	R/W	0h	
2	DIS_CABLEN_LED	*Disable cable length led indication* When this bit is set to 0, SPDLED, COLLED and LNKACTLED are used to represent twisted pair cable length. See SPDLED description for more detail 1'b1 : disable cable length led 1'b0 : enable cable length led	RO	1h	
1	INTR_ACTIVE	Interrupt active value control 1: active low 0: active low	R/W	1h	
0	Reserved	Infineon-ADMtek Co Ltd reserved bits. Writing value other than 0 to this bit may cause abnormal operation.	R/W	0h	

4.3.12 LED Configuration Register (Register 13h)

Bit #	Name	Description	Type	Default	Interface
15:12	Reserved		RO	0h	
11:8	LNKCTRL	*Link/Act LED Control.* 0000: Collision 0001: All Errors 0010: Duplex 0011: Duplex/Collision 0100: Speed 0101: Link 0110: Transmit Activity 0111: Receive Activity 1000: TX/RX Activity 1001: Link/Receive Activity 1010: Link and TX/RX Activity 1011: 100M False Carrier Error/10M Receive Jabber 1100: 100M Error End of Stream/10M Transmit Jabber 1101: Reserved 1110: Distance (See LED Description for more detail)	RO	1010	
7:4	COLCTRL	*COLLISION LED Control.* 0000: Collision	RO	0000	

Bit #	Name	Description	Type	Default	Interface
		0001: All Errors 0010: Duplex 0011: Duplex/Collision 0100: Speed 0101: Link 0110: Transmit Activity 0111: Receive Activity 1000: TX/RX Activity 1001: Link/Receive Activity 1010: Link and TX/RX Activity 1011: 100M False Carrier Error/10M Receive Jabber 1100: 100M Error End of Stream/10M Transmit Jabber 1101: Reserved 1110: Distance (See LED Description for more detail)			
3:0	SPDCTRL	*Speed LED Control.* 0000: Collision 0001: All Errors 0010: Duplex 0011: Duplex/Collision 0100: Speed 0101: Link 0110: Transmit Activity 0111: Receive Activity 1000: TX/RX Activity 1001: Link/Receive Activity 1010: Link and TX/RX Activity 1011: 100M False Carrier Error/10M Receive Jabber 1100: 100M Error End of Stream/10M Transmit Jabber 1101: reserved 1110: Distance (See LED Description for more detail)	RO	0100	

4.3.13 Interrupt Enable Register (Register 14h)

Bit #	Name	Description	Type	Default	Interface
15:10	Reserved		RO	00h	
9	XOVCHG	*Cross Over mode Changed Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
8	SPDCHG	*Speed Changed Interrupt Enable*	R/W	1h	

Bit #	Name	Description	Type	Default	Interface
		1: Interrupt Enable 0: Interrupt Disable			
7	DUPCHG	*Duplex Changed Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
6	PGRCHG	*Page Received Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
5	LNKCHG	*Link Status Changed Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
4	SYMERR	*Symbol Error Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
3	FCAR	*False Carrier Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
2	TJABINT	*Transmit Jabber Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
1	RJABINT	*Receive Jabber Interrupt Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	
0	ESDERR	*Error End of Stream Enable* 1: Interrupt Enable 0: Interrupt Disable	R/W	1h	

4.3.14 PHY Generic Status Register (Register 16h)

Note: PHY Status Registers start from 22 to 28 (29 to 30 reserves for further use)

Bit #	Name	Description	Type	Default	Interface
15:14	Reserved		RO	00h	
13:11	Reserved	Not Applicable			
10	MD	*Medium Detect. Real Time Status for Medium_Detect Signal* 0: Medium_Detect Fail 1: Medium_Detect Pass	RO	0h	
9	FXEN	*Fiber Enable. Only Changed when PHY Reset* 0: TX 1: FX mode OR'ed result of FXEN and 17.9 (SELFX)	RO	pin	FXEN
8	XOVER	*Cross Over status.* 0: MDI mode	RO	0h	

Bit #	Name	Description	Type	Default	Interface
		1: MDIX mode			
7:0	CBLEN	*Cable Length.* Only valid for 100M MSB is IC0 8'h1a: 40 meters 8'h22: 60 meters 8'h94: 80 meters 8'h9a: 100 meters 8'ha2: 120 meters 8'hab: 140 meters	RO	00h	

4.3.15 PHY Specific Status Register (Register 17h)

Bit #	Name	Description	Type	Default	Interface
15:12	Reserved		RO	0h	Force to 0 all the time.
11	JAB-RX	*Real Time 10M Receive Jabber Status* 1: Jabber 0: No jabber	RO	0h	
10	JAB_TX	*Real Time 10M Transmit Jabber Status* 1:Jabber 0: No Jabber	RO	0h	Updated by 10M Block
9	POLAR	*Polarity.* Only available in 10M 0: Normal Polarity 1: Polarity Reversed	RO	0h	
8	PAUOUT	*Pause Out capability.* Disabled when Half Duplex. 0: Lack of Pause Out capability 1: Has Pause Out capability	RO	0h	
7	PAUIN	*Pause In capability.* Disabled when Half Duplex. 0: Lack of Pause In capability 1: Has Pause In capability	RO	0h	
6	DUPLEX	*Operating Duplex* 1: Full Duplex 0: Half Duplex	RO	1h	
5	SPEED	*Operating Speed* 1: 100Mb/s 0: 10Mb/s	RO	1h	
4	LINK	*Real Time Link Status* 1: Link Up 0: Link Down	RO	0h	

Bit #	Name	Description	Type	Default	Interface
3	RECPAU	*Pause Recommend Value.* Only Changed when PHY Reset. This bit is disabled automatically when RECDUP is 0. 0: Pause Disable 1: Pause Enable	RO	pin	
2	RECDUP	*Duplex Recommended Value.* Only Changed when PHY Reset 1: Full Duplex 0: Half Duplex	RO	pin	DUPFUL
1	RECSPD	*Speed Recommend Value.* Only Changed when PHY Reset 1: 100M 0: 10M	RO	pin	SPD100
0	RECANEN	*Recommended Auto Negotiation Value***.** Only Changed when PHY Reset	RO	pin	ANEN

4.3.16 PHY Recommend Value Status Register (Register 18h)

Bit #	Name	Description	Type	Default	Interface
15	Reserved	Not Applicable	RO	pin	
14	RECAN	*Auto Negotiation Recommend Value*	RO	pin	
13	SELFX	*Fiber Select Recommend Value*	RO	pin	
12	REC100	*Speed Recommend Value* 0: 10M 1: 100M	RO	pin	
11	RECFUL	*Duplex Recommend Value.* 0: Half Duplex 1: Full Duplex	RO	pin	
10	PAUREC	*Pause Capability Recommend Value* 1: Pause Enable 0: Pause Disable	RO	1'b0	
9	DISFEFI	*Far End Fault Disable.* 0: Enable 1: Disable	RO	1'b0	
8	XOVEN	*Cross Over Capability Recommend Value.* 0: Disable 1: Enable	RO	Pin	
7	XOVER	*Cross Over Status.* 0: Non-Cross Over 1: Cross Over	RO	0h	

Bit #	Name	Description	Type	Default	Interface
6	RMII_SMII	*RMII_SMII Interface* 1: RMII or SMII Interface used 0: Non RMII_SMII Interface	RO	Pin	
5	REPEATER	*Repeater Mode Recommend Value* 1: Repeater 0: NIC/SW	RO	Pin	
4:0	PHYA	*PHY Address*	RO	01h	

4.3.17 Interrupt Status Register (Register 19h)

Bit #	Name	Description	Type	Default	Interface
15:10	Reserved		COR	00h	
9	XOVCHG	*Cross Over mode Changed* 1: Cross Over mode Changed 0: Cross Over mode Not Changed	COR	0h	Updated By PMD Block
28	SPDCHG	*Speed Changed* 1: Speed Changed 0: Speed Not Changed	COR	0h	Updated By Auto Negotiation Block
7	DUPCHG	*Duplex Changed* 1: Duplex Changed 0: Duplex not changed	COR	0h	Updated By Auto Negotiation Block
6	PGRCHG	*Page Received* 1: Page Received 0: Page not received	COR	0h	Updated By Auto Negotiation Block
5	LNKCHG	*Link Status Changed* 1:Link Status Changed 0: Link Status not Changed	COR	0h	Updated By Auto Negotiation Block
4	SYMERR	*Symbol Error* 1: Symbol Error 0: No symbol Error	COR	0h	Updated By 100M Block
3	FCAR	*False Carrier* 1: False Carrier 0: No false carrier ***Note:*** high whenever Link is Failed.	COR	0h	Updated By 100M Block
2	TJABINT	*Transmit Jabber* 1: Jabber 0: No Jabber	COR	0h	Updated By 10M Block
1	RJABINT	*Receive Jabber* 1: Jabber 0: No Jabber	COR	0h	Updated By 10M Block
0	ESDERR	*Error End of Stream* 1: ESD Error 0: No ESD Error	COR	0h	Updated By 100M Block

4.3.18 Receive Error Counter Register (Register 1Dh)

Bit #	Name	Description	Type	Default	Interface
15:0	ERB[15:0]	*Error Counter.* Includes 1.100M False Carrier 2.100M Symbol Error 3.10M Transmit Jabber 4.10M Receive Jabber 5.Error Start of Stream 6.Error End of Stream	RO	0000h	

4.3.19 Chip ID Register (Register 1Fh)

Bit(s)	Name	Description	R/W	Default	Interface
15:0	CHIPID[15:0]	Infineon-ADMtek Co Ltd CHIP ID	RO	8125	

Chapter 5 Electrical Specification

5.1 DC Characterization

5.1.1 Absolute Maximum Rating

Symbol	Parameter	Rating	Units
V_{CC33}	3.3V Power Supply	3.0 to 3.6	V
V_{CC25}	2.5V Power Supply	2.25 to 2.75	V
V_{IN}	Input Voltage	-0.3 to V_{CC33} + 0.3	V
Vout	Output Voltage	-0.25 to Vcc_{25} + 0.25	V
TSTG	Storage Temperature	-55 to 155	°C
ESD	ESD Rating	2000	V
P_C	Power Consumption	0.5	W

Table 5-1 Electrical Absolute Maximum Rating

5.1.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{CC33}	Power Supply	3.135	3.3	3.465	V
Vin	Input Voltage	0	-	V_{CC33}	V
Tj	Junction Operating Temperature	0	25	115	°C

Table 5-2 Recommended Operating Conditions

5.1.3 DC Electrical Characteristics for 2.5V Operation

(Under Vcc=3.0V~3.6V, Tj= 0 °C ~ 115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IL}	Input Low Voltage	CMOS			0.3 * Vcc	V
V_{IH}	Input High Voltage	CMOS	0.7 * Vcc			V
V_{OL}	Output Low Voltage	CMOS			0.4	V
V_{OH}	Output High Voltage	CMOS	2.0			V
R_I	Input Pull_up/down Resistance	VIL=0V or VIH = V_{CC33}		75		KΩ

Table 5-3 DC Electrical Characteristics for 2.5V Operation

5.2 AC Characterization

5.2.1 XI/OSCI (Crystal/Oscillator) Timing (In MII Mode)

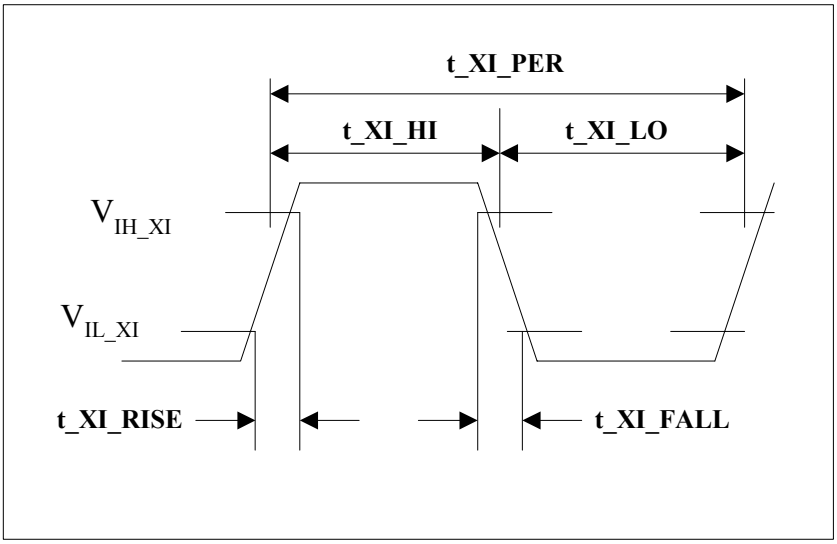


Figure 5-1 Crystal/Oscillator Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_XI_PER	XI/OSCI Clock Period (Note^{-1})	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
T_XI_HI	XI/OSCI Clock High	14	20.0		ns
T_XI_LO	XI/OSCI Clock Low	14	20.0		ns
T_XI_RISE	XI/OSCI Clock Rise Time , V_{IL} (max) to V_{IH} (min)			4	ns
T_XI_FALL	XI/OSCI Clock Fall Time , V_{IH} (min) to V_{IL} (max)			4	ns

Table 5-4 Crystal/Oscillator Timing

Note^{-1} : Clock period less then 40ns – 50ppm or greater than 40ns + 50ppm may introduce peer receive CRC due to insufficient receive FIFO depth. Check peer receive FIFO description to confirm.

5.3 RMII Timing

5.3.1 REFCLK Input Timing (XI in RMII Mode)

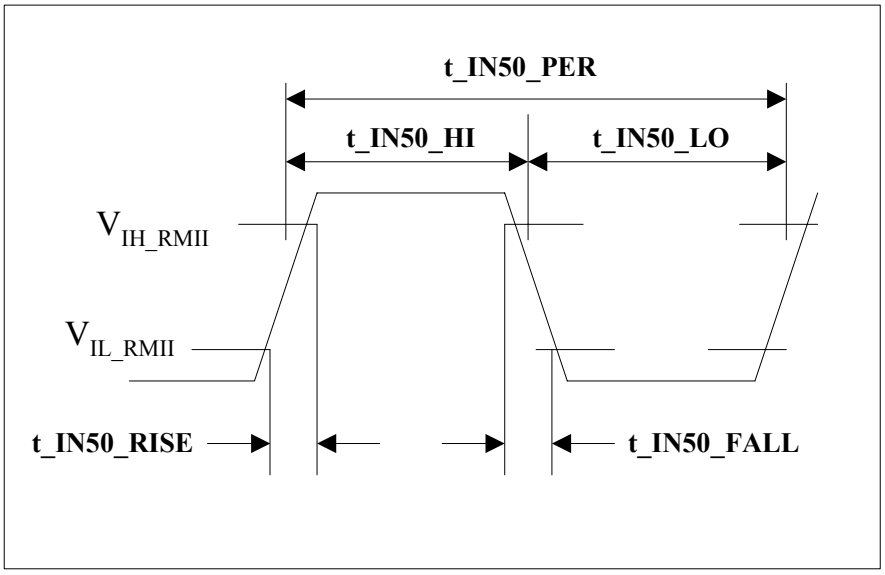


Figure 5-2 REFCLK Input Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_IN50_PER	REFCLK Clock Period	20.0 - 50ppm	20.0	20.0 + 50ppm	ns
t_IN50_HI	REFCLK Clock High	8	10.0		ns
t_IN50_LO	REFCLK Clock Low	8	10.0		ns
t_IN50_RISE	REFCLK Clock Rise Time , V_{IL} (max) to V_{IH} (min)			2	ns
t_IN50_FALL	REFCLK Clock Fall Time , V_{IH} (min) to V_{IL} (max)			2	ns

Table 5-5 REFCLK Input Timing

5.3.2 REFCLK Output Timing (CLKO50 in RMII Mode)

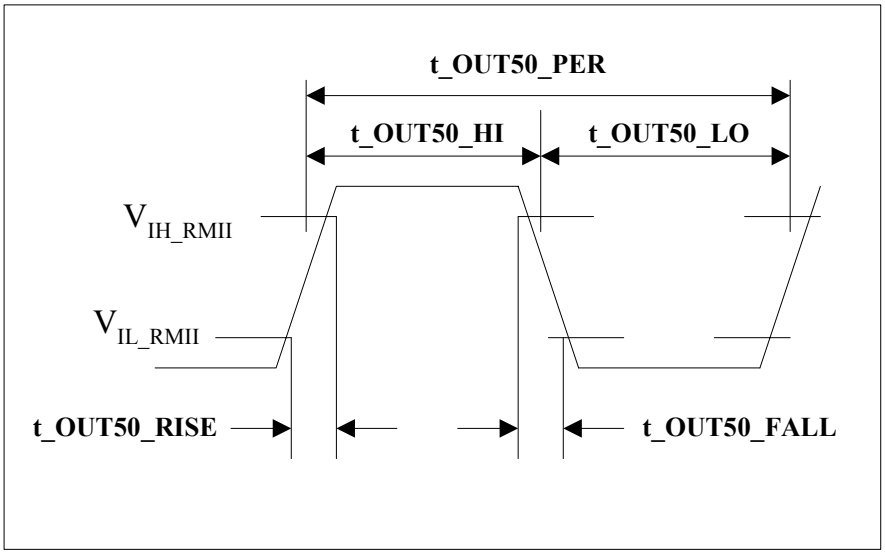


Figure 5-3 REFCLK Output Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_OUT50_PER	REFCLK Clock Period	20.0 - 50ppm	20.0	20.0 + 50ppm	ns
t_OUT50_HI	REFCLK Clock High	8	10.0	12	ns
t_OUT50_LO	REFCLK Clock Low	8	10.0	12	ns
t_OUT50_RISE	REFCLK Clock Rise Time , V_{IL} (max) to V_{IH} (min)			2	ns
t_OUT50_FALL	REFCLK Clock Fall Time , V_{IH} (min) to V_{IL} (max)			2	ns
t_OUT50_JIT	REFCLK Clock Jittering (p-p)		0.15		ns

Table 5-6 REFCLK Output Timing

5.3.3 RMII Transmit Timing

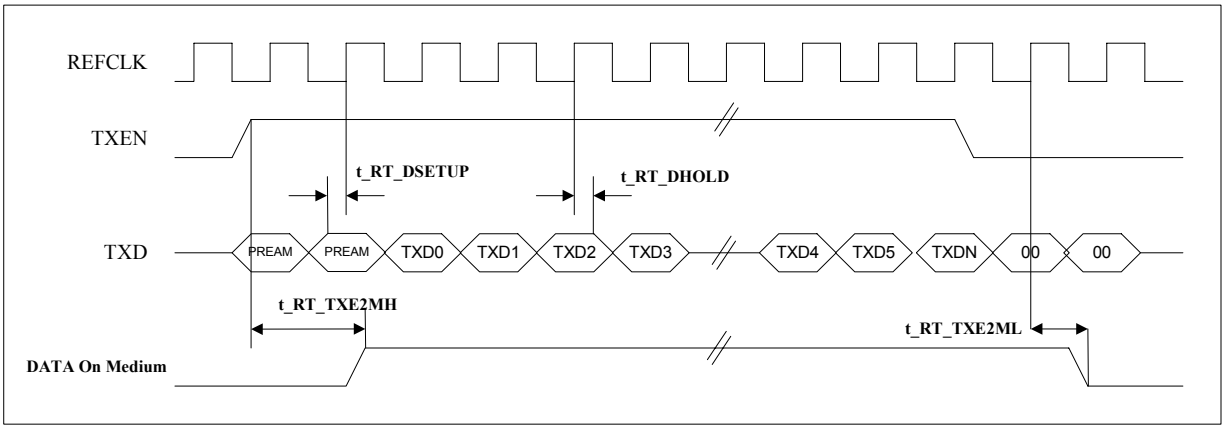


Figure 5-4 RMII Transmit Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_RT_DSETUP	TXD to REFCLK Rising Setup Time	2			**ns**
t_RT_DHOLD	TXD to REFCLK Rising Hold Time	2			**ns**
$t\_RT\_TXE2MH_{100}$	TXEN asserts to data transmit to medium			235	**ns**
$t\_RT\_TXE2MH_{10}$	TXEN asserts to data transmit to medium			1550	**ns**
$t\_RT\_TXE2ML_{100}$	TXEN de-asserts to finish transmitting			260	**ns**
$t\_RT\_TXE2ML_{10}$	TXEN de-asserts to finish transmitting			1250	**ns**

Table 5-7 RMII Transmit Timing

5.3.4 RMII Receive Timing

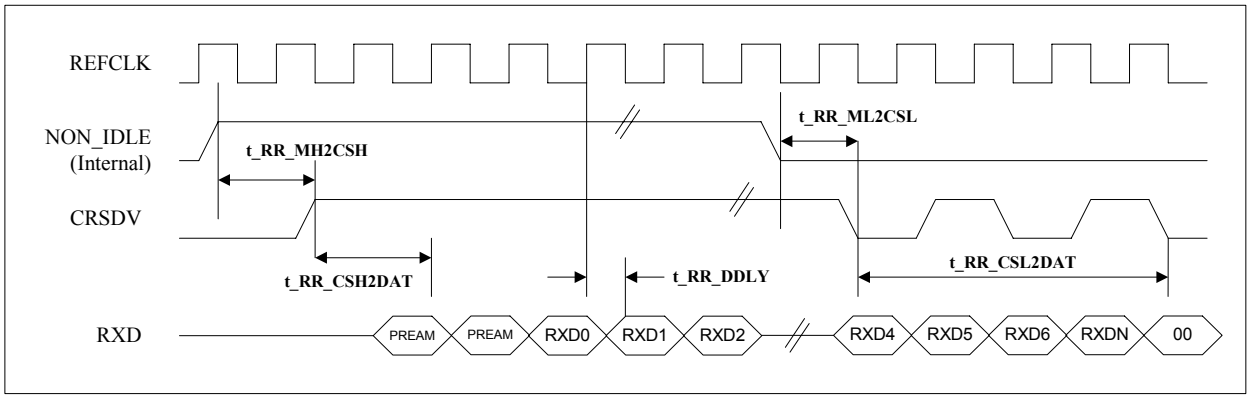


Figure 5-5 RMII Receive Timing

Symbol	Description	MIN	TYP	MAX	UNIT
$t\_RR\_MH2CSH_{100}$	Signal Detected on Medium to CRSDV High			265	ns
$t\_RR\_MH2CSH_{0}$	Signal Detected on Medium to CRSDV High			1000	ns
$t\_RR\_ML2CSL_{100}$	IDLE Detected on Medium to CRSDV low			260	ns
$t\_RR\_ML2CSL_{10}$	IDLE Detected on Medium to CRSDV low			570	ns
$t\_RR\_CSH2DAT_{100}$	CRSDV High to Receive Data on RXD			160	ns
$t\_RR\_CSH2DAT_{10}$	CRSDV High to Receive Data on RXD			1600	ns
$t\_RR\_CSL2DAT_{100}$	CRSDV Toggle to End of Data Receiving		160		ns
$t\_RR\_CSL2DAT_{10}$	CRSDV Toggle to End of Data Receiving		1600		ns
t_RR_DDLY	REFCLK Rising to RXD/CRSDV Delay Time			5	ns

Table 5-8 RMII Receive Timing

5.4 MII Timing

5.4.1 RXCLK Clock Timing

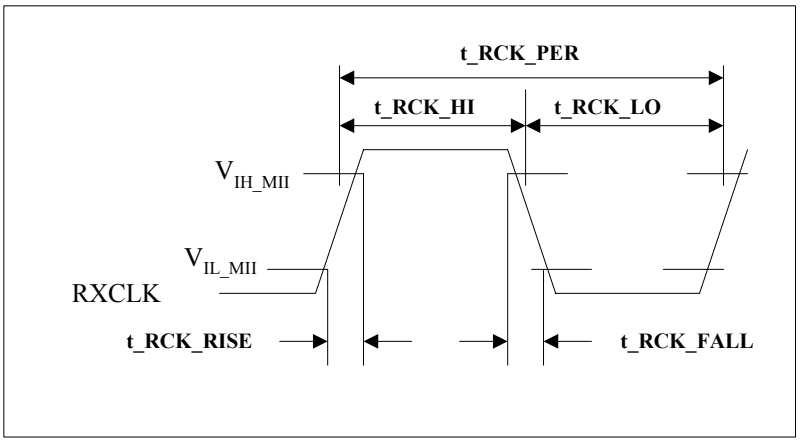


Figure 5-6 RXCLK Output Timing

Symbol	Description	MIN	TYP	MAX	UNIT
$t\_RCK\_PER_{100}$	RXCLK Clock Period (100M) (Note^{-1})	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
$t\_RCK\_PER_{10}$	RXCLK Clock Period (10M) (Note^{-1})	400 - 50ppm	400	400 + 50ppm	ns
$t\_RCK\_HI_{100}$	RXCLK Clock High (100M)	16		24	ns
$t\_RCK\_HI_{10}$	RXCLK Clock High (10M)		200		ns
$t\_RCK\_LO_{100}$	RXCLK Clock Low (100M)	16		24	ns
$t\_RCK\_LO_{10}$	RXCLK Clock Low (10M)		200		ns
t_RCK_RISE	RXCLK Clock Rise Time , V_{IL} (max) to V_{IH} (min)			2	ns
t_RCK_FALL	RXCLK Clock Fall Time , V_{IH} (min) to V_{IL} (max)			2	ns
t_RCK_JIT	REFCLK Clock Jittering (p-p)		0.15		ns

Table 5-9 RXCLK Output Timing

Note $^{-1}$: Clock period ppm value is highly depended upon peer transmitter clock source skew.

5.4.2 MII Receive Timing

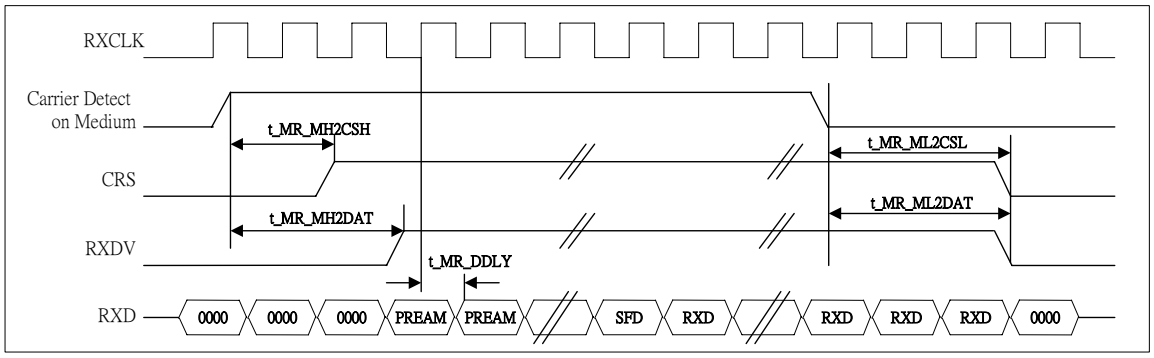


Figure 5-7 MII Receive Timing

Symbol	Description	MIN	TYP	MAX	UNIT
$t\_MR\_MH2CSH_{100}$	Signal Detected on Medium to CRS High			140	ns
$t\_MR\_MH2CSH_{10}$	Signal Detected on Medium to CRS High			1450	ns
$t\_MR\_MH2DAT_{100}$	Signal Detected on Medium to RXDV High			150	ns
$t\_MR\_MH2DAT_{10}$	Signal Detected on Medium to RXDV High			2300	ns
$t\_MR\_DDLY_{100}$	RXCLK rising to Data Valid Delay Time	10		25	ns
$t\_MR\_DDLY_{10}$	RXCLK rising to Data Valid Delay Time	10		25	ns
$T\_MR\_ML2CSL_{100}$	IDLE Detected on Medium to CRS Low			120	ns
$T\_MR\_ML2CSL_{10}$	IDLE Detected on Medium to CRS Low			235	ns
$T\_MR\_ML2DAT_{100}$	IDLE Detected on Medium to RXDV Low			150	ns
$T\_MR\_ML2DAT_{10}$	IDLE Detected on Medium to RXDV Low			1450	ns

Table 5-10 MII Receive Timing

5.4.3 TXCLK Output Timing

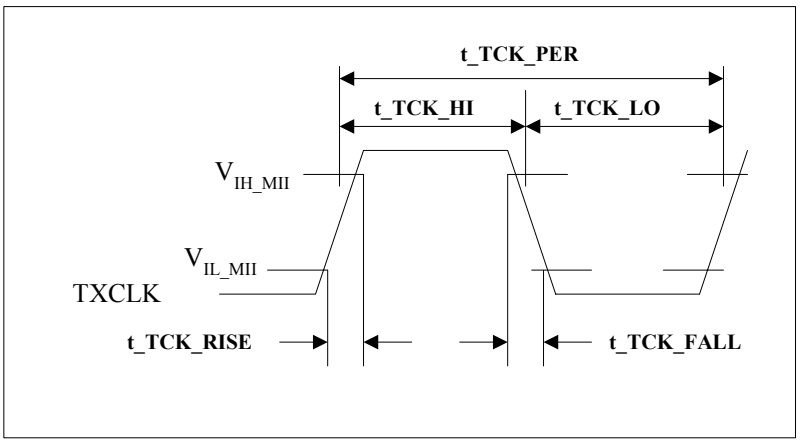


Figure 5-8 TXCLK Output Timing

Symbol	Description	MIN	TYP	MAX	UNIT
$t\_TCK\_PER_{100}$	TXCLK Clock Period (100M)	40.0 - 50ppm	40.0	40.0 + 50ppm	ns
$t\_TCK\_PER_{10}$	TXCLK Clock Period (10M)	400 - 50ppm	400	400 + 50ppm	ns
$t\_TCK\_HI_{100}$	TXCLK Clock High (100M)	16		24	ns
$t\_TCK\_HI_{10}$	TXCLK Clock High (10M)	160		240	ns
$t\_TCK\_LO_{100}$	TXCLK Clock Low (100M)	16		24	ns
$t\_TCK\_LO_{10}$	TXCLK Clock Low (10M)	160		240	ns
t_TCK_RISE	TXCLK Clock Rise Time , V_{IL} (max) to V_{IH} (min)			2	ns
t_TCK_FALL	TXCLK Clock Fall Time , V_{IH} (min) to V_{IL} (max)			2	ns
t_TCK_JIT	TXCLK Clock Jittering (p-p)		0.15		ns

Table 5-11 TXCLK Input Timing

5.4.4 MII Transmit Timing

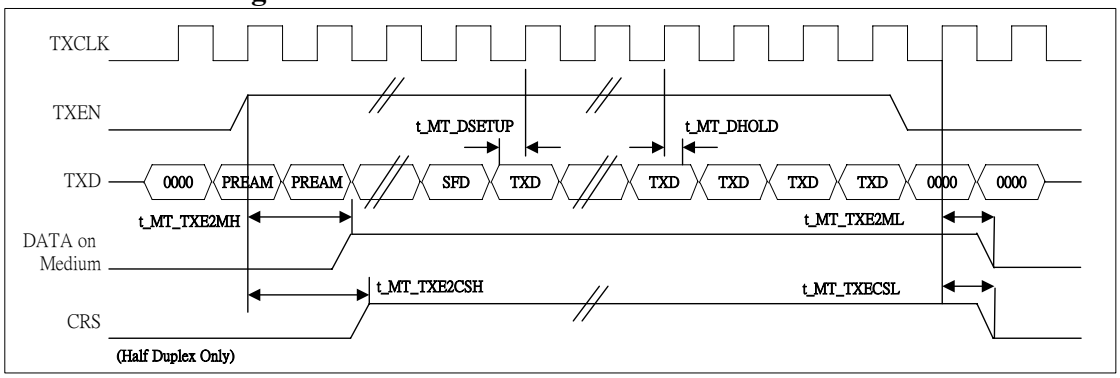


Figure 5-9 MII Transmit Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_MT_DSETUP	TXD to TXCLK Rising Setup Time	10		25	**ns**
t_MT_DHOLD	TXD to TXCLK Rising Hold Time	10		25	**ns**
$t\_MT\_TXE2MH_{100}$	TXEN asserts to data transmit to medium (100M)			75	**ns**
$t\_MT\_TXE2MH_{10}$	TXEN asserts to data transmit to medium (10M)			350	**ns**
$t\_MT\_TXE2CSH_{100}$	TXEN asserts to CRS Assert (100M Half)			15	**ns**
$t\_MT\_TXE2CSH_{10}$	TXEN asserts to CRS Assert (10M Half)			200	**ns**
$t\_MT\_TXE2ML_{100}$	TXEN de-asserts to finish transmitting (100M)			95	**ns**
$t\_MT\_TXE2ML_{10}$	TXEN de-asserts to finish transmitting (10M)			660	**ns**
$t\_MT\_TXECSL_{100}$	TXEN de-asserts to CRS de-asserts (100M)			15	**ns**
$t\_MT\_TXECSL_{10}$	TXEN de-asserts to CRS de-asserts (10M)			190	**ns**

Table 5-12 MII Transmit Timing

5.5 GPSI Timing

5.5.1 GPSI Receive Timing

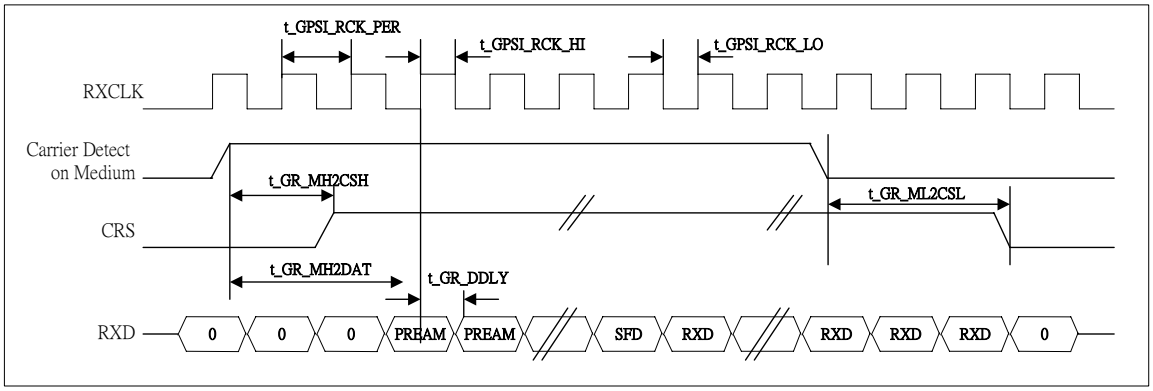


Figure 5-10 GPSI Receive Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_GPSI_RCK_PER	10M Receive Clock Period	100 - 50ppm	100	100 + 50ppm	ns
t_GPSI_RCK_HI	10M Receive Clock High	40			ns
t_GPSI_RCK_LO	10M Receive Clock Low	40			ns
t_GR_MH2CSH	Signal Detected on Medium to CRS High			1500	ns
t_GR_MH2DAT	Signal Detected on Medium to Data Valid			1600	ns
t_GR_DDLY	RXCLK rising to Data Valid Delay Time	40		60	ns
T_GR_ML2CSL	IDLE Detected on Medium to CRS Low			230	ns

Table 5-13 GPSI Receive Timing

5.5.2 GPSI Transmit Timing

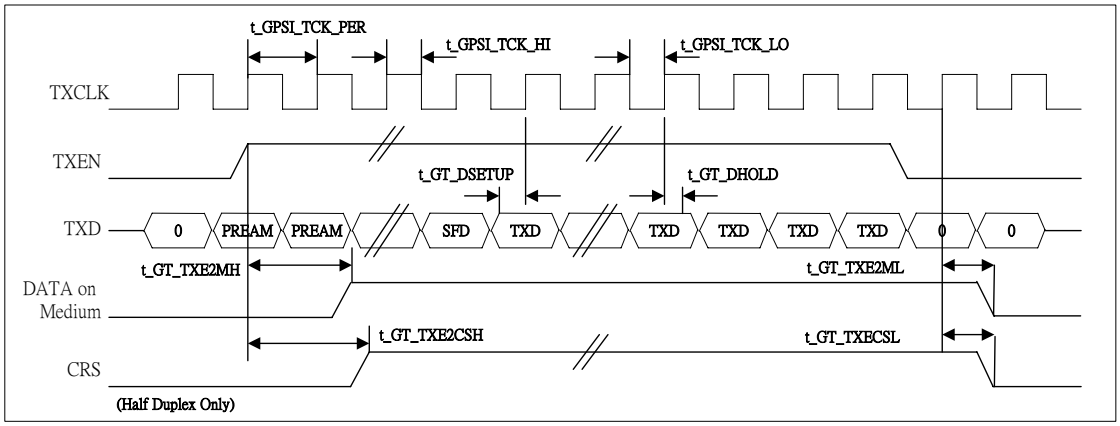


Figure 5-11 GPSI Transmit Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_GPSI_TCK_PER	10M Transmit Clock Period	100 - 50ppm	100	100 + 50ppm	ns
t_GPSI_TCK_HI	10M Transmit Clock High	40			ns
t_GPSI_TCK_LO	10M Transmit Clock Low	40			ns
t_GT_DSETUP	TXD to TXCLK Rising Setup Time	40			**Ns**
t_GT_DHOLD	TXD to TXCLK Rising Hold Time	40			**ns**
t_GT_TXE2MH	TXEN asserts to data transmit to medium			150	**ns**
t_GT_TXE2CSH	TXEN asserts to CRS Assert (Half)			10	**ns**
t_GT_TXE2ML	TXEN de-asserts to finish transmitting			900	**ns**
t_GT_TXECSL	TXEN de-asserts to CRS de-asserts			10	**ns**

Table 5-14 GPSI Transmit Timing

5.6 Serial Management Interface (MDC/MDIO) Timing

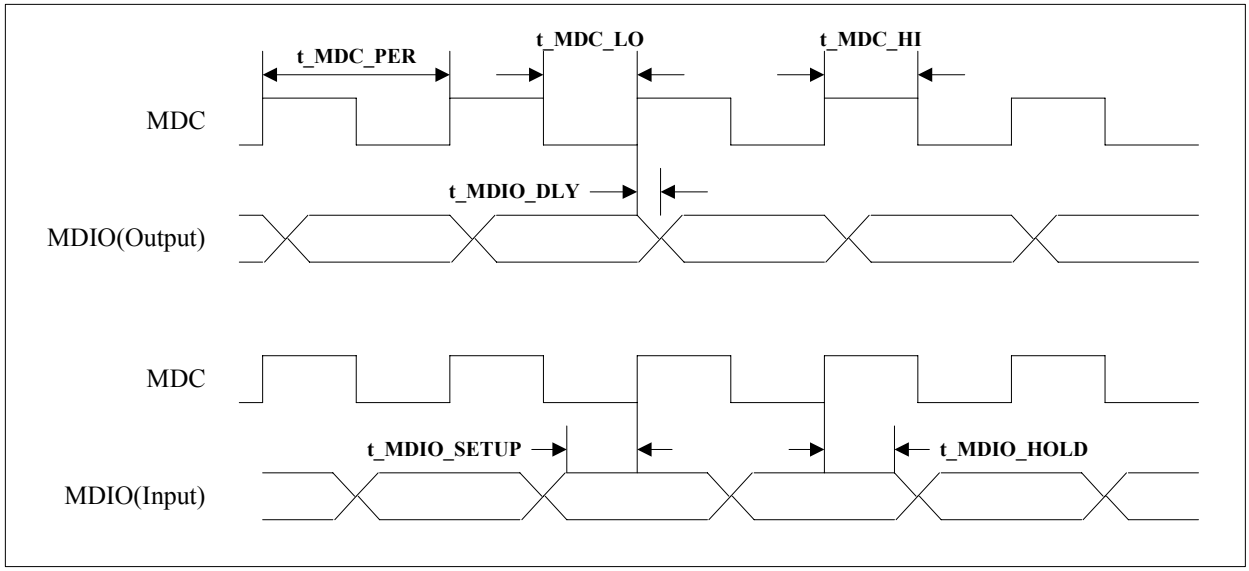


Figure 5-12 Serial Management Interface (MDC/MDIO) Timing

Symbol	Description	MIN	TYP	MAX	UNIT
t_MDC_PER	MDC Period	100			**ns**
t_MDC_HI	MDC High	40			**ns**
t_MDC_LO	MDC High	40			**ns**
t_MDIO_DLY	MDC to MDIO Delay Time			20	**ns**
t_MDIO_SETUP	MDIO Input to MDC Setup Time	10			**ns**
t_MDIO_HOLD	MDIO Input to MDC Hold Time	10			**ns**

Table 5-15 Serial Management Interface (MDC/MDIO) Timing

5.6 Power On Configuration Timing

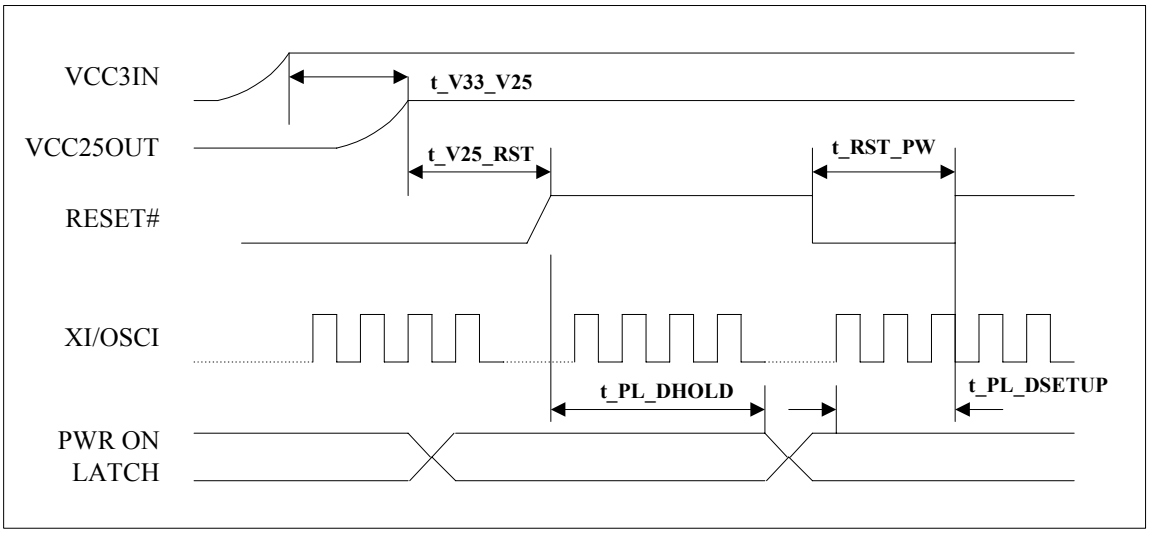


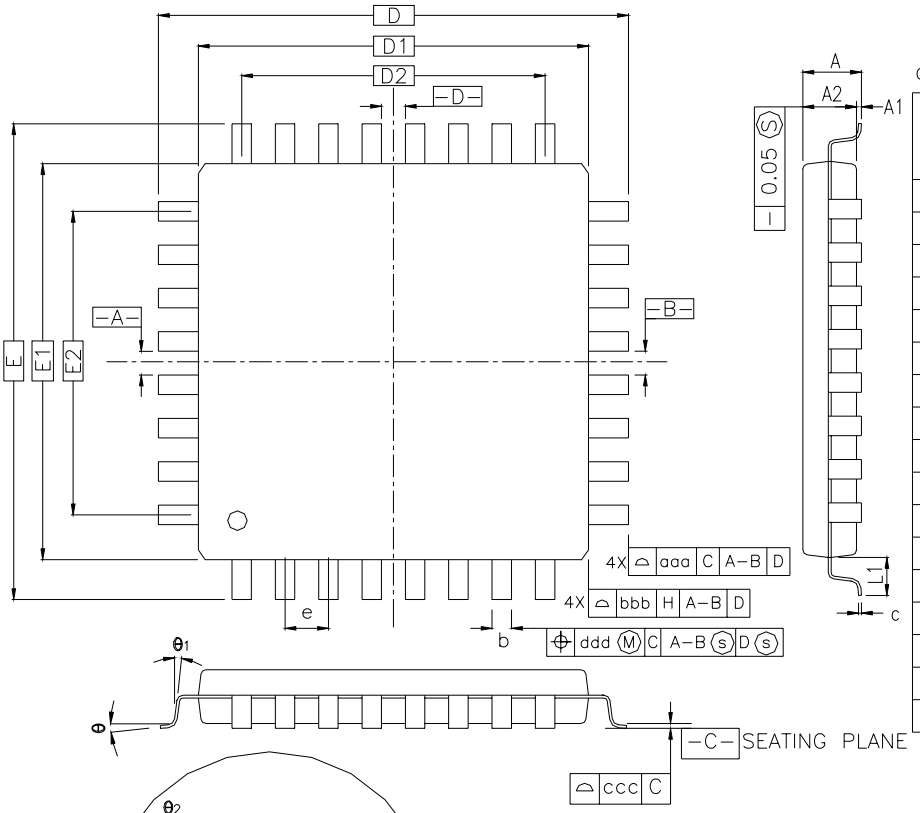
Figure 5-13 Power On Configuration Timing

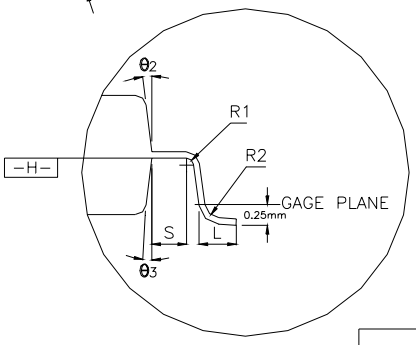
Symbol	Description	MIN	TYP	MAX	UNIT
t_V33_V25	3.3V Power Good to 2.5V Power Good	TBD			**ms**
t_V25_RST	Hardware Reset With Device Powered up	200			**ms**
t_RST_PW	Hardware Reset With Clock Running	800			**ns**
t_PL_DSETUP	Reset High to Configuration Setup Time	200			**ns**
t_PL_DHOLD	Reset High to Configuration Hold Time	0			**ns**

Table 5-16 Power On Configuration Timing

Chapter 6 Packaging

6.1 ADM7001 Low Profile Quad Flat Package (LQFP) 48 Pin





COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

SYMBOL	32L						44L						48L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.17	0.20	0.27	0.007	0.008	0.011	0.17	0.20	0.27	0.007	0.008	0.011
e	0.80 BSC.			0.031 BSC.			0.50 BSC.			0.020 BSC.			0.50 BSC.			0.020 BSC.		
D2	5.60			0.220			5.00			0.197			5.50			0.217		
E2	5.60			0.220			5.00			0.197			5.50			0.217		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.003			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.08			0.003			0.08			0.003		