24 GHz to 29.5 GHz, 5G, Microwave Upconverter and Downconverter

FEATURES

- Integration of an upconverter (a transmitter), a downconverter (a receiver), and a LO chain with options of a 2× or 4× multiplier in one chip
- RF frequency range: 24 GHz to 29.5 GHz
- LO input frequency range:
  8 GHz to 15 GHz for x2 mode, 5 GHz to 7.5 GHz for x4 mode
- Complex IF operation (IF mode) with optional on-chip hybrid
  - Direct conversion of differential baseband I/Q (baseband mode)
- Programmable baseband I/Q common-mode voltage
- Common-mode input pin to track desired common mode, 0 V to 1.5 V voltage range
- Optional on-chip RF switch port between the transmitter and the receiver
- Matched, 50 Ω impedance, single-ended RF input and output, and RF switch port
- Matched, 50 Ω impedance single-ended LO input
- Low phase variation vs. gain control
- Upconversion mode
  - Sideband rejection and carrier feedthrough optimization
  - Envelope detector for LO feedthrough calibration
- Downconversion mode
  - Image rejection and I/Q imbalance optimization
  - Baseband I/Q dc offset correction
  - Receiver mixer power detector for receiver gain setting
- LO chain features
  - Variable gain to accommodate the various LO drive strength values
  - 360° phase control shifter for LO synchronization
  - Programmable LO harmonic reject filter
  - I/Q phase correction
- Fast TDD switching time via external pins
- Calibration probes for array calibration
- Programmable via a 3-wire or 4-wire SPI, compatible with ADMV4928 interface
- 131-ball, 6 mm × 6.5 mm, BGA package

APPLICATIONS

- Millimeter-wave 5G applications
- Point to point microwave radios
- Radar and electronic warfare systems
- Instrumentation and automatic test equipment (ATE)

GENERAL DESCRIPTION

The ADMV1128 is a silicon on isolator (SOI), microwave, upconverter and downconverter optimized for 5G radio designs operating in the 24 GHz to 29.5 GHz frequency range.

Both upconverters and downconverters offer two modes of frequency translation. One mode is conversion from and/or to single-ended or complex intermediate frequency (IF) signals, which then pass through an on-chip 90° IF hybrid, known as IF mode.

The other mode is a direct conversion from and/or to differential baseband inphase/quadrature (I/Q) inputs and outputs, known as baseband mode. The I/Q baseband output common-mode voltage is programmable between 0 V and 1.5 V. The SPI provides fine adjustment of the quadrature phase to optimize I/Q demodulation performance.

When the device is used as an image rejecting downconverter, the unwanted image term is typically rejected to 24 dBc, before calibration. The ADMV1128 offers a square law power detector to allow monitoring of the power levels at the mixer inputs of the downconverter.

The RF receive input, RF transmit output, and local oscillator (LO) interface are all single-ended and matched to 50 Ω. The on-chip RF switch provides the option to combine the transmit and receive RF ports together for time division duplex (TDD) applications.

The serial port interface (SPI) provides adjustment of the quadrature phase to allow optimum sideband rejection. In addition, the SPI allows powering down the output envelope detector to reduce power consumption when carrier feedthrough optimization is not necessary.

The ADMV1128 upconverter and downconverter is housed in a compact, thermally enhanced, 6 mm × 6.5 mm, ball grid array (BGA) package. This BGA package enables the ability to heat sink the ADMV1128 from the top of the package for the most efficient thermal heat sinking. The ADMV1128 operates over the −40°C to +95°C T_C range.

Throughout the figures within this data sheet, Rx means receiver and Tx means transmitter.

For more information about the ADMV1128, contact Analog Devices, Inc., sales office at: mmWave5G@analog.com.

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