81 GHz to 86 GHz, 1 W E-Band Power Amplifier with Power Detector

Data Sheet

ADMV7810

FEATURES

Gain: 20 dB typical
Output power for 1 dB compression: 28 dBm typical
Saturated output power: 29 dBm typical
Output third-order intercept: 33 dBm typical
Input return loss: 12 dB typical
Output return loss: 20 dB typical
DC supply: 4 V at 800 mA
No external matching required
Die size: 2.999 mm × 3.799 mm × 0.05 mm

APPLICATIONS

E-band communication systems
High capacity wireless backhaul radio systems
Test and measurement

GENERAL DESCRIPTION

The ADMV7810 is an integrated E-band gallium arsenide (GaAs), pseudomorphic, high electron mobility transfer (pHEMT), monolithic microwave integrated circuit (MMIC), medium power amplifier with a temperature compensated on-chip power detector that operates from 81 GHz to 86 GHz. The ADMV7810 provides 20 dB of gain, 28 dBm of output power at 1 dB compression, and 29 dBm of saturated output power at 18% power added efficiency from a 4 V power supply. The ADMV7810 exhibits excellent linearity and is optimized for E-band communications and high capacity wireless backhaul radio systems. The amplifier configuration and high gain make the device an excellent candidate for last stage signal amplification before the antenna. All data is taken with the chip in a 50 Ω test fixture connected via a 3 mil wide × 0.5 mil thick × 7 mil long ribbon on each port. The ADMV7810 is available in a 40-pad bare die (CHIP) and operates over the −55°C to +85°C temperature range.

FUNCTIONAL BLOCK DIAGRAM

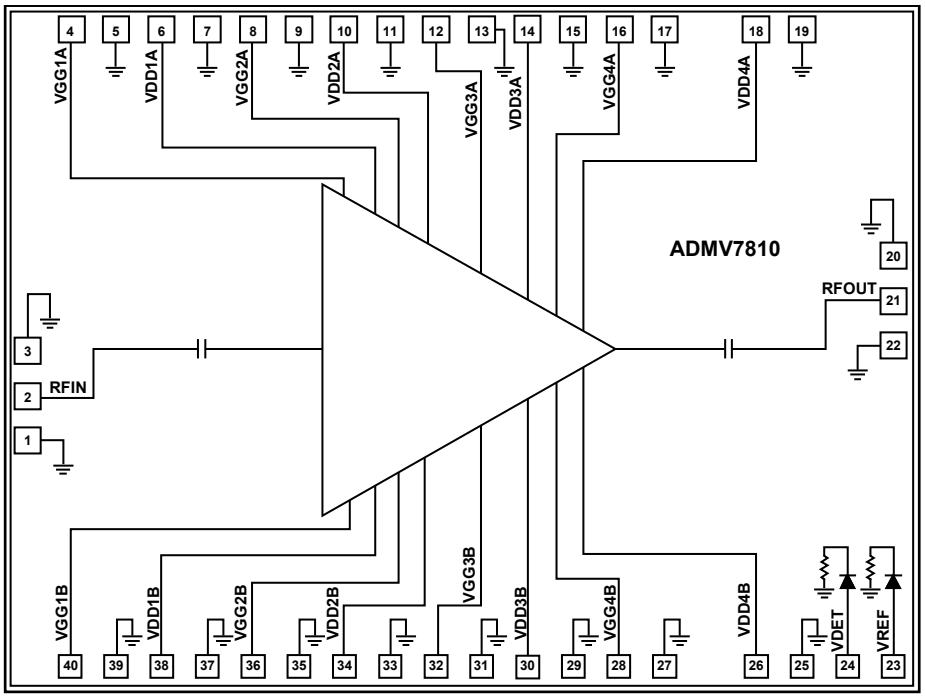

Figure 1.

Rev. 0 **Document Feedback**

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Tel: 781.329.4700 **Technical Support**

www.analog.com

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REVISION HISTORY

3/2018—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, VDDxA and VDDxB = 4 V, I_{DD} = 800 mA, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit
OPERATING CONDITIONS					
Frequency Range		81		86	GHz
PERFORMANCE					
Gain		18	20		dB
Gain Variation over Temperature			0.02		dB/°C
Output Power for 1 dB Compression	OP1dB	26	28		dBm
Saturated Output Power	P_{SAT}		29		dBm
Output Third-Order Intercept at Maximum Gain[1]	OIP3		33		dBm
Power Added Efficiency	PAE		18		%
Input Return Loss			12		dB
Output Return Loss			20		dB
POWER SUPPLY					
Total Drain Current[2]	I_{DD}		800		mA

[1] Data taken at output power (P_{OUT}) = 14 dBm per tone, 1 MHz spacing.
[2] Adjust the VGGxA and VGGxB pads from −2 V to 0 V to achieve the total drain current (I_{DD}) = 800 mA.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Drain Bias Voltage (VDD1A to VDD4A, VDD1B to VDD4B)	4.5 V
Gate Bias Voltage (VGG1A to VGG4A, VGG1B to VGG4B)	−3 V to 0 V
Maximum Junction Temperature (to Maintain 1 Million Hours Mean Time to Failure (MTTF))	175°C
Operating Temperature Range	−55°C to +85°C
Storage Temperature Range	−65°C to +150°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	250 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case (or die to package) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
C-40-3	24.2	°C/W

[1] Based on the ATROX 800HT1V ® as the die attach epoxy.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

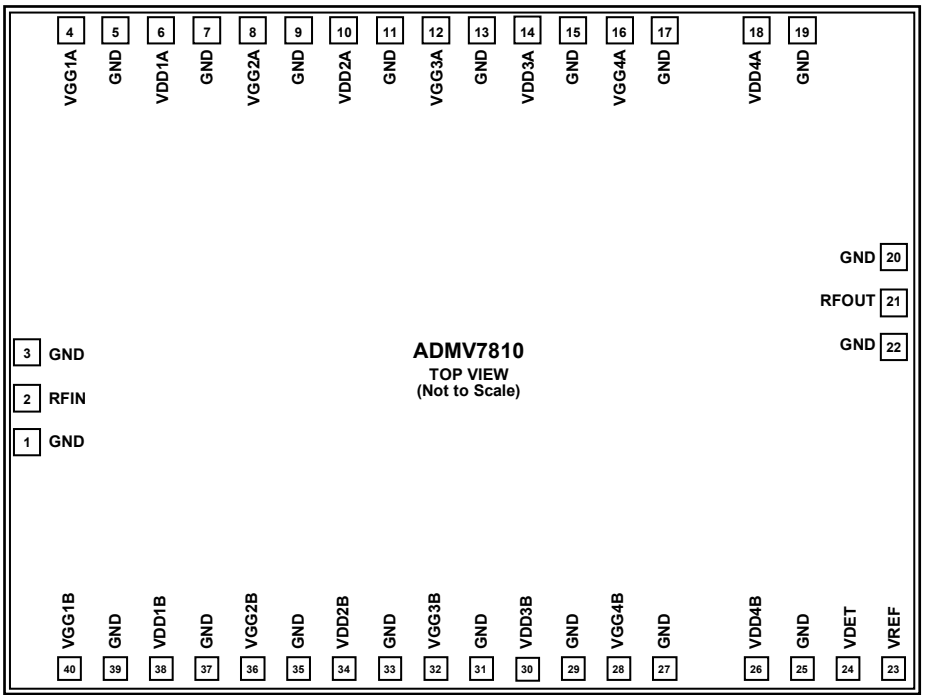

Figure 2. Pad Configuration

Table 4. Pad Function Descriptions

Pad No.	Mnemonic	Description
1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 20, 22, 25, 27, 29, 31, 33, 35, 37, 39	GND	Ground Connection (See Figure 3).
2	RFIN	RF Input. AC-couple RFIN and match it to 50 Ω (See Figure 4).
4, 8, 12, 16	VGG1A to VGG4A	First Stage Gate Bias Voltage for the Power Amplifier (See Figure 8). For the required external components, see Figure 46.
6, 10, 14, 18	VDD1A to VDD4A	First Stage Drain Bias Voltage for the Power Amplifier (See Figure 5).
21	RFOUT	RF Output. AC-couple RFOUT and match it to 50 Ω (see Figure 6).
23	VREF	Reference Voltage for the Power Detector (See Figure 7). VREF is the dc bias of the diode biased through an external resistor used for temperature compensation of VDET. Refer to the typical application circuit (see Figure 46) for the required external components.
24	VDET	Detector Voltage for the Power Detector (See Figure 7). VDET is the dc voltage representing the RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit (see Figure 46) for the required external components.
26, 30, 34, 38	VDD4B to VDD1B	Second Stage Drain Bias Voltage for the Power Amplifier (See Figure 5).
28, 32, 36, 40	VGG4B to VGG1B	Second Stage Gate Bias Voltage for the Power Amplifier (See Figure 8). For the required external components, see Figure 46.
Die Bottom	GND	Ground. The die bottom must be connected to the RF/dc ground (see Figure 3).

INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

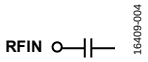

Figure 4. RFIN Interface Schematic

Figure 5. VDD1A to VDD4A and VDD1B to VDD4B Interface Schematic

Figure 6. RFOUT Interface Schematic

Figure 7. VREF, VDET Interface Schematic

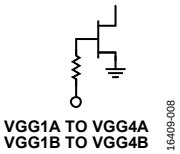

Figure 8. VGG1A to VGG4A and VGG1B to VGG4B Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

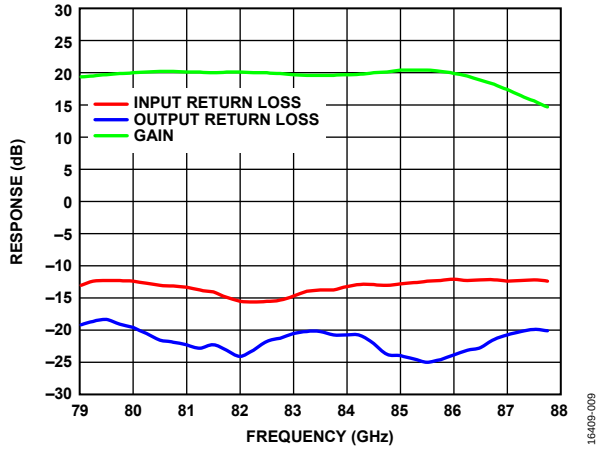

Figure 9. Broadband Gain and Return Loss Response vs. Frequency, I_{DD} = 800 mA

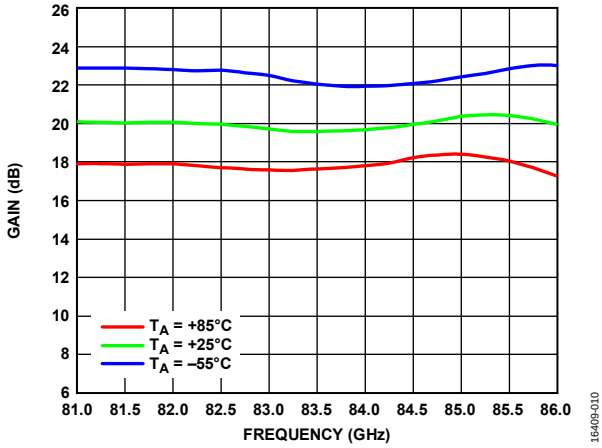

Figure 10. Gain vs. Frequency over Various Temperatures, I_{DD} = 800 mA

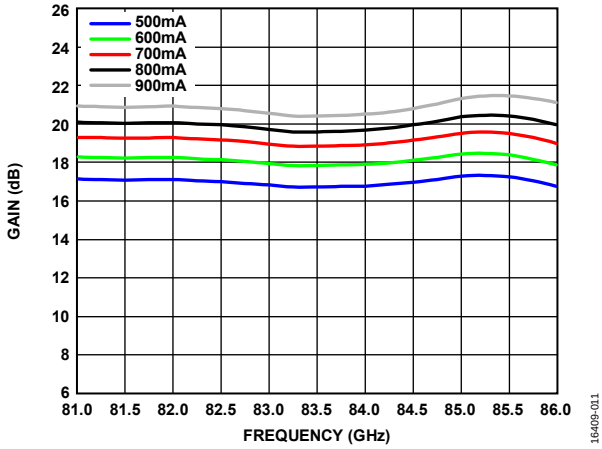

Figure 11. Gain vs. Frequency over I_{DD}

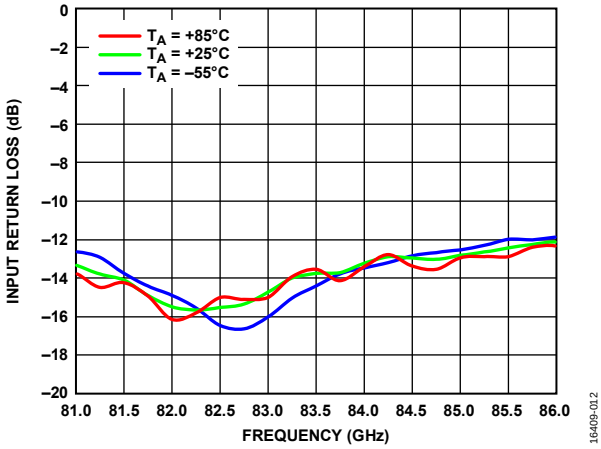

Figure 12. Input Return Loss vs. Frequency over Various Temperatures, I_{DD} = 800 mA

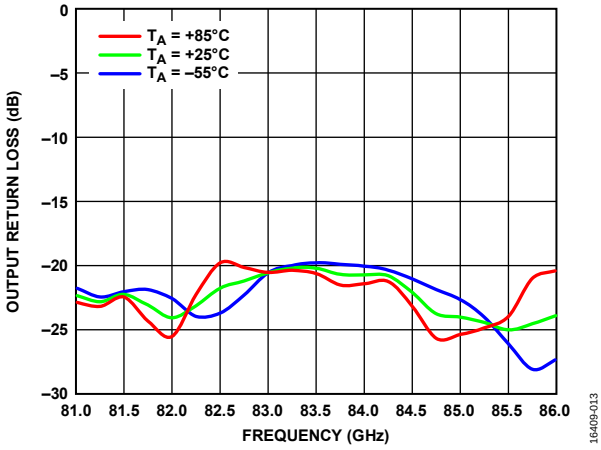

Figure 13. Output Return Loss vs. Frequency over Various Temperatures, I_{DD} = 800 mA

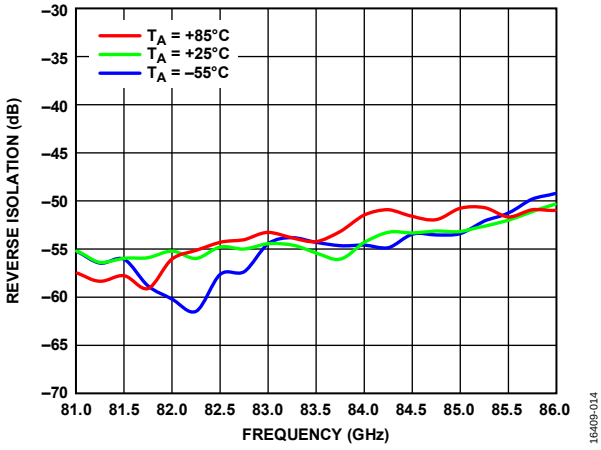

Figure 14. Reverse Isolation vs. Frequency over Various Temperatures, I_{DD} = 800 mA

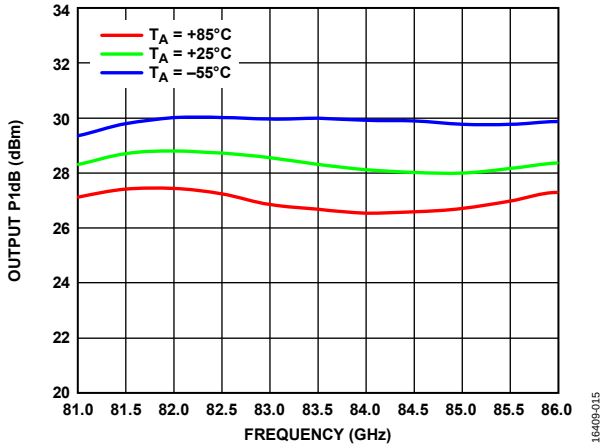

Figure 15. Output P1dB vs. Frequency over Various Temperatures, I_{DD} = 800 mA

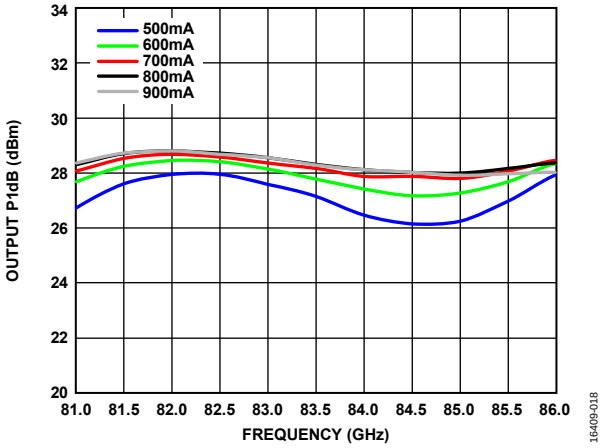

Figure 18. Output P1dB vs. Frequency over I_{DD}

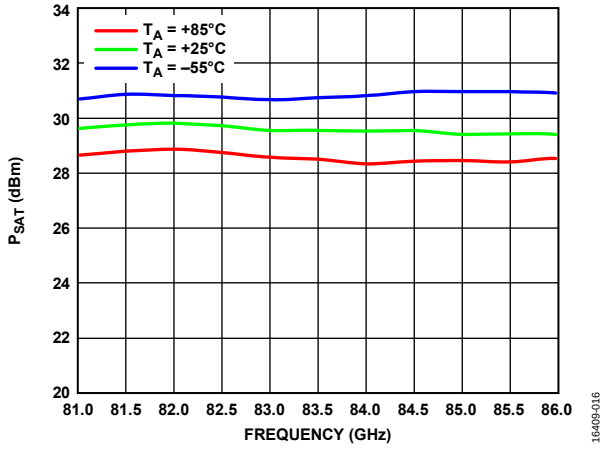

Figure 16. P_{SAT} vs. Frequency over Various Temperatures, I_{DD} = 800 mA

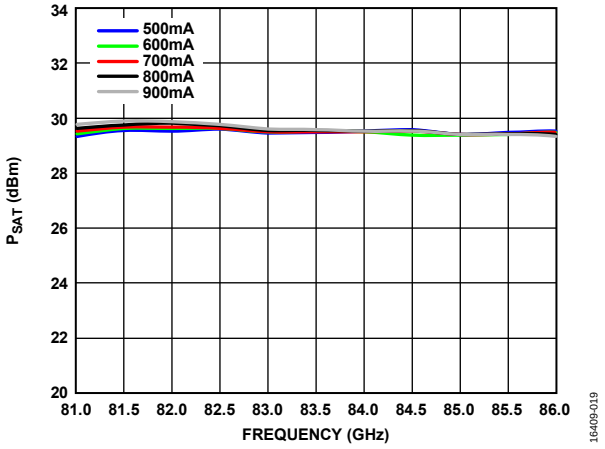

Figure 19. P_{SAT} vs. Frequency over I_{DD}

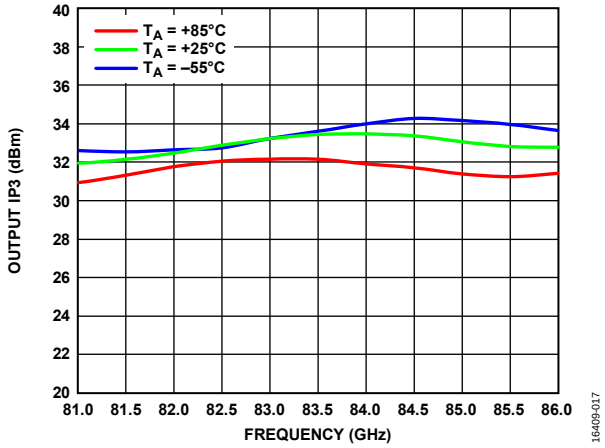

Figure 17. Output IP3 vs. Frequency over Various Temperatures, I_{DD} = 800 mA, P_{OUT}/Tone = 14 dBm

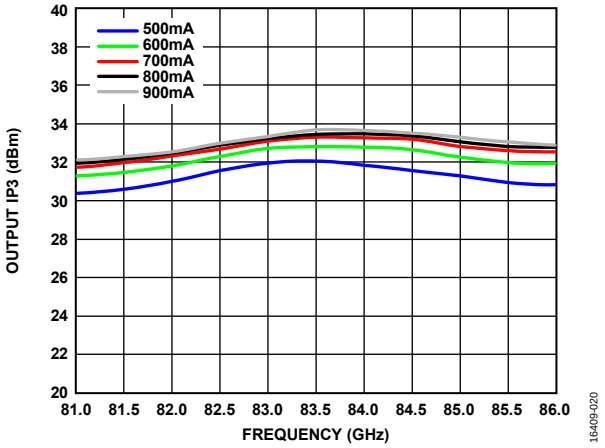

Figure 20. Output IP3 vs. Frequency over I_{DD}, P_{OUT}/Tone = 14 dBm

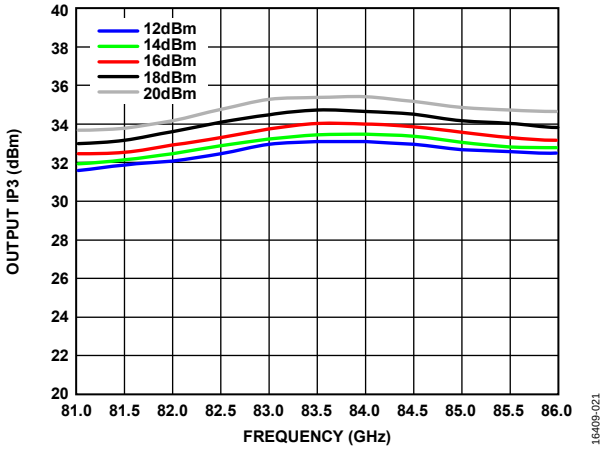

Figure 21. Output IP3 vs. Frequency over P_{OUT} per Tone , I_{DD} = 800 mA

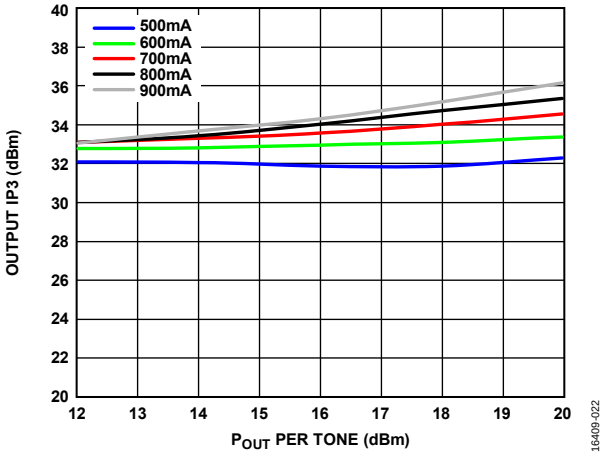

Figure 22. Output IP3 vs. P_{OUT} per Tone over I_{DD}, RF = 83.5 GHz

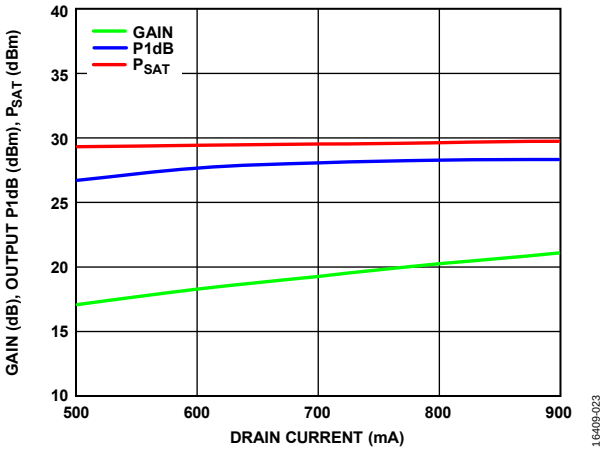

Figure 23. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}), RF = 81 GHz

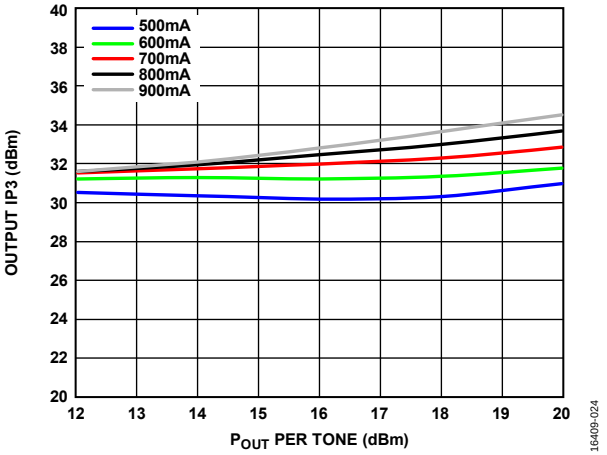

Figure 24. Output IP3 vs. P_{OUT} per Tone over I_{DD}, RF = 81 GHz

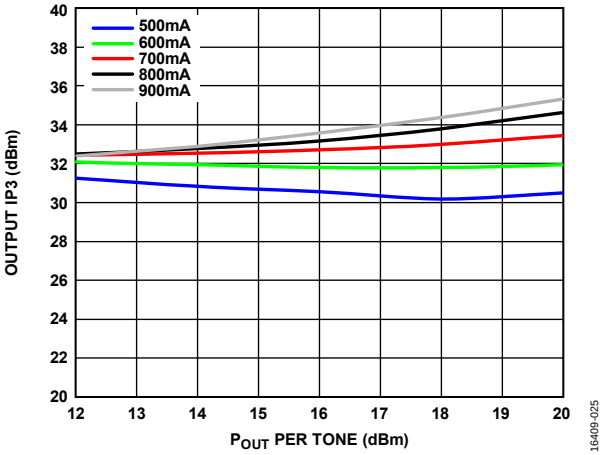

Figure 25. Output IP3 vs. P_{OUT} per Tone over I_{DD}, RF = 86 GHz

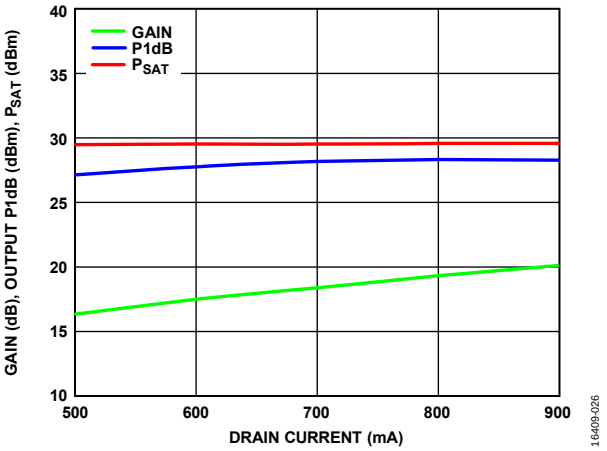

Figure 26. Gain, Output P1dB, and P_{SAT} vs. Drain Current (I_{DD}), RF = 83.5 GHz

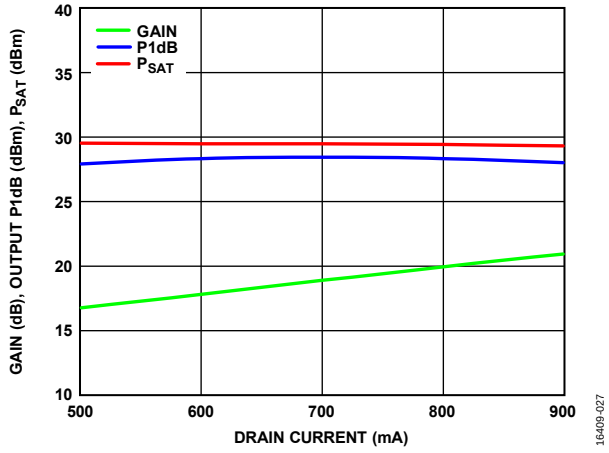

Figure 27. Gain, Output P1dB, and P_{SAT} vs. I_{DD}, RF = 86 GHz

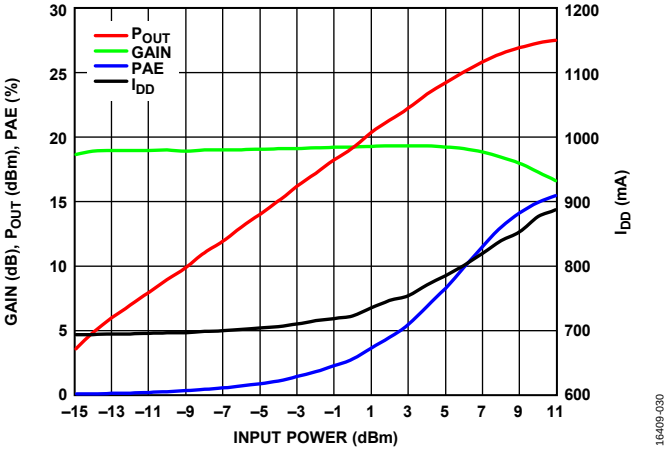

Figure 30. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 86 GHz, I_{DD} = 700 mA

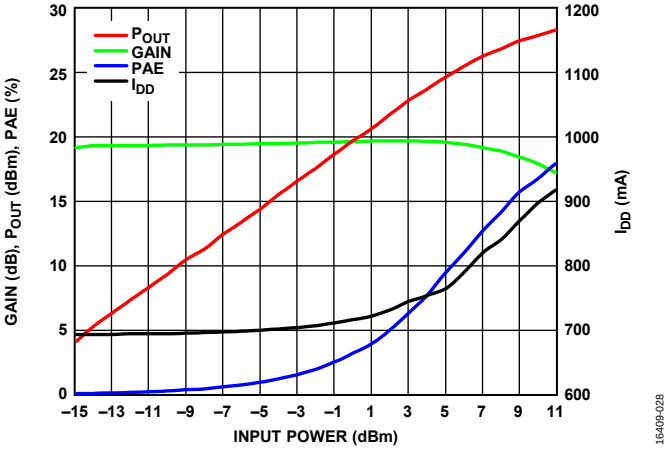

Figure 28. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 81 GHz, I_{DD} = 700 mA

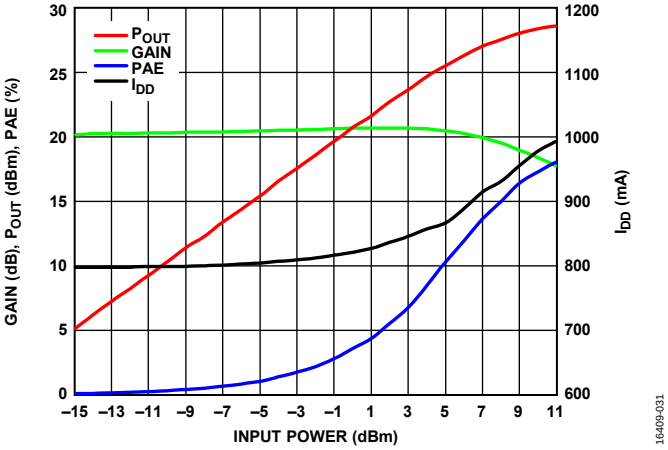

Figure 31. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 81 GHz, I_{DD} = 800 mA

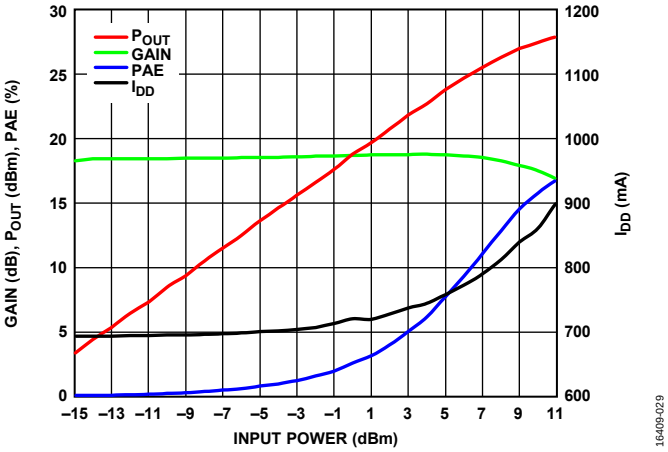

Figure 29. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 83.5 GHz, I_{DD} = 700 mA

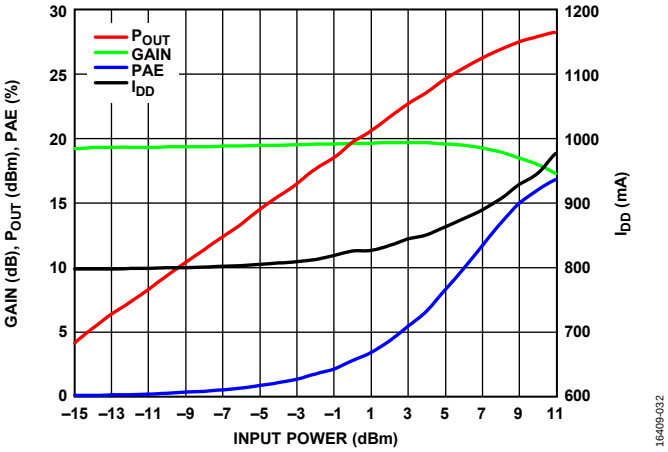

Figure 32. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 83.5 GHz, I_{DD} = 800 mA

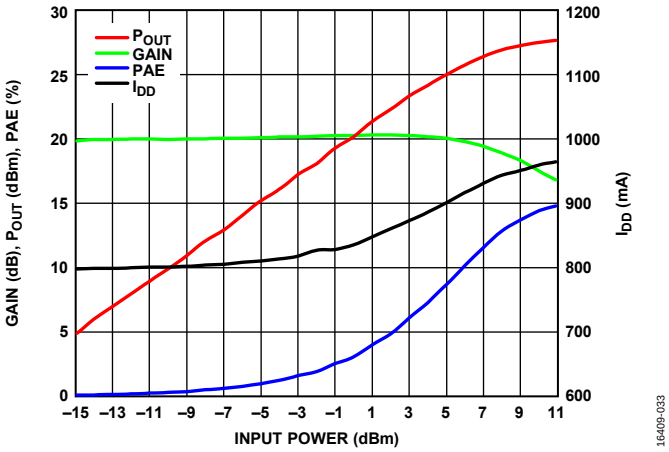

Figure 33. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 86 GHz, I_{DD} = 800 mA

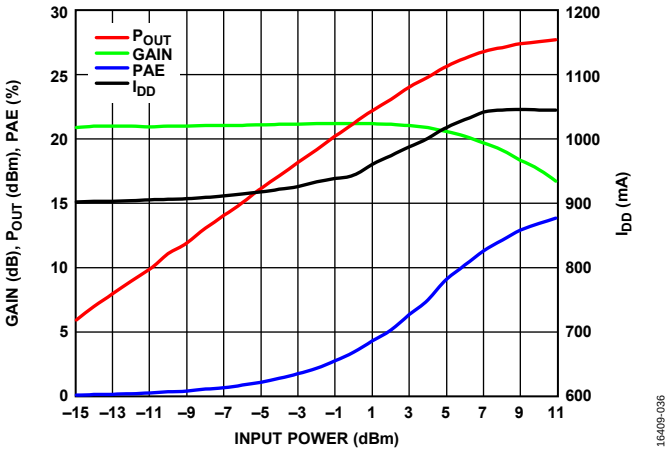

Figure 36. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 86 GHz, I_{DD} = 900 mA

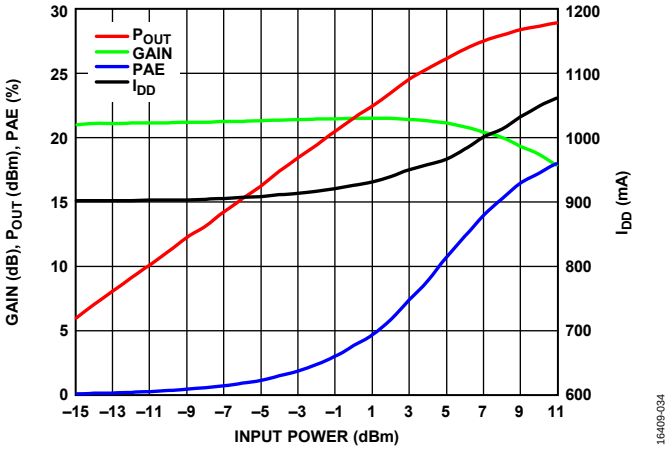

Figure 34. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 81 GHz, I_{DD} = 900 mA

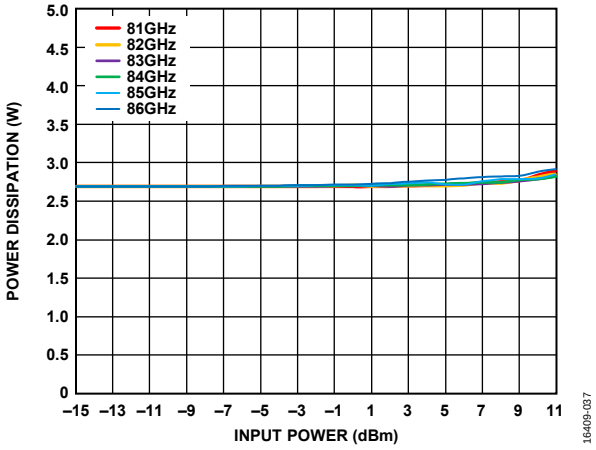

Figure 37. Power Dissipation vs. Input Power over Various Frequencies, I_{DD} = 700 mA, T_A = 85°C

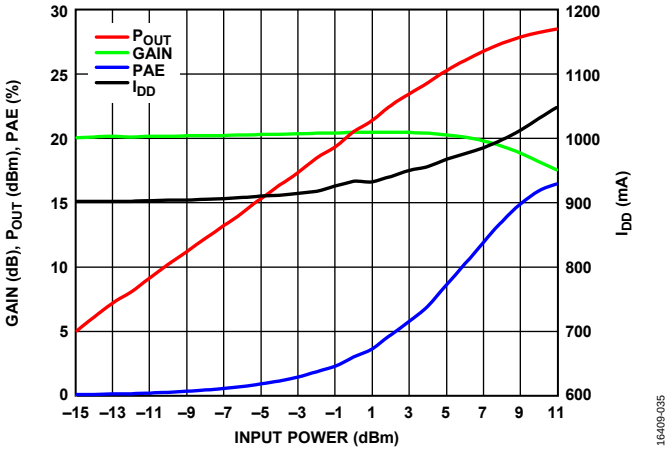

Figure 35. Gain, P_{OUT}, PAE, and I_{DD} vs. Input Power, RF = 83.5 GHz, I_{DD} = 900 mA

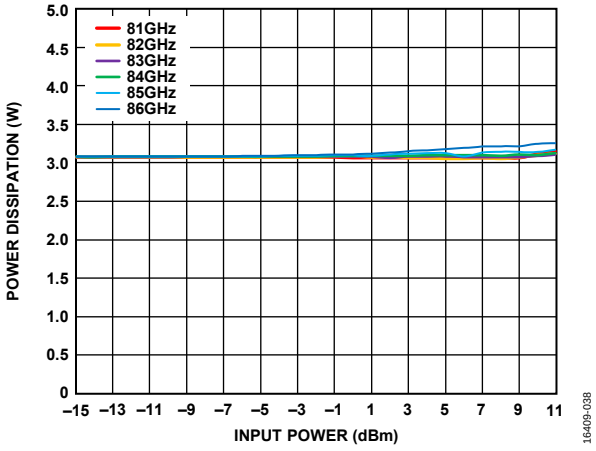

Figure 38. Power Dissipation vs. Input Power over Various Frequencies, I_{DD} = 800 mA, T_A = 85°C

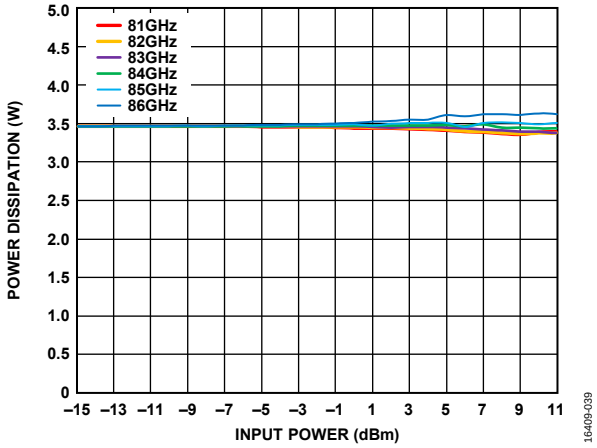

Figure 39. Power Dissipation vs. Input Power over Various Frequencies, I_{DD} = 900 mA, T_A = 85°C

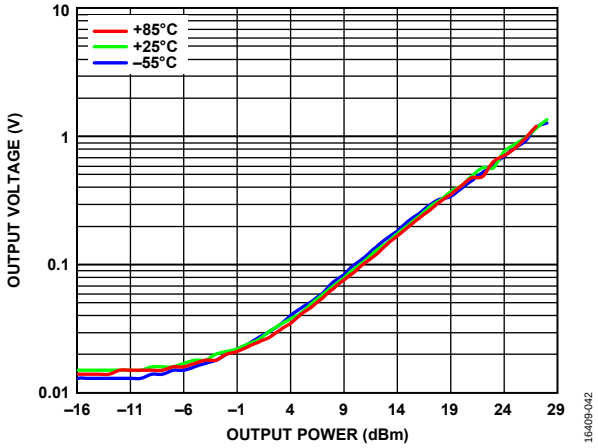

Figure 42. Detector Output Voltage (V_{OUT}) vs. Output Power over Various Temperatures, I_{DD} = 800 mA, RF = 81 GHz

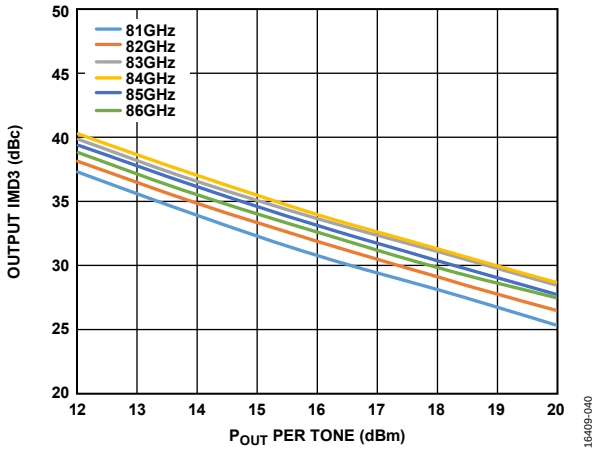

Figure 40. Lower Output Third-Order Intermodulation Distortion (IMD3) vs. P_{OUT}/Tone over Various Frequencies, I_{DD} = 800 mA

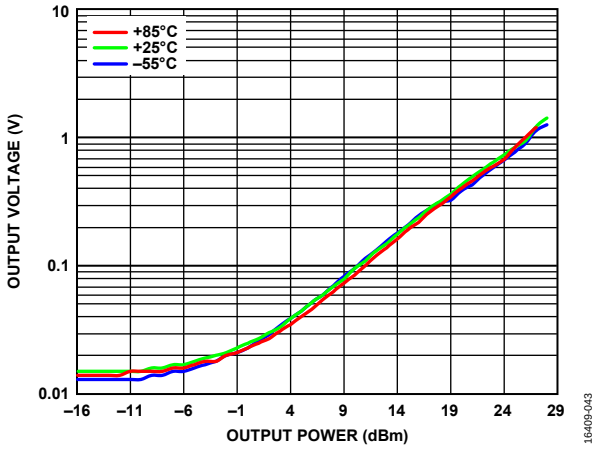

Figure 43. Detector Output Voltage (V_{OUT}) vs. Output Power over Various Temperatures, I_{DD} = 800 mA, RF = 83.5 GHz

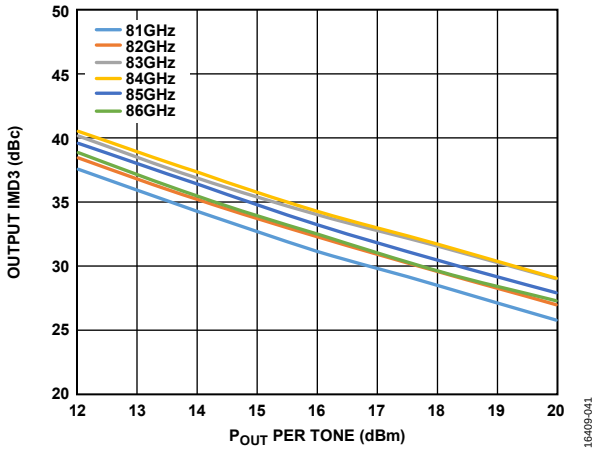

Figure 41. Upper Output Third-Order Intermodulation Distortion (IMD3) vs. P_{OUT}/Tone over Various Frequencies, I_{DD} = 800 mA

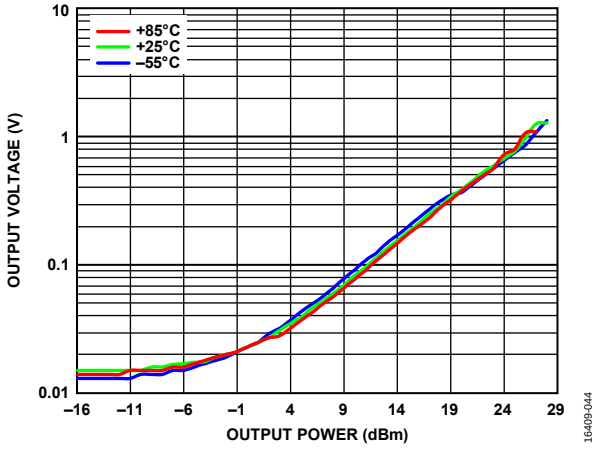

Figure 44. Detector Output Voltage (V_{OUT}) vs. Output Power over Temperatures, I_{DD} = 800 mA, RF = 86 GHz

THEORY OF OPERATION

The circuit architecture of the ADMV7810 power amplifier is shown in Figure 45. The ADMV7810 uses four cascaded gain stages to form an amplifier with a combined gain of 20 dB and a saturated output power (P_{SAT}) of 29 dBm. At the output of the last stage, a coupler taps off a small portion of the output signal. The coupled signal is presented to an on-chip diode detector for external monitoring of the output power. A matched reference diode is included to correct detector temperature dependencies. See the application circuit shown in Figure 46 for further details on biasing the different blocks and using the detector features.

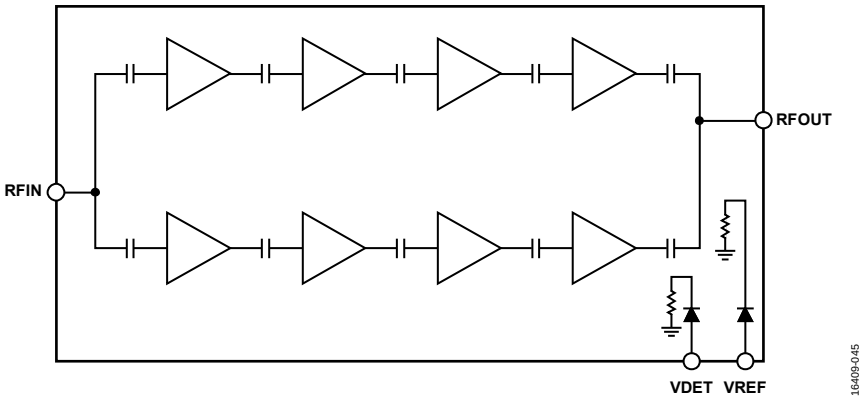

Figure 45. Power Amplifier Circuit Architecture

APPLICATIONS INFORMATION

A typical application circuit for the ADMV7810 is shown in Figure 46. Combine supply lines as shown in the application circuit schematic to minimize external component count and simplify power supply routing.

The ADMV7810 uses several amplifier, detector, and attenuator stages. All stages use depletion mode pHEMT transistors. It is important to follow the following power-up bias sequence to avoid transistor damage.

1. Apply a −2 V bias to the VGG1A to VGG4A and VGG1B to VGG4B pads.
2. Apply 4 V to the VDD1A to VDD1B and VDD1B to VDD4B pads.
3. Adjust VGG1A to VGG4A and VGG1B to VGG4B between −2 V and 0 V to achieve a total amplifier drain current of 800 mA.

To power down the ADMV7810, follow the reverse procedure. For additional guidance on general bias sequencing, see the *MMIC Amplifier Biasing Procedure* application note.

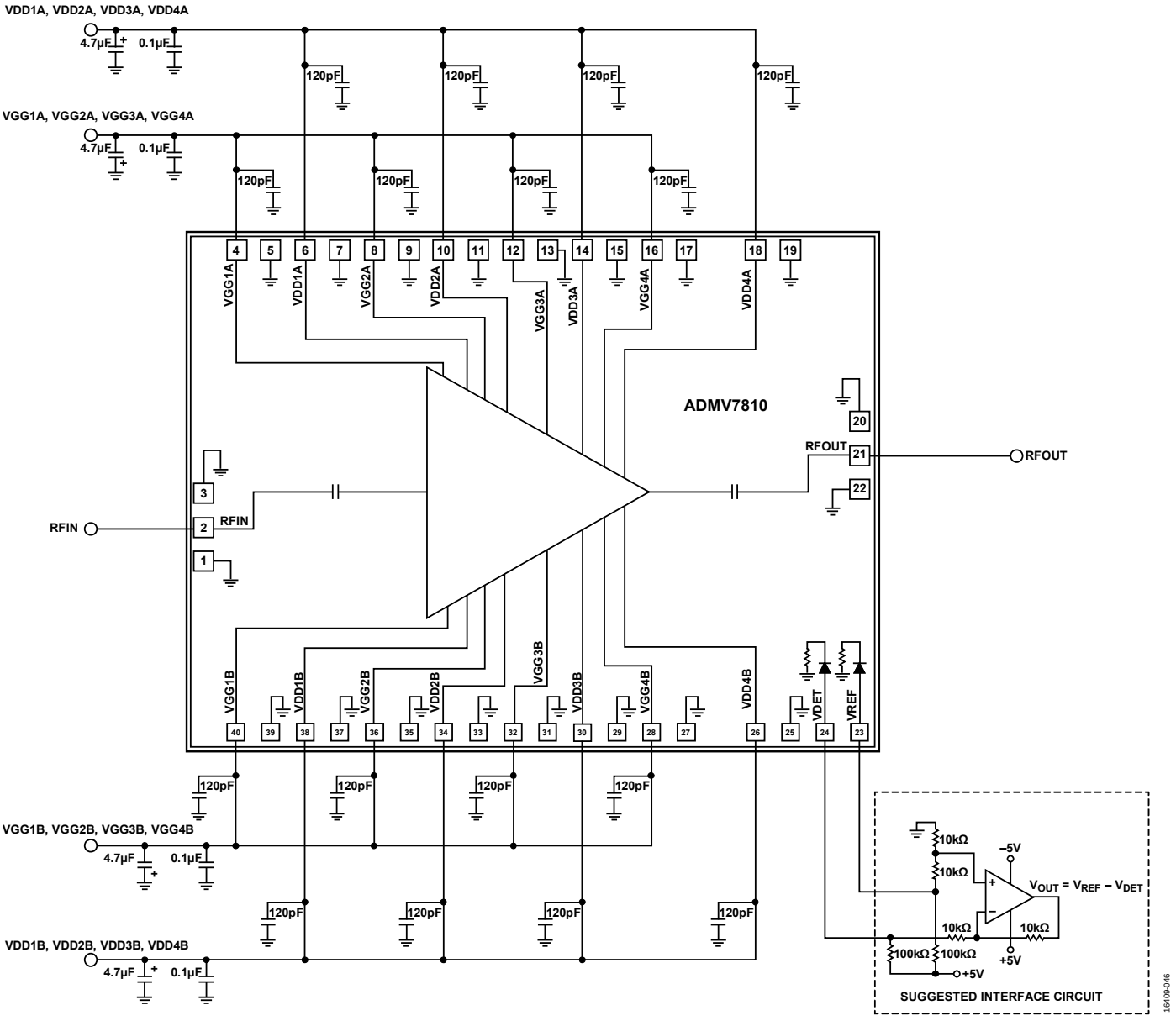

Figure 46. Typical Application Circuit

ASSEMBLY DIAGRAM

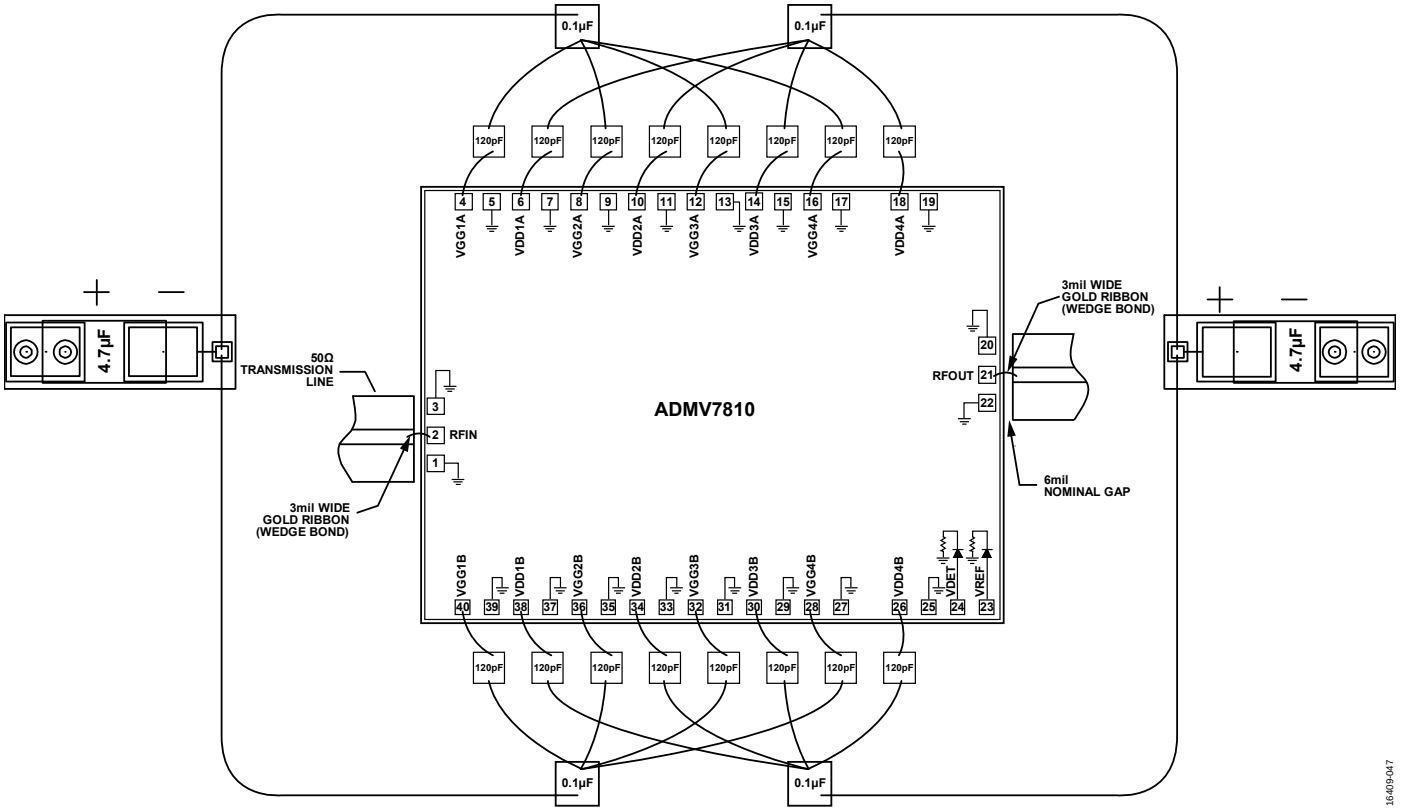

Figure 47. Assembly Diagram

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane eutectically or with conductive epoxy.

To bring RF to and from the chip, use 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates (see Figure 48).

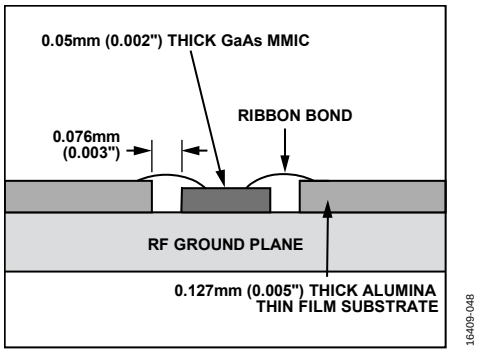

Figure 48. Routing RF Signals

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

HANDLING PRECAUTIONS

To avoid permanent damage, adhere to the following precautions.

Storage

All bare die ship in either waffle or gel-based ESD protective containers, sealed in an ESD protective bag. After opening the sealed ESD protective bag, all die must be stored in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Never use liquid cleaning systems to clean the chip.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes.

Transients

Suppress instrument and bias supply transients while bias is applied. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or with a sharp pair of bent tweezers. Because the surface of the chip has fragile air bridges, never touch the surface of the chip with a vacuum collet, tweezers, or fingers.

MOUNTING

The chip is back metallized and can be die mounted with gold/tin (AuSn) eutectic preforms or with electrically conductive epoxy. The mounting surface must be clean and flat.

Eutectic Die Attach

It is best to use an 80% Au/20% Sn preform with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, maintain tool tip temperature at 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

The ATROX 800HT1V is recommended for die attachment. Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after placing it into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with 3 mil × 0.5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. DC bonds of 1 mil (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).

OUTLINE DIMENSIONS

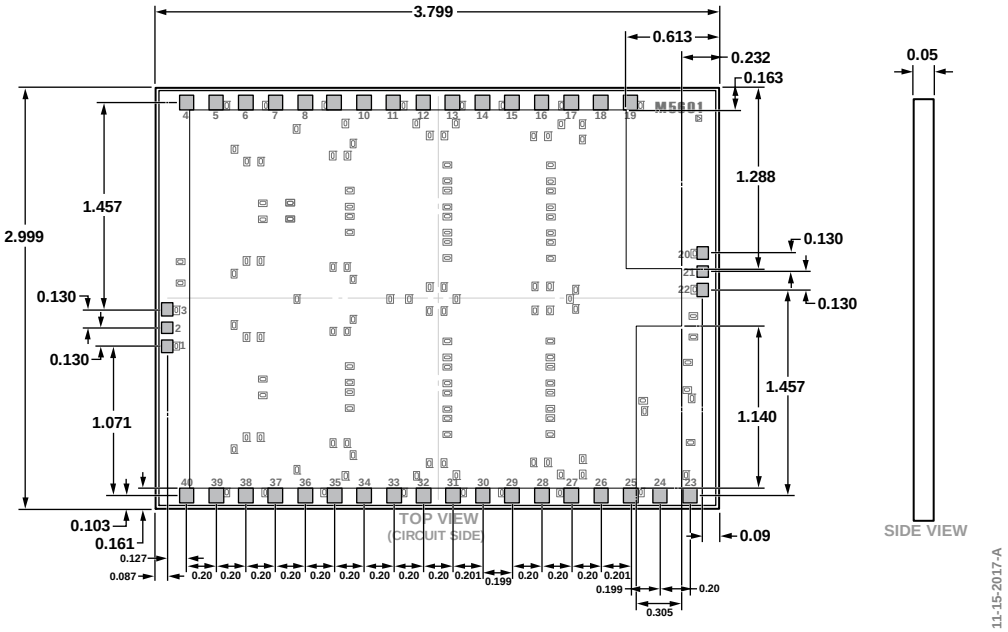

Figure 49. 40-Pad Bare Die [CHIP]
(C-40-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option[2]
ADMV7810CHIPS	−55°C to +85°C	40-Pad Bare Die [CHIP]	C-40-3
ADMV7810-SX	−55°C to +85°C	40-Pad Bare Die [CHIP]	C-40-3

[1] The ADMV7810-SX consists of two pairs of the die in a gel pack for sample orders.
[2] This is a waffle pack option; contact Analog Devices, Inc., sales representatives for additional packaging options.