

225 MHz to 520 MHz, Digitally Tunable, Band-Pass Filter

FEATURES

- ▶ Digitally tunable, octave, band-pass tuning
- ▶ 3 dB bandwidth: $9\% \pm 2\%$
- ▶ Rejection (20 dB): 19% away from f_{CENTER}
- ▶ Single chip replacement for discrete filter banks
- ▶ Compact 10 mm × 10 mm LGA package

APPLICATIONS

- ▶ Land mobile radios
- ▶ Test and measurement equipment
- ▶ Military radars and electronic warfare and electronic counter-measures
- ▶ Satellite communications
- ▶ Industrial and medical equipment

GENERAL DESCRIPTION

The ADMV8505¹ is an RF band-pass filter that features a digitally selectable frequency of operation. The filter center frequency (f_{CENTER}) can be adjusted from 225 MHz to 520 MHz using an 8-bit value (256 states) that incorporates a patented calibration technique.

The typical 3 dB bandwidth is 9%, and adjustability is $\pm 2\%$. Insertion loss is typically 4.5 dB, and the 20 dB rejection is 19% away from the f_{CENTER} , which is ideally suited for minimizing system interferers.

The ADMV8505 tunable filter can be used as a smaller alternative to large switched filter banks and discrete component-based tunable filters, providing a dynamically adjustable solution in advanced communications applications.

FUNCTIONAL BLOCK DIAGRAM

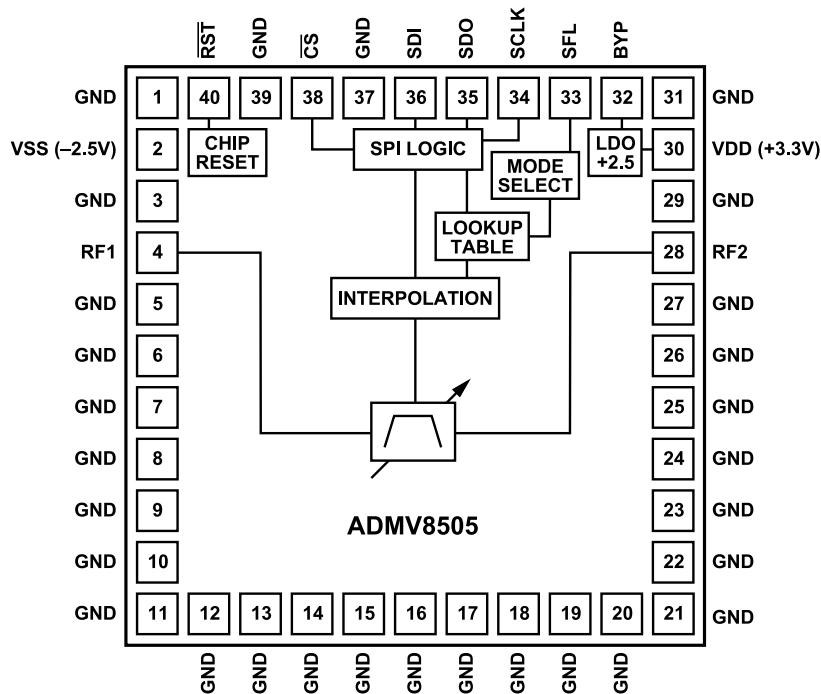


Figure 1. Functional Block Diagram

¹ Protected by U.S. Patent Number 11201600B1.

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REVISION HISTORY**4/2024—Rev. 0 to Rev. A**

| | |
|------------------------|---|
| Change to Table 3..... | 5 |
|------------------------|---|

12/2023—Revision 0: Initial Version

SPECIFICATIONS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1. Specifications

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------|---------------------------------|------|-----------------------|--|
| FREQUENCY RANGE (f_{CENTER}) | 225 | | 520 | MHz | |
| BANDWIDTH (3 dB) | | 9 | | % | |
| BANDWIDTH ADJUSTABILITY | | ± 2 | | % | |
| RESOLUTION | | 1 | | % | 8 bits per filter |
| REJECTION (20 dB) | | | | | |
| Low-Side | | $0.84 \times f_{\text{CENTER}}$ | | GHz | |
| High-Side | | $1.19 \times f_{\text{CENTER}}$ | | GHz | |
| RE-ENTRY FREQUENCY | | >3 | | GHz | ≤ 30 dB |
| INSERTION LOSS | | 4.5 | | dB | |
| RETURN LOSS | | 20 | | dB | |
| DYNAMIC PERFORMANCE | | | | | |
| Input Compression (P0.1dB) | | 24 | | dBm | |
| Input Third-Order Intercept (IP3) | | | | | Input power (P_{IN}) is 10 dBm; f_1 is Input Frequency 1 and f_2 is Input Frequency 2 |
| Low-Side IP3 | | 53 | | dBm | $f_1 = 0.9 \times f_{\text{CENTER}}$, $f_2 = 0.95 \times f_{\text{CENTER}}$ |
| High-Side IP3 | | 48 | | dBm | $f_1 = 1.05 \times f_{\text{CENTER}}$, $f_2 = 1.1 \times f_{\text{CENTER}}$ |
| In-Band IP3 | | 47 | | dBm | $f_1 = f_{\text{CENTER}} - 5$ kHz, $f_2 = f_{\text{CENTER}} + 5$ kHz |
| Group Delay | | 19 | | ns | Measured at $f_{\text{CENTER}} = 225$ MHz |
| Amplitude Settling Time | | 5 | | μs | To within ≤ 1 dB of static insertion loss |
| Phase Settling Time | | 10 | | μs | To within $\leq 2^\circ$ of static phase |
| Drift Rate | | | | | At $f_{\text{CENTER}} = 365$ MHz |
| Amplitude | | -0.01 | | dB/ $^\circ\text{C}$ | |
| Frequency | | -45 | | ppm/ $^\circ\text{C}$ | |
| SUPPLY VOLTAGE | | | | | |
| VSS | -2.6 | -2.5 | -2.4 | V | |
| VDD | +3.2 | +3.3 | +3.4 | V | |
| SUPPLY CURRENT (STATIC) | | | | | |
| Static | | | | | |
| VSS Current (I_{SS}) | | -2 | | μA | |
| VDD Current (I_{DD}) | | 125 | | μA | |
| Dynamic | | | | | |
| I_{DD} | | $f_{\text{SCLK}}/4$ | | mA | Where f_{SCLK} is the SCLK toggle frequency in MHz For example, continuous serial peripheral interface (SPI) writing at 10 MHz yields 2.5 mA of dynamic supply current |
| LOGIC ($\overline{\text{RST}}$, $\overline{\text{CS}}$, SCLK, SDI, SDO, and SFL) | | | | | |
| Logic Low | -0.3 | 0 | +0.8 | V | |
| Logic High | +1.2 | +3.3 | +3.6 | V | |

SPECIFICATIONS

TIMING SPECIFICATIONS

Table 2. Timing Specifications

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------|-----|-----|-----|------|--|
| t ₁ | 10 | | | ns | RST low time to perform reset |
| | 10 | | | ns | SCLK cycle time (write) |
| t ₂ | 20 | | | ns | SCLK cycle time (read) |
| t ₃ | 2.5 | | | ns | SCLK high time |
| t ₄ | 2.5 | | | ns | SCLK low time |
| t ₅ | 5 | | | ns | CS falling edge to SCLK rising edge setup time |
| t ₆ | 2 | | | ns | SCLK rising edge to hold time |
| t ₇ | 5 | | | ns | Minimum CS high time for latching in data (for multiple SPI transactions) |
| t ₈ | 5 | | | ns | CS rising edge to next SCLK rising edge ignore |
| t ₉ | 5 | | | ns | SDI data setup time |
| t ₁₀ | 2 | | | ns | SDI data hold time |
| t ₁₁ | 10 | | | ns | SFL falling edge (exiting SFL mode) to CS falling edge time (start of SPI transaction) |
| t ₁₂ | 10 | | | ns | CS rising edge (end of SPI transaction) to SFL rising edge time (entering SFL mode) |
| t ₁₃ | 10 | | | ns | SFL rising edge to CS falling edge time |
| t ₁₄ | 10 | | | ns | CS cycle time (SFL mode) |
| t ₁₅ | 2.5 | | | ns | CS high time (SFL mode) |
| t ₁₆ | 2.5 | | | ns | CS low time (SFL mode) |
| t ₁₇ | | 6 | | ns | SCLK falling edge to SDO valid (load capacitance (C _L) = 10 pF) |
| t ₁₈ | | 5 | | ns | SDO rise and fall time (C _L = 10 pF) |
| t ₁₉ | | 4 | | ns | CS rising edge to SDO tristate (C _L = 10 pF) |

Timing Diagram

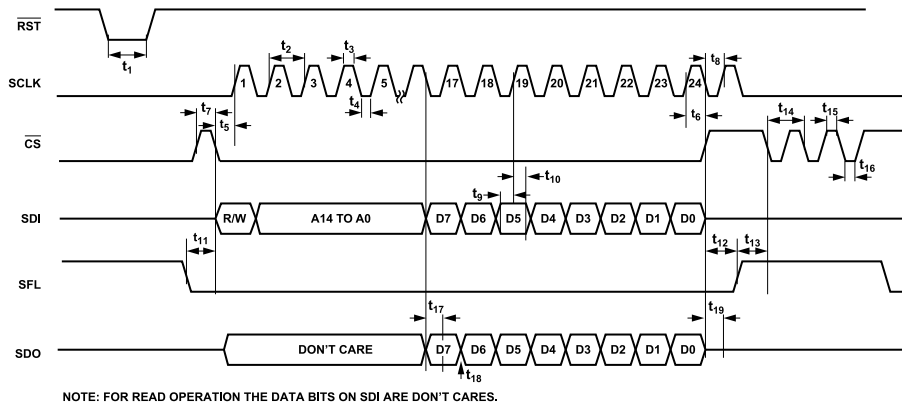


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

| Parameter | Rating |
|---|---------------------------------|
| Supply | |
| VDD | -0.3 V to +3.6 V |
| VSS | -2.75 V to +0.3 V |
| Digital Control Inputs | |
| Voltage | -0.3 V to VDD + 0.3 V |
| Current | 2 mA |
| Continuous RF Input Power | P0.1dB |
| Survivability | Maximum 5 minutes over lifetime |
| Temperature | |
| Operating Range | -40°C to +85°C |
| Storage Range | -55°C to +150°C |
| Junction to Maintain 1 Million Hours Mean Time to Failure (MTTF) | 135°C |
| Nominal Junction (Paddle Temperature (T _{PADDLE}) = 85°C) | 90°C |
| Moisture Sensitivity Level (MSL) Rating | MSL3 |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001-2010.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for ADMV8505

Table 4. ADMV8505, 40-Terminal LGA

| ESD Model | Withstand Threshold (V) | Class |
|-----------|-------------------------|-------|
| HBM | 1000 | 1C |
| FICDM | 500 | C2a |

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

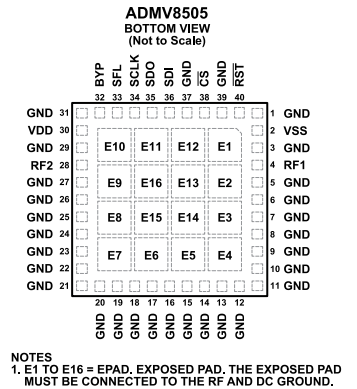


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|-------------------------------|------------------|--|
| 1, 3, 5 to 27, 29, 31, 37, 39 | GND | Ground. Connect the GND pins to the RF and DC ground. |
| 2 | VSS | The -2.5 V Power Supply Pin. Place 0.1 μ F and 100 pF decoupling capacitors close to VSS. |
| 4 | RF1 | RF Pin 1. RF1 is DC-coupled and matched to 50 Ω . Do not apply an external voltage to RF1. |
| 28 | RF2 | RF Pin 2. RF2 is DC-coupled and matched to 50 Ω . Do not apply an external voltage to RF2. |
| 30 | VDD | The 3.3 V Power Supply Pin. Place 0.1 μ F and 100 pF decoupling capacitors close to VDD. |
| 32 | BYP | The 2.5 V LDO Decoupling Bypass Pin. Place 47 μ F, 0.1 μ F, and 100 pF decoupling capacitors close to BYP. |
| 33 | SFL | SPI Fast Latch Enable, 3.3 V Logic. Set SFL high to enable fast latching of filter states on each rising edge of \overline{CS} . While SFL is in this mode, the SCLK, SDO, and SDI pins are not active. The SFL pin is internally pulled low with a 260 k Ω resistor. |
| 34 | SCLK | SPI Clock, 3.3 V Logic. The SCLK pin is internally pulled low with a 260 k Ω resistor. |
| 35 | SDO | SPI Data Output, 3.3 V Logic. The SDO pin is internally pulled low with a 260 k Ω resistor. |
| 36 | SDI | SPI Data Input, 3.3 V Logic. The SDI pin is internally pulled low with a 260 k Ω resistor. |
| 38 | \overline{CS} | SPI Chip Select, 3.3 V Logic. Active low. The \overline{CS} pin is internally pulled low with a 260 k Ω resistor. |
| 40 | \overline{RST} | Chip Reset, 3.3 V Logic. Active low. The \overline{RST} pin is internally pulled high with a 260 k Ω resistor |
| E1 to E16 | EPAD | Exposed Pad. The exposed pad must be connected to the RF and DC ground. |

TYPICAL PERFORMANCE CHARACTERISTICS

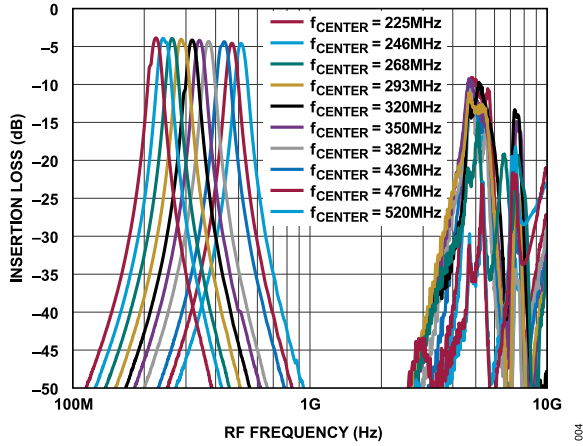


Figure 4. Insertion Loss vs. RF Frequency for Nominal Bandwidth

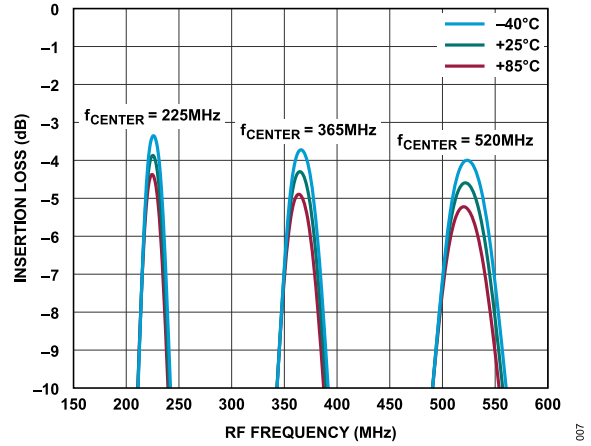


Figure 7. Insertion Loss vs. RF Frequency for Nominal Bandwidth at Various Temperatures and Center Frequencies

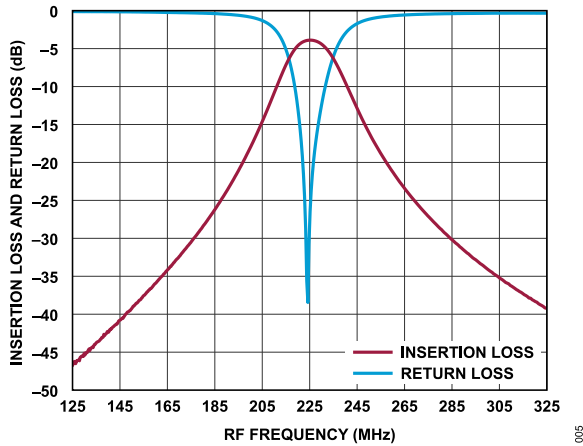


Figure 5. Insertion Loss and Return Loss vs. RF Frequency for Nominal Bandwidth at 225 MHz

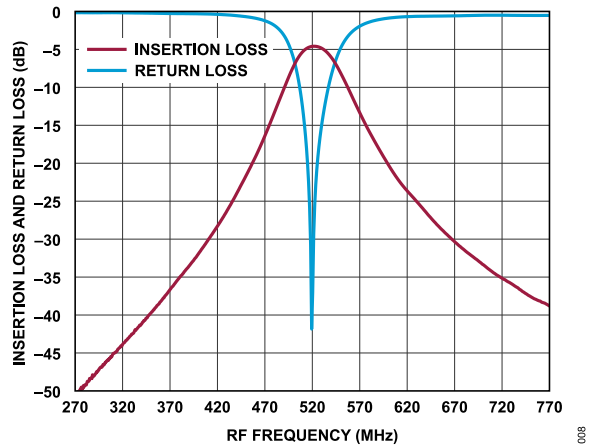


Figure 8. Insertion Loss and Return Loss vs. RF Frequency for Nominal Bandwidth at 520 MHz

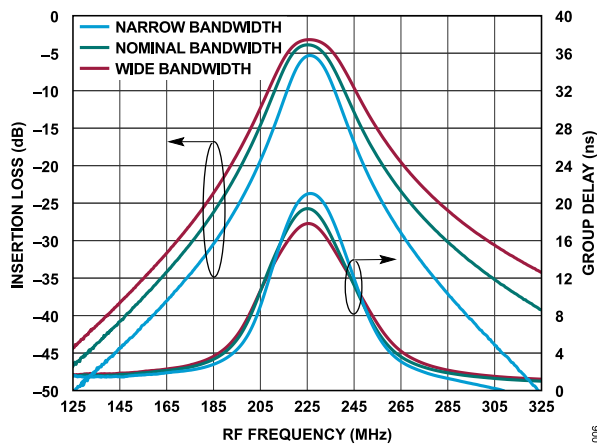


Figure 6. Insertion Loss and Group Delay vs. RF Frequency at 225 MHz

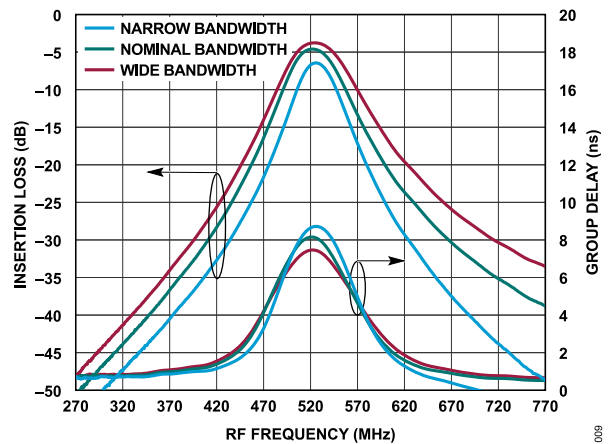


Figure 9. Insertion Loss and Group Delay vs. RF Frequency at 520 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

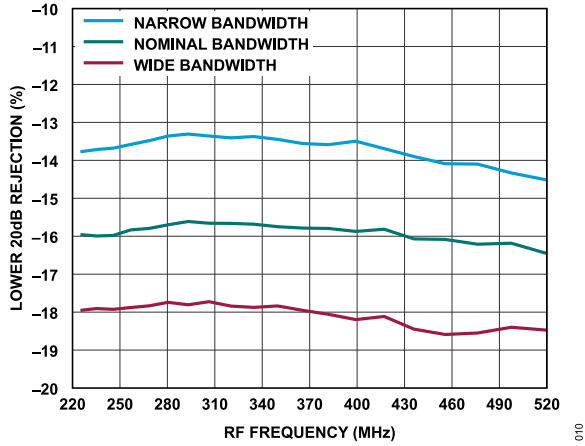


Figure 10. Percentage Away from f_{CENTER} for Lower 20 dB Rejection vs. RF Frequency for Various Bandwidths

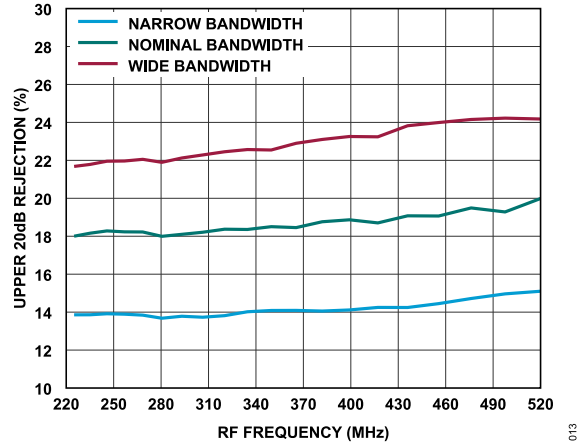


Figure 13. Percentage Away from f_{CENTER} for Upper 20 dB Rejection vs. RF Frequency for Various Bandwidths

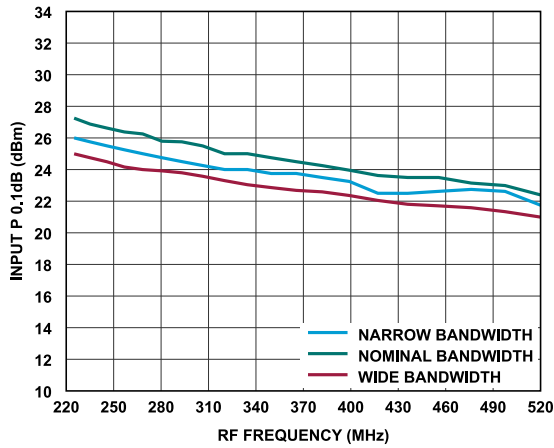


Figure 11. Input P0.1dB vs. RF Frequency for Various Bandwidths

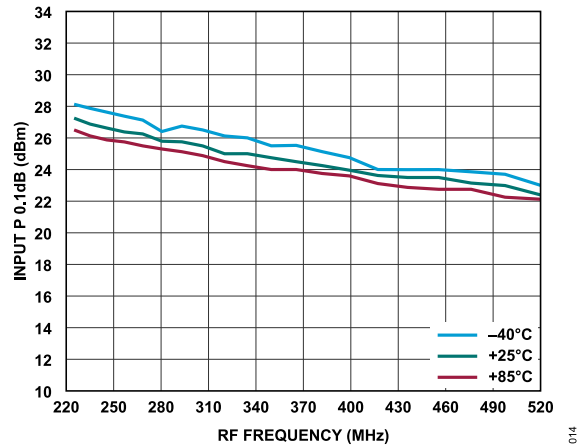


Figure 14. Input P0.1dB vs. RF Frequency for Nominal Bandwidth and Various Temperatures

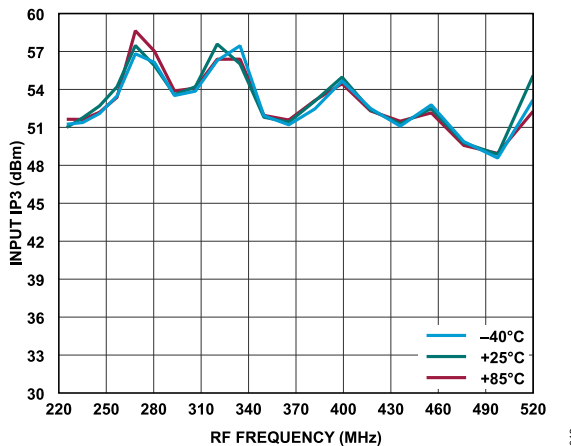


Figure 12. Low-Side Input IP3 vs. RF Frequency for Nominal Bandwidth and Various Temperatures (See the Specifications Section for Further Information)

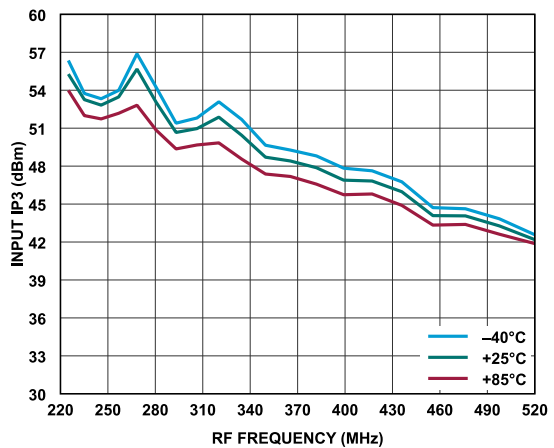


Figure 15. High-Side Input IP3 vs. RF Frequency for Nominal Bandwidth and Various Temperatures (See the Specifications Section for Further Information)

TYPICAL PERFORMANCE CHARACTERISTICS

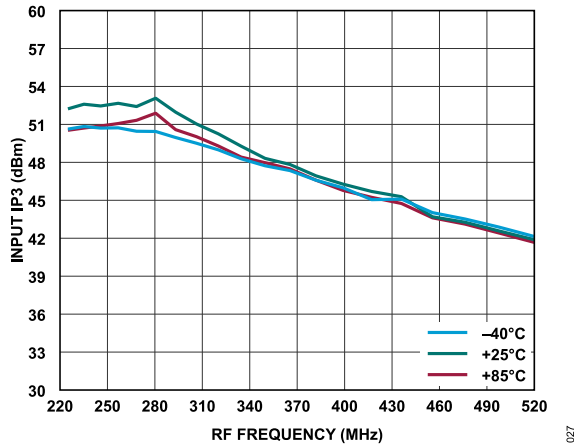


Figure 16. In-Band Input IP3 vs. RF Frequency for Nominal Bandwidth and Various Temperatures (See the Specifications Section for Further Information)

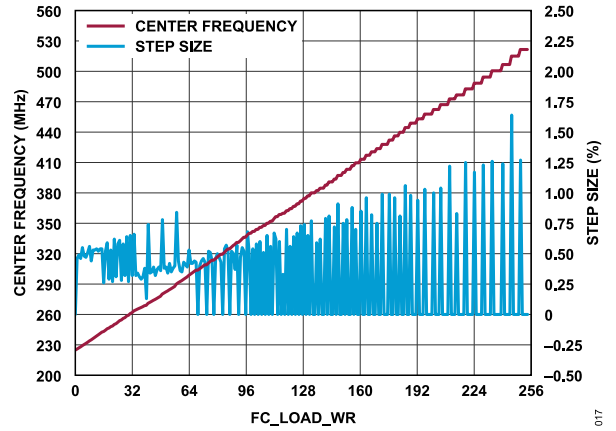


Figure 18. Center Frequency and Step Size vs. FC_LOAD_WR

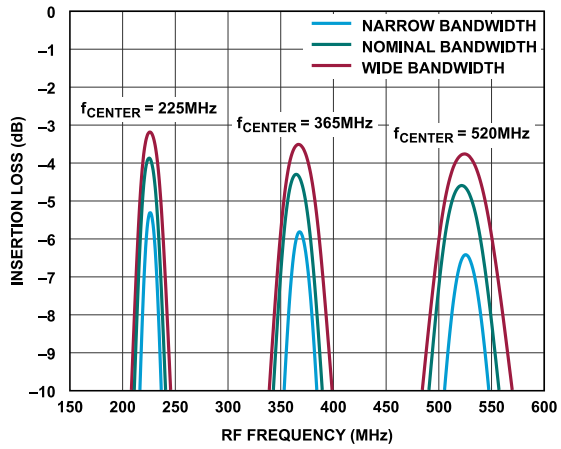


Figure 17. Insertion Loss vs. RF Frequency at Various Bandwidths and Center Frequencies

THEORY OF OPERATION

CHIP ARCHITECTURE

The ADMV8505 contains several switched capacitors that allow the RF performance to vary. A simplified diagram of the filter architecture is shown in Figure 19.

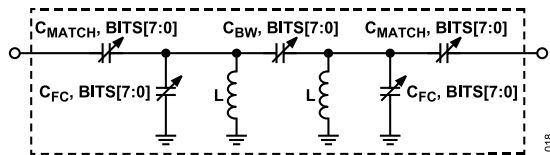


Figure 19. Simplified Filter Architecture Diagram

The two center frequency capacitors (C_{FC}) are configured by the f_{CENTER} load value, which manipulates the f_{CENTER} of the filter. Likewise, the bandwidth capacitor (C_{BW}) is configured by the bandwidth load value, which adjusts the bandwidth response of the filter. Additionally, the two match capacitors (C_{MATCH}) are set by the match load value, which allows adjustments to impedance matching of the filter.

The f_{CENTER} , bandwidth, and match load values each have 256 states (8 bits). In theory, there are over 16 million possible states for f_{CENTER} , bandwidth, and match load values for each band within the ADMV8505. To simplify selection of these values, Analog Devices, Inc., has developed three patent pending interpolation functions to ease implementation.

RF CONNECTIONS

The RF1 and RF2 pins of the ADMV8505 are DC-coupled to on-chip ESD protection diodes. If a DC voltage is present on the RF1 and RF2 pins from other components within the system, it is recommended to place DC blocking capacitors in series with these pins. The DC blocking capacitors must be selected based on the operating frequency of the filter. Generally, a value greater than 10 nF is sufficient to minimize insertion loss at the lower frequencies of operation. At higher frequencies of operation, it may be necessary to consider the parasitic elements of the selected capacitor. Figure 20 shows a general model of a capacitor with the parasitic elements. The parasitic series inductance (L_{ESL}) is typically of most concern given that its impedance can become dominant. The other parasitic elements, including the leakage resistance (R_L), the dielectric absorption resistance (R_{DA}), the dielectric absorption capacitance (C_{DA}), and electrical series resistance (R_{ESR}) are less critical elements for consideration but are shown in Figure 20 for completeness.

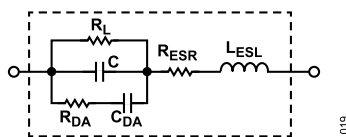


Figure 20. Model of a Capacitor

SPI CONFIGURATION

The SPI of the ADMV8505 allows configuration of the device for specific functions or operations via the 5-pin SPI port. This interface provides users with added flexibility and customization. The SPI consists of five control lines: SFL, SCLK, SDI, SDO, and \overline{CS} . For normal SPI operations, keep the SFL pin low.

The SPI protocol consists of an R/W bit followed by 15 register address bits and 8 data bits. The address field and data field are organized MSB first and end with the LSB.

Set the MSB to 0 for a write operation, and set the MSB to 1 for a read operation. The write cycle must be sampled on the rising edge of SCLK. The 24 bits of the serial write address and data are shifted in on the SDI control line, MSB to LSB. The ADMV8505 input logic level for the write cycle supports a 3.3 V interface.

For a read cycle, the R/W bit and the 15 register address bits shift in on the rising edge of SCLK on the SDI control line. Then, 8 bits of serial read data shift out on the SDO control line, MSB first, on the falling edge of the SCLK. The output logic level for a read cycle is 3.3 V. The output drivers of the SDO are enabled after the last rising edge of the SCLK of the instruction cycle and remain active until the end of the read cycle. In a read operation, when the \overline{CS} is deasserted, the SDO returns to high impedance until the next read transaction. The \overline{CS} is active low and must be deasserted at the end of the write or read sequence.

An active low input on the \overline{CS} starts and gates a communication cycle. The \overline{CS} pin allows more than one device to be used on the same serial communications lines. The SDO pin goes to a high impedance state when the \overline{CS} input is high. During the communication cycle, the chip select must stay low. The SPI communications protocol follows the Analog Devices SPI standard. For more information, see the [ADI-SPI Serial Control Interface Standard \(Rev 1.0\)](#).

THEORY OF OPERATION

MODE SELECTION

The ADMV8505 has two modes of operation: SPI write and SPI fast latch. The SPI write mode is the normal operating mode, and the SPI fast latch mode is used to sequence through the on-chip lookup table (LUT) using the internal state machine. To select the SPI write mode, set the SFL pin low. For operation in SPI fast latch mode, program the on-chip lookup table and fast latch parameters with the SFL pin low. Then, bring the SFL pin high to enter the SPI fast latch mode. Figure 21 shows a simplified representation of the SPI with the register map and internal state machine.

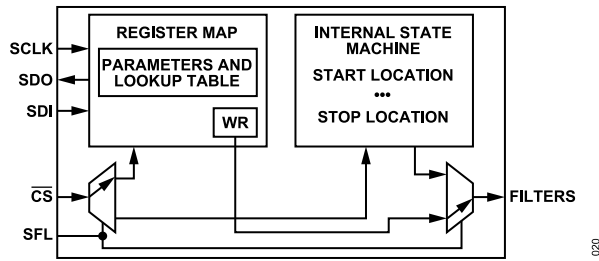


Figure 21. Simplified SPI Diagram

SPI WRITE MODE

The SPI write mode has a write grouping (WR) in Register 0x020 through Register 0x022. The grouping consists of the following:

- ▶ f_{CENTER} load value
- ▶ Bandwidth load value
- ▶ Match load value

See the Register Details section more information regarding the write grouping.

SPI STREAMING

In general, there are two types of SPI streaming transactions, Endian register ascending order and descending order. The ADMV8505 supports only the ascending order. To enable SPI streaming with Endian register ascending order, program Register 0x000 to value 0x3C.

For SPI streaming to the write grouping, Register 0x020 to Register 0x022 (recommended), the transaction points to Register 0x020 and streams out 3 bytes of data. The transaction is 40 bits in total (R/W bit + 15 bits address + 24 bits data).

For SPI streaming to the lookup table, Register 0x100 to Register 0x15F (recommended), the transaction points to Register 0x100 and streams out 96 bytes of data. The transaction is 784 bits in total (R/W bit + 15 bits address + 768 bits data).

INTERPOLATION FUNCTIONS

The ADMV8505 has three interpolation functions that allow the user to specify the f_{CENTER} of the filter using the f_{CENTER} load value only. Then, the appropriate capacitor codes are determined automatically. To enable these functions, set the INTERPOLATE bit (Register 0x050) high. Figure 22 shows a simplified diagram of the interpolation functions.

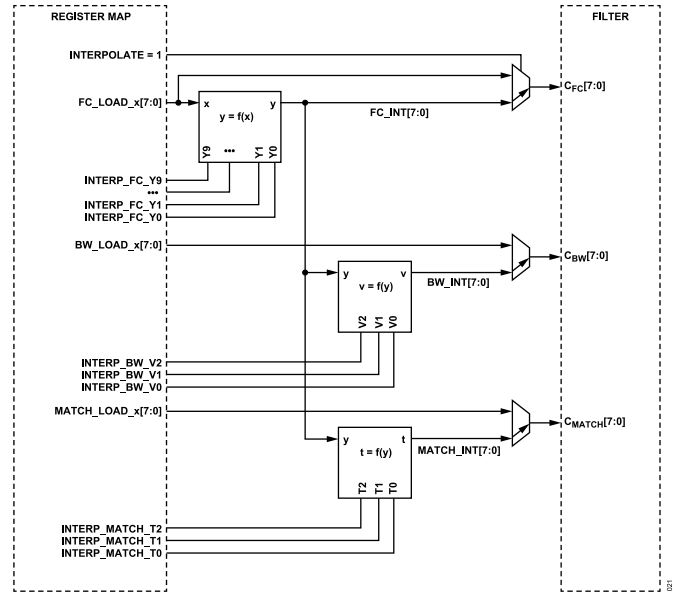


Figure 22. Interpolation Diagram

When the interpolation functions are enabled, the f_{CENTER} load range is 0 to 255, where 0 corresponds to the lowest frequency, and 255 corresponds to the highest frequency. For example, a value of 0 corresponds to approximately 225 MHz, and 255 corresponds to approximately 520 MHz. The f_{CENTER} load value is used to determine the appropriate capacitor codes based on the on-chip interpolation coefficients.

By default, the recommended interpolation coefficients are set for nominal bandwidth. The interpolation coefficients can be adjusted between $\pm 2\%$ of nominal bandwidth with reasonable insertion loss. Narrower bandwidth, down to approximately 5%, can also be achieved at the expense of insertion loss.

THEORY OF OPERATION

INTERPOLATION EQUATIONS

The following equations describe the input to the interpolation functions:

$$f_{CMIN} = \min(f_{CENTER}) \quad (1)$$

$$f_{CMAX} = \max(f_{CENTER}) \quad (2)$$

$$f_{CSTEP} \approx \frac{f_{CMAX} - f_{CMIN}}{255} \quad (3)$$

$$x = FC_LOAD_X, \text{ Bits}[7:0] \quad (4)$$

The anticipated f_{CENTER} of the filter is then computed as follows:

$$f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times x \quad (5)$$

The equations for the interpolation function of $y = f(x)$ that determines the capacitor codes (C_{FC}) are shown in Table 6.

Table 6. Equations for $y = f(x)$

| Condition | Logic Shift Form ¹ |
|---------------------------|---|
| If ($0 \leq x < 16$) | $y = Y1 + (((16 - x)(Y0 - Y1)) \gg 4)$ |
| If ($16 \leq x < 32$) | $y = Y2 + (((32 - x)(Y1 - Y2)) \gg 4)$ |
| If ($32 \leq x < 64$) | $y = Y3 + (((64 - x)(Y2 - Y3)) \gg 5)$ |
| If ($64 \leq x < 96$) | $y = Y4 + (((96 - x)(Y3 - Y4)) \gg 5)$ |
| If ($96 \leq x < 128$) | $y = Y5 + (((128 - x)(Y4 - Y5)) \gg 5)$ |
| If ($128 \leq x < 160$) | $y = Y6 + (((160 - x)(Y5 - Y6)) \gg 5)$ |
| If ($160 \leq x < 192$) | $y = Y7 + (((192 - x)(Y6 - Y7)) \gg 5)$ |
| If ($192 \leq x < 224$) | $y = Y8 + (((224 - x)(Y7 - Y8)) \gg 5)$ |
| If ($224 \leq x < 255$) | $y = Y9 + (((256 - x)(Y8 - Y9)) \gg 5)$ |
| Else | $y = Y9$ |

¹ Y0 to Y9 are the f_{CENTER} coefficients.

The equations for the interpolation function of $v = f(y)$ that determines the bandwidth capacitor codes (C_{BW}) are shown in Table 7.

Table 7. Equations for $v = f(y)$

| Condition | Logic Shift Form ¹ |
|--------------------------|--|
| If ($0 \leq y < 32$) | $v = V0 + ((y \times (V1 - V0)) \gg 5)$ |
| If ($32 \leq y < 255$) | $v = V1 + (((y - 32)(V2 - V1) \times 295) \gg 16)$ |
| Else | $v = V2$ |

¹ Y0 to Y2 are the bandwidth coefficients.

The equations for the interpolation function of $t = f(y)$ that determines the match capacitor codes (C_{MATCH}) are shown in Table 8.

Table 8. Equations for $t = f(y)$

| Condition | Logic Shift Form ¹ |
|--------------------------|--|
| If ($0 \leq y < 32$) | $t = T0 + ((y \times (T1 - T0)) \gg 5)$ |
| If ($32 \leq y < 255$) | $t = T1 + (((y - 32)(T2 - T1) \times 295) \gg 16)$ |
| Else | $t = T2$ |

¹ T0 to T2 are the match coefficients.

INTERPOLATION TABLES

Solving the interpolation equations for the lower bounds of each condition in the interpolation function of $y = f(x)$ yields what is detailed in Table 9.

Table 9. Equations for Anticipated f_{CENTER} for Each Significant x Value

| x | f_{CENTER} | $y = f(x)$ |
|-----|--|------------|
| 0 | $f_{CENTER} \approx f_{CMIN}$ | Y0 |
| 16 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 16$ | Y1 |
| 32 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 32$ | Y2 |
| 64 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 64$ | Y3 |
| 96 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 96$ | Y4 |
| 128 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 128$ | Y5 |
| 160 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 160$ | Y6 |
| 192 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 192$ | Y7 |
| 224 | $f_{CENTER} \approx f_{CMIN} + f_{CSTEP} \times 224$ | Y8 |
| 255 | $f_{CENTER} \approx f_{CMAX}$ | Y9 |

Similarly, solving the equations for the lower bounds of each condition in the interpolation functions of $v = f(y)$ and $t = f(y)$ yields what is detailed in Table 10.

Table 10. Equations for $v = f(y)$ and $t = f(y)$ for Each Significant y Value

| y | $v = f(y)$ | $t = f(y)$ |
|-----|------------|------------|
| 0 | V0 | T0 |
| 32 | V1 | T1 |
| 255 | V2 | T2 |

THEORY OF OPERATION

INTERPOLATION PLOTS

To garner a visual representation of the interpolation functions, the interpolation coefficients vs. their input (from the interpolation tables) can be plotted on a scatter plot. [Figure 23](#), [Figure 24](#), and [Figure 25](#) are the interpolation functions of y , v , and t using the interpolation coefficients.

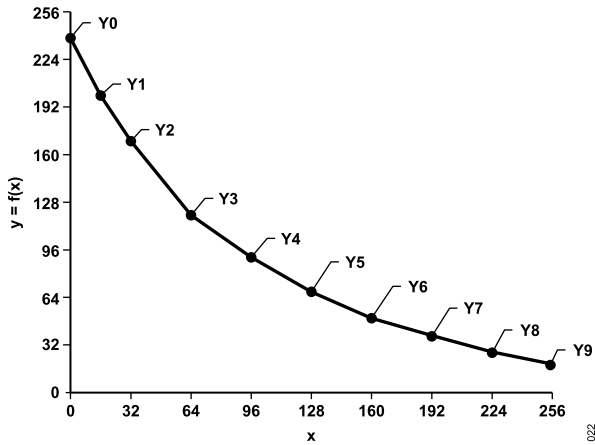


Figure 23. Interpolation Function of $y = f(x)$

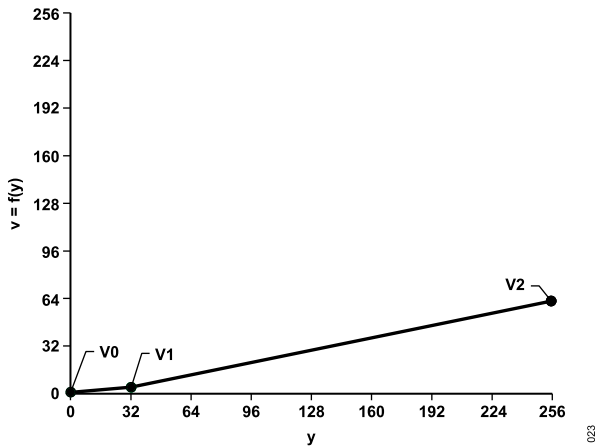


Figure 24. Interpolation Function of $v = f(y)$

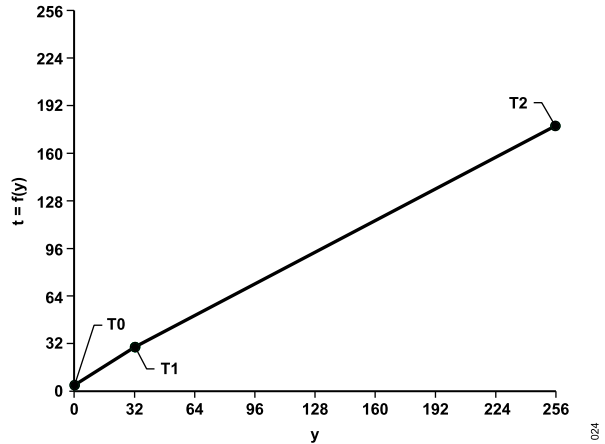


Figure 25. Interpolation Function of $t = f(y)$

INTERPOLATION COEFFICIENT CALIBRATION

The two primary reasons for the need to calibrate the interpolation coefficients include accounting for chip process variation and a different required operating bandwidth. The calibration of interpolation coefficients normally follows a four phase process (see [Figure 27](#)).

In the first calibration phase, the bandwidth and match coefficients, $V1$ and $T1$, are determined for a desired bandwidth. To perform this calibration phase, the f_{CENTER} load value must be set to 32. Then, the bandwidth and match load values are adjusted. When satisfied with the results, the $V1$ and $T1$ coefficients can be set to the bandwidth and match load values, respectively.

For the second calibration phase, the bandwidth and match coefficients, $V2$ and $T2$, are determined for a desired bandwidth. To perform this calibration phase, the f_{CENTER} load value must be set to a high value (180 is recommended). Then, the bandwidth and match load values are adjusted. When satisfied with the results, the $V2$ coefficient can be adjusted so that the computed result of $v = f(y) = f(180)$ is equal to the bandwidth load value. Similarly, the $T2$ coefficient can be adjusted so that the computed result of $t = f(y) = f(180)$ is equal to the match load value.

For the third calibration phase, the bandwidth and match coefficients, $V0$ and $T0$, are determined for a desired bandwidth. To perform this calibration phase, the f_{CENTER} load value must be set to a low value (18 is recommended). Then, the bandwidth and match load values are adjusted. When satisfied with the results, the $V0$ coefficient can be adjusted so that the computed result of $v = f(y) = f(18)$ is equal to the bandwidth load value. Similarly, the $T0$ coefficient can be adjusted so that the computed result of $t = f(y) = f(18)$ is equal to the match load value.

For the fourth calibration phase, adjustments are made to all of the y coefficients to ensure the operating f_{CENTER} is as close as possible to the anticipated f_{CENTER} . To perform this calibration phase, use [Table 9](#) as a reference for determining the target frequency for each y coefficient. For each x value listed in [Table 9](#), compute the y , v ,

THEORY OF OPERATION

and t functions, and then, set the f_{CENTER} , bandwidth, and match load values, respectively.

FILTER CODE READ BACK

The capacitor codes that are applied to the filter can be read back from the chip using Register 0x060 to Register 0x062. These registers represent the actual state of the capacitors on chip. This information can be useful for debugging purposes or during interpolation coefficient calibration.

SPI FAST LATCH MODE

The ADMV8505 has a 32-state LUT and an internal state machine that is useful for quickly changing filter states in the SPI fast latch mode. When the SFL pin is high, the SPI fast latch mode enables, and the internal state machine sequences on each rising edge of the $\overline{\text{CS}}$ pin.

The LUT has 32 groupings, LUT0 through LUT31, in Register 0x100 through Register 0x15F. Each grouping consists of the same type of parameters as those for the SPI write mode.

The functionality of the internal state machine is such that on each rising edge of the $\overline{\text{CS}}$ pin, the internal state machine sequences a pointer based on the programmed direction.

The internal state machine has the following parameters:

- ▶ FAST_LATCH_STOP (Register 0x011)
- ▶ FAST_LATCH_START (Register 0x012)
- ▶ FAST_LATCH_DIRECTION (Register 0x013)
- ▶ FAST_LATCH_STATE (Register 0x014)

The FAST_LATCH_STATE is the next LUT grouping that is selected on the next rising edge of the $\overline{\text{CS}}$ pin. The FAST_LATCH_STATE is considered the internal pointer location.

When the FAST_LATCH_DIRECTION bit is set to 0, the sequencing direction is incremental. When the FAST_LATCH_DIRECTION bit is set to 1, the sequencing direction is decremental.

The FAST_LATCH_START and FAST_LATCH_STOP bits are used to set the start location and the stop location, respectively. For incremental direction, the internal state machine sequences from the start location to the stop location and then rolls over to the start location. For the decremental direction, the sequence is from the stop location to the start location and then rolls over to the stop location.

The FAST_LATCH_STATE internal pointer is set to the values stored in FAST_LATCH_START for the incremental direction. For the decremental direction, the internal pointer is set to the values stored in FAST_LATCH_STOP. For this transaction to occur, one rising edge of the $\overline{\text{CS}}$ pin is necessary. By nature, this occurs during an SPI transaction in the SPI write mode. However, when exiting the SPI fast latch mode (SFL pin brought low), be sure to toggle the $\overline{\text{CS}}$ pin low then high or to perform an SPI transaction so that the

FAST_LATCH_STATE refreshes to either the start or stop location accordingly.

CHIP RESET

Two methods are available to reset the ADMV8505 registers to their default power-on state, a hard reset and a soft reset. The hard reset uses the $\overline{\text{RST}}$ pin, and the soft reset utilizes Register 0x000.

To perform a hard reset, momentarily bring the $\overline{\text{RST}}$ pin low and then high. See Figure 2 for the minimum required duration time for the $\overline{\text{RST}}$ pin to be low.

To perform a soft reset, set Register 0x000 to 0x81. This action sets the SOFTRESET and SOFTRESET_ bits high to initiate the reset. The SOFTRESET and SOFTRESET_ bits are self resetting once the reset operation completes.

Regardless of the reset method used, it is recommended to perform the following after the chip resets:

- ▶ Set Register 0x000 to 0x3C to enable the SDO pin and allow SPI streaming with Endian ascending order.
- ▶ Read back all registers on the chip.

APPLICATIONS INFORMATION

INTERPOLATION COEFFICIENTS

For reference, the ADMV8505 interpolation coefficients that were used for device characterization are listed in [Table 11](#). These interpolation coefficients are provided as a good starting point for use in a system. Depending upon the system requirements and allowable process tolerance, some minor adjustments may be needed to the interpolation coefficients. For most applications, the device process tolerance within a particular lot of material allows for one set of interpolation coefficients, such that interpolation coefficient calibration only needs to be performed once per lot. Refer to the [Interpolation Coefficient Calibration](#) section for more information on how to adjust the interpolation coefficients.

Table 11. Interpolation Coefficients

| Coefficient | Bit Field | Narrow Bandwidth | Nominal Bandwidth | Wide Bandwidth |
|-------------|-----------------|------------------|-------------------|----------------|
| Y0 | INTERP_FC_Y0 | 187 | 192 | 194 |
| Y1 | INTERP_FC_Y1 | 157 | 161 | 162 |
| Y2 | INTERP_FC_Y2 | 133 | 136 | 137 |
| Y3 | INTERP_FC_Y3 | 97 | 100 | 101 |
| Y4 | INTERP_FC_Y4 | 74 | 75 | 76 |
| Y5 | INTERP_FC_Y5 | 56 | 58 | 58 |
| Y6 | INTERP_FC_Y6 | 44 | 45 | 45 |
| Y7 | INTERP_FC_Y7 | 34 | 35 | 36 |
| Y8 | INTERP_FC_Y8 | 27 | 28 | 28 |
| Y9 | INTERP_FC_Y9 | 21 | 22 | 22 |
| V0 | INTERP_BW_V0 | 6 | 3 | 0 |
| V1 | INTERP_BW_V1 | 15 | 7 | 0 |
| V2 | INTERP_BW_V2 | 71 | 33 | 0 |
| T0 | INTERP_MATCH_T0 | 8 | 9 | 9 |
| T1 | INTERP_MATCH_T1 | 28 | 34 | 41 |
| T2 | INTERP_MATCH_T2 | 146 | 174 | 199 |

PRINTED CIRCUIT BOARD (PCB) DESIGN GUIDELINES

The PCB used to implement the ADMV8505 can use standard quality dielectric materials between the top metallization layer and the internal ground layer, such as the Isola 370HR. The Rogers 4003 or the Rogers 4350 do not have to be used. The characteristic impedance of the transmission lines to the RF1 and RF2 pins of the ADMV8505 must be controlled to 50 Ω to ensure optimal RF performance. Connect the GND pins and exposed pads of the ADMV8505 directly to the ground plane of the PCB. Use a sufficient number of via holes to connect the top and bottom ground planes of the PCB.

FLOW CHARTS

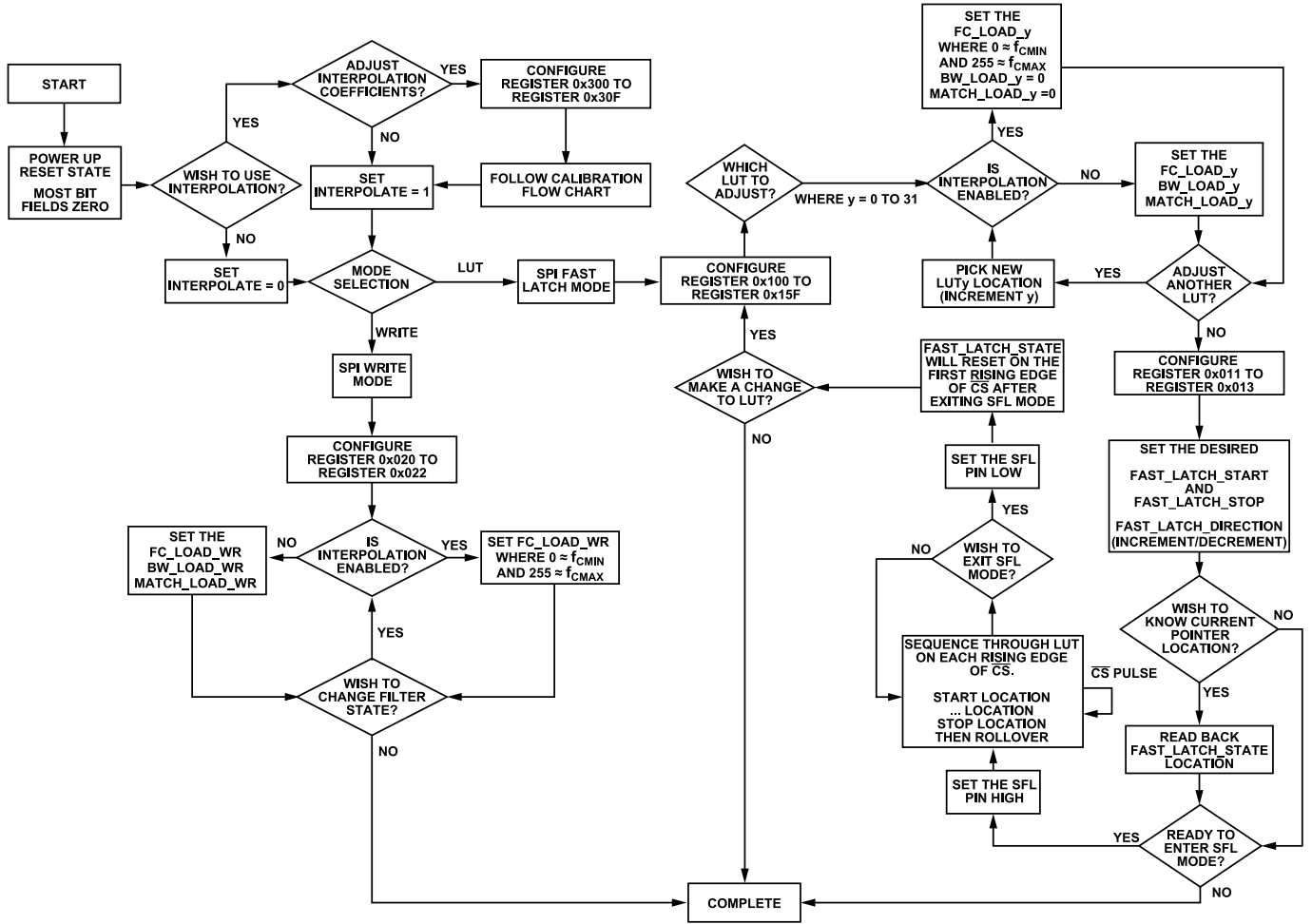


Figure 26. Programming Flow Chart

025

FLOW CHARTS

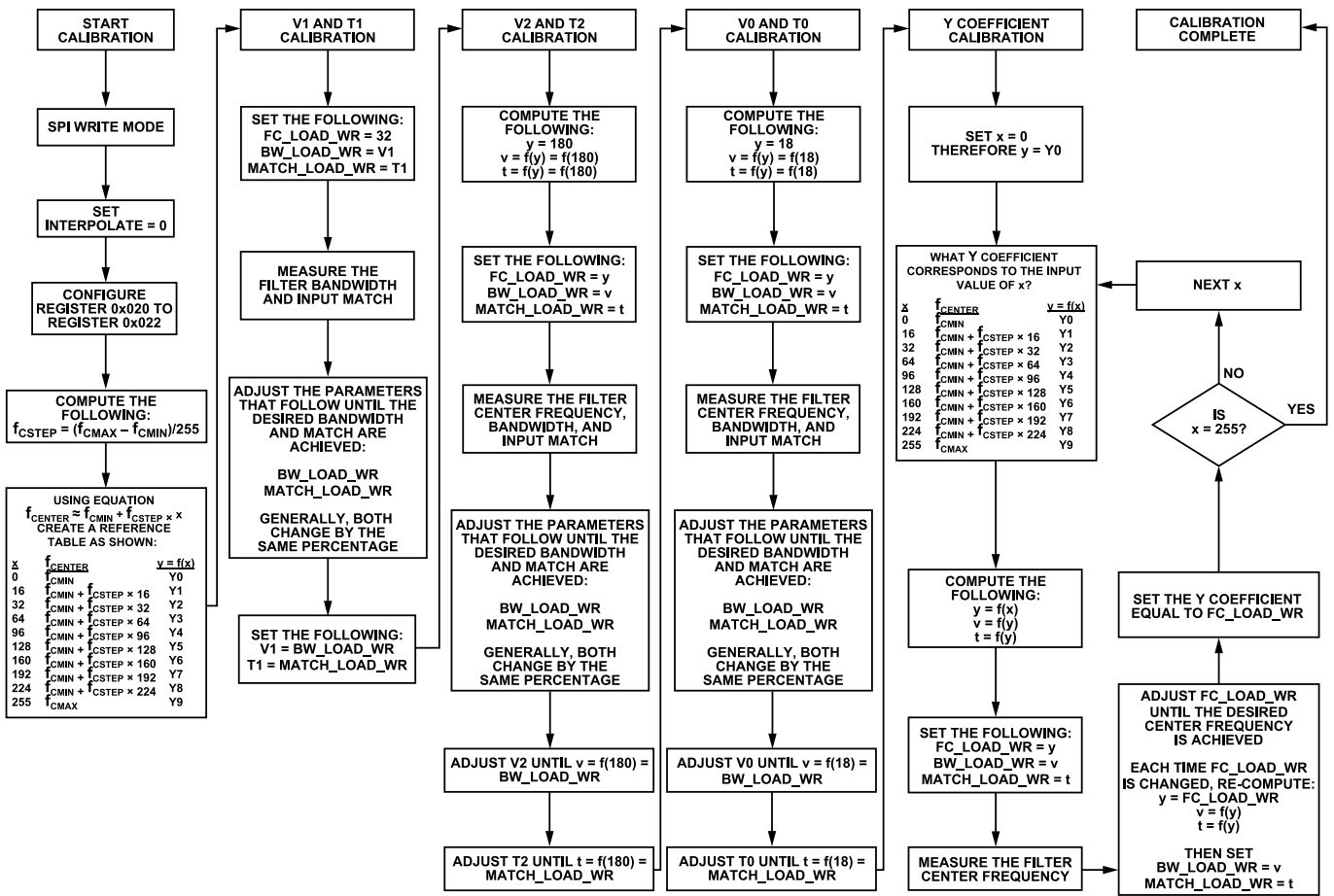


Figure 27. Interpolation Coefficient Calibration Flow Chart

REGISTER SUMMARY

Table 12. ADMV8505 Register Summary

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW | |
|-------|---------------------------|-------|-----------------------------------|------------------|-------------------------------------|-----------------|----------------|--------|---------------|---|-------|------|-----|
| 0x000 | ADI_SPI_CONFIG_A | [7:0] | SOFTRE- SET_ | LSB_FIRS T_ | ENDIAN_ | SDOAC- TIVE_ | SDOAC- TIVE | ENDIAN | LSB_FIRS T | SOFTRE- SET | 0x00 | R/W | |
| 0x001 | ADI_SPI_CONFIG_B | [7:0] | SIN- GLE_IN- STRUC- TION | CSB_STA LL | CON- TROL- LER_TAR- GET_RB | RESERVED | | | | CON- TROL- LER_TAR- GET_TRA NSFER | 0x00 | R/W | |
| 0x003 | CHIPTYPE | [7:0] | CHIPTYPE | | | | | | | | | 0x01 | R |
| 0x004 | PRODUCT_ID_L | [7:0] | PRODUCT_ID_L | | | | | | | | | 0x05 | R |
| 0x005 | PRODUCT_ID_H | [7:0] | PRODUCT_ID_H | | | | | | | | | 0x85 | R |
| 0x00C | VARIANT | [7:0] | RESERVED | | | | VARIANT | | | | 0x01 | R | |
| 0x011 | FAST_LATCH_STOP | [7:0] | RE- SERVED | FAST_LATCH_STOP | | | | | | | | 0x7F | R/W |
| 0x012 | FAST_LATCH_START | [7:0] | RE- SERVED | FAST_LATCH_START | | | | | | | | 0x00 | R/W |
| 0x013 | FAST_LATCH_DIREC- TION | [7:0] | RESERVED | | | | | | | FAST_LAT CH_DI- RECTION | 0x00 | R/W | |
| 0x014 | FAST_LATCH_STATE | [7:0] | RE- SERVED | FAST_LATCH_STATE | | | | | | | | 0x00 | R |
| 0x020 | WR_FC | [7:0] | FC_LOAD_WR | | | | | | | | | 0x00 | R/W |
| 0x021 | WR_BW | [7:0] | BW_LOAD_WR | | | | | | | | | 0x00 | R/W |
| 0x022 | WR_MATCH | [7:0] | MATCH_LOAD_WR | | | | | | | | | 0x00 | R/W |
| 0x050 | FILTER_CONFIG | [7:0] | RESERVED | | | | | | | INTERPO- LATE | 0x00 | R/W | |
| 0x060 | FC_READBACK | [7:0] | FC_READBACK | | | | | | | | | 0x00 | R |
| 0x061 | BW_READBACK | [7:0] | BW_READBACK | | | | | | | | | 0x00 | R |
| 0x062 | MATCH_READBACK | [7:0] | MATCH_READBACK | | | | | | | | | 0x00 | R |
| 0x100 | LUT0_FC | [7:0] | FC_LOAD_0 | | | | | | | | | 0x00 | R/W |
| 0x101 | LUT0_BW | [7:0] | BW_LOAD_0 | | | | | | | | | 0x00 | R/W |
| 0x102 | LUT0_MATCH | [7:0] | MATCH_LOAD_0 | | | | | | | | | 0x00 | R/W |
| 0x103 | LUT1_FC | [7:0] | FC_LOAD_1 | | | | | | | | | 0x00 | R/W |
| 0x104 | LUT1_BW | [7:0] | BW_LOAD_1 | | | | | | | | | 0x00 | R/W |
| 0x105 | LUT1_MATCH | [7:0] | MATCH_LOAD_1 | | | | | | | | | 0x00 | R/W |
| 0x106 | LUT2_FC | [7:0] | FC_LOAD_2 | | | | | | | | | 0x00 | R/W |
| 0x107 | LUT2_BW | [7:0] | BW_LOAD_2 | | | | | | | | | 0x00 | R/W |
| 0x108 | LUT2_MATCH | [7:0] | MATCH_LOAD_2 | | | | | | | | | 0x00 | R/W |
| 0x109 | LUT3_FC | [7:0] | FC_LOAD_3 | | | | | | | | | 0x00 | R/W |
| 0x10A | LUT3_BW | [7:0] | BW_LOAD_3 | | | | | | | | | 0x00 | R/W |
| 0x10B | LUT3_MATCH | [7:0] | MATCH_LOAD_3 | | | | | | | | | 0x00 | R/W |
| 0x10C | LUT4_FC | [7:0] | FC_LOAD_4 | | | | | | | | | 0x00 | R/W |
| 0x10D | LUT4_BW | [7:0] | BW_LOAD_4 | | | | | | | | | 0x00 | R/W |
| 0x10E | LUT4_MATCH | [7:0] | MATCH_LOAD_4 | | | | | | | | | 0x00 | R/W |
| 0x10F | LUT5_FC | [7:0] | FC_LOAD_5 | | | | | | | | | 0x00 | R/W |
| 0x110 | LUT5_BW | [7:0] | BW_LOAD_5 | | | | | | | | | 0x00 | R/W |

REGISTER SUMMARY

Table 12. ADMV8505 Register Summary (Continued)

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|-------|-------------|-------|-------|-------|-------|-------|---------------|-------|-------|-------|-------|-----|
| 0x111 | LUT5_MATCH | [7:0] | | | | | MATCH_LOAD_5 | | | | 0x00 | R/W |
| 0x112 | LUT6_FC | [7:0] | | | | | FC_LOAD_6 | | | | 0x00 | R/W |
| 0x113 | LUT6_BW | [7:0] | | | | | BW_LOAD_6 | | | | 0x00 | R/W |
| 0x114 | LUT6_MATCH | [7:0] | | | | | MATCH_LOAD_6 | | | | 0x00 | R/W |
| 0x115 | LUT7_FC | [7:0] | | | | | FC_LOAD_7 | | | | 0x00 | R/W |
| 0x116 | LUT7_BW | [7:0] | | | | | BW_LOAD_7 | | | | 0x00 | R/W |
| 0x117 | LUT7_MATCH | [7:0] | | | | | MATCH_LOAD_7 | | | | 0x00 | R/W |
| 0x118 | LUT8_FC | [7:0] | | | | | FC_LOAD_8 | | | | 0x00 | R/W |
| 0x119 | LUT8_BW | [7:0] | | | | | BW_LOAD_8 | | | | 0x00 | R/W |
| 0x11A | LUT8_MATCH | [7:0] | | | | | MATCH_LOAD_8 | | | | 0x00 | R/W |
| 0x11B | LUT9_FC | [7:0] | | | | | FC_LOAD_9 | | | | 0x00 | R/W |
| 0x11C | LUT9_BW | [7:0] | | | | | BW_LOAD_9 | | | | 0x00 | R/W |
| 0x11D | LUT9_MATCH | [7:0] | | | | | MATCH_LOAD_9 | | | | 0x00 | R/W |
| 0x11E | LUT10_FC | [7:0] | | | | | FC_LOAD_10 | | | | 0x00 | R/W |
| 0x11F | LUT10_BW | [7:0] | | | | | BW_LOAD_10 | | | | 0x00 | R/W |
| 0x120 | LUT10_MATCH | [7:0] | | | | | MATCH_LOAD_10 | | | | 0x00 | R/W |
| 0x121 | LUT11_FC | [7:0] | | | | | FC_LOAD_11 | | | | 0x00 | R/W |
| 0x122 | LUT11_BW | [7:0] | | | | | BW_LOAD_11 | | | | 0x00 | R/W |
| 0x123 | LUT11_MATCH | [7:0] | | | | | MATCH_LOAD_11 | | | | 0x00 | R/W |
| 0x124 | LUT12_FC | [7:0] | | | | | FC_LOAD_12 | | | | 0x00 | R/W |
| 0x125 | LUT12_BW | [7:0] | | | | | BW_LOAD_12 | | | | 0x00 | R/W |
| 0x126 | LUT12_MATCH | [7:0] | | | | | MATCH_LOAD_12 | | | | 0x00 | R/W |
| 0x127 | LUT13_FC | [7:0] | | | | | FC_LOAD_13 | | | | 0x00 | R/W |
| 0x128 | LUT13_BW | [7:0] | | | | | BW_LOAD_13 | | | | 0x00 | R/W |
| 0x129 | LUT13_MATCH | [7:0] | | | | | MATCH_LOAD_13 | | | | 0x00 | R/W |
| 0x12A | LUT14_FC | [7:0] | | | | | FC_LOAD_14 | | | | 0x00 | R/W |
| 0x12B | LUT14_BW | [7:0] | | | | | BW_LOAD_14 | | | | 0x00 | R/W |
| 0x12C | LUT14_MATCH | [7:0] | | | | | MATCH_LOAD_14 | | | | 0x00 | R/W |
| 0x12D | LUT15_FC | [7:0] | | | | | FC_LOAD_15 | | | | 0x00 | R/W |
| 0x12E | LUT15_BW | [7:0] | | | | | BW_LOAD_15 | | | | 0x00 | R/W |
| 0x12F | LUT15_MATCH | [7:0] | | | | | MATCH_LOAD_15 | | | | 0x00 | R/W |
| 0x130 | LUT16_FC | [7:0] | | | | | FC_LOAD_16 | | | | 0x00 | R/W |
| 0x131 | LUT16_BW | [7:0] | | | | | BW_LOAD_16 | | | | 0x00 | R/W |
| 0x132 | LUT16_MATCH | [7:0] | | | | | MATCH_LOAD_16 | | | | 0x00 | R/W |
| 0x133 | LUT17_FC | [7:0] | | | | | FC_LOAD_17 | | | | 0x00 | R/W |
| 0x134 | LUT17_BW | [7:0] | | | | | BW_LOAD_17 | | | | 0x00 | R/W |
| 0x135 | LUT17_MATCH | [7:0] | | | | | MATCH_LOAD_17 | | | | 0x00 | R/W |
| 0x136 | LUT18_FC | [7:0] | | | | | FC_LOAD_18 | | | | 0x00 | R/W |
| 0x137 | LUT18_BW | [7:0] | | | | | BW_LOAD_18 | | | | 0x00 | R/W |
| 0x138 | LUT18_MATCH | [7:0] | | | | | MATCH_LOAD_18 | | | | 0x00 | R/W |
| 0x139 | LUT19_FC | [7:0] | | | | | FC_LOAD_19 | | | | 0x00 | R/W |
| 0x13A | LUT19_BW | [7:0] | | | | | BW_LOAD_19 | | | | 0x00 | R/W |
| 0x13B | LUT19_MATCH | [7:0] | | | | | MATCH_LOAD_19 | | | | 0x00 | R/W |

REGISTER SUMMARY

Table 12. ADMV8505 Register Summary (Continued)

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|-------|--------------|-------|-------|-------|-------|-------|---------------|-------|-------|-------|-------|-----|
| 0x13C | LUT20_FC | [7:0] | | | | | FC_LOAD_20 | | | | 0x00 | R/W |
| 0x13D | LUT20_BW | [7:0] | | | | | BW_LOAD_20 | | | | 0x00 | R/W |
| 0x13E | LUT20_MATCH | [7:0] | | | | | MATCH_LOAD_20 | | | | 0x00 | R/W |
| 0x13F | LUT21_FC | [7:0] | | | | | FC_LOAD_21 | | | | 0x00 | R/W |
| 0x140 | LUT21_BW | [7:0] | | | | | BW_LOAD_21 | | | | 0x00 | R/W |
| 0x141 | LUT21_MATCH | [7:0] | | | | | MATCH_LOAD_21 | | | | 0x00 | R/W |
| 0x142 | LUT22_FC | [7:0] | | | | | FC_LOAD_22 | | | | 0x00 | R/W |
| 0x143 | LUT22_BW | [7:0] | | | | | BW_LOAD_22 | | | | 0x00 | R/W |
| 0x144 | LUT22_MATCH | [7:0] | | | | | MATCH_LOAD_22 | | | | 0x00 | R/W |
| 0x145 | LUT23_FC | [7:0] | | | | | FC_LOAD_23 | | | | 0x00 | R/W |
| 0x146 | LUT23_BW | [7:0] | | | | | BW_LOAD_23 | | | | 0x00 | R/W |
| 0x147 | LUT23_MATCH | [7:0] | | | | | MATCH_LOAD_23 | | | | 0x00 | R/W |
| 0x148 | LUT24_FC | [7:0] | | | | | FC_LOAD_24 | | | | 0x00 | R/W |
| 0x149 | LUT24_BW | [7:0] | | | | | BW_LOAD_24 | | | | 0x00 | R/W |
| 0x14A | LUT24_MATCH | [7:0] | | | | | MATCH_LOAD_24 | | | | 0x00 | R/W |
| 0x14B | LUT25_FC | [7:0] | | | | | FC_LOAD_25 | | | | 0x00 | R/W |
| 0x14C | LUT25_BW | [7:0] | | | | | BW_LOAD_25 | | | | 0x00 | R/W |
| 0x14D | LUT25_MATCH | [7:0] | | | | | MATCH_LOAD_25 | | | | 0x00 | R/W |
| 0x14E | LUT26_FC | [7:0] | | | | | FC_LOAD_26 | | | | 0x00 | R/W |
| 0x14F | LUT26_BW | [7:0] | | | | | BW_LOAD_26 | | | | 0x00 | R/W |
| 0x150 | LUT26_MATCH | [7:0] | | | | | MATCH_LOAD_26 | | | | 0x00 | R/W |
| 0x151 | LUT27_FC | [7:0] | | | | | FC_LOAD_27 | | | | 0x00 | R/W |
| 0x152 | LUT27_BW | [7:0] | | | | | BW_LOAD_27 | | | | 0x00 | R/W |
| 0x153 | LUT27_MATCH | [7:0] | | | | | MATCH_LOAD_27 | | | | 0x00 | R/W |
| 0x154 | LUT28_FC | [7:0] | | | | | FC_LOAD_28 | | | | 0x00 | R/W |
| 0x155 | LUT28_BW | [7:0] | | | | | BW_LOAD_28 | | | | 0x00 | R/W |
| 0x156 | LUT28_MATCH | [7:0] | | | | | MATCH_LOAD_28 | | | | 0x00 | R/W |
| 0x157 | LUT29_FC | [7:0] | | | | | FC_LOAD_29 | | | | 0x00 | R/W |
| 0x158 | LUT29_BW | [7:0] | | | | | BW_LOAD_29 | | | | 0x00 | R/W |
| 0x159 | LUT29_MATCH | [7:0] | | | | | MATCH_LOAD_29 | | | | 0x00 | R/W |
| 0x15A | LUT30_FC | [7:0] | | | | | FC_LOAD_30 | | | | 0x00 | R/W |
| 0x15B | LUT30_BW | [7:0] | | | | | BW_LOAD_30 | | | | 0x00 | R/W |
| 0x15C | LUT30_MATCH | [7:0] | | | | | MATCH_LOAD_30 | | | | 0x00 | R/W |
| 0x15D | LUT31_FC | [7:0] | | | | | FC_LOAD_31 | | | | 0x00 | R/W |
| 0x15E | LUT31_BW | [7:0] | | | | | BW_LOAD_31 | | | | 0x00 | R/W |
| 0x15F | LUT31_MATCH | [7:0] | | | | | MATCH_LOAD_31 | | | | 0x00 | R/W |
| 0x300 | INTERP_FC_Y0 | [7:0] | | | | | INTERP_FC_Y0 | | | | 0xC0 | R/W |
| 0x301 | INTERP_FC_Y1 | [7:0] | | | | | INTERP_FC_Y1 | | | | 0xA1 | R/W |
| 0x302 | INTERP_FC_Y2 | [7:0] | | | | | INTERP_FC_Y2 | | | | 0x88 | R/W |
| 0x303 | INTERP_FC_Y3 | [7:0] | | | | | INTERP_FC_Y3 | | | | 0x64 | R/W |
| 0x304 | INTERP_FC_Y4 | [7:0] | | | | | INTERP_FC_Y4 | | | | 0x4B | R/W |
| 0x305 | INTERP_FC_Y5 | [7:0] | | | | | INTERP_FC_Y5 | | | | 0x3A | R/W |
| 0x306 | INTERP_FC_Y6 | [7:0] | | | | | INTERP_FC_Y6 | | | | 0x2D | R/W |

REGISTER SUMMARY

Table 12. ADMV8505 Register Summary (Continued)

| Reg | Name | Bits | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Reset | RW |
|-------|-----------------|-------|-------|-------|-------|-------|-----------------|-------|-------|-------|-------|-----|
| 0x307 | INTERP_FC_Y7 | [7:0] | | | | | INTERP_FC_Y7 | | | | 0x23 | R/W |
| 0x308 | INTERP_FC_Y8 | [7:0] | | | | | INTERP_FC_Y8 | | | | 0x1C | R/W |
| 0x309 | INTERP_FC_Y9 | [7:0] | | | | | INTERP_FC_Y9 | | | | 0x16 | R/W |
| 0x30A | INTERP_BW_V0 | [7:0] | | | | | INTERP_BW_V0 | | | | 0x03 | R/W |
| 0x30B | INTERP_BW_V1 | [7:0] | | | | | INTERP_BW_V1 | | | | 0x07 | R/W |
| 0x30C | INTERP_BW_V2 | [7:0] | | | | | INTERP_BW_V2 | | | | 0x21 | R/W |
| 0x30D | INTERP_MATCH_T0 | [7:0] | | | | | INTERP_MATCH_T0 | | | | 0x09 | R/W |
| 0x30E | INTERP_MATCH_T1 | [7:0] | | | | | INTERP_MATCH_T1 | | | | 0x22 | R/W |
| 0x30F | INTERP_MATCH_T2 | [7:0] | | | | | INTERP_MATCH_T2 | | | | 0xAE | R/W |

REGISTER DETAILS

Address: 0x000, Reset: 0x00, Name: ADI_SPI_CONFIG_A

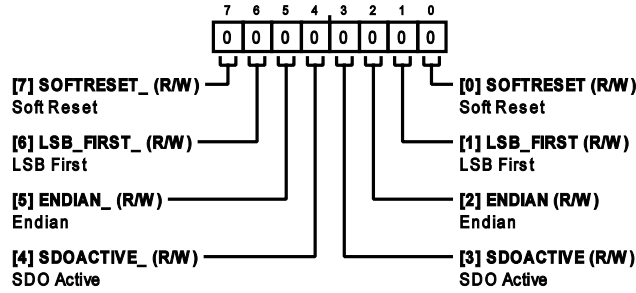
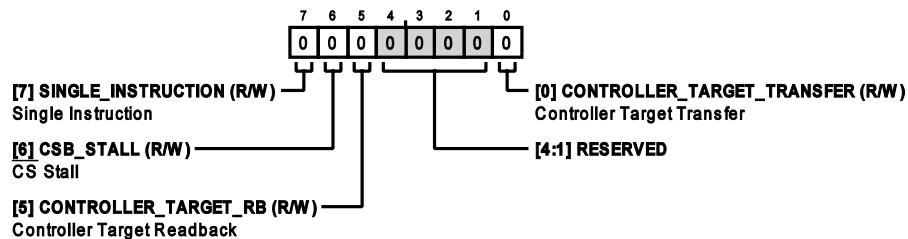


Table 13. Bit Descriptions for ADI_SPI_CONFIG_A

| Bits | Bit Name | Description | Reset | Access |
|------|------------|---|-------|--------|
| 7 | SOFTRESET_ | Soft Reset. 0: Reset Not Asserted. 1: Reset Asserted. | 0x0 | R/W |
| 6 | LSB_FIRST_ | LSB First. 0: MSB First. 1: LSB First. | 0x0 | R/W |
| 5 | ENDIAN_ | Endian. 0: Little Endian. 1: Big Endian. | 0x0 | R/W |
| 4 | SDOACTIVE_ | SDO Active. 0: SDO Inactive. 1: SDO Active. | 0x0 | R/W |
| 3 | SDOACTIVE | SDO Active. 0: SDO Inactive. 1: SDO Active. | 0x0 | R/W |
| 2 | ENDIAN | Endian. 0: Little Endian. 1: Big Endian. | 0x0 | R/W |
| 1 | LSB_FIRST | LSB First. 0: MSB First. 1: LSB First. | 0x0 | R/W |
| 0 | SOFTRESET | Soft Reset. 0: Reset Not Asserted. 1: Reset Asserted. | 0x0 | R/W |

Address: 0x001, Reset: 0x00, Name: ADI_SPI_CONFIG_B



REGISTER DETAILS

Table 14. Bit Descriptions for ADI_SPI_CONFIG_B

| Bits | Bit Name | Description | Reset | Access |
|-------|----------------------------|--|-------|--------|
| 7 | SINGLE_INSTRUCTION | Single Instruction. 0: Enable Streaming. 1: Disable Streaming Regardless of CSB. | 0x0 | R/W |
| 6 | CSB_STALL | $\overline{\text{CS}}$ Stall. | 0x0 | R/W |
| 5 | CONTROLLER_TARGET_RB | Controller Target Readback. | 0x0 | R/W |
| [4:1] | RESERVED | Reserved. | 0x0 | R |
| 0 | CONTROLLER_TARGET_TRANSFER | Controller Target Transfer. | 0x0 | R/W |

Address: 0x003, Reset: 0x01, Name: CHIPTYPE

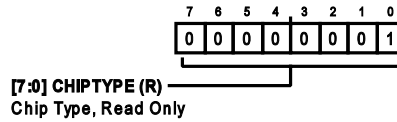


Table 15. Bit Descriptions for CHIPTYPE

| Bits | Bit Name | Description | Reset | Access |
|-------|----------|-----------------------|-------|--------|
| [7:0] | CHIPTYPE | Chip Type, Read Only. | 0x1 | R |

Address: 0x004, Reset: 0x05, Name: PRODUCT_ID_L

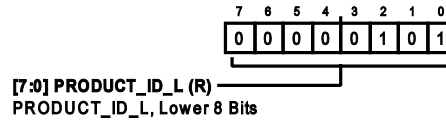


Table 16. Bit Descriptions for PRODUCT_ID_L

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|-----------------------------|-------|--------|
| [7:0] | PRODUCT_ID_L | PRODUCT_ID_L, Lower 8 Bits. | 0x5 | R |

Address: 0x005, Reset: 0x85, Name: PRODUCT_ID_H

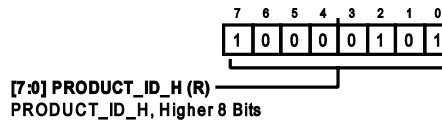
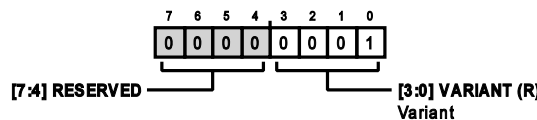


Table 17. Bit Descriptions for PRODUCT_ID_H

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|------------------------------|-------|--------|
| [7:0] | PRODUCT_ID_H | PRODUCT_ID_H, Higher 8 Bits. | 0x85 | R |

Address: 0x00C, Reset: 0x01, Name: VARIANT



REGISTER DETAILS

Table 18. Bit Descriptions for VARIANT

| Bits | Bit Name | Description | Reset | Access |
|-------|----------|-------------|-------|--------|
| [7:4] | RESERVED | Reserved. | 0x0 | R |
| [3:0] | VARIANT | Variant. | 0x1 | R |

Address: 0x011, Reset: 0x7F, Name: FAST_LATCH_STOP

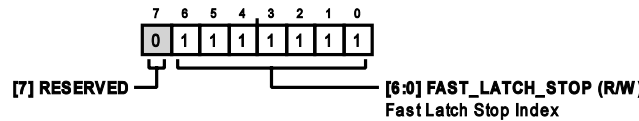


Table 19. Bit Descriptions for FAST_LATCH_STOP

| Bits | Bit Name | Description | Reset | Access |
|-------|-----------------|---|-------|--------|
| 7 | RESERVED | Reserved. | 0x0 | R |
| [6:0] | FAST_LATCH_STOP | Fast Latch Stop Index. This sets the stop index within the fast latch lookup table. | 0x7F | R/W |

Address: 0x012, Reset: 0x00, Name: FAST_LATCH_START

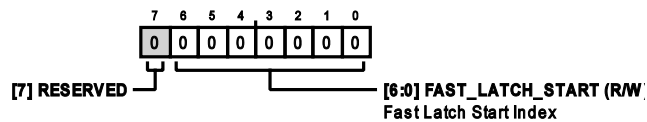


Table 20. Bit Descriptions for FAST_LATCH_START

| Bits | Bit Name | Description | Reset | Access |
|-------|------------------|---|-------|--------|
| 7 | RESERVED | Reserved. | 0x0 | R |
| [6:0] | FAST_LATCH_START | Fast Latch Start Index. This sets the start index within the fast latch lookup table. | 0x0 | R/W |

Address: 0x013, Reset: 0x00, Name: FAST_LATCH_DIRECTION

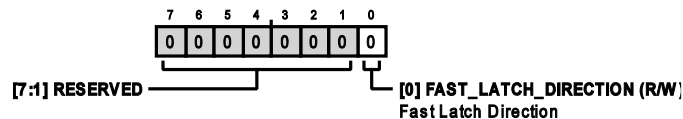
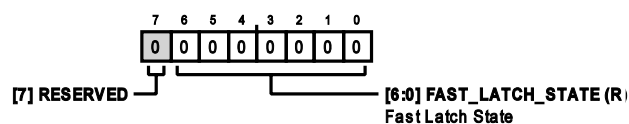


Table 21. Bit Descriptions for FAST_LATCH_DIRECTION

| Bits | Bit Name | Description | Reset | Access |
|-------|----------------------|--|-------|--------|
| [7:1] | RESERVED | Reserved. | 0x0 | R |
| 0 | FAST_LATCH_DIRECTION | Fast Latch Direction. This bit determines which direction to sequence within the fast latch lookup table. When the direction is set to increment, then the internal state machine will be set to the start index. When the direction is set to decrement, then the internal state machine will be set to the stop index. 0: Increment. 1: Decrement. | 0x0 | R/W |

Address: 0x014, Reset: 0x00, Name: FAST_LATCH_STATE



REGISTER DETAILS

Table 22. Bit Descriptions for FAST_LATCH_STATE

| Bits | Bit Name | Description | Reset | Access |
|-------|------------------|--|-------|--------|
| 7 | RESERVED | Reserved. | 0x0 | R |
| [6:0] | FAST_LATCH_STATE | Fast Latch State. Reads back the internal state machine index for fast latch lookup table (SFL mode). This index is the next location the internal state machine will advance to, on the next CSB rising edge. The internal state machine index will be set to the start index if the direction is set to increment and will be set to the stop index if the direction set to is decrement. Upon changes to the start index, stop index, and direction, the index will update accordingly. | 0x0 | R |

Address: 0x020, Reset: 0x00, Name: WR_FC

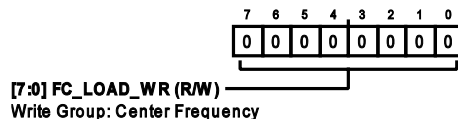


Table 23. Bit Descriptions for WR_FC

| Bits | Bit Name | Description | Reset | Access |
|-------|------------|--------------------------------|-------|--------|
| [7:0] | FC_LOAD_WR | Write Group: Center Frequency. | 0x0 | R/W |

Address: 0x021, Reset: 0x00, Name: WR_BW

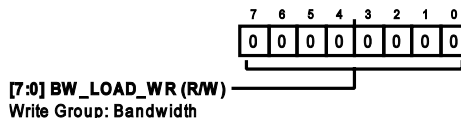


Table 24. Bit Descriptions for WR_BW

| Bits | Bit Name | Description | Reset | Access |
|-------|------------|-------------------------|-------|--------|
| [7:0] | BW_LOAD_WR | Write Group: Bandwidth. | 0x0 | R/W |

Address: 0x022, Reset: 0x00, Name: WR_MATCH

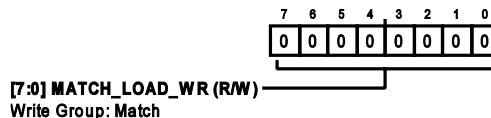


Table 25. Bit Descriptions for WR_MATCH

| Bits | Bit Name | Description | Reset | Access |
|-------|---------------|---------------------|-------|--------|
| [7:0] | MATCH_LOAD_WR | Write Group: Match. | 0x0 | R/W |

REGISTER DETAILS

Address: 0x050, Reset: 0x00, Name: FILTER_CONFIG

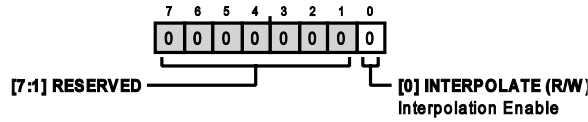


Table 26. Bit Descriptions for FILTER_CONFIG

| Bits | Bit Name | Description | Reset | Access |
|-------|-------------|---|-------|--------|
| [7:1] | RESERVED | Reserved. | 0x0 | R |
| 0 | INTERPOLATE | Interpolation Enable. When this bit is set to zero, then must program center frequency, bandwidth, and match. When this bit is set to one, then capacitors for center frequency, bandwidth and match will be determined from interpolation. | 0x0 | R/W |

Address: 0x060, Reset: 0x00, Name: FC_READBACK

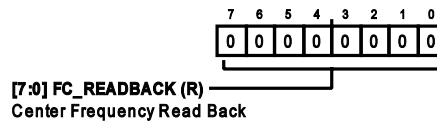


Table 27. Bit Descriptions for FC_READBACK

| Bits | Bit Name | Description | Reset | Access |
|-------|-------------|-----------------------------|-------|--------|
| [7:0] | FC_READBACK | Center Frequency Read Back. | 0x0 | R |

Address: 0x061, Reset: 0x00, Name: BW_READBACK

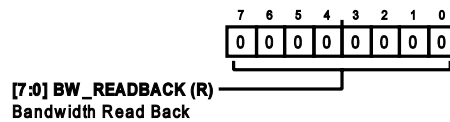


Table 28. Bit Descriptions for BW_READBACK

| Bits | Bit Name | Description | Reset | Access |
|-------|-------------|----------------------|-------|--------|
| [7:0] | BW_READBACK | Bandwidth Read Back. | 0x0 | R |

Address: 0x062, Reset: 0x00, Name: MATCH_READBACK

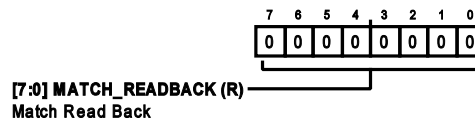
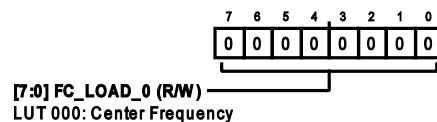


Table 29. Bit Descriptions for MATCH_READBACK

| Bits | Bit Name | Description | Reset | Access |
|-------|----------------|------------------|-------|--------|
| [7:0] | MATCH_READBACK | Match Read Back. | 0x0 | R |

Address: 0x100, Reset: 0x00, Name: LUT0_FC



REGISTER DETAILS

Table 30. Bit Descriptions for LUT0_FC

| Bits | Bit Name | Description | Reset | Access |
|-------|-----------|----------------------------|-------|--------|
| [7:0] | FC_LOAD_0 | LUT 000: Center Frequency. | 0x0 | R/W |

Address: 0x101, Reset: 0x00, Name: LUT0_BW

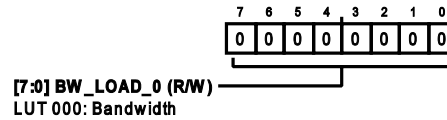


Table 31. Bit Descriptions for LUT0_BW

| Bits | Bit Name | Description | Reset | Access |
|-------|-----------|---------------------|-------|--------|
| [7:0] | BW_LOAD_0 | LUT 000: Bandwidth. | 0x0 | R/W |

Address: 0x102, Reset: 0x00, Name: LUT0_MATCH

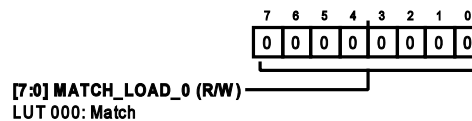


Table 32. Bit Descriptions for LUT0_MATCH

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|-----------------|-------|--------|
| [7:0] | MATCH_LOAD_0 | LUT 000: Match. | 0x0 | R/W |

Address: 0x103 to 0x15F, Reset: 0x00

The LUT1 to LUT31 bit field functionality (Register 0x103 through Register 0x15F) is similar to LUT0 (Register 0x100 through Register 0x102), see [Table 12](#) for the register address information.

Address: 0x300, Reset: 0xC0, Name: INTERP_FC_Y0

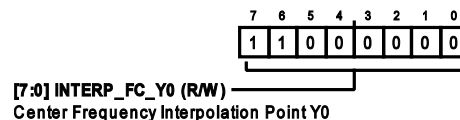


Table 33. Bit Descriptions for INTERP_FC_Y0

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y0 | Center Frequency Interpolation Point Y0. | 0xC0 | R/W |

Address: 0x301, Reset: 0xA1, Name: INTERP_FC_Y1

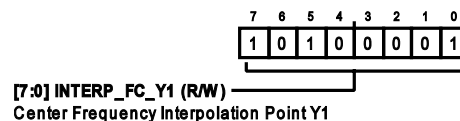


Table 34. Bit Descriptions for INTERP_FC_Y1

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y1 | Center Frequency Interpolation Point Y1. | 0xA1 | R/W |

REGISTER DETAILS

Address: 0x302, Reset: 0x88, Name: INTERP_FC_Y2

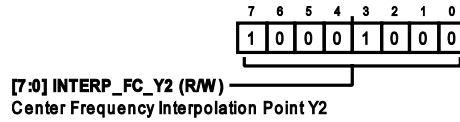


Table 35. Bit Descriptions for INTERP_FC_Y2

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y2 | Center Frequency Interpolation Point Y2. | 0x88 | R/W |

Address: 0x303, Reset: 0x64, Name: INTERP_FC_Y3

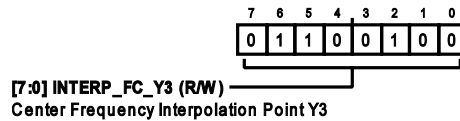


Table 36. Bit Descriptions for INTERP_FC_Y3

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y3 | Center Frequency Interpolation Point Y3. | 0x64 | R/W |

Address: 0x304, Reset: 0x4B, Name: INTERP_FC_Y4

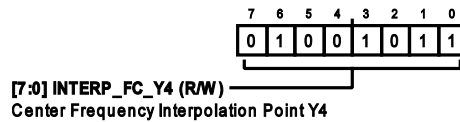


Table 37. Bit Descriptions for INTERP_FC_Y4

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y4 | Center Frequency Interpolation Point Y4. | 0x4B | R/W |

Address: 0x305, Reset: 0x3A, Name: INTERP_FC_Y5

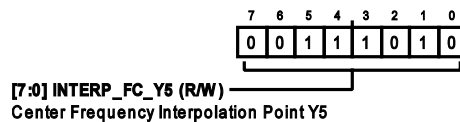


Table 38. Bit Descriptions for INTERP_FC_Y5

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y5 | Center Frequency Interpolation Point Y5. | 0x3A | R/W |

Address: 0x306, Reset: 0x2D, Name: INTERP_FC_Y6

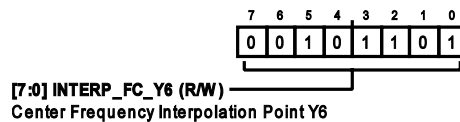


Table 39. Bit Descriptions for INTERP_FC_Y6

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y6 | Center Frequency Interpolation Point Y6. | 0x2D | R/W |

REGISTER DETAILS

Address: 0x307, Reset: 0x23, Name: INTERP_FC_Y7

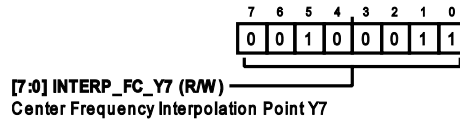


Table 40. Bit Descriptions for INTERP_FC_Y7

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y7 | Center Frequency Interpolation Point Y7. | 0x23 | R/W |

Address: 0x308, Reset: 0x1C, Name: INTERP_FC_Y8

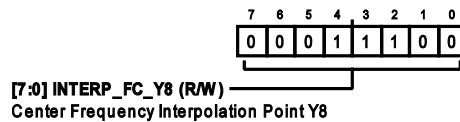


Table 41. Bit Descriptions for INTERP_FC_Y8

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y8 | Center Frequency Interpolation Point Y8. | 0x1C | R/W |

Address: 0x309, Reset: 0x16, Name: INTERP_FC_Y9

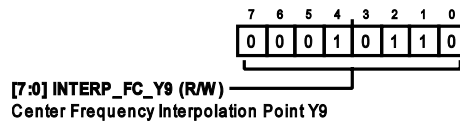


Table 42. Bit Descriptions for INTERP_FC_Y9

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|--|-------|--------|
| [7:0] | INTERP_FC_Y9 | Center Frequency Interpolation Point Y9. | 0x16 | R/W |

Address: 0x30A, Reset: 0x03, Name: INTERP_BW_V0

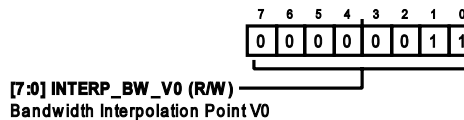
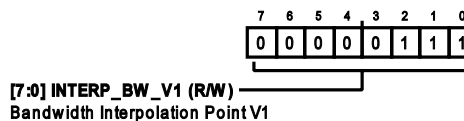


Table 43. Bit Descriptions for INTERP_BW_V0

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|-----------------------------------|-------|--------|
| [7:0] | INTERP_BW_V0 | Bandwidth Interpolation Point V0. | 0x3 | R/W |

Address: 0x30B, Reset: 0x07, Name: INTERP_BW_V1



REGISTER DETAILS

Table 44. Bit Descriptions for INTERP_BW_V1

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|-----------------------------------|-------|--------|
| [7:0] | INTERP_BW_V1 | Bandwidth Interpolation Point V1. | 0x7 | R/W |

Address: 0x30C, Reset: 0x21, Name: INTERP_BW_V2

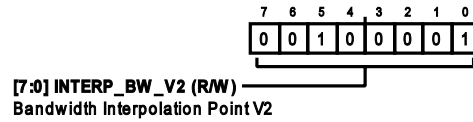


Table 45. Bit Descriptions for INTERP_BW_V2

| Bits | Bit Name | Description | Reset | Access |
|-------|--------------|-----------------------------------|-------|--------|
| [7:0] | INTERP_BW_V2 | Bandwidth Interpolation Point V2. | 0x21 | R/W |

Address: 0x30D, Reset: 0x09, Name: INTERP_MATCH_T0

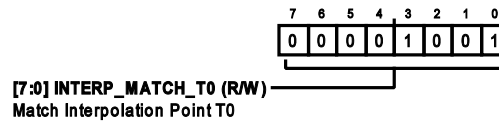


Table 46. Bit Descriptions for INTERP_MATCH_T0

| Bits | Bit Name | Description | Reset | Access |
|-------|-----------------|-------------------------------|-------|--------|
| [7:0] | INTERP_MATCH_T0 | Match Interpolation Point T0. | 0x9 | R/W |

Address: 0x30E, Reset: 0x22, Name: INTERP_MATCH_T1

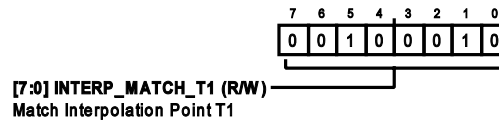


Table 47. Bit Descriptions for INTERP_MATCH_T1

| Bits | Bit Name | Description | Reset | Access |
|-------|-----------------|-------------------------------|-------|--------|
| [7:0] | INTERP_MATCH_T1 | Match Interpolation Point T1. | 0x22 | R/W |

Address: 0x30F, Reset: 0xAE, Name: INTERP_MATCH_T2

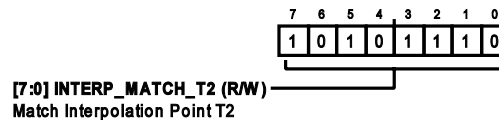


Table 48. Bit Descriptions for INTERP_MATCH_T2

| Bits | Bit Name | Description | Reset | Access |
|-------|-----------------|-------------------------------|-------|--------|
| [7:0] | INTERP_MATCH_T2 | Match Interpolation Point T2. | 0xAE | R/W |

OUTLINE DIMENSIONS

| Package Drawing (Option) | Package Type | Package Description |
|--------------------------|--------------|-----------------------------|
| CC-40-17 | LGA | 40-Terminal Land Grid Array |

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

Updated: April 01, 2024

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Packing Quantity | Package Option |
|--------------------|-------------------|-----------------------------------|------------------|----------------|
| ADMV8505ACCZ | -40°C to +85°C | 40-Terminal [LGA] (10 mm × 10 mm) | Reel, 300 | CC-40-17 |
| ADMV8505ACCZ-R7 | -40°C to +85°C | 40-Terminal [LGA] (10 mm × 10 mm) | Reel, 300 | CC-40-17 |

¹ Z = RoHS Compliant Part.

EVALUATION BOARDS

| Model ¹ | Description |
|--------------------|------------------|
| ADMV8505-EVALZ | Evaluation Board |

¹ Z = RoHS Compliant Part.