EDFA and CW Laser Controller

Preliminary Technical Data

ADN8820*

FEATURES

Four Operational Modes Including:
- **Constant Laser Current**
- **Constant Optical Output Power**
- **Constant EDFA Gain**
- **Constant Laser Power**

High Power Efficiency: >90%
Three Built-In Photodiode TIAs
Adjustable Laser Diode and EDFA Protection Limits
Free-run or Synchronous Switching Frequency Modes
Adjustable Phase Delay for Synchornous Clock Mode
Optional Dithering Built-In
Programmable Dither Frequency and Amplitude

APPLICATIONS

EDFA Pump Laser Diode Control
CW Laser Bias Control
Raman Amplifiers

GENERAL DESCRIPTION

The ADN8820 is a versatile Continuous Wave (CW) and EDFA laser diode driver and controller. It provides a low noise and precise current control for driving a source or pump laser diode.

It can be set to operate in one of four controller modes: Constant Current (CC), Constant Laser Power (CLP), Constant Output Power (COP), or Constant EDFA Gain (CG). Multiple pump laser applications are easily supported by the ADN8820. Common-cathode-to-ground and common-anode-to-VDD configurations are also supported.

The ADN8820 has a high speed closed-loop control, making it suitable for add/drop applications in telecommunication systems. It has a low-current shutdown mode and a soft-start feature to minimize power supply bounce on start-up.

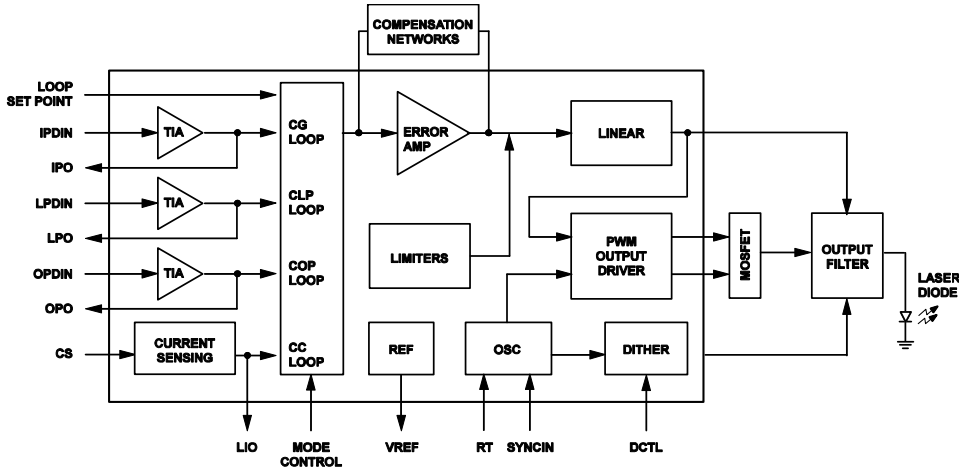
Protection circuitry is built into the device. The protection limits are easily adjustable and are used to set maximum output current and voltage, optical output power, EDFA gain, and pump or CW laser power.

The output stage consists of a high-efficiency PWM amplifier in parallel with a high-speed linear amplifier. This provides the fastest settling time response along with the lowest power and heat dissipation. A pair of external MOSFETs on the PWM amplifier provide output currents of up to 5A.

Three low-bias current TIAs are built-in. These allow amplification for the laser back-facet photodiode and EDFA input and output photodiodes. For CW laser applications, the two unused TIAs can be used for etalon photodiode amplification, allowing continuous wavelength monitoring.

The ADN8820 is available in a 7 x 7 mm lead-frame chip scale package (LFCSP) with a package height of less than 1 mm.

FUNCTIONAL BLOCK DIAGRAM



* U.S. Patent Pending

Rev. PrB

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Table 1. ADN8820—Electrical Characteristics (AVDD = PVDD = 5V, AGND = PGND = 0V, T_A = 25°C, using typical circuit in Figure 1, unless otherwise noted.)[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
TRANSIMPEDANCE AMPLIFIERS						
Detection Range	I_{IP}	From IPDIN Photodiode	0.005		5,000	μA
	I_{OP}	From OPDIN Photodiode	0.005		5,000	μA
	I_{LP}	From LPDIN Photodiode	5		5,000	μA
Input Bias Current	IB_{IPDIN}	IPDIN, OPDIN, LPDIN Amplifier		100		pA
	IB_{OPDIN}	Inputs		100		pA
	IB_{LPDIN}			100		pA
Input Voltage Range	VBLP, VB		0		VDD	V
Monitor Output Range	V_{IPO}	IPO, LPO, OPO Outputs	0		VDD	V
	V_{LPO}		0		VDD	V
	V_{OPO}		0		VDD	V
Input Offset Voltage	V_{OSIP}	IPDIN, OPDIN, LPDIN Amplifiers		10		μV
	V_{OSOP}			10		μV
	V_{OSLP}			2		mV
Maximum Output Current	I_{OUTIPO}	IPO, LPO, OPO Outputs		±10		mA
	I_{OUTLPO}			±10		mA
	I_{OUTOPO}			±10		mA
Gain-Bandwidth Product	GBW_{IP}	IPDIN, OPDIN, LPDIN Amplifiers		10		MHz
	GBW_{OP}			10		MHz
	GBW_{LP}			1		MHz
LIMIT CONTROLS						
Input Voltage Range	V_{INLIM}	IPMIN, OPLIM, LPLIM, ILIM, and VLIM	0		2.6	V
Limiter Accuracy	V_{OSLIM}	OPLIM, LPLIM, ILIM, IPMIN			±10	mV
Open Circuit Voltage	V_{LIMNC}	Voltage for OPLIM, LPLIM, and ILIM with no connection	2.5	2.6	2.7	V
Pull-up Current	IB_{LIM}	Flowing out of OPLIM, LPLIM, and ILIM with LIM Voltage <2.0V		500		nA
IPMIN Disable Threshold	$V_{IPMINLO}$	V_{IPO} = 0V		200		mV
VLIM Input Bias Current	I_{VLIM}	Flowing into VLIM pin			1	μA
VLIM Voltage Control Accuracy		$\lvert V_{LINOUT} - VLIM \rvert$			50	mV
ERROR AMPLIFIER						
Input Offset Voltage	V_{OSEA}			10	25	μV
Input Common-Mode Voltage Range	V_{CMEA}		0		VDD	V
Output Voltage Swing	V_{OUTEA}		0		VDD	V
Maximum Output Current	I_{MAXEA}			±10		mA
Gain-Bandwidth	GBW_{EA}			10		MHz
SET INPUT						
Input Voltage Range	V_{SET}		0		VDD	V
Input Bias Current	IB_{SET}			±1		μA
MULTIPLEXERS						
Ouput Impedance				100		Ω
Output Voltage Range			0		VDD	V

[1] Specifications subject to change without notice
[2] Capital letters denote pin names.

Table 1. ADN8820—Electrical Characteristics (AVDD = PVDD = 5V, AGND = PGND = 0V, T_A = 25°C, using typical circuit in Figure 1, unless otherwise noted.)[2]

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
LINEAR OUTPUT						
Short-Circuit Output Current	I_{OUTLIN}		300			mA
Output Voltage Compliance	V_{LINMAX}	I_{OUTLIN} = 300mA (sourcing)	4.5			V
	V_{LINMIN}	I_{OUTLIN} = -160mA (sinking)			0.5	V
Power Supply Rejection Ratio	$PSRR_{LIN}$			68		dB
Gain-Bandwidth Product	GBW_{LIN}			10		MHz
PWM OUTPUT						
Offset Voltage	V_{OSPWM}	V_{OSPWM} = LINOUT - FB			±10	mV
Non-Overlap Delay						
Output Transistion Time	t_R, t_F	FET $C_{ISS} \leq$ 3nF		40		ns
Output Driver Resistance	R_{NGATE}			6		Ω
	R_{PGATE}			6		Ω
Output Current Ripple		I_{OUT} = 300mA, V_{OUT} = 2V		1		%
Soft-Start Time		C_{SS} = 0.1 μF		15		ms
Standby Mode Threshold	V_{SSSB}	PWM and LINOUT disabled			0.4	V
OSCILLATOR						
Free-Run Oscillation Frequency	f_{CLK}	CMPOSC = VDD; SYNCIN = 0V	100		1,000	kHz
Synchornization Capture Range		SYNCIN driven with external clock	100		1,000	kHz
Phase Adjustment	ϕ_{CLK}		45		315	degrees
CURRENT SENSE AMPLIFIER						
Input Common-Mode Voltage Range	V_{CMCS}		0		VDD	V
Input Resistance	R_{INCS}			10.5		kΩ
Output Offset Voltage	V_{OSLIO}	$V_{CSP} = V_{CSN}$ = 2.5V		1		mV
Gain	A_{VCS}	$V_{LIO} / (V_{CSP} - V_{CSN})$		20		V/V
Output Voltage Range	V_{LIO}		0		VDD	V
DITHER GENERATOR						
Frequency Range	f_{DITHER}	xx kΩ ≤ RT ≤ xx kΩ	0.2		2	MHz
Frequency Multiplier Programming Voltage		See Table II				
Dither Current Control Votlage	V_{DCTL}	V_{LIO} = 2.5 V	1.2	1.25	1.3	V
Programming Current Range	I_{DCTL}	V_{LIO} = 2.5 V	0		100	μA
Maximum DO Output Current	I_{MAXDO}		±19	±20	±21	mA
DO Output Voltage	V_{DO}			1.5		V
POWER SUPPLY						
Power Supply Range	V_{DD}		3.0		5.5	V
Supply Current	I_{SY}	DSEL/$\overline{SD}$ ≥ 0.8V; I_{OUT} = 0A		25	30	mA
		-40°C ≤ T_A ≤ +85°C				
Shutdown Current	I_{SD}	DSEL/$\overline{SD}$ ≤ 0.2V		10		μA
Standby Current	I_{SB}	SS/$\overline{SB}$ ≤ 0.2V		2.5		mA
Undervoltage Lockout	V_{UVLO}			2.4	2.5	V
REFERNCE OUTPUT						
Reference Voltage	V_{REF}	$I_{REF} \leq$ 2 mA	2.4	2.5	2.6	V
Power Supply Rejection Ratio	$PSRR_{REF}$	With respct to AVDD		68		V

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Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DUAL OUTPUT						
Output Voltage Range	V_{DUAL}	$I_{DUAL} \leq 500\ \mu A$	0.4		VDD-0.4	V
Voltage Gain	A_{VDUAL}	A_{VDUAL} = DUAL / LIO; V_{ILIM} = 2.25V with 1.9 V ≤ V_{LIO} ≤ 2.1V		20		V/V
CONTROL LOOP STATUS OUTPUT						
CLGD High	V_{CLGDHI}	0.05 x VDD ≤ V_{EAOUT} ≤ 0.95 x VDD	4.8			V
CLGD Low	V_{CLGDLO}	Otherwise			0.2	V
LOGIC CONTROL						
Logic Low Input Threshold	V_{IL}	MODE0, MODE1, SYNCIN			0.2	V
Logic High Input Threshold	V_{IH}	MODE0, MODE1, SYNCIN	VDD-0.2			V
Logic Low Output Level	V_{OL}				0.2	V
Logic High Output Level	V_{OH}		VDD-0.2			V
Input Current					±1	μA

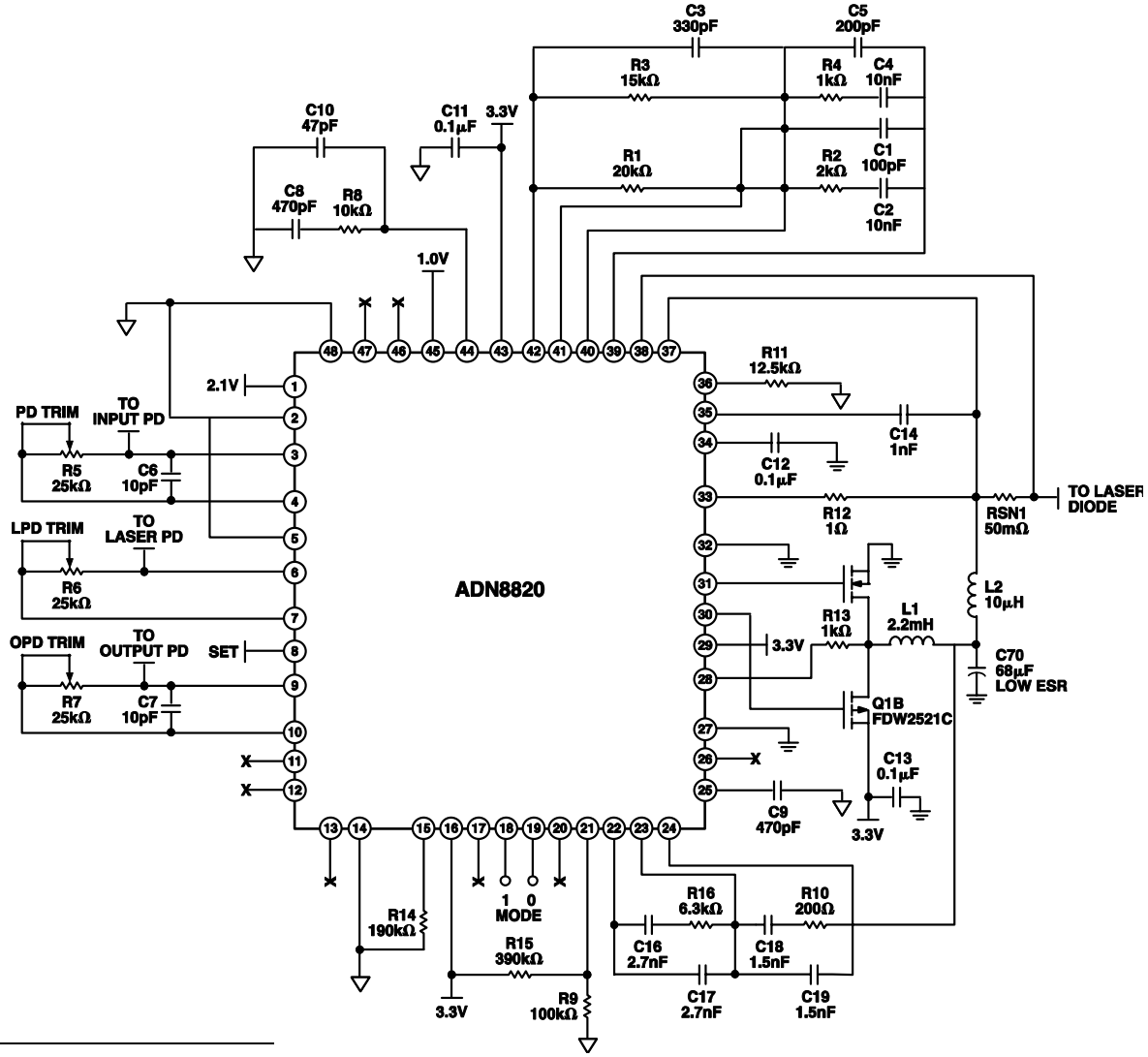


Figure 1. Typical Application Circuit

[1] Specifications subject to change without notice
[2] Capital letters denote pin names.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings (at 25°C, unless otherwise noted)

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–40°C to +85°C
Junction Temperature Range: CP Packages	–65°C to +150°C
Lead Temperature Range (Soldering, 60 Sec)	300°C

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
LFSCP-48 (CP-48)	32	12	°C/W

[1] θ_{JA} is specified for the worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface mount packages.

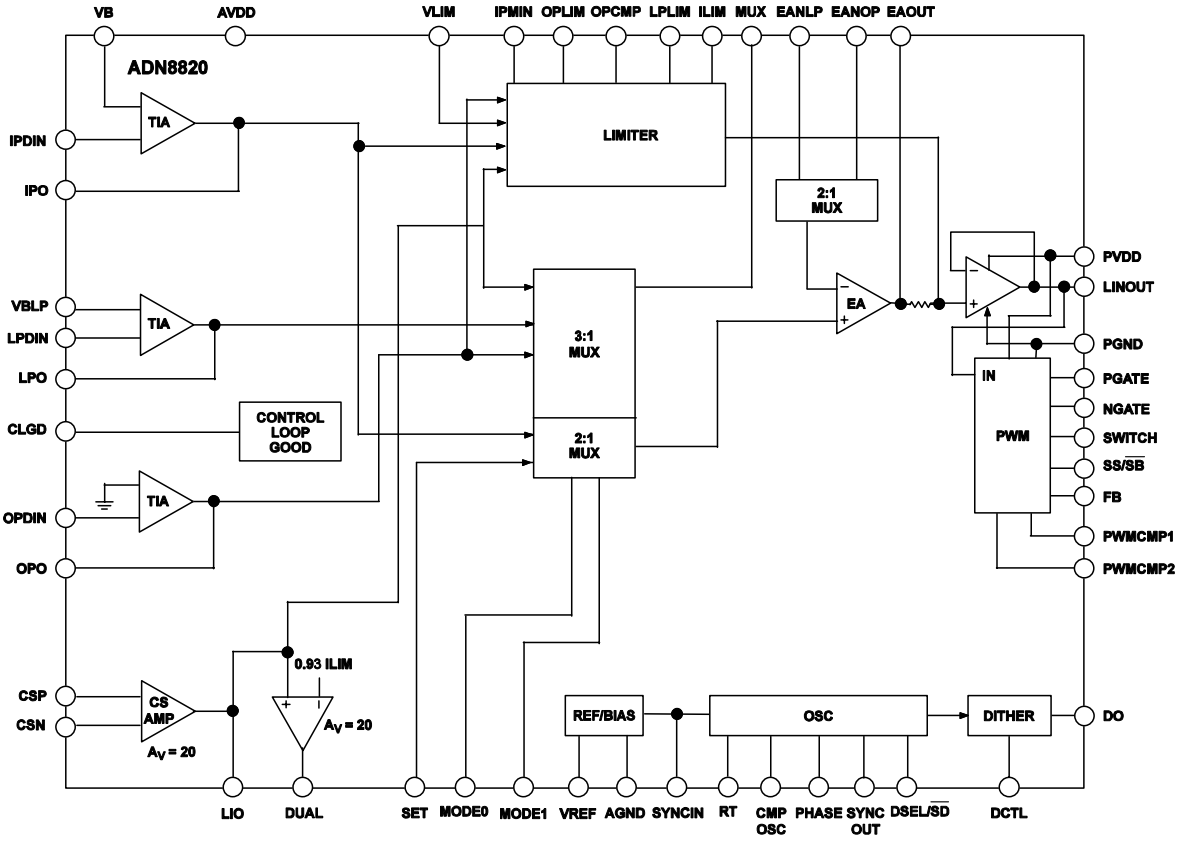
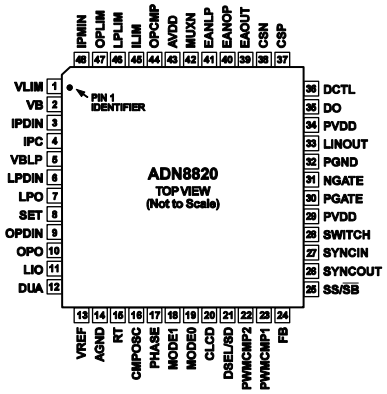


Figure 2. System Block Diagram

PIN CONFIGURATION



PIN FUNCTIONS

Name	Pin	Function	Connections
AMPLIFIER INPUTS			
IPDIN	3	Input to TIA for EDFA input photodiode	EDFA input photodiode and feedback resistor
LPDIN	6	Input to TIA for laser photodiode	Laser photodiode and feedback resistor
OPDIN	9	Input to TIA for EDFA output photodiode	EDFA output photodiode and feedback resistor
VB	2	Bias voltage for EDFA input and output photodiodes	External bias voltage required
VBLP	5	Bias voltage for laser photodiode	External bias voltage required
CSP	37	Non-inverting input of current sense amplifier	High-side of laser current sense resistor (50 mΩ typ.)
CSN	38	Inverting input of current sense amplifier	Low-side of laser current sense resistor (50 mΩ typ.)
LIMIT INPUTS			
VLIM	1	Laser diode voltage will not exceed VLIM	External voltage required
ILIM	45	Limits output voltage if LIO > ILIM	External voltage or no connection (defaults to 2.5 V)
OPLIM	47	Limits output voltage if OPO > OPLIM	External voltage or no connection (defaults to 2.5 V)
LPLIM	46	Limits output voltage if LPO > LPLIM	External voltage or no connection (defaults to 2.5 V)
IPMIN	48	Limits output voltage if IPO is lower than IPMIN	External voltage required
ERROR (COMPENSATION) AMPLIFIER (EA)			
EANLP	41	Compensation network for laser diode loop	Internally connects inverting input of EA to laser diode compensation network
EANOP	40	Compensation network for EDFA loop	Internally connects inverting input of EA to EDFA compensation network
EAOUT	39	Output of compensation amplifier	Internal connection to linear output amplifier
MUX	42	Allows separate compensation for EDFA and laser diode	Connects to two external compensation networks: one for EDFA loop, one for laser diode loop
OPCMP	44	Compensation for limiter section	R-C network to ground
SET	8	Sets output power or current based on MODE settings	External voltage or DAC
POWER OUTPUT AMPLIFIERS			
LINOUT	33	Linear amplifier output	Laser diode through 1 Ω series resistor
PGATE	30	PWM switching for PMOS	Gate of external PMOS for PWM output
NGATE	31	PWM switching for NMOS	Gate of external NMOS for PWM output
SWITCH	28	PWM amplifier output	Drains of external NMOS, PMOS, and input of L-C filter
FB	24	Feedback input for PWM amplifier	Output of L-C filter and laser diode
PWMCMP1	23	Compensation for PWM amplifier	Series R-C networks to FB and PWMCMP2
PWMCMP2	22	Compensation for PWM amplifier	Series R-C to PWMCMP1
SS/$\overline{SB}$	25	Constant current charges external capacitor to soft-start PWM output from 0% duty cycle	Optional external FET can pull down and to engage standby mode
OUTPUT MONITOR VOLTAGES			
IPO	4	Output of EDFA input photodiode TIA	Feedback resistor to IPDIN
OPO	10	Output of EDFA output photodiode TIA	Feedback resistor to OPDIN
LPO	7	Output of laser diode photodiode TIA	Feedback resistor to LPDIN
LIO	11	Output of current sense amplifier	
DUAL	12	Compares LIO to 90% of ILIM	To SET pin of additional ADN8820 device in multi-pump optical amplifier applications
EAOUT	39	Output of compesnation amplifier	Internal connection to linear output amplifier
OSCILLATOR SECTION			
SYNCIN	27	Optional clock input signal for PLL	Ground or external clock
SYNCOUT	26	Follows rising edge of SYNCIN plus phase shift	Optional connection to SYNCIN of additional ADN8820 device
CMPOSC	16	Compensation for synchronizing PLL	R-C network to ground
PHASE	17	Sets rising edge phase shift of SYNCOUT	External voltage or no connection (default is 0.7V)
RT	15	Sets PWM clock frequency	Resistor (R_T) to ground

Name	Pin	Function	Connections
DITHER GENERATOR			
DSEL/$\overline{SD}$	21	4-level logic input to set dither frequency or engage shutdown	External voltage
DCTL	36	Sets dither current as a percentage of the laser diode current	Resistor (R_{DCTL}) to ground
DO	35	Optional dither AC current to laser diode	To laser diode through 1 nF series capacitor
LOGIC INPUTS			
MODE1	18	Sets control loop mode (see Table I)	External logic voltage
MODE0	19	Sets control loop mode (see Table I)	External logic voltage
DSEL/$\overline{SD}$	21	Pulling voltage low engages shutdown	External voltage
SS/$\overline{SB}$	25	Pulling voltage low engages standby	470 pF soft-start capacitor to ground; optional external FET can pull down to engage standby
LOGIC OUTPUTS			
CLGD	20	Logic high if EAOUT is within 5% to 95% of AVDD; Logic low otherwise	
POWER			
PVDD	29, 34	Power for output amplifiers and digital sections	3.0 V to 5.5 V
AVDD	43	Low noise power for TIAs, limiter section, and EA	3.0 V to 5.5 V
PGND	32	Current return for output amplifiers	0 V
AGND	14	Low noise ground	0 V
VREF	13	2.5 V reference voltage	Can be used as refernce for VB, VBLP, SET, and limiter inputs

TABLE 4. MODE CONTROL LOGIC

MODE Inputs			Error Amplifier		MUX	
MODE1	MODE0	Mode Setting	-Input	+Input	Output	Description
0	0	Constant Current	EANLP	SET	LIO	Maintains a fixed current through laser diode; generally used for calibration.
0	1	Constant Laser Power	EANLP	SET	LPO	Maintains a constant optical output power from laser diode.
1	0	Constant Ouptut Power	EANOP	SET	OPO	Maintains a constant optical power at output of EDFA.
1	1	Constant Gain	EANOP	IPO	OPO	Monitors both input and output optical power to maintain constant gain from optical amplifier.

TABLE 5. PWM CLOCK FREQUENCY SELECTION LEVELS

DSEL/$\overline{SD}$ (V)			PWM Clock Frequency
Min	Max	Mode	Division
0	0.5	Shutdown	N/A
0.7	1.2	Active	f_{DITHER} ÷2
1.3	1.8	Active	f_{DITHER} ÷4
2.0	VDD	Active	f_{DITHER} ÷8

Note: f_{DITHER} is the ADN8820 dither frequency and is set by a resistor connected from RT to ground.

OUTLINE DIMENSIONS

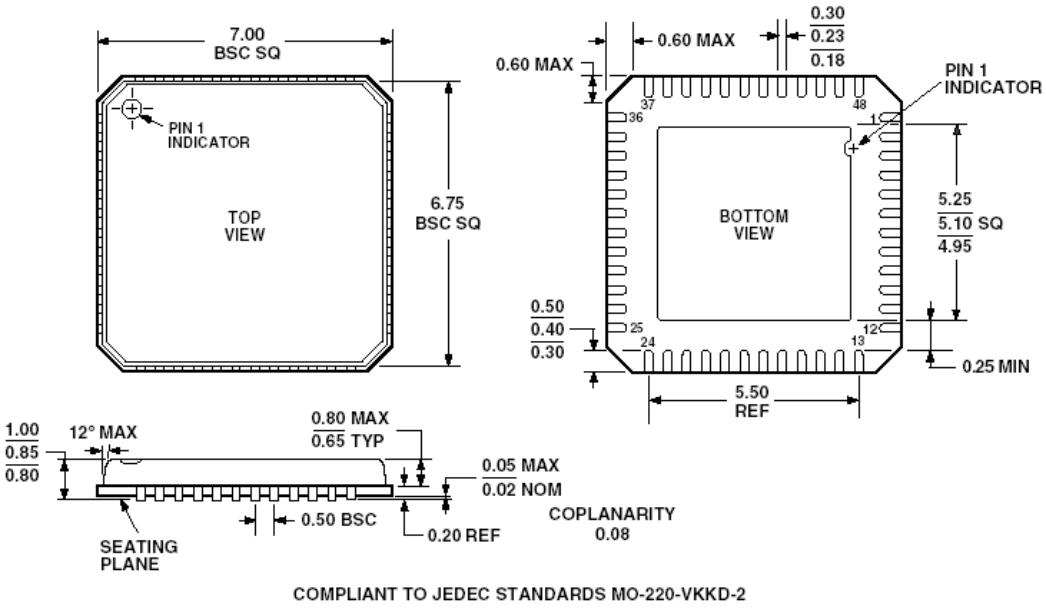


Figure 3. 48-Lead Frame (LFCSP-48) Chip Scale Package

7 x 7 mm Body
(CP-48)
Dimensions Shown in Millimeters

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these products feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Table 6. ADN8820 Ordering Guide

Product	Package Description	Package Option	Top Mark	No. of Parts per Reel	Temperature Range (°C)
ADN8820	48-Lead LFCSP	CP-48	TBD	N/A	–40 to +125
ADN8820-REEL7	48-Lead LFCSP	CP-48	TBD	TBD	–40 to +125
ADN8820-EVAL	Eval board	N/A	N/A	N/A	–40 to +125