ADNB-3552
Low Power LED Integrated Slim Mouse Sensor

AVAGO TECHNOLOGIES

Data Sheet

Description

The ADNB-3552 LED mouse bundle is a small form factor (SFF) LED illuminated navigation system. The bundle consists of an integrated chip-on-board (COB) LED mouse sensor ADNS-3550 and a SFF lens ADNS-3150-001.

The ADNS-3550 is a low-power optical navigation sensor. It has a new, low-power architecture and automatic power management modes, making it ideal for battery- and power-sensitive applications such as cordless input devices.

The ADNS-3550 is capable of high-speed motion detection — up to 20 ips and 8 G. In addition, it has an on-chip oscillator and integrated LED to minimize external components.

The ADNS-3550, along with the ADNS-3150-001 lens, form a complete and compact mouse tracking system. There are no moving parts which means high reliability and less maintenance for the end user. In addition, precision optical alignment is not required, facilitating high volume assembly.

The bundle sensor is programmed via registers through a four-wire serial port. It is packaged in a 16 I/O surface mountable package.

Theory of Operation

The ADNS-3550 is based on Optical Navigation Technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement.

The ADNS-3550 contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port.

The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values.

An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

Features

- Low power architecture
- Small form factor
- Surface mount technology (SMT) device
- Self-adjusting power-saving modes for longest battery life
- High speed motion detection up to 20 ips and 8 G
- Self-adjusting frame rate for optimum performance
- Motion detect pin output
- Internal oscillator — no clock input needed
- Selectable 500 and 1000 cpi resolution
- Wide operating voltage: 2.7 V - 3.6 V nominal
- Four wire serial port
- Minimal number of passive components
- Integrated chip-on-board LED

Applications

- Optical mice
- Optical trackballs
- Integrated input devices
- Battery-powered input device

Bundle Part Number	Part Number	Description
ADNB-3552	ADNS-3550	Integrated sensor
	ANDS-3150-001	Small form factor lens

Pinout of ADNS-3550 Optical Mouse Sensor

Pin	Name	Description
1	MISO	Serial Data Output (Master In/Slave Out)
2	SCLK	Serial Clock Input
3	MOSI	Serial Data Input (Master Out/Slave In)
4	MOTION	Motion Detect (Active Low Output)
5	XY_LED	LED Control
6	LED_GND	Ground for LED Current
7	SHTDWN	Shutdown (Active High Input)
8	LED (+)	LED Positive Terminal
9	LED (-)	LED Negative Terminal
10	AVDD	Analog Supply Voltage
11	GND	Ground
12	GND	Ground
13	AGND	Analog Ground
14	VDD	Supply Voltage
15	GND	Ground
16	NCS	Chip Select (Active Low Input)

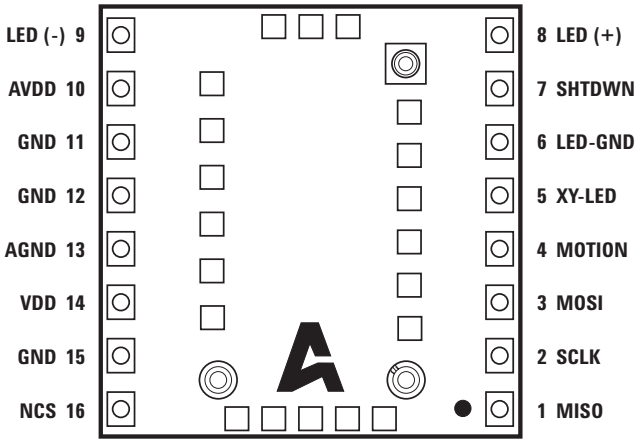


Figure 1a. Package outline drawing (top view)

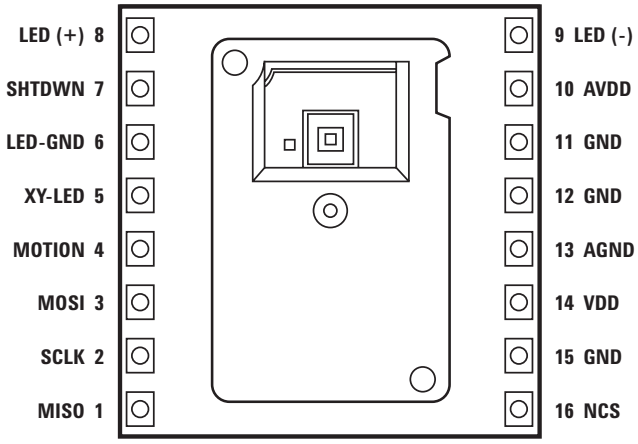


Figure 1b. Package outline drawing (bottom view)

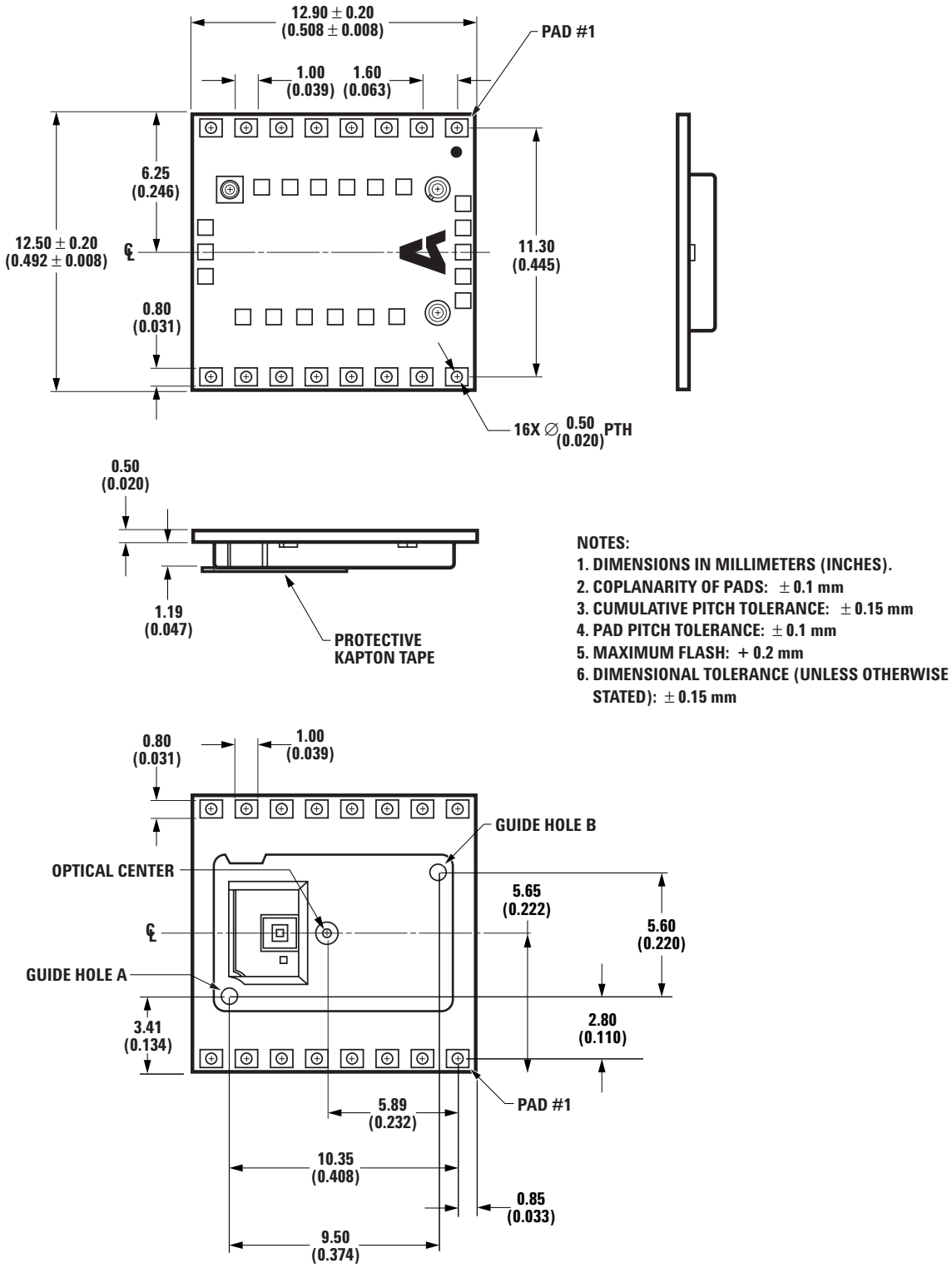


Figure 2. Package outline drawing

Caution: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Overview of Optical Mouse Sensor Assembly

Avago Technologies provides an IGES file drawing describing the base plate molding features for lens and PCB alignment.

The components interlock as they are mounted onto defined features on the base plate.

The ADNS-3550 sensor is designed for surface mounting on a PCB, looking down. There is an aperture stop and features on the package that align to the lens.

The ADNS-3150-001 lens provides optics for the imaging of the surface as well as illumination of the surface at the optimum angle. Features on the lens align it to the sensor and base plate.

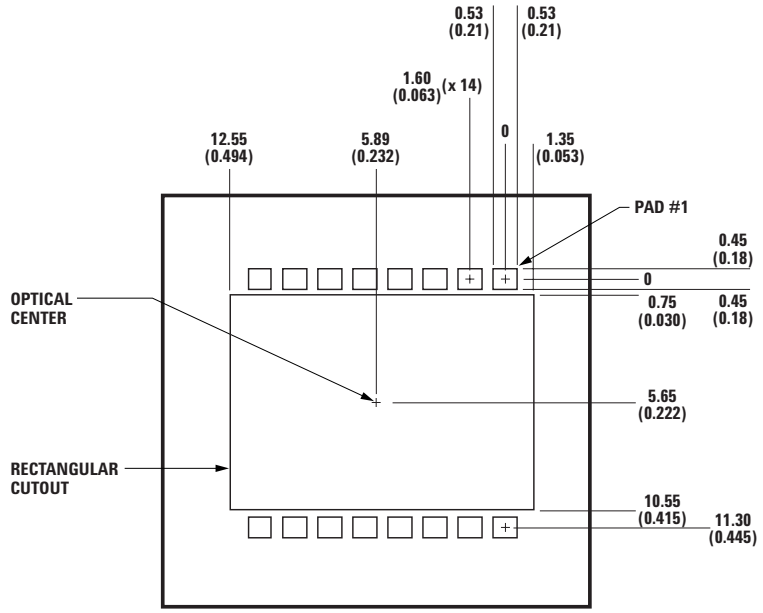


Figure 3. Recommended customer PCB PADOUT and spacing

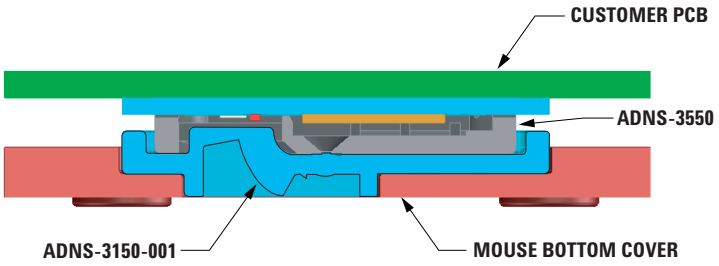


Figure 4a. 2D assembly drawing of ADNB-3552 (mounted on the bottom side of customer PCB)

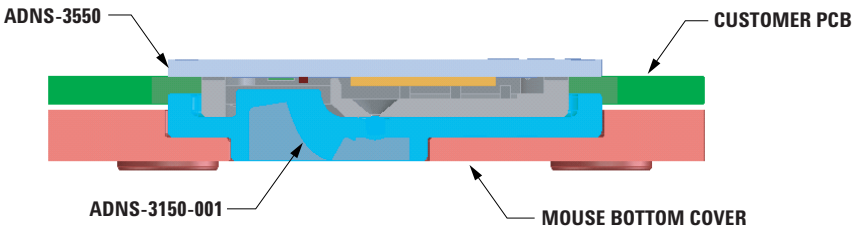


Figure 4b. 2D assembly drawing of ADNB-3552 (mounted on the top side of customer PCB)

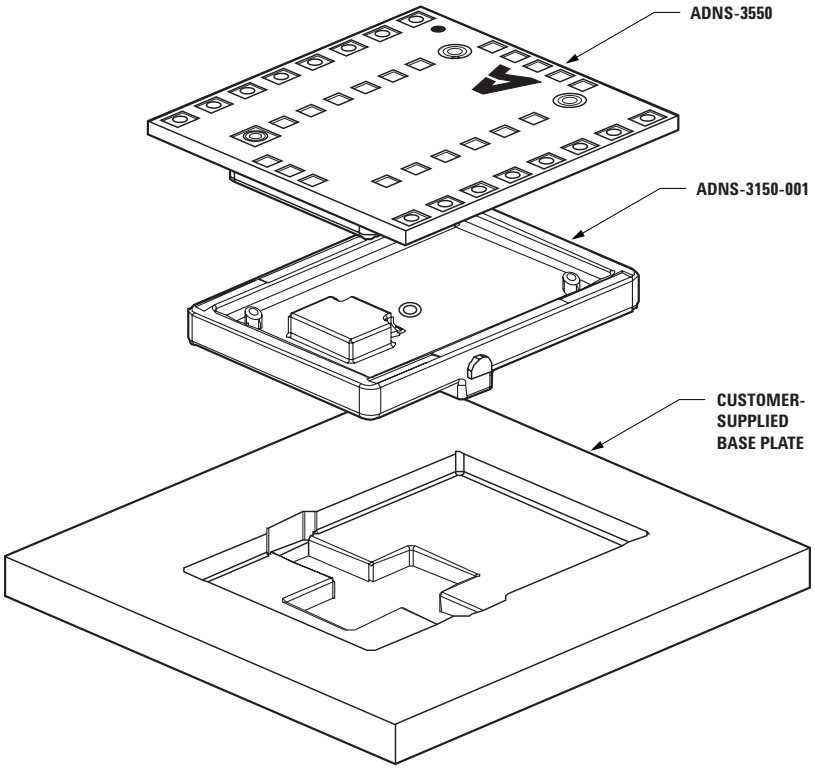


Figure 5a. Exploded top view

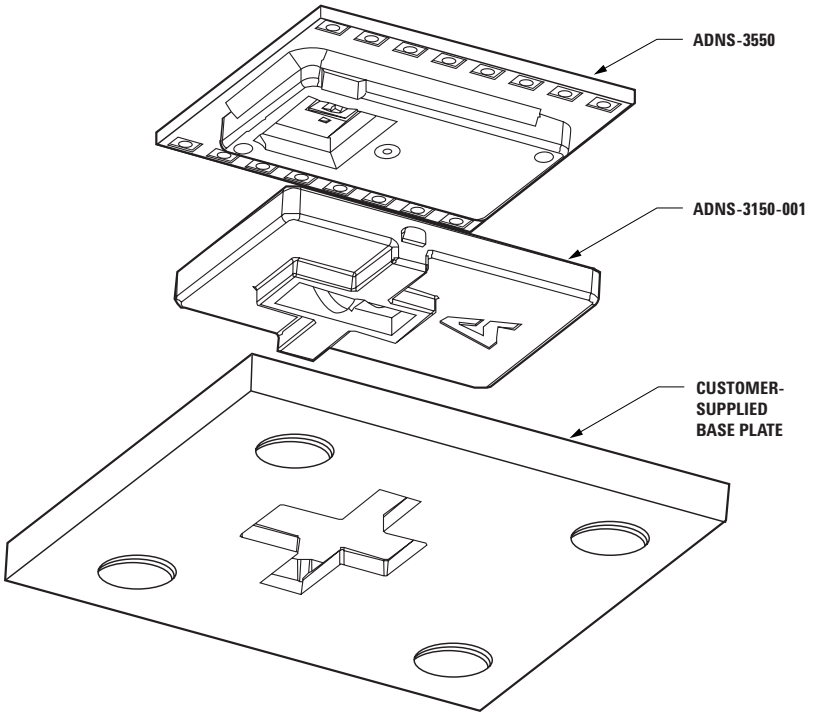


Figure 5b. Exploded bottom view

PCB Assembly Considerations

1. Surface mount the sensor and all other electrical components into PCB.
2. Reflow the entire assembly in a no-wash solder process.
3. Place the lens onto the base plate. Care must be taken to avoid contaminating or staining the lens.
4. Remove the protective kapton tape from optical aperture of the sensor and LED. Care must be taken to keep contaminants from entering the aperture. Recommend not to place the PCB facing up during the entire mouse assembly process. Recommend to hold the PCB first vertically for the kapton removal process.
5. Insert PCB assembly over the lens onto the base plate aligning post to retain PCB assembly. The lens piece has alignment posts which will mate with the alignment holes on the sensor aperture.
6. The optical position reference for the PCB is set by the base plate and lens. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
7. Install mouse top case. There MUST be a feature in the top case to press down onto the sensor to ensure the sensor and lens components are interlocked to the correct vertical height.

Design Considerations for Improved ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the Avago Technologies supplied IGES file and ADNS-3150-001 lens.

Typical Distance	Millimeters
Creepage	0.6
Clearance	2.76

Note that the lens material is polycarbonate and therefore, cyanoacrylate-based adhesives or other adhesives that may damage the lens should NOT be used.

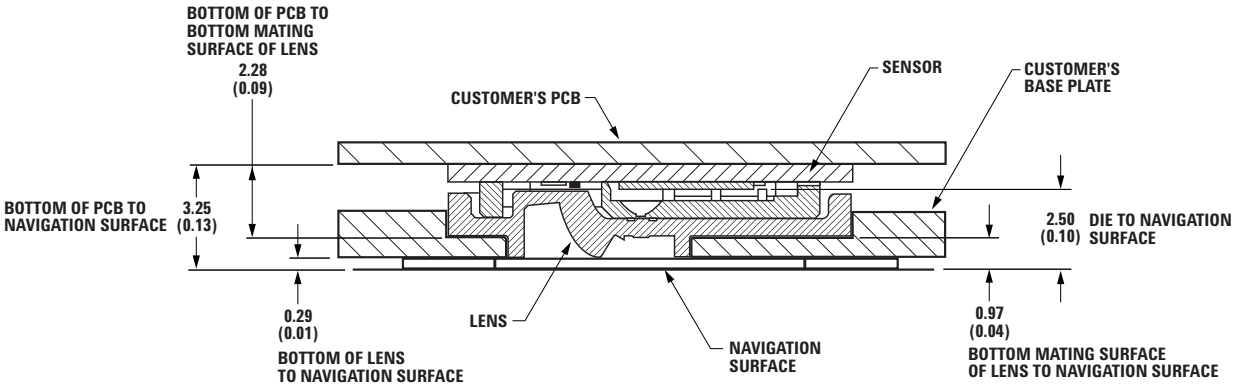


Figure 6a. Sectional view of PCB assembly (bottom mount)

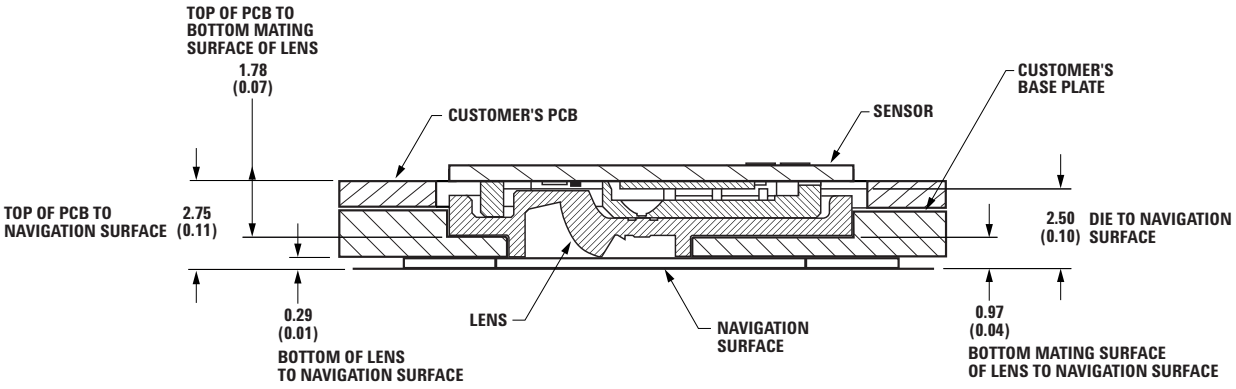


Figure 6b. Sectional view of PCB assembly (top mount)

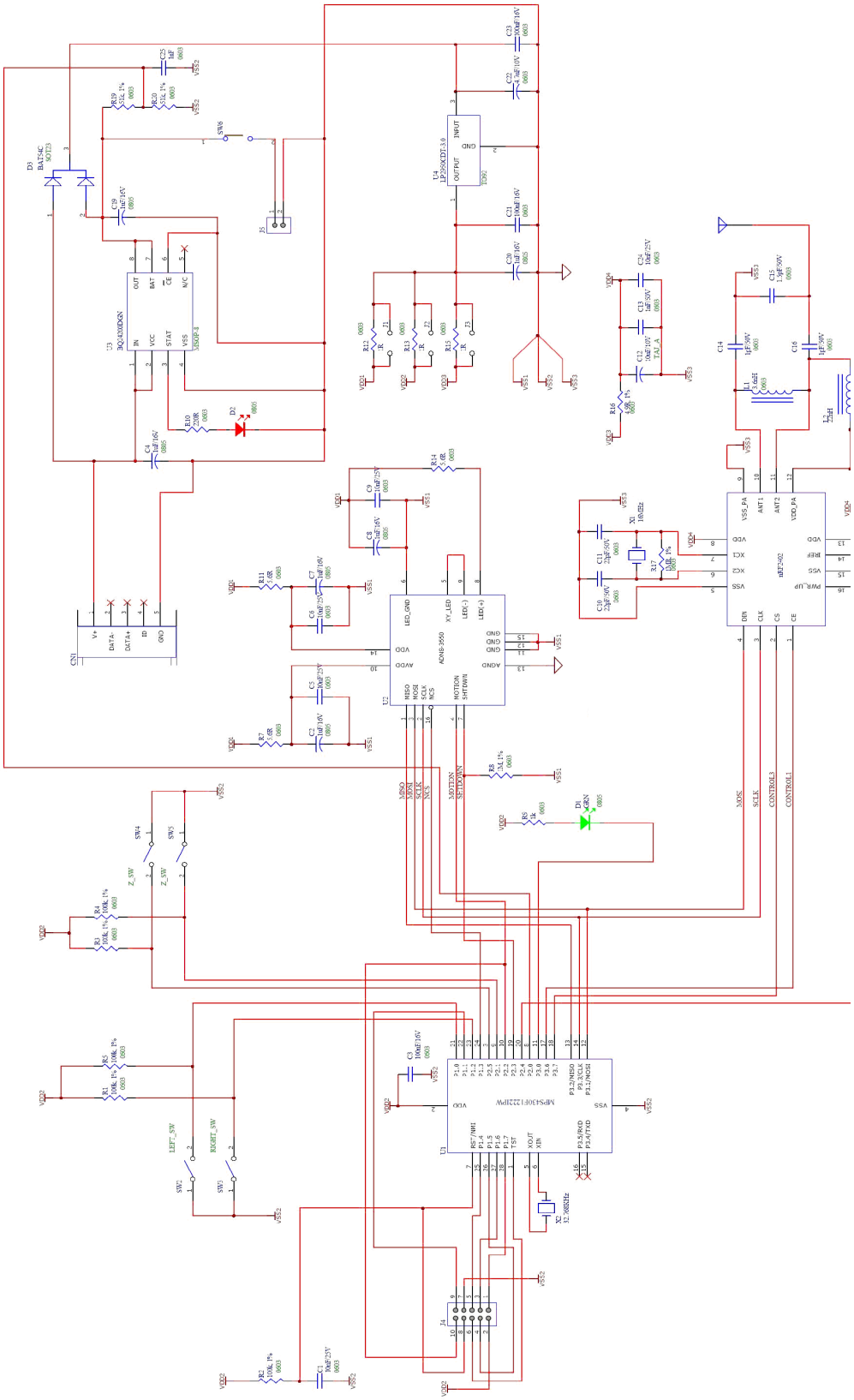


Figure 7. Schematic diagram for interface between ADNS-3550 and microcontroller

Note: The supply and ground paths should be laid out using a star topology.

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following Avago Technologies recommendations.
- UL flammability level UL94 V-0.

Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_S	-40	85	°C	
Lead Solder Temperature			260	°C	For 10 seconds, 1.6 mm below seating plane
Supply Voltage	V_{DD}	-0.5	3.7	V	
ESD (Sensor Only)			2	kV	All pins, human body model MIL 883 Method 3015
Input Voltage	V_{IN}	-0.5	V_{DD} + 0.5	V	All pins
Latchup Current	Iout		20	mA	All pins

Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Operating Temperature	T_A	0		40	°C	
Power Supply Voltage	V_{DD}	2.7		3.6	volts	Including noise
Power Supply Rise Time	V_{RT}	0.001		100	ms	0 to 2.8 V
Supply Noise (Sinusoidal)	V_{NA}			100	mVp-p	10 kHz - 50 MHz
Serial Port Clock Frequency	f_{SCLK}			1	MHz	Active drive, 50% duty cycle
Distance from Lens Reference Plane to Surface	Z	-0.1	0.97	+0.1	mm	Result in 0.1 mm DOF
Speed	S			20	in/sec	
Acceleration	A			8	G	

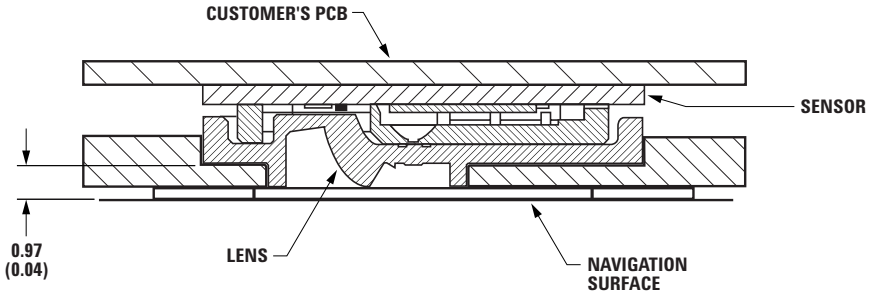


Figure 8a. Distance from lens reference plane to surface (bottom mount)

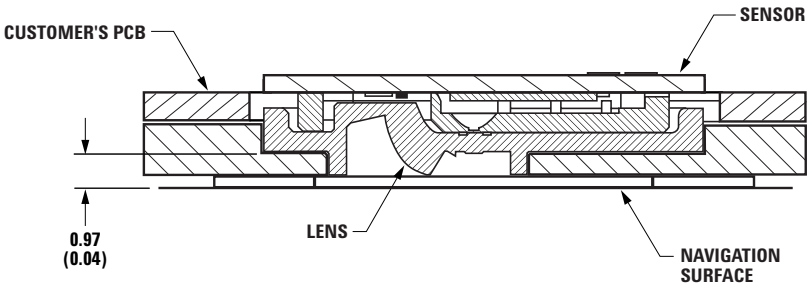


Figure 8b. Distance from lens reference plane to surface (top mount)

AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD3} = 2.85 V.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
Motion Delay After Reset	$t_{MOT-RST}$			23	ms	From POWER_UP_RESET register write to valid motion, assuming motion is present
Shutdown	t_{SHTDWN}			50	ms	From SHTDWN pin active to low current
Wake from Shutdown	t_{WAKEUP}	1			s	From SHTDWN pin inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown and Forced Rest," also note $t_{MOT-RST}$
Forced Rest Enable	$t_{REST-EN}$			1	s	From RESTEN bits set to low current
Wake from Forced Rest	$t_{REST-DIS}$			1	s	From RESTEN bits cleared to valid motion
MISO Rise Time	t_{r-MISO}		150	300	ns	C_L = 100 pF
MISO Fall Time	t_{f-MISO}		150	300	ns	C_L = 100 pF
MISO Delay After SCLK	$t_{DLY-MISO}$			120	ns	From SCLK falling edge to MISO data valid, no load conditions
MISO Hold Time	$t_{hold-MISO}$	0.5		$1/f_{SCLK}$	µs	Data held until next falling SCLK edge
MOSI Hold Time	$t_{hold-MOSI}$	200			ns	Amount of time data is valid after SCLK rising edge
MOSI Setup Time	$t_{setup-MOSI}$	120			ns	From data valid to SCLK rising edge
SPI Time Between Write Commands	t_{SWW}	30			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte
SPI Time Between Write and Read Commands	t_{SWR}	20			µs	From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte
SPI Time Between Read and Subsequent Commands	t_{SRW} t_{SRR}	500			ns	From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command
SPI Read Address-Data Delay	t_{SRAD}	4			µs	From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read
NCS Inactive After Motion Burst	t_{BEXIT}	500			ns	Minimum NCS inactive time after motion burst before next SPI usage
NCS to SCLK Active	$t_{NCS-SCLK}$	120			ns	From NCS falling edge to first SCLK rising edge
SCLK to NCS Inactive (for Read Operation)	$t_{SCLK-NCS}$	120			ns	From last SCLK rising edge to NCS rising edge, for valid MISO data transfer
SCLK to NCS Inactive (for Write Operation)	$t_{SCLK-NCS}$	20			µs	From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer
NCS to MISO High-Z	$t_{NCS-MISO}$			500	ns	From NCS rising edge to MISO high-Z state
MOTION Rise Time	$t_{r-MOTION}$		150	300	ns	C_L = 100 pF
MOTION Fall Time	$t_{f-MOTION}$		150	300	ns	C_L = 100 pF
SHTDWN Pulse Width	$t_{P-SHTDWN}$	1			s	
Transient Supply Current	I_{DDT}			45	mA	Max supply current during a V_{DD} ramp from 0 to 2.8 V

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. Typical values at 25°C, V_{DD} = 2.85 V.

Parameter	Symbol	Min.	Typical	Max.	Units	Notes
DC Supply Current in Various Modes	I_{DD_RUN} I_{DD_REST1} I_{DD_REST2} I_{DD_REST3}		3.6 0.6 0.15 0.04	10 1.8 0.40 0.15	mA	Average current, including LED current. No load on MISO, MOTION
Peak Supply Current				40	mA	Peak current in 100 kHz bandwidth, including LED current
Shutdown Supply Current	$I_{DDSHTDWN}$		1	12	µA	SCLK, MOSI and NCS must be within 300 mV of GND or V_{DD}. SHTDWN must be within 300 mV of V_{DD}
Input Low Voltage	V_{IL}			0.5	V	SCLK, MOSI, NCS, SHTDWN
Input High Voltage	V_{IH}	V_{DD} – 0.6			V	SCLK, MOSI, NCS, SHTDWN
Input Hysteresis	V_{I_HYS}		100		mV	SCLK, MOSI, NCS, SHTDWN
Input Leakage Current	I_{leak}		±1	±10	µA	Vin = V_{DD} - 0.6 V, SCLK, MOSI, NCS, SHTDWN
Output Low Voltage	V_{OL}			0.7	V	I_{out} = 1 mA, MISO, MOTION
Output High Voltage	V_{OH}	V_{DD} – 0.7			V	I_{out} = -1 mA, MISO, MOTION
Input Capacitance	C_{in}			10	pF	MOSI, NCS, SCLK, SHTDWN

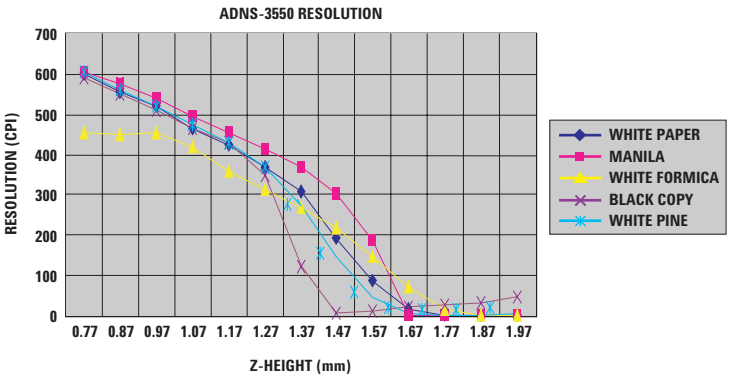


Figure 9. Mean resolution vs. Z

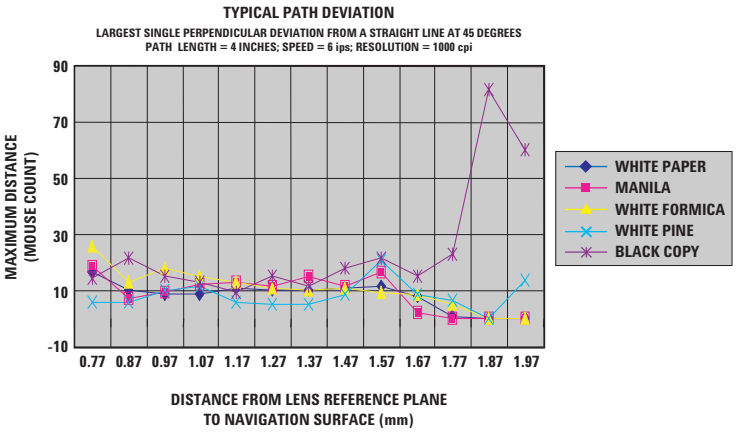


Figure 10. Typical path deviation vs. Z distance (mm)

Relationship of mouse count to distance = m (*mouse count*)/n (cpi). E.g.: Deviation of 7 mouse count = 7/1000 = 0.007 inch, where m = 7, n = 1000.

Power Management Modes

The ADNS-3550 has three power-saving modes. Each mode has a different motion detection period, affecting response time to mouse motion (Response Time). The sensor automatically changes to the appropriate mode, depending on the time since the last reported motion (Downshift Time). The parameters of each mode are shown in the following table.

Mode	Response Time (Nominal)	Downshift Time (Nominal)
Rest 1	16.5 ms	237 ms
Rest 2	82 ms	8.4 s
Rest 3	410 ms	504 s

Motion Pin Timing

The motion pin is a level-sensitive output that signals the microcontroller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X or Delta_Y registers. Clearing the motion bit (by reading Delta_Y and Delta_X, or writing to the Motion register) will put the motion pin high.

LED Mode

For power savings, the LED will not be continuously on. ADNS-3550 will flash the LED only when needed.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-3550, and to read out the motion information.

The port is a four wire serial port. The host microcontroller always initiates communication; the ADNS-3550 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a microcontroller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

SCLK: Clock input. It is always generated by the master (the microcontroller).

MOSI: Input data. (Master Out/Slave In).

MISO: Output data. (Master In/Slave Out).

NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the microcontroller to the ADNS-3550, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address (seven bits) and has a “1” as its MSB to indicate data direction. The second byte contains the data. The ADNS-3550 reads MOSI on rising edges of SCLK.

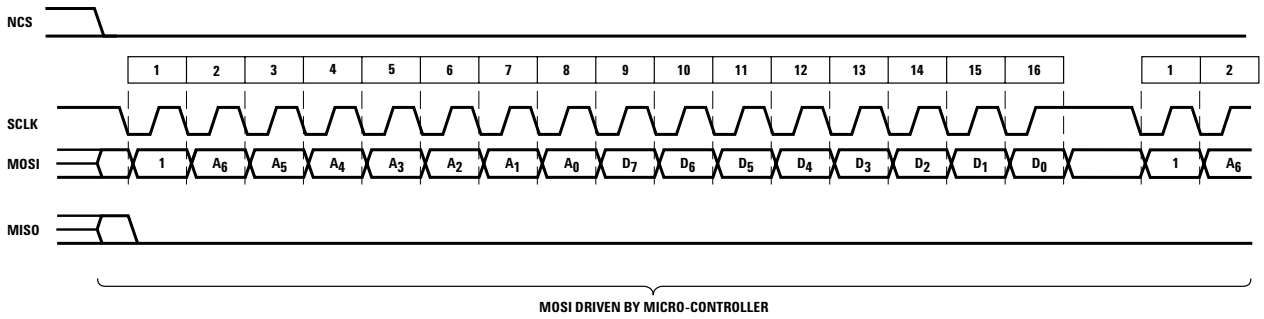


Figure 11. Write operation

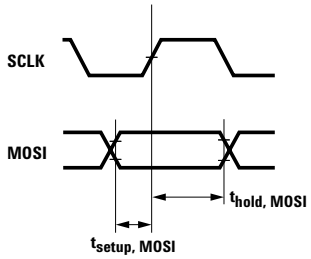


Figure 12. MOSI setup and hold time

Read Operation

A read operation, defined as data going from the ADNS-3550 to the microcontroller, is always initiated by the microcontroller and consists of two bytes. The first byte contains the address, is sent by the microcontroller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-3550 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

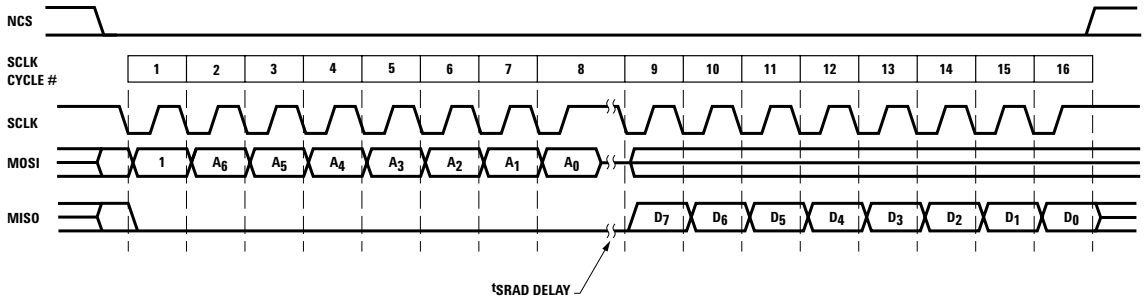


Figure 13. Read operation

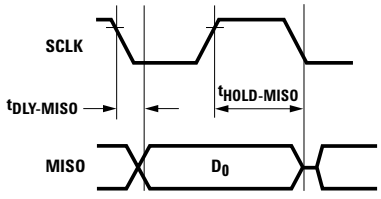


Figure 14. MISO delay and hold time

NOTE: The $0.5/f_{SCLK}$ minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-3550. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-3550 will hold the state of data on MISO until the falling edge of SCLK

Required Timing Between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

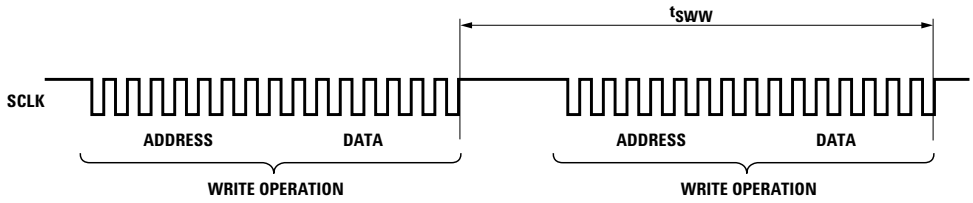


Figure 15. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

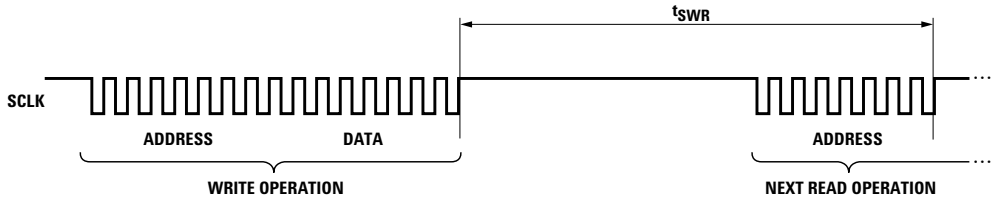


Figure 16. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

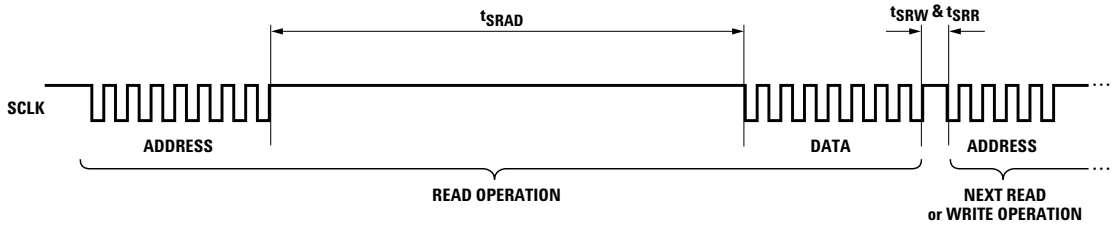


Figure 17. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-3550 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion_Burst register. The ADNS-3550 will respond with the contents of the Motion, Delta_Y, Delta_X, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. The burst transaction can be terminated after the first three bytes of the sequence are read by bringing the NCS pin high. After sending the register address, the microcontroller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data is latched into the output buffer after the last address bit is received. After the burst transmission is complete, the microcontroller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

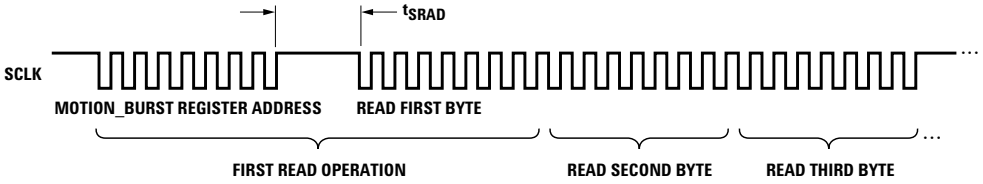


Figure 18. Motion burst timing

Notes on Power-Up

The ADNS-3550 does not perform an internal power up self-reset; the POWER_UP_RESET register must be written every time power is applied. The appropriate sequence is as follows:

1. Apply power
2. Drive NCS high, then low to reset the SPI port
3. Write 0x5a to register 0x3a
4. Read from registers 0x02, 0x03 and 0x04 (or read these same three bytes from burst motion register 0x42) one time regardless the state of the motion pin.

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

	State of Signal Pins After V_{DD} is Valid			
Pin	**On Power-Up**	**NCS High Before Reset**	**NCS Low Before Reset**	**After Reset**
NCS	Functional	High	Low	Functional
MISO	Undefined	Undefined	Functional	Depends on NCS
SCLK	Ignored	Ignored	Functional	Depends on NCS
MOSI	Ignored	Ignored	Functional	Depends on NCS
XY_LED	Undefined	Undefined	Undefined	Functional
MOTION	Undefined	Undefined	Undefined	Functional
SHTDWN	Must Be Low	Must Be Low	Must Be Low	Functional

Notes on Shutdown and Forced Rest

The ADNS-3550 can be set in Rest mode through the Configuration_Bits register (0x11). This is to allow for further power savings in applications where the sensor does not need to operate all the time.

The ADNS-3550 can be set in Shutdown mode by asserting the SHTDWN pin. For proper operation, SHTDWN pulse width must be at least t_{SHTDWN}. Shorter pulse widths may cause the chip to enter an undefined state. In addition, the SPI port should not be accessed when SHTDWN is asserted. (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. After deasserting SHTDWN, a full reset must be initiated. Wait t_{WAKEUP} before accessing the SPI port, then write 0x5A to the POWER_UP_RESET register. Any register settings must then be reloaded.

Pin	SHTDWN active
NCS	Functional*
MISO	Undefined
SCLK	Undefined
MOSI	Undefined
XY_LED	Low Current
MOTION	Undefined

*NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It can be in either state if the sensor is the only device in addition to the microcontroller.

Note: There are long wakeup times from shutdown and forced Rest. These features should not be used for power management during normal mouse motion.

Registers

The ADNS-3550 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

Address	Register	Read/Write	Default Value
0x00	Product_ID	R	0x0D
0x01	Revision_ID	R	0x02
0x02	Motion	R/W	0x00
0x03	Delta_Y	R	Any
0x04	Delta_X	R	Any
0x05	SQUAL	R	Any
0x06	Shutter_Upper	R	Any
0x07	Shutter_Lower	R	Any
0x08	Maximum_Pixel	R	Any
0x09	Pixel_Sum	R	Any
0x0a	Minimum_Pixel	R	Any
0x0b	Pixel_Grab	R/W	Any
0x0c	CRC0	R	Any
0x0d	CRC1	R	Any
0x0e	CRC2	R	Any
0x0f	CRC3	R	Any
0x10	Self_Test	W	
0x11	Configuration_Bits	R/W	0x03
0x12-0x2d	Reserved		
0x2e	Observation	R/W	Any
0x2f-0x38	Reserved		
0x3a	POWER_UP_RESET	W	
0x3b-0x3d	Reserved		
0x3e	Inverse_Revision_ID	R	0xFD
0x3f	Inverse_Product_ID	R	0xF2
0x42	Motion_Burst	R	Any

Product_ID Address: 0x00
Access: Read Reset Value: 0x0D

Bit	7	6	5	4	3	2	1	0
Field	PID_7	PID_6	PID_5	PID_4	PID_3	PID_2	PID_1	PID_0

Data Type: 8-bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-3550. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID Address: 0x01
Access: Read Reset Value: 0x02

Bit	7	6	5	4	3	2	1	0
Field	RID_7	RID_6	RID_5	RID_4	RID_3	RID_2	RID_1	RID_0

Data Type: 8-bit unsigned integer

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

Motion Address: 0x02
Access: Read/Write Reset Value: 0x00

Bit	7	6	5	4	3	2	1	0
Field	MOT	PIXRDY	PIXFIRST	OVF	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_Y and Delta_X registers.

Writing anything to this register clears the MOT and OVF bits, Delta_Y and Delta_X registers. The written data byte is not saved.

Internal buffers can accumulate more than eight bits of motion for X or Y. If either one of the internal buffers overflows, then absolute path data is lost and the OVF bit is set. This bit is cleared once some motion has been read from the Delta_X and Delta_Y registers, and if the buffers are not at full scale. Since more data is present in the buffers, the cycle of reading the Motion, Delta_X and Delta_Y registers should be repeated until the motion bit (MOT) is cleared. Until MOT is cleared, either the Delta_X or Delta_Y registers will read either positive or negative full scale. If the motion register has not been read for long time, at 500 cpi it may take up to 16 read cycles to clear the buffers, at 1000 cpi, up to 32 cycles. To clear an overflow, write anything to this register.

The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel_Dump register. Check that this bit is set before reading from Pixel_Dump. To ensure that the Pixel_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel_Grab, check to see if PIXFIRST is set to high.

Field Name	Description
MOT	Motion since last report **0 = No motion** 1 = Motion occurred, data ready for reading in Delta_X and Delta_Y registers
PIXRDY	Pixel Dump data byte is available in Pixel_Dump register **0 = data not available** 1 = data available
PIXFIRST	This bit is set when the Pixel_Grab register is written to or when the complete pixel array has been read, initiating an increment to pixel 0,0. **0 = Pixel_Grab data not from pixel 0,0** 1 = Pixel_Grab data is from pixel 0,0
OVF	Motion overflow, _Y and/or _X buffer has overflowed since last report **0 = no overflow** 1 = Overflow has occurred

Delta_Y Address: 0x03
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0

Data Type: Eight bit 2's complement number

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.

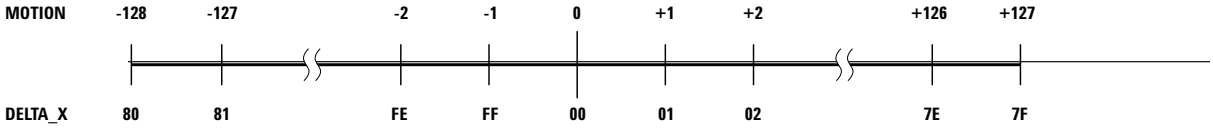
NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

Delta_X Address: 0x04
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	Y_7	Y_6	Y_5	Y_4	Y_3	Y_2	Y_1	Y_0

Data Type: Eight bit 2's complement number

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: Avago Technologies RECOMMENDS that registers 0x03 and 0x04 be read sequentially.

SQUAL Address: 0x05
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	SQ_7	SQ_6	SQ_5	SQ_4	SQ_3	SQ_2	SQ_1	SQ_0

Data Type: Upper 8 bits of a 9-bit unsigned integer

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame. The maximum SQUAL register value is 167. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected.

Shutter_Upper Address: 0x06
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	S_{15}	S_{14}	S_{13}	S_{12}	S_{11}	S_{10}	S_9	S_8

Shutter_Lower Address: 0x07
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

Data Type: Sixteen bit unsigned integer

USAGE: Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

Maximum_Pixel Address: 0x08
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

Pixel_Sum Address: 0x09
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	AP_7	AP_6	AP_5	AP_4	AP_3	AP_2	AP_1	AP_0

Data Type: High 8 bits of an unsigned 17-bit integer

USAGE: This register is used to find the average pixel value. It reports the seven bits of a 16-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 512. To find the average pixel value, use the following formula:

Average Pixel = Register Value * 128/121 = Register Value * 1.06

The maximum register value is 240. The minimum is 0. The pixel sum value can change on every frame.

Minimum_Pixel Address: 0x0a
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	MP_7	MP_6	MP_5	MP_4	MP_3	MP_2	MP_1	MP_0

Data Type: Eight-bit number

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

Pixel_Grab Address: 0x0b
Access: Read/Write Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	PD_7	PD_6	PD_5	PD_4	PD_3	PD_2	PD_1	PD_0

Data Type: Eight-bit word

USAGE: For test purposes, the sensor will read out the contents of the pixel array, one pixel per frame. To start a pixel grab, write anything to this register to reset the pointer to pixel 0,0. Then read the PIXRDY bit in the Motion register. When the PIXRDY bit is set, there is valid data in this register to read out. After the data in this register is read, the pointer will automatically increment to the next pixel. Reading may continue indefinitely; once a complete frame's worth of pixels has been read, PIXFIRST will be set to high to indicate the start of the first pixel and the address pointer will start at the beginning location again.

(Pixel Array Map Looking Through the ADNS-3150-001 Lens)

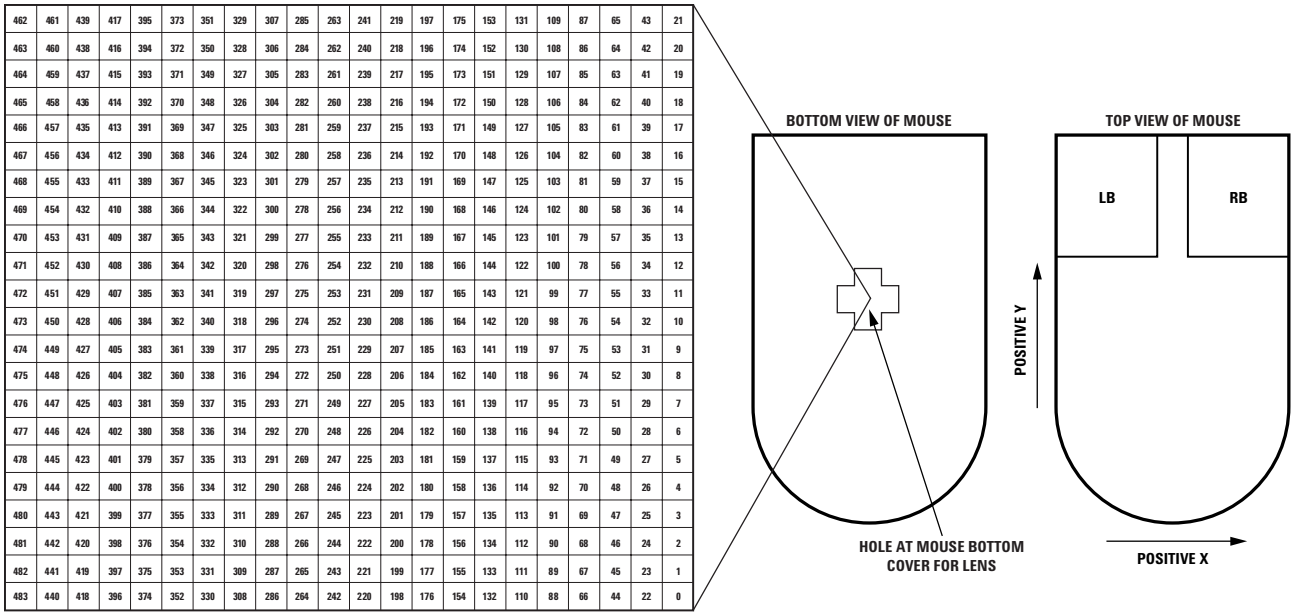


Figure 19. Surface image pixel address map

CRC0 Address: 0x0c
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	$CRC0_7$	$CRC0_6$	$CRC0_5$	$CRC0_4$	$CRC0_3$	$CRC0_2$	$CRC0_1$	$CRC0_0$

Data Type: Eight-bit number

USAGE: Register 0x0c reports the first byte of the system self test results. Value = 0xAF. See Self Test register 0x10.

CRC1 Address: 0x0d
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	$CRC1_7$	$CRC1_6$	$CRC1_5$	$CRC1_4$	$CRC1_3$	$CRC1_2$	$CRC1_1$	$CRC1_0$

Data Type: Eight-bit number

USAGE: Register 0x0c reports the second byte of the system self test results. Value = 0x4E. See Self Test register 0x10.

CRC2 Address: 0x0e
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	$CRC2_7$	$CRC2_6$	$CRC2_5$	$CRC2_4$	$CRC2_3$	$CRC2_2$	$CRC2_1$	$CRC2_0$

Data Type: Eight-bit number

USAGE: Register 0x0e reports the third byte of the system self test results. Value = 0x31. See Self Test register 0x10.

CRC3 Address: 0x0f
Access: Read Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	$CRC3_7$	$CRC3_6$	$CRC3_5$	$CRC3_4$	$CRC3_3$	$CRC3_2$	$CRC3_1$	$CRC3_0$

Data Type: Eight-bit number

USAGE: Register 0x0f reports the fourth byte of the system self test results. Value = 0x22. See Self Test register 0x10.

Self_Test Address: 0x10
Access: Write Reset Value: NA

Bit	7	6	5	4	3	2	1	0
Field	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TESTEN

Data Type: Bit field

USAGE: Set the TESTEN bit in register 0x10 to start the system self-test. The test takes 250 ms. During this time, do not write or read through the SPI port. Results are available in the CRC0-3 registers. After self-test, reset the chip to start normal operation.

Field Name	Description
TESTEN	Enable System Self Test **0 = Disabled** 1 = Enable

Configuration_bits Address: 0x11
Access: Read/Write Reset Value: 0x03

Bit	7	6	5	4	3	2	1	0
Field	RES	Reserved	RESTEN 1	RESTEN 0	Reserved	Reserved	Reserved	Reserved

Data Type: Bit field

USAGE: Register 0x11 allows the user to change the configuration of the sensor. Setting the RESTEN bit forces the sensor into Rest mode, as described in the power modes section above. The RES bit allows selection between 500 and 1000 cpi resolution.

Note: Forced Rest has a long wakeup time and should not be used for power management during normal mouse motion.

Field Name	Description
$RESTEN_{1-0}$	Puts chip into Rest mode **00 = normal operation** 01 = force Rest1 10 = force Rest2 11 = force Rest3
RES	Sets resolution **0 = 500** 1 = 1000

Reserved Address: 0x12-0x2d

Observation Address: 0x2e
Access: Read/Write Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	$MODE_1$	$MODE_0$	Reserved	Reserved	OBS_3	OBS_2	OBS_1	OBS_0

Data Type: Bit field

USAGE: Register 0x2e provides bits that are set every frame. It can be used during EFTB testing to check that the chip is running correctly. Writing anything to this register will clear the bits.

Field Name	Description
$MODE_{1-0}$	Mode Status: Reports which mode the sensor is in. 00 = Run 01 = Rest1 10 = Rest2 11 = Rest3
OBS_{3-0}	Set every frame

Reserved Address: 0x2f-0x39

POWER_UP_RESET Address: 0x3a
Access: Write Reset Value: Undefined

Bit	7	6	5	4	3	2	1	0
Field	RST_7	RST_6	RST_5	RST_4	RST_3	RST_2	RST_1	RST_0

Data Type: 8-bit integer

USAGE: Write 0x5A to this register to reset the chip. All settings will revert to default values.

Inverse_Revision_ID Address: 0x3e
Access: Read Reset Value: 0xFD

Bit	7	6	5	4	3	2	1	0
Field	$NRID_7$	$NRID_6$	$NRID_5$	$NRID_4$	$NRID_3$	$NRID_2$	$NRID_1$	$NRID_0$

Data Type: Inverse 8-bit unsigned integer

USAGE: This value is the inverse of the Revision_ID. It can be used to test the SPI port.

Inverse_Product_ID Address: 0x3f
Access: Read Reset Value: 0xF2

Bit	7	6	5	4	3	2	1	0
Field	$NPID_7$	$NPID_6$	$NPID_5$	$NPID_4$	$NPID_3$	$NPID_2$	$NPID_1$	$NPID_0$

Data Type: Inverse 8-bit unsigned integer

USAGE: This value is the inverse of the Product_ID. It can be used to test the SPI port.

Motion_Burst Address: 0x42
Access: Read Reset Value: Any

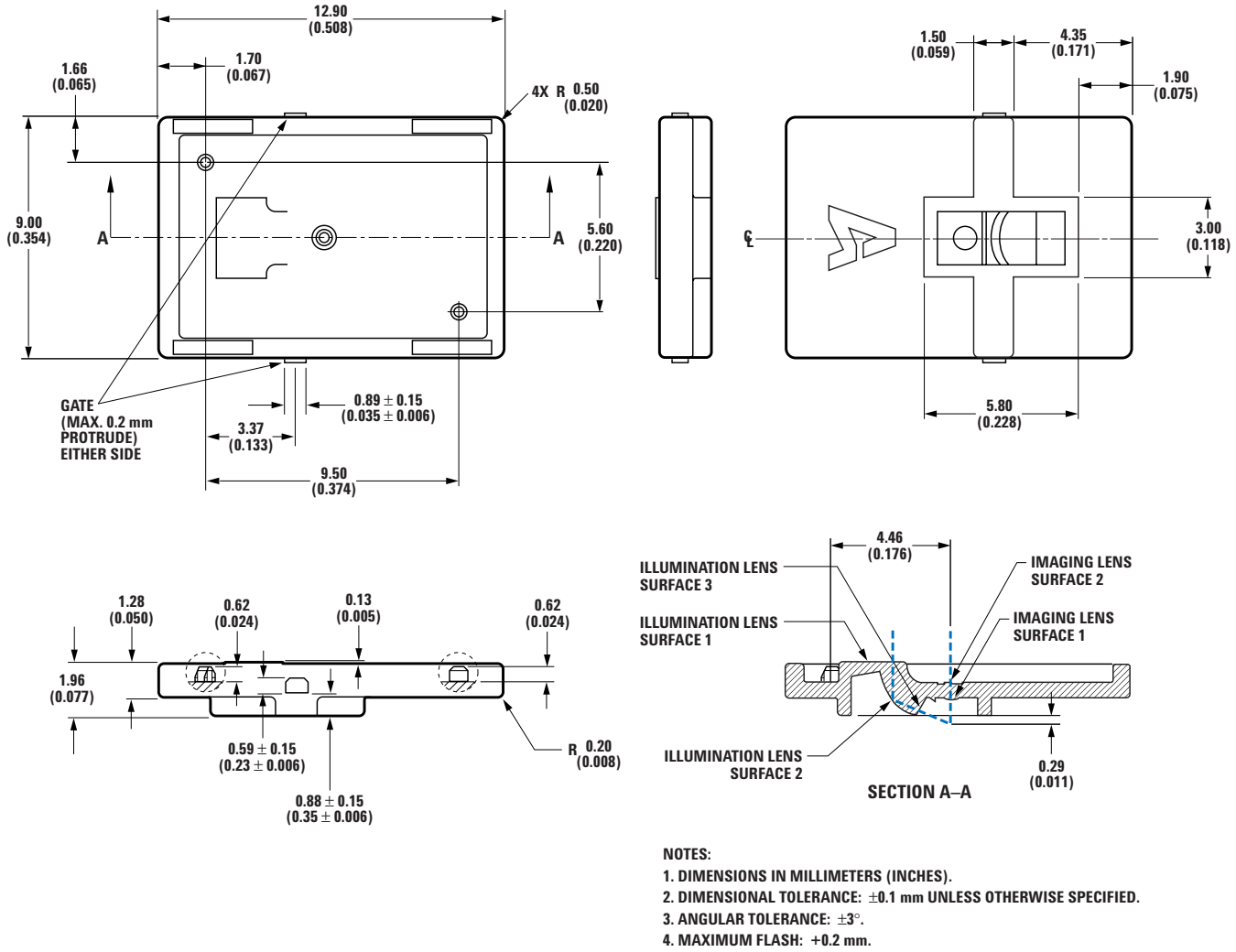
Bit	7	6	5	4	3	2	1	0
Field	MB_7	MB_6	MB_5	MB_4	MB_3	MB_2	MB_1	MB_0

Data Type: Various

USAGE: Read from this register to activate burst mode. The sensor will return the data in the Motion register, Delta_Y, Delta_X, Squal, Shutter_Upper, Shutter_Lower, and Maximum_Pixel. A minimum of 3 bytes should be read during a burst read. Reading the first 3 bytes clears the motion data.

Description

The ADNS-3150-001 small form factor (SFF) lens is designed for use with Avago Technologies ADNS-3550 integrated COB sensor. Together with the LED, the ADNS-3150-001 SFF lens provide the direct illumination and optical imaging necessary for proper operation of the sensor. ADNS-3150-001 SFF lens is a precision molded optical component and should be handled with care to avoid scratching of the optical surfaces.



NOTES:
1. DIMENSIONS IN MILLIMETERS (INCHES).
2. DIMENSIONAL TOLERANCE: ±0.1 mm UNLESS OTHERWISE SPECIFIED.
3. ANGULAR TOLERANCE: ±3°.
4. MAXIMUM FLASH: +0.2 mm.

Figure 20. ADNS-3150-001 SFF lens outline drawings and details

Lens Design Optical Performance Specifications

All specifications are based on the Mechanical Assembly Requirements.

	Symbol	Min.	Typical	Max.	Units	Conditions
Numerical Aperture	NA		0.1642			
Magnification			-1			Image at nominal location
Design Wavelength	λ		639		nm	
Depth of Field	DOF		±0.1		mm	
Die Coverage Radius			0.85		mm	Image circle radius

**Lens material is polycarbonate. Cyanoacrylate based adhesives should not be used as they will cause lens material deformation.*

Mounting Instructions for the ADNS-3150-001 Lens to the Base Plate

An IGES format drawing file with design specifications for mouse base plate features is available.

These features are useful in maintaining proper positioning and alignment of the ADNS-3150-001 when used with the Avago Technologies Optical Sensor. This file can be obtained by contacting your local Avago Technologies sales representative.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

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