
ADNS-7550

Integrated molded lead-frame DIP Sensor

Data Sheet



Theory of Operation

The ADNS-7550 integrated molded lead-frame DIP sensor comprises of sensor and VCSEL in a single package.

The advanced class of VCSEL was engineered by PixArt Imaging to provide a laser diode with a single longitudinal and a single transverse mode. In contrast to most oxide-based single-mode VCSEL, this class of PixArt VCSEL remains within single mode operation over a wide range of output power. It has significantly lower power consumption than a LED. It is an excellent choice for optical navigation applications.

The sensor is based on Laser technology, which measures changes in position by optically acquiring sequential surface images (frames) and mathematically determining the direction and magnitude of movement. It contains an Image Acquisition System (IAS), a Digital Signal Processor (DSP), and a four wire serial port. The IAS acquires microscopic surface images via the lens and illumination system. These images are processed by the DSP to determine the direction and distance of motion. The DSP calculates the Δx and Δy relative displacement values. An external microcontroller reads the Δx and Δy information from the sensor serial port. The microcontroller then translates the data into PS2, USB, or RF signals before sending them to the host PC or game console.

Features

- Wide operating voltage: 4.0V-5.25V.
- Small form factor, integrated molded lead-frame chip-on-board package
- Laser Technology
- High speed motion detection up to 30 ips and 8g
- Enhanced SmartSpeed self-adjusting frame rate for optimum performance
- Motion detect pin output
- 12-bits motion data registers.
- Internal oscillator – no clock input needed.
- Selectable 400, 800, 1200, 1600, 2000 cpi resolution.
- Four wire serial port
- Minimal number of passive components
- Laser fault detect circuitry on-chip for Eye Safety Compliance
- Advanced Technology VCSEL chip
- Single Mode Lasing operation
- 832-865 nm wavelength

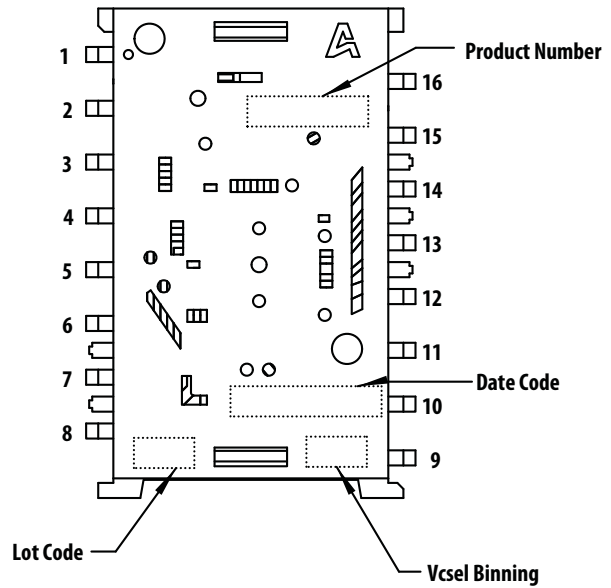
Applications

- Laser Mice
- Optical trackballs
- Integrated molded lead-frame input devices

ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Pinout of ADNS-7550 Optical Mouse Sensor

| Pin | Name | Description |
|-----|-----------|--|
| 1 | VCSEL+VE | Positive Terminal of VCSEL |
| 2 | LASER_NEN | LASER Enable (Active LOW) |
| 3 | NCS | Chip select (active low input) |
| 4 | MISO | Serial data output (Master In/Slave Out) |
| 5 | SCLK | Serial clock input |
| 6 | MOSI | Serial data input (Master Out/Slave In) |
| 7 | MOTION | Motion Detect (active low output) |
| 8 | XYLASER | XYLASER |
| 9 | VDD5 | 5V Input |
| 10 | NC | No Connection |
| 11 | GND | Ground |
| 12 | RefB | 3V output |
| 13 | RefA | 1.8V regulator output |
| 14 | DGND | Digital Ground |
| 15 | VDDIO | IO Voltage input (1.65~3.6V) |
| 16 | VCSEL-VE | Negative Terminal of VCSEL |



| Item | Marking | Remarks |
|----------------|---------|--|
| Product Number | A7550 | |
| Date Code | XYWWZV | X = Subcon Code YYWW = Date Code Z = Sensor Die Source V = VCSEL Die Source |
| VCSEL Binning | KL | |
| Lot Code | VVV | Numeric |

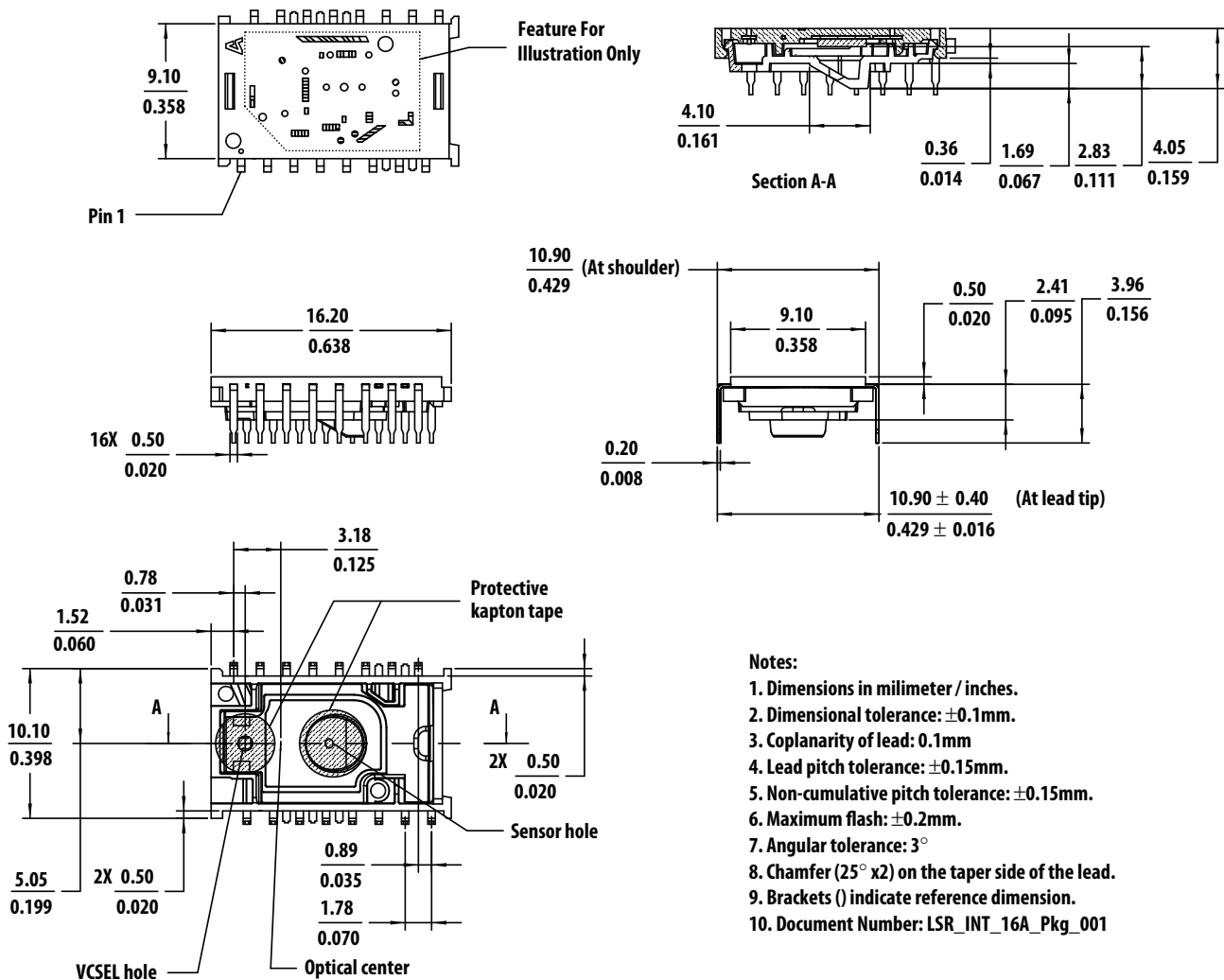
Figure 1. Device pin-out for ADNS-7550

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CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD

ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

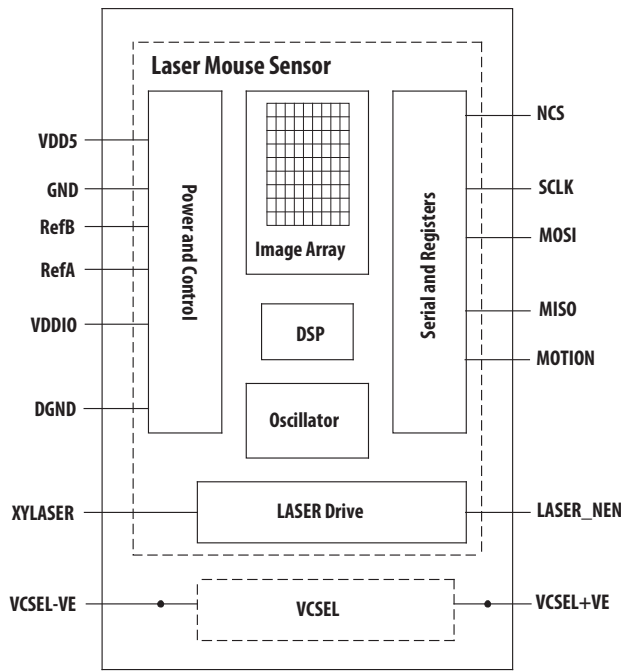


Figure 3. Block diagram of ADNS-7550 integrated molded lead-frame DIP sensor

Regulatory Requirements

- Passes FCC B and worldwide analogous emission limits when assembled into a mouse with shielded cable and following PixArt recommendations.
- Passes IEC-1000-4-3 radiated susceptibility level when assembled into a mouse with shielded cable and following PixArt recommendations.
- Passes EN61000-4-4/IEC801-4 EFT tests when assembled into a mouse with shielded cable and following PixArt recommendations.
- Provides sufficient ESD creepage/clearance distance to avoid discharge up to 15kV when assembled into a mouse according to usage instructions above.

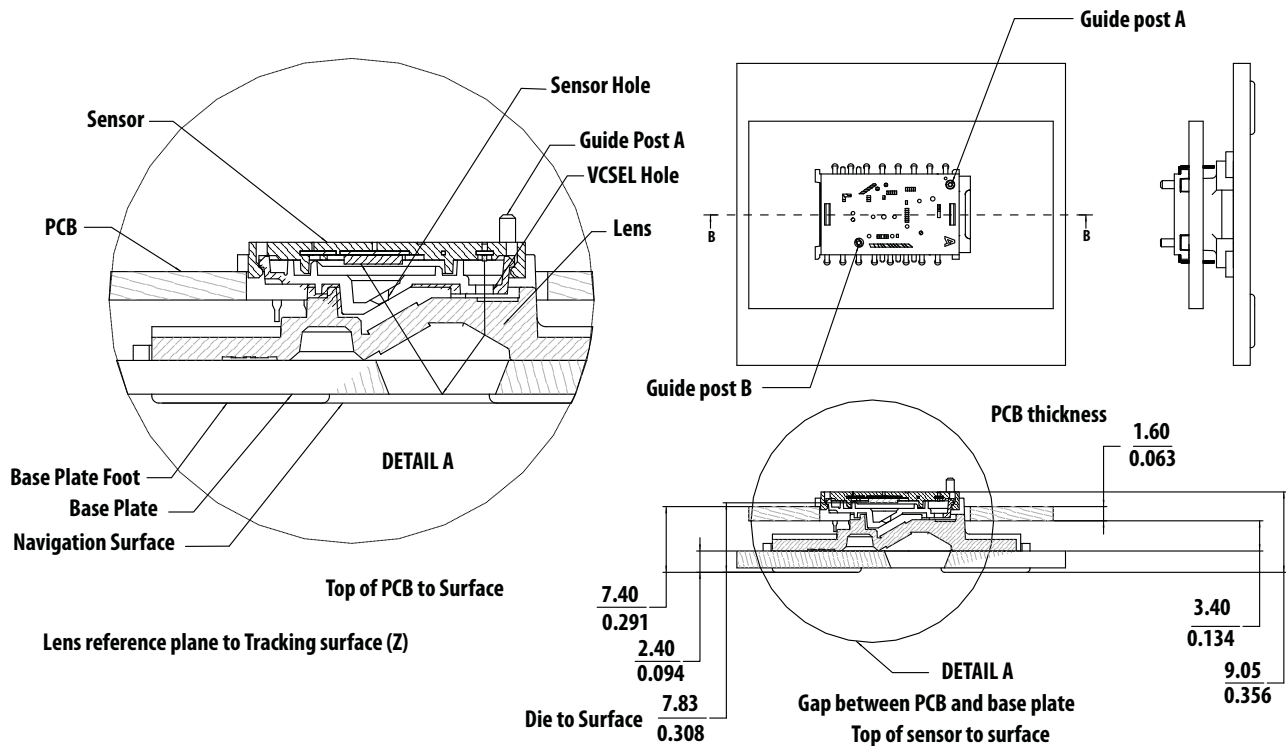


Figure 4. 2D Assembly drawing of ADNS-7550 sensor coupled with the ADNS-6150 lens, PCB and base plate (top and cross-sectional view)

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Assembly Recommendation

1. Insert the integrated molded lead-frame DIP sensor and all other electrical components into the application PCB.
2. This sensor package is only qualified for wave-solder process.
3. Wave-solder the entire assembly in a no-wash solder process utilizing a solder fixture. The solder fixture is needed to protect the sensor during the solder process. The fixture should be designed to expose the sensor leads to solder while shielding the optical aperture from direct solder contact.
4. Place the lens onto the base plate. Care must be taken to avoid contamination on the optical surfaces.
5. Remove the protective kapton tapes from the optical aperture of the sensor and VCSEL respectively. Care must be taken to keep contaminants from entering the aperture.
6. Insert the PCB assembly over the lens onto the base plate. The sensor package should self-align to the lens. The optical position reference for the PCB is set by the base plate and lens. The alignment guide post of the lens locks the lens and integrated molded lead-frame DIP sensor together. Note that the PCB motion due to button presses must be minimized to maintain optical alignment.
7. Optional: The lens can be permanently locked to the sensor package by melting the lens' guide posts over the sensor with heat staking process.
8. Tune the laser output power from the VCSEL to meet the Eye Safe Class I Standard as detailed in the LASER Power Adjustment Procedure.
9. Install the mouse top case. There must be a feature in the top case (or other area) to press down onto the sensor to ensure the sensor and lenses are interlocked to the correct vertical height.

Design considerations for improving ESD Performance

For improved electrostatic discharge performance, typical creepage and clearance distance are shown in the table below. Assumption: base plate construction as per the PixArt supplied IGES file and ADNS-6150, ADNS-6160-001 or ADNS-6170-002 lens:

| Lens | ADNS-6150 | ADNS-6160-001 | ADNS-6170-002 |
|-----------|-----------|---------------|---------------|
| Creepage | 12.0 mm | 13.50 mm | 20.30 mm |
| Clearance | 2.1 mm | 1.28 mm | 1.28 mm |

Note that the lens material is polycarbonate and therefore, cyanoacrylate based adhesives or other adhesives that may damage the lens should NOT be used.

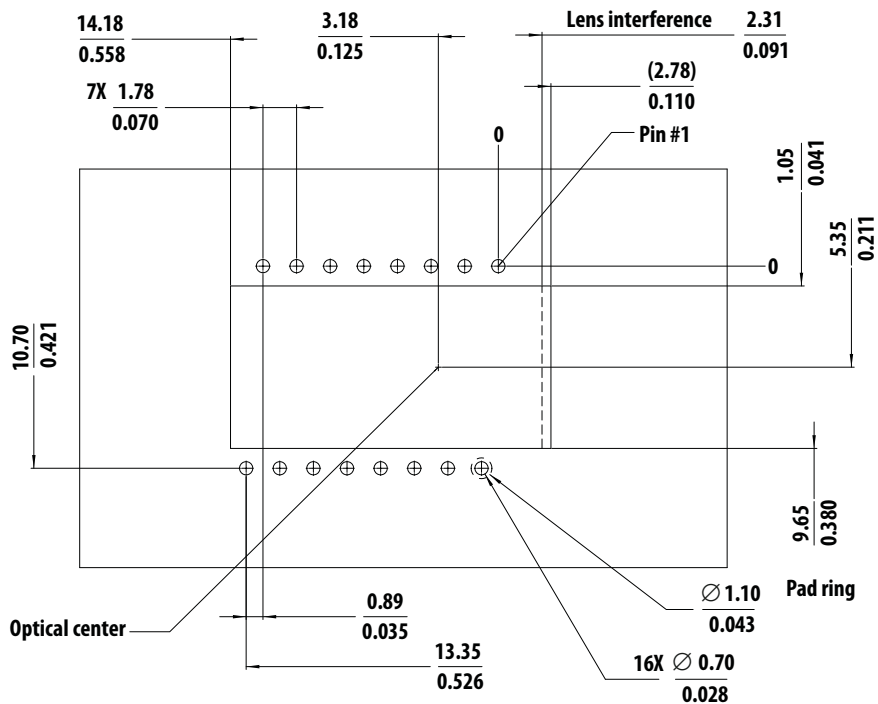


Figure 5. Recommended PCB mechanical cutouts and spacing

Application Circuit

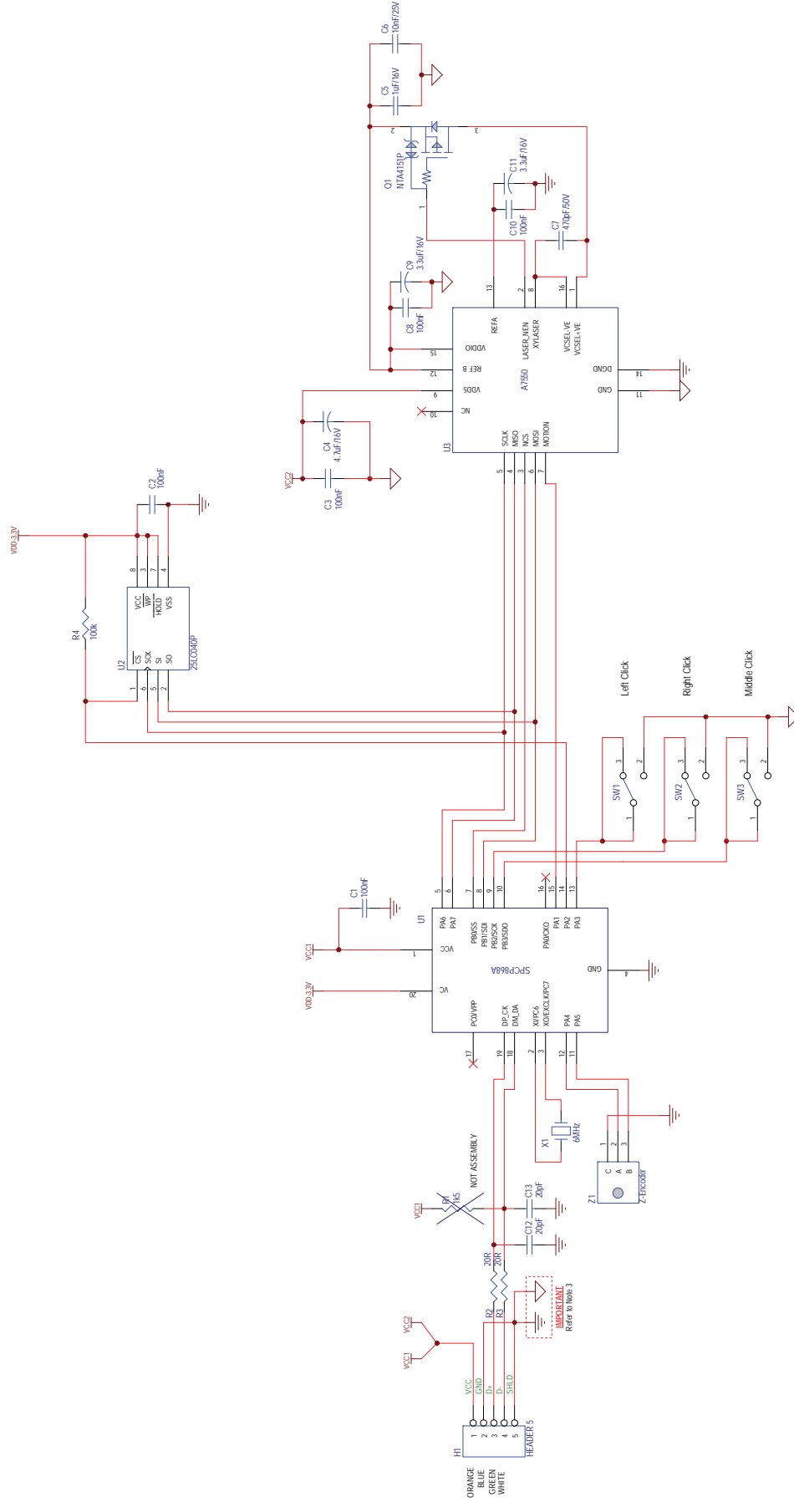


Figure 6. Schematic Diagram for 3-Button Scroll Wheel Corded Mouse

Notes

1. The supply and ground paths should be laid out using a star methodology.
2. Level shifting is required to interface a 5V micro-controller to the ADNS-7550. If a 3V micro-controller is used, the 74VHC125 component shown may be omitted.
3. All grounds MUST be correctly separated into digital and analog grounds. The digital and analog ground lines MUST be reconnected as far away as possible at either the negative terminal of the battery or at the USB connector.

LASER Drive Mode

The laser is driven in pulsed mode during normal operation. A calibration mode is provided which drives the laser in continuous (CW) operation.

Eye Safety

The ADNS-7550 integrated molded lead-frame DIP sensor and the associated components in the schematic of Figure 5 are intended to comply with Class 1 Eye Safety Requirements of IEC 60825-1. PixArt Imaging suggests that manufacturers perform testing to verify eye safety on each mouse. It is also recommended to review possible single fault mechanisms beyond those described below in the section "Single Fault Detection". Under normal conditions, the sensor generates the drive current for the VCSEL.

In order to stay below the Class 1 power requirements, LASER_CTRL0 (register 0x1a), LASER_CTRL1 (register 0x1f), LSRPWR_CFG0 (register 0x1c) and LSRPWR_CFG1 (register 0x1d) must be programmed to appropriate values. The ADNS-7550 integrated molded lead-frame DIP sensor which comprised of the sensor and VCSEL; is designed to maintain the output beam power within Class 1 requirements over components manufacturing tolerances and the recommended temperature range when adjusted per the procedure below and implemented as shown in the recommended application circuit of Figure 6. For more information, please refer to Eye Safety Application Note AN 5361.

LASER Power Adjustment Procedure

1. The ambient temperature should be 25C +/- 5C.
2. Set V_{DD5} to its permanent value.
3. Set the Range bits (bit 7 and 6 of register 0x1f) to b'01.
4. Set the Range_C1 and Range_C0 complement bits (bit 7 and 6 of register 0x1f) to b'10.
5. Enable the Calibration mode by writing to bits [3, 2, 1] of register 0x1A so the laser will be driven with 100% duty cycle.
6. Set the laser current to the minimum value by writing 0x00 to register 0x1c, and the complementary value 0xFF to register 0x1d.

7. Program registers 0x1c and 0x1d with increasing values to achieve an output power of not more than 506uW to meet class 1 Eye Safety over temperature. If this power is obtained, the calibration is complete, skip to step 11.
8. If it was not possible to achieve the power target, set the laser current to the minimum value by writing 0x00 to register 0x1c, and the complementary value 0xff to register 0x1d.
9. Set the Range and Range_C bits in registers 0x1a and 0x1f, respectively, to choose to the higher laser current range.
10. Program registers 0x1c and 0x1d with increasing values to achieve an output power of not more than 506uW to meet class 1 Eye Safety over temperature.
11. Save the value of registers 0x1a, 0x1c, 0x1d, and 0x1f in non-volatile memory in the mouse. These registers must be restored to these values every time the ADNS-7550 is reset.
12. Reset the mouse, reload the register values from non-volatile memory, enable Calibration mode, and measure the laser power to verify that the calibration is correct.

Good engineering practices such as regular power meter calibration, random quality assurance retest of calibrated mice, etc. should be used to guarantee performance, reliability and safety for the product design.

LASER Output Power

The laser beam output power as measured at the navigation surface plane is specified below. The following conditions apply:

1. The system is adjusted according to the above procedure.
2. The system is operated within the recommended operating temperature range.
3. No allowance for optical power meter accuracy is assumed.

Disabling the LASER

LASER_NEN is connected to the gate of a P-channel MOSFET transistor which when ON connects RefB to the LASER. In normal operation, LASER_NEN is low. In the case of a fault condition (ground or RefB at XYLASER), LASER_NEN goes high to turn the transistor off and disconnect RefB from the LASER.

Single Fault Detection

ADNS-7550 is able to detect a short circuit or fault condition at the XYLASER pin, which could lead to excessive laser power output. A path to ground on this

pin will trigger the fault detection circuit, which will turn off the laser drive current source and set the LASER_NEN output high. When used in combination with external components as shown in the block diagram below, the system will prevent excess laser power for a resistive path to ground at XYLASER by shutting off the laser. In addition to the ground path fault detection described above, the fault detection circuit is continuously checking for proper operation by internally generating a path to ground with the laser turned off via LASER_NEN. If the XYLASER pin is shorted to V_{DD5} /RefA/RefB, this test will fail and will be reported as a fault.

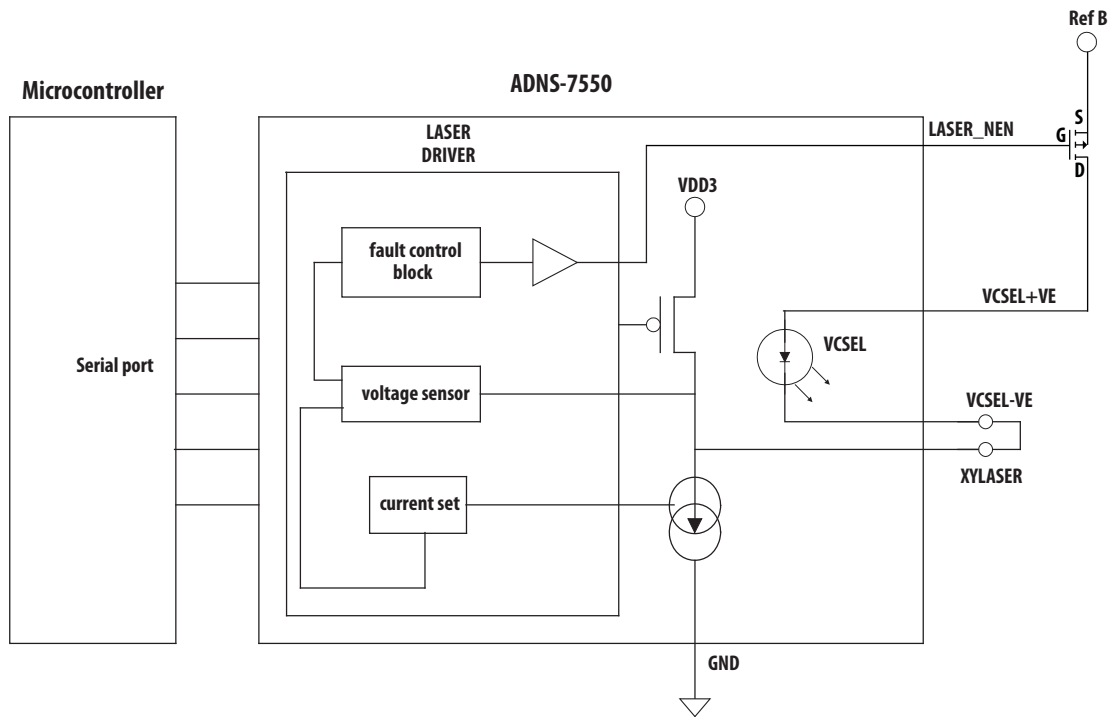


Figure 7. Single Fault Detection and Eye-safety Feature Block Diagram

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Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Units | Notes |
|----------------------------|---------------------|------|------------------------|-------|---|
| Storage Temperature | T _S | -40 | 85 | °C | |
| Lead Soldering Temperature | T _{Solder} | | 260 | °C | For 10 seconds, 1.8mm below seating plane. See soldering reflow profile in Figure 9 |
| Supply Voltage | V _{DD3} | -0.5 | 3.7 | V | |
| | V _{DDIO} | -0.5 | 3.7 | V | |
| ESD (Human-body model) | V _{ESD} | | 2 | kV | All pins |
| Input Voltage | V _{IN} | -0.5 | V _{DDIO} +0.5 | | |
| Latchup Current | I _{OUT} | | 20 | mA | All pins |

| VCSEL Die Source Marking | | V = A,V | | V = C | | | |
|----------------------------|----------------|---------|-----|-------|-----|-------|----------------------------------|
| Parameter (For VCSEL only) | Symbol | Min | Max | Min | Max | Units | Notes |
| DC Forward current | I _F | | 12 | | 7.0 | mA | |
| Peak Pulsing current | I _P | | 19 | | 9 | mA | Duration = 100ms, 10% duty cycle |
| Power Dissipation | P | | 24 | | 24 | mW | |
| Reverse voltage | V _R | | 5 | | 8 | V | I = 10μA |
| Laser Junction Temperature | T _J | | 150 | | 170 | °C | |

Notes:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are the stress ratings only and functional operation of the device at these or any other condition beyond those indicated for extended period of time may affect device reliability.
- The maximum ratings do not reflect eye-safe operation. Eye safe operating conditions are listed in the power adjustment procedure section.
- The inherent design of this component causes it to be sensitive to electrostatic discharge. The ESD threshold is listed above. To prevent ESD-induced damage, take adequate ESD precautions when handling this product.

Recommended Operating Conditions

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|-------------------|---------|---------|---------|--------|---|
| Operating Temperature | T _A | 0 | | 40 | °C | |
| Power supply voltage | V _{DD5} | 4.0 | 5.0 | 5.25 | Volts | Including noise. |
| Power supply rise time | V _{RT5} | 1 | | 100 | ms | 0 to 5.0V |
| Supply noise (Sinusoidal) | V _{NA} | | | 100 | mVp-p | 10kHz-50MHz |
| Serial Port Clock Frequency | f _{SCLK} | | | 1 | MHz | Active drive, 50% duty cycle |
| Distance from lens reference plane to surface | Z | 2.18 | 2.40 | 2.62 | mm | Results in +/- 0.22 mm minimum DOF. See Figure 8. |
| Speed | S | | | 30 | in/sec | |
| Acceleration | A | | | 8 | g | |
| Load Capacitance | C _{OUT} | | | 100 | pF | MOTION, MISO |

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Optical/Electrical Characteristics (at Tc = 5°C to 45°C):

| VCSEL Die Source Marking | Symbol | V = A,V | | | V = C | | Units | Notes | |
|------------------------------------|---------------------|---------|-------|-----|-------|-------|-------|-------|--|
| | | Min | Typ | Max | Min | Typ | | | Max |
| Peak Wavelength | λ | 832 | | 865 | 832 | | 865 | nm | |
| Maximum Radiant Power | LOPmax | | 4.5 | | | 4.0 | | mW | Maximum output power under any condition. This is not a recommended operating condition and does not meet eye safety requirements. |
| Wavelength Temperature coefficient | $d\lambda/dT$ | | 0.065 | | | 0.065 | | nm/°C | |
| Wavelength Current coefficient | $d\lambda/dI$ | | 0.21 | | | 0.3 | | nm/mA | |
| Beam Divergence | $\theta_{FW@1/e^2}$ | | 15 | | | 16 | | deg | |
| Threshold current | I _{th} | | 4.2 | | | 3.0 | | mA | |
| Slope Efficiency | SE | | 0.4 | | | 0.35 | | W/A | |
| Forward Voltage | VF | | 2.1 | 2.4 | | 2.1 | 2.4 | V | At 500uW output power |

Comments:

1. VCSELs are sorted into bins as specified in the power adjustment procedure. Appropriate binning register data values are used in the application circuit to achieve the target output power. The VCSEL binning is marked on the integrated molded lead-frame DIP sensor package.
2. When driven with current or temperature range greater than specified in the power adjustment procedure section, eye safety limits may be exceeded. The VCSEL should then be treated as a Class IIIb laser and as a potential eye hazard.
3. Over driving beyond LOP_{max} limit will cause the VCSEL to enter into an unstable region. Any LOP reference point in the laser power calibration process.

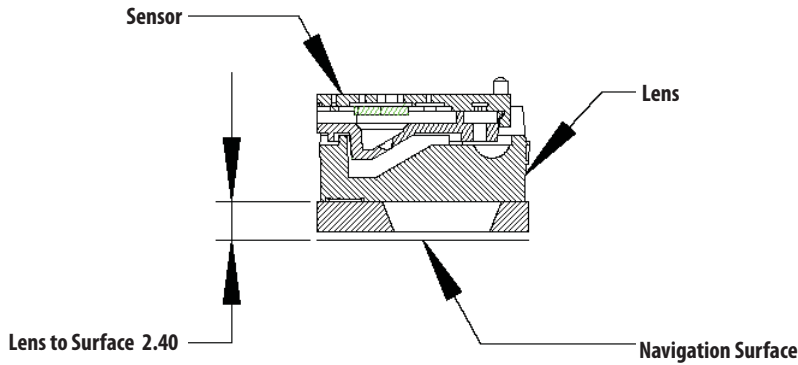


Figure 8. Distance from lens reference plane to surface, Z

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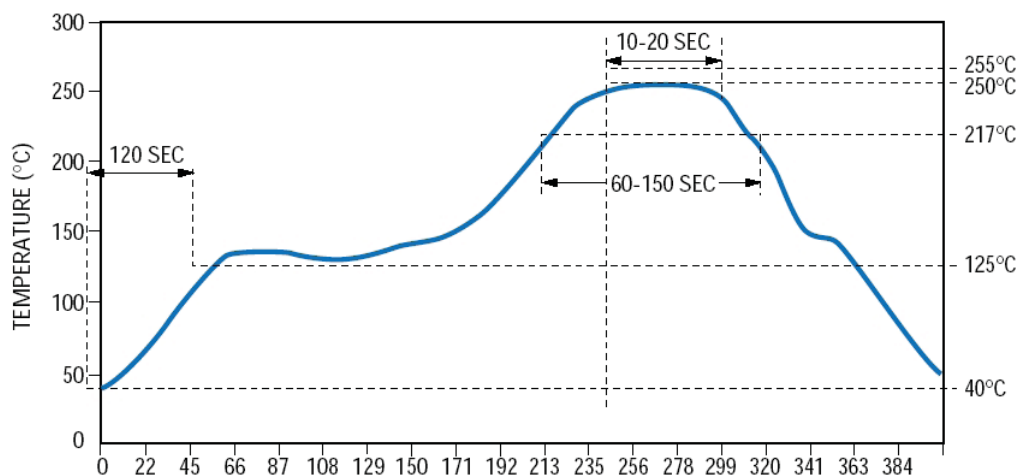


Figure 9. Recommended Soldering Reflow Profile

DC Electrical Specifications

Electrical Characteristics over recommended operating conditions. (Typical values at 25 °C, V_{DD}=5.0 V, V_{DDIO}= 2.8V)

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|------------------------------------|------------------------|-----------------------|---------|-----------------------|-------|---|
| DC Supply Current in various modes | I _{DD_RUN} | | 2.8 | 3.5 | mA | Average current, including LASER current. No load on MISO, MOTION. |
| Peak Supply Current | | | | 40 | mA | |
| Shutdown Supply Current | I _{DDSTDWN} | | 150 | 200 | µA | NCS, SCLK = V _{DDIO} MOSI, MISO = Hi-Z |
| Input Low Voltage | V _{IL} | | | 0.2V _{DDIO} | V | SCLK, MOSI, NCS |
| Input High Voltage | V _{IH} | 0.8V _{DDIO} | | | V | SCLK, MOSI, NCS |
| Input Hysteresis | V _{I_HYS} | | 100 | | mV | SCLK, MOSI, NCS |
| Input Leakage Current | I _{leak} | | ±1 | ±10 | µA | V _{in} = 0.7*V _{DDIO} , SCLK, MOSI, NCS |
| XY_LASER Current | I _{LAS} | | 0.8 | | mA | V _{XY_LASER} >=0.3V LSRPWR_CFG0 = 0xFF LSRPWR_CFG 1 = 0x00 |
| Laser Current (fault mode) | I _{LAS_FAULT} | | | 300 | uA | XY_LASER R _{leakage} < 75kOhms to Gnd |
| Output Low Voltage, MISO, MOTION | V _{OL} | | | 0.2*V _{DDIO} | V | I _{out} =1mA, MISO, MOTION |
| Output High Voltage, MISO, MOTION | V _{OH} | 0.8*V _{DDIO} | | | V | I _{out} =-1mA, MISO, MOTION |
| Output Low Voltage, LASER_NEN | V _{OL} | | | 0.2*V _{REFB} | V | I _{out} = 1mA, LASER_NEN |
| Output High Voltage, LASER_NEN | V _{OH} | 0.8*V _{REFB} | | | V | I _{out} = -0.5mA, LASER_NEN |
| Input Capacitance | C _{in} | | 10 | | pF | MOSI, NCS, SCLK |

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AC Electrical Specifications

Electrical Characteristics over recommended operating conditions. (Typical values at 25 °C, VDD=5.0V, VDDIO= 2.8V)

| Parameter | Symbol | Minimum | Typical | Maximum | Units | Notes |
|---|--------------------------------------|---------|---------|---------------------|-------|---|
| Motion delay after reset | t _{MOT-RST} | | | 23 | ms | From SW_RESET register write to valid motion, assuming motion is present |
| Shutdown | t _{STDWN} | | | 50 | ms | From Shutdown mode active to low current |
| Wake from shutdown | t _{WAKEUP} | 23 | | | ms | From Shutdown mode inactive to valid motion. Notes: A RESET must be asserted after a shutdown. Refer to section "Notes on Shutdown also note t _{MOT-RST} |
| MISO rise time | t _{r-MISO} | | 150 | 300 | ns | C _L = 100pF |
| MISO fall time | t _{f-MISO} | | 150 | 300 | ns | C _L = 100pF |
| MISO delay after SCLK | t _{DLY-MISO} | | | 120 | ns | From SCLK falling edge to MISO data valid, no load conditions |
| MISO hold time | t _{hold-MISO} | 0.5 | | 1/f _{SCLK} | us | Data held until next falling SCLK edge |
| MOSI hold time | t _{hold-MOSI} | 200 | | | ns | Amount of time data is valid after SCLK rising edge |
| MOSI setup time | t _{setup-MOSI} | 120 | | | ns | From data valid to SCLK rising edge |
| SPI time between write commands | t _{SWW} | 30 | | | μs | From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second data byte. |
| SPI time between write and read commands | t _{SWR} | 20 | | | μs | From rising SCLK for last bit of the first data byte, to rising SCLK for last bit of the second address byte. |
| SPI time between read and subsequent commands | t _{SRW} t _{SRR} | 500 | | | ns | From rising SCLK for last bit of the first data byte, to falling SCLK for the first bit of the address byte of the next command. |
| SPI read address -data delay | t _{SRAD} | 4 | | | μs | From rising SCLK for last bit of the address byte, to falling SCLK for first bit of data being read. |
| NCS inactive after motion burst | t _{BEXIT} | 500 | | | ns | Minimum NCS inactive time after motion burst before next SPI usage |
| NCS to SCLK active | t _{NCS-SCLK} | 120 | | | ns | From NCS falling edge to first SCLK rising edge |
| SCLK to NCS inactive (for read operation) | t _{SCLK-NCS} | 120 | | | ns | From last SCLK rising edge to NCS rising edge, for valid MISO data transfer |
| SCLK to NCS inactive (for write operation) | t _{SCLK-NCS} | 20 | | | us | From last SCLK rising edge to NCS rising edge, for valid MOSI data transfer |
| NCS to MISO high-Z | t _{NCS-MISO} | | | 500 | ns | From NCS rising edge to MISO high-Z state |
| MOTION rise time | t _{r-MOTION} | | 150 | 300 | ns | C _L = 100pF |
| MOTION fall time | t _{f-MOTION} | | 150 | 300 | ns | C _L = 100pF |
| Transient Supply Current | I _{DDT} | | | 45 | mA | Max supply current during a VDD ramp from 0 to 2.8V |

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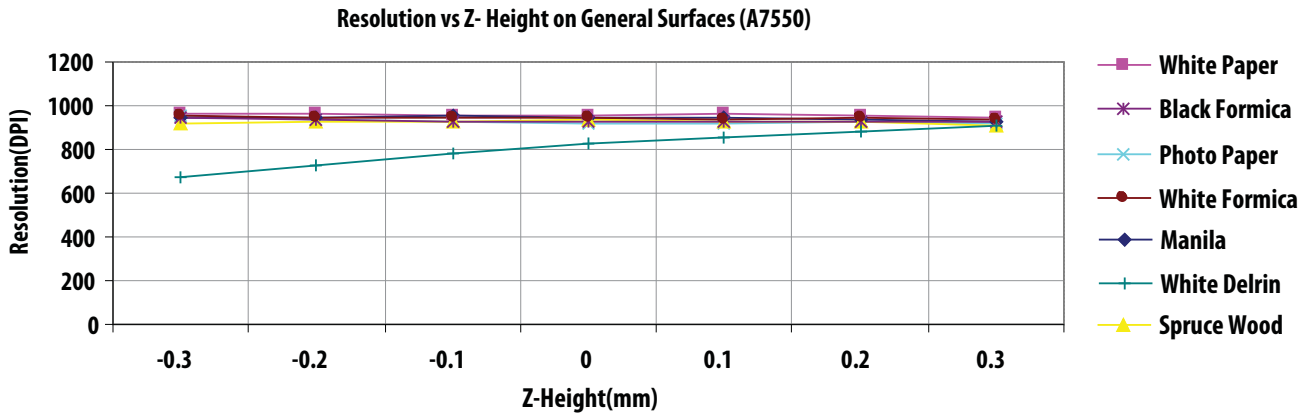


Figure 10. Mean Resolution vs. Z at 800cpi

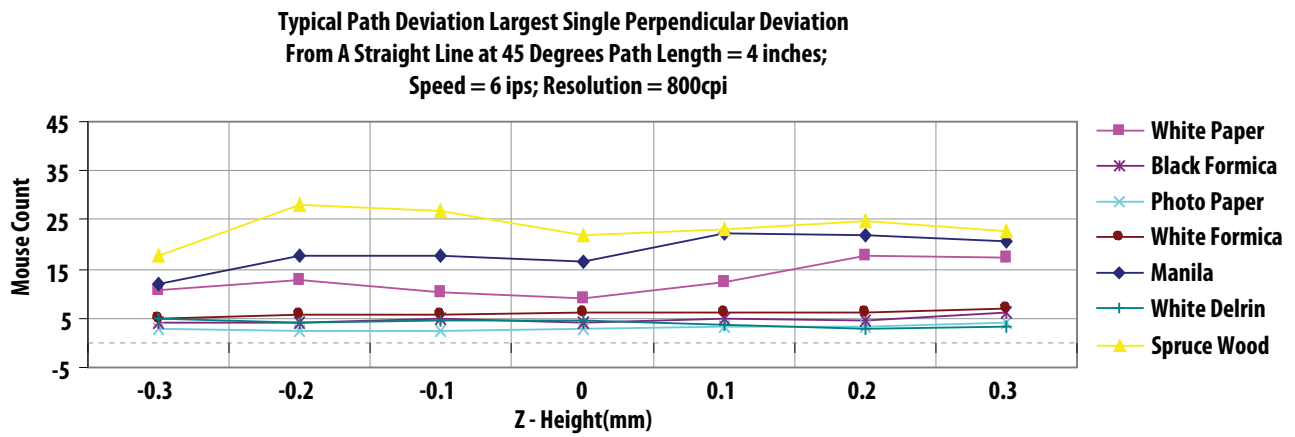


Figure 11. Average Error vs. Distance at 800cpi (mm)

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VCSEL's Typical Characteristics

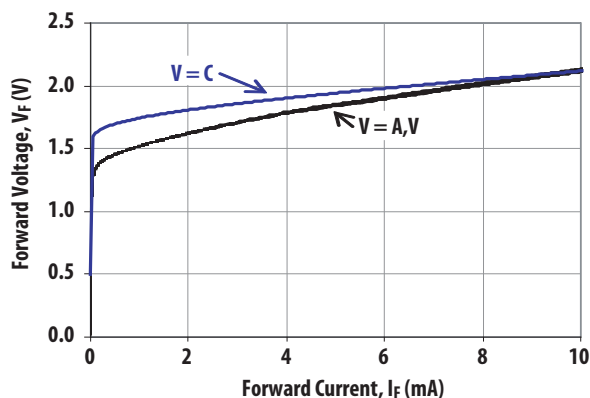


Figure 12. Forward Voltage vs. Forward Current for VCSEL

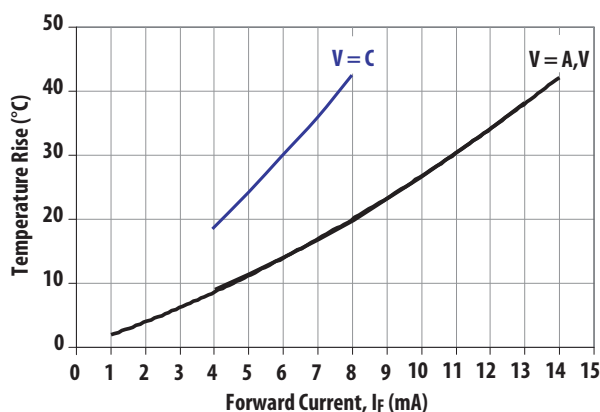


Figure 13. Junction Temperature Rise vs. Forward Current for VCSEL

Motion Pin Timing

The motion pin is a level-sensitive output that signals the micro-controller when motion has occurred. The motion pin is lowered whenever the motion bit is set; in other words, whenever there is data in the Delta_X or Delta_Y registers. Clearing the motion bit (by reading Delta_X and Delta_Y, or writing to the Motion register) will put the motion pin high.

LASER Mode

For power savings, the VCSEL will not be continuously on. ADNS-7550 will flash the VCSEL only when needed.

Synchronous Serial Port

The synchronous serial port is used to set and read parameters in the ADNS-7550, and to read out the motion information. The port is a four-wire port. The host micro-controller always initiates communication; the ADNS-7550 never initiates data transfers. SCLK, MOSI, and NCS may be driven directly by a micro-controller. The port pins may be shared with other SPI slave devices. When the NCS pin is high, the inputs are ignored and the output is tri-stated.

The lines that comprise the SPI port:

- SCLK: Clock input. It is always generated by the master (the micro-controller).
- MOSI: Input data. (Master Out/Slave In)
- MISO: Output data. (Master In/Slave Out)
- NCS: Chip select input (active low). NCS needs to be low to activate the serial port; otherwise, MISO will be high Z, and MOSI & SCLK will be ignored. NCS can also be used to reset the serial port in case of an error.

Chip Select Operation

The serial port is activated after NCS goes low. If NCS is raised during a transaction, the entire transaction is aborted and the serial port will be reset. This is true for all transactions. After a transaction is aborted, the normal address-to-data or transaction-to-transaction delay is still required before beginning the next transaction. To improve communication reliability, all serial transactions should be framed by NCS. In other words, the port should not remain enabled during periods of non-use because ESD and EFT/B events could be interpreted as serial communication and put the chip into an unknown state. In addition, NCS must be raised after each burst-mode transaction is complete to terminate burst-mode. The port is not available for further use until burst-mode is terminated.

Write Operation

Write operation, defined as data going from the micro-controller to the ADNS-7550, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address (seven bits) and has a "1" as its MSB to indicate data direction. The second byte contains the data. The ADNS-7550 reads MOSI on rising edges of SCLK.

Read Operation

A read operation, defined as data going from the ADNS-7550 to the micro-controller, is always initiated by the micro-controller and consists of two bytes. The first byte contains the address, is sent by the micro-controller over MOSI, and has a "0" as its MSB to indicate data direction. The second byte contains the data and is driven by the ADNS-7550 over MISO. The sensor outputs MISO bits on falling edges of SCLK and samples MOSI bits on every rising edge of SCLK.

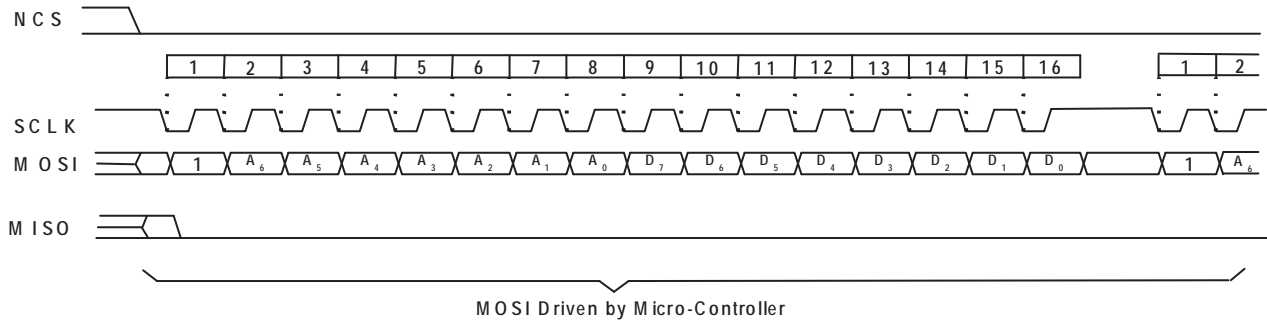


Figure 14. Write Operation

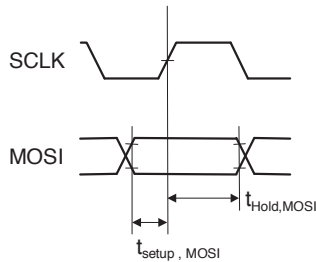


Figure 15. MOSI Setup and Hold Time

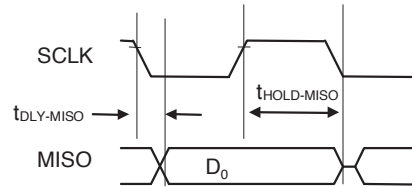


Figure 17. MISO Delay and Hold Time

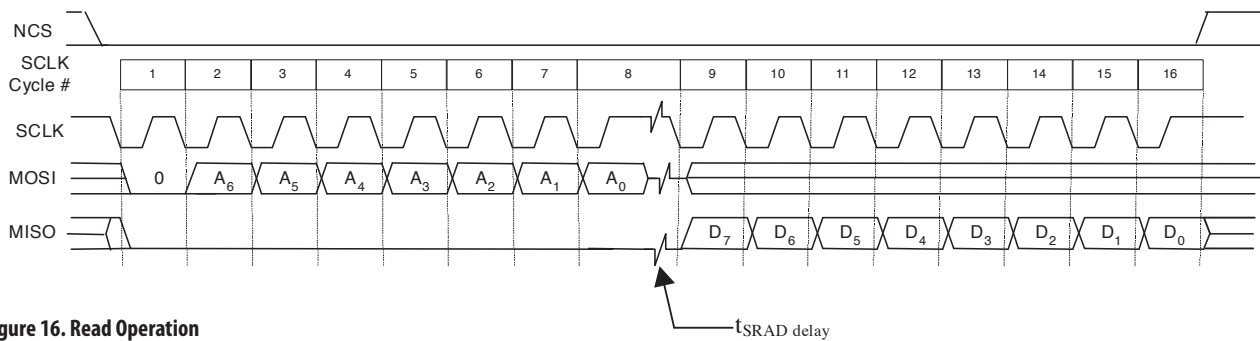


Figure 16. Read Operation

Note:

The 0.5/fSCLK minimum high state of SCLK is also the minimum MISO data hold time of the ADNS-7550. Since the falling edge of SCLK is actually the start of the next read or write command, the ADNS-7550 will hold the state of data on MISO until the falling edge of SCLK.

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Required timing between Read and Write Commands

There are minimum timing requirements between read and write commands on the serial port.

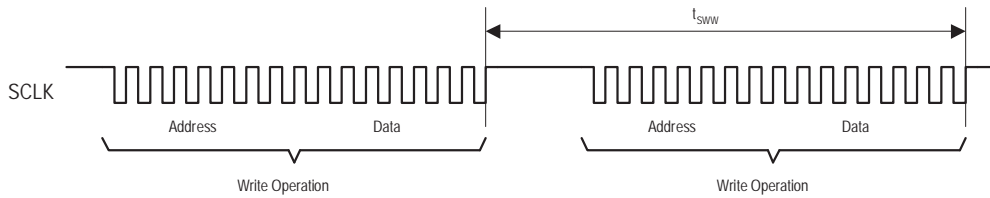


Figure 18. Timing between two write commands

If the rising edge of the SCLK for the last data bit of the second write command occurs before the required delay (t_{SWW}), then the first write command may not complete correctly.

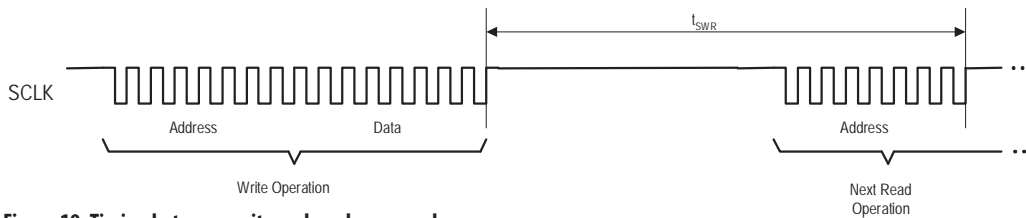


Figure 19. Timing between write and read commands

If the rising edge of SCLK for the last address bit of the read command occurs before the required delay (t_{SWR}), the write command may not complete correctly.

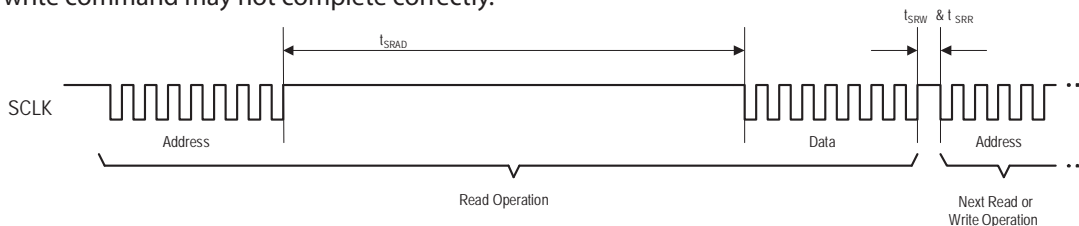


Figure 20. Timing between read and either write or subsequent read commands

During a read operation SCLK should be delayed at least t_{SRAD} after the last address data bit to ensure that the ADNS-7550 has time to prepare the requested data. The falling edge of SCLK for the first address bit of either the read or write command must be at least t_{SRR} or t_{SRW} after the last SCLK rising edge of the last data bit of the previous read operation.

Burst Mode Operation

Burst mode is a special serial port operation mode that may be used to reduce the serial transaction time for a motion read. The speed improvement is achieved by continuous data clocking to or from multiple registers without the need to specify the register address, and by not requiring the normal delay period between data bytes.

Burst mode is activated by reading the Motion_Burst register. The ADNS-7550 will respond with the contents of the Motion, Delta_X_L, Delta_Y_L, Delta_XY_H, SQUAL, Shutter_Upper, Shutter_Lower and Maximum_Pixel registers in that order. The burst transaction can be terminated anywhere in the sequence after the Delta_X value by bringing the NCS pin high. After sending the register address, the micro-controller must wait t_{SRAD} and then begin reading data. All data bits can be read with no delay between bytes by driving SCLK at the normal rate. The data are latched into the output buffer after the last address bit is received. After the burst transmission is complete, the micro-controller must raise the NCS line for at least t_{BEXIT} to terminate burst mode. The serial port is not available for use until it is reset with NCS, even for a second burst transmission.

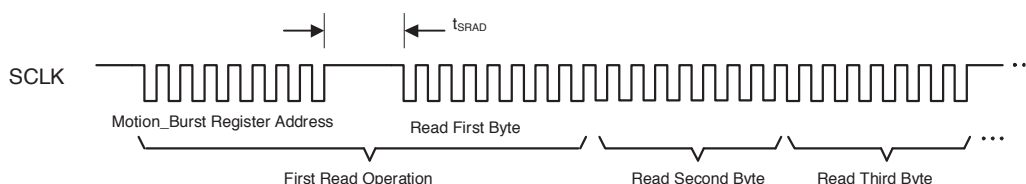


Figure 21. Motion Burst Timing

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Notes on Power-up

The ADNS-7550 does not perform an internal power up self-reset; the POWER_UP_RESET register must be written every time power is applied. The appropriate sequence is as follows:

- i. Apply power to VDD5 and VDDIO in any order, with the delay of no more than 100ms in between each supply. Ensure all supplies are stable.
- ii. Drive NCS high, then low to reset the SPI port.
- iii. Write 0x5a to register 0x3a.
- iv. Wait for at least one frame.
- v. Clear observation register.
- vi. Wait at least one frame and check observation register, all bits 0-3 must be set.
- vii. Read from registers 0x02, 0x03, 0x04 and 0x05 (or read these same 4 bytes from burst motion register 0x42) one time regardless of the motion pin state.
- viii. Write 0x27 to register 0x3C
- ix. Write 0x0a to register 0x22
- x. Write 0x01 to register 0x21
- xi. Write 0x32 to register 0x3C
- xii. Write 0x20 to register 0x23
- xiii. Write 0x05 to register 0x3C
- xiv. Write 0xB9 to register 0x37

During power-up there will be a period of time after the power supply is high but before any clocks are available. The table below shows the state of the various pins during power-up and reset.

State of Signal Pins After VDD is Valid

| Pin | On Power-Up | Before Reset | | After Reset |
|-----------|-------------|--------------|------------|----------------|
| | | NCS High | NCS Low | |
| NCS | Functional | Hi | Low | Functional |
| MISO | Undefined | Undefined | Functional | Depends on NCS |
| SCLK | Ignored | Ignored | Functional | Depends on NCS |
| MOSI | Ignored | Ignored | Functional | Depends on NCS |
| MOTION | Undefined | Undefined | Undefined | Functional |
| LASER_NEN | Undefined | Undefined | Undefined | Functional |

Notes on Shutdown

The ADNS-7550 can be set in Shutdown mode by writing 0xe7 to register 0x3b. The SPI port should not be accessed when Shutdown mode is asserted, except the power-up command (writing 0x5a to register 0x3a). (Other ICs on the same SPI bus can be accessed, as long as the sensor's NCS pin is not asserted.) The table below shows the state of various pins during shutdown. To deassert Shutdown mode:

- i. Write 0x5a to register 0x3a
- ii. Wait for at least one frame.
- iii. Clear observation register.
- iv. Wait at least one frame
- v. Check observation register, all bits 0-3 must be set to 1.
- vi. Write 0x27 to register 0x3C
- vii. Write 0x0a to register 0x22
- viii. Write 0x01 to register 0x21
- ix. Write 0x32 to register 0x3C
- x. Write 0x20 to register 0x23
- xi. Write 0x05 to register 0x3C
- xii. Write 0xB9 to register 0x37
- xiii. Any register settings must then be reloaded.

| Pin | Status when Shutdown Mode |
|-----------|----------------------------------|
| NCS | Functional ^[1] |
| MISO | Undefined ^[2] |
| SCLK | Ignore if NCS = 1 ^[3] |
| MOSI | Ignore if NCS = 1 ^[4] |
| LASER_NEN | High(off) |
| MOTION | Undefined ^[2] |

1. NCS pin must be held to 1 (high) if SPI bus is shared with other devices. It is recommended to hold to 1 (high) during Power Down unless powering up the Sensor. It must be held to 0 (low) if the sensor is to be re-powered up from shutdown (writing 0x5a to register 0x3a).
2. Depend on last state
3. SCLK is ignore if NCS is 1 (high). It is functional if NCS is 0 (low).
4. MOSI is ignore if NCS is 1 (high). If NCS is 0 (low), any command present on the MOSI pin will be ignored except power-up command (writing 0x5a to register 0x3a).

Note:

There are long wakeup times from shutdown. These features should not be used for power management during normal mouse motion.

ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Registers

The ADNS-7550 registers are accessible via the serial port. The registers are used to read motion data and status as well as to set the device configuration.

| Address | Register | Read/Write | Default Value |
|-----------|---------------------|------------|---------------|
| 0x00 | Product_ID | R | 0x32 |
| 0x01 | Revision_ID | R | 0x03 |
| 0x02 | Motion | R/W | 0x00 |
| 0x03 | Delta_X_L | R | 0x00 |
| 0x04 | Delta_Y_L | R | 0x00 |
| 0x05 | Delta_XY_H | R | 0x00 |
| 0x06 | SQUAL | R | 0x00 |
| 0x07 | Shutter_Upper | R | 0x00 |
| 0x08 | Shutter_Lower | R | 0x64 |
| 0x09 | Maximum_Pixel | R | 0xd0 |
| 0x0a | Pixel_Sum | R | 0x80 |
| 0x0b | Minimum_Pixel | R | 0x00 |
| 0x0c | CRC0 | R | 0x00 |
| 0x0d | CRC1 | R | 0x00 |
| 0x0e | CRC2 | R | 0x00 |
| 0x0f | CRC3 | R | 0x00 |
| 0x10 | Self_Test | W | NA |
| 0x11 | Reserved | | |
| 0x12 | Configuration2_Bits | R/W | 0x28 |
| 0x13-0x19 | Reserved | | |
| 0x1a | LASER_CTRL0 | R/W | 0x00 |
| 0x1b | Reserved | | |
| 0x1c | LSRPWR_CFG0 | R/W | 0x00 |
| 0x1d | LSRPWR_CFG1 | R/W | 0x00 |
| 0x1e | Reserved | | |
| 0x1f | LASER_CTRL1 | R/W | 0x00 |
| 0x20-0x2d | Reserved | | |
| 0x2e | Observation | R/W | 0x00 |
| 0x2f-0x34 | Reserved | | |
| 0x35 | Pixel_Grab | R/W | 0x00 |
| 0x36 | H_RESOLUTION | R/W | 0x04 |
| 0x37-0x39 | Reserved | | |
| 0x3a | POWER_UP_RESET | W | NA |
| 0x3b | Shutdown | W | NA |
| 0x3c | Reserved | | |
| 0x3d | Shut_thr | R/W | 0x56 |
| 0x3e | Inverse_Revision_ID | R | 0xfc |
| 0x3f | Inverse_Product_ID | R | 0xcd |
| 0x42 | Motion_Burst | R | 0x00 |

ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Product_ID

Address: 0x00

Access: Read

Reset Value: 0x32

| | | | | | | | | |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | PID ₇ | PID ₆ | PID ₅ | PID ₄ | PID ₃ | PID ₂ | PID ₁ | PID ₀ |

Data Type: 8-Bit unsigned integer

USAGE: This register contains a unique identification assigned to the ADNS-7550. The value in this register does not change; it can be used to verify that the serial communications link is functional.

Revision_ID

Address: 0x01

Access: Read

Reset Value: 0x03

| | | | | | | | | |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | RID ₇ | RID ₆ | RID ₅ | RID ₄ | RID ₃ | RID ₂ | RID ₁ | RID ₀ |

Data Type: 8-Bit unsigned integer.

USAGE: This register contains the IC revision. It is subject to change when new IC versions are released.

ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Motion**Address: 0x02**

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|-----|--------|----------|-----|----------|-------|----------|----------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MOT | PIXRDY | PIXFIRST | OVF | LP_VALID | FAULT | Reserved | Reserved |

Data Type: Bit field.

USAGE: Register 0x02 allows the user to determine if motion has occurred since the last time it was read. If the MOT bit is set, then the user should read registers 0x03 and 0x04 to get the accumulated motion. Read this register before reading the Delta_X_L, Delta_Y_L and Delta_XY_H registers.

Writing anything to this register clears the MOT and OVF bits, Delta_X_L, Delta_Y_L and Delta_XY_H registers. The written data byte is not saved.

If one of the 12 bits motion registers overflows, then absolute path data is lost and the OVF bit is set. Once OVF bit set, Sensor will stop accumulating motion data. Motion registers and OVF bit will be clear after data been read out.

The PIXRDY bit will be set whenever a valid pixel data byte is available in the Pixel_Grab register. Check that this bit is set before reading from Pixel_Grab. To ensure that the Pixel_Grab pointer has been reset to pixel 0,0 on the initial write to Pixel_Grab, check to see if PIXFIRST is set to high.

| Field Name | Description |
|------------|---|
| MOT | Motion since last report 0 = No motion 1 = Motion occurred, data ready for reading in Delta_X_L, Delta_Y_L and Delta_XY_H registers |
| PIXRDY | Pixel_Grab data byte is available in Pixel_Grab register 0 = data not available 1 = data available |
| PIXFIRST | This bit is set when the Pixel_Grab register is written to or when a complete pixel array has been read, initiating an increment to pixel 0,0. 0 = Pixel_Grab data not from pixel 0,0 1 = Pixel_Grab data is from pixel 0,0 |
| OVF | Motion overflow, ΔY and/or ΔX buffer has overflowed since last report 0 = no overflow 1 = Overflow has occurred |
| LP_VALID | Laser Power Settings 0 = register 0x1a and register 0x1f or register 0x1c and register 0x1d do not have complementary values 1 = laser power is valid |
| FAULT | Indicates that VCSEL is shorted to GND or VDD 0 = no fault detected 1 = fault detected. |

Note: PixArt recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

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ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Delta_X_L

Address: 0x03

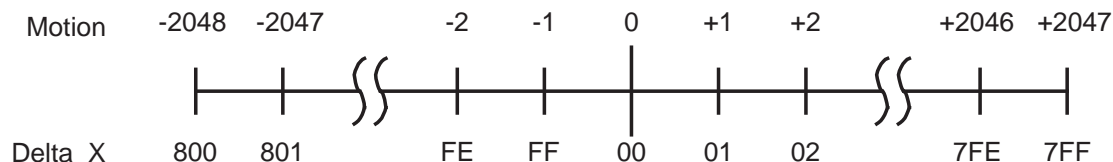
Access: Read

Reset Value: 0x00

| | | | | | | | | |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | X ₇ | X ₆ | X ₅ | X ₄ | X ₃ | X ₂ | X ₁ | X ₀ |

Data Type: Eight bit 2's complement number.

USAGE: X movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: PixArt recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

Delta_Y_L

Address: 0x04

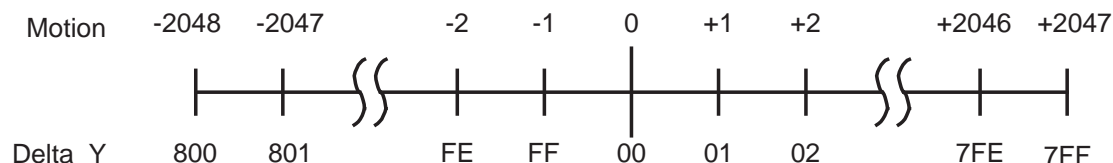
Access: Read

Reset Value: 0x00

| | | | | | | | | |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Y ₇ | Y ₆ | Y ₅ | Y ₄ | Y ₃ | Y ₂ | Y ₁ | Y ₀ |

Data Type: Eight bit 2's complement number.

USAGE: Y movement is counts since last report. Absolute value is determined by resolution. Reading clears the register.



NOTE: PixArt recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

Delta_XY_H

Address: 0x05

Access: Read

Reset Value: 0x00

| | | | | | | | | |
|-------|-----------------|-----------------|----------------|----------------|-----------------|-----------------|----------------|----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | X ₁₁ | X ₁₀ | X ₉ | X ₈ | Y ₁₁ | Y ₁₀ | Y ₉ | Y ₈ |

Data Type: 2's complement number, upper 4 bits of Delta_X and Delta_Y.

USAGE: Delta_XY_H must be read after Delta_X_L and Delta_Y_L to have the full motion data. Reading clear the registers.

NOTE: PixArt recommends that registers 0x02, 0x03, 0x04 and 0x05 be read sequentially.

ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

SQUAL

Address: 0x06

Access: Read

Reset Value: 0x00

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | SQ ₇ | SQ ₆ | SQ ₅ | SQ ₄ | SQ ₃ | SQ ₂ | SQ ₁ | SQ ₀ |

Data Type: Upper 8 bits of a 9-bit unsigned integer.

USAGE: SQUAL (Surface Quality) is a measure of the number of valid features visible by the sensor in the current frame.

The maximum SQUAL register value is 242. Since small changes in the current frame can result in changes in SQUAL, variations in SQUAL when looking at a surface are expected. The graph below shows 800 sequentially acquired SQUAL values, while a sensor was moved slowly over white paper. SQUAL is nearly equal to zero, if there is no surface below the sensor. SQUAL is typically maximized when the navigation surface is at the optimum distance from the imaging lens (the nominal Z-height).

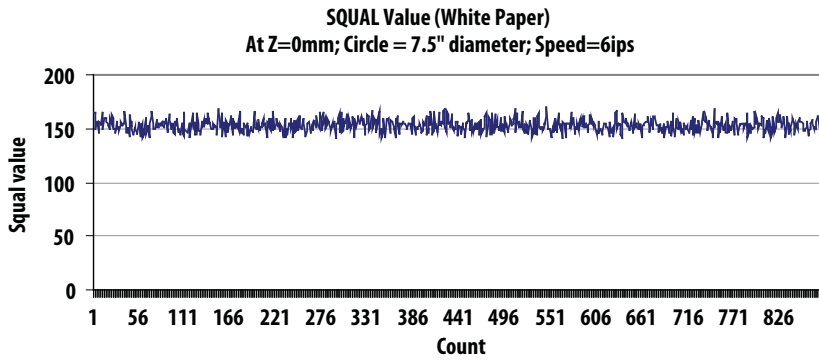


Figure 22. SQUAL Values at 800dpi (White Paper)

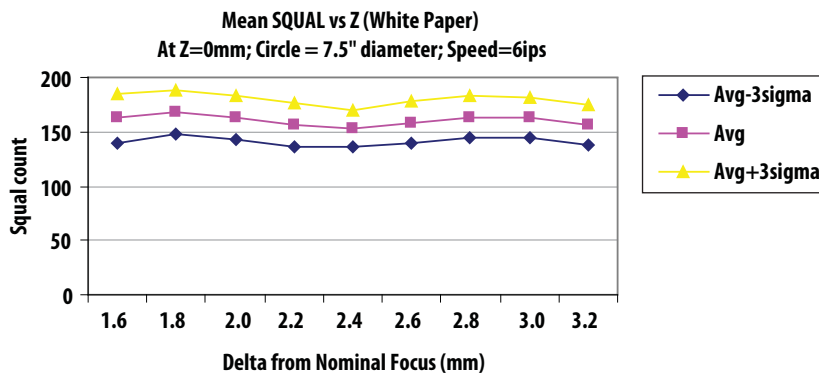


Figure 23. Mean SQUAL vs. Z (White Paper)

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ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Shutter_Upper

Address: 0x07

Access: Read

Reset Value: 0x00

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | S ₁₅ | S ₁₄ | S ₁₃ | S ₁₂ | S ₁₁ | S ₁₀ | S ₉ | S ₈ |

Shutter_Lower

Address: 0x08

Access: Read

Reset Value: 0x64

| | | | | | | | | |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | S ₇ | S ₆ | S ₅ | S ₄ | S ₃ | S ₂ | S ₁ | S ₀ |

Data Type: Sixteen bit unsigned integer.

USAGE: Units are clock cycles. Read Shutter_Upper first, then Shutter_Lower. They should be read consecutively. The shutter is adjusted to keep the average and maximum pixel values within normal operating ranges. The shutter value is automatically adjusted.

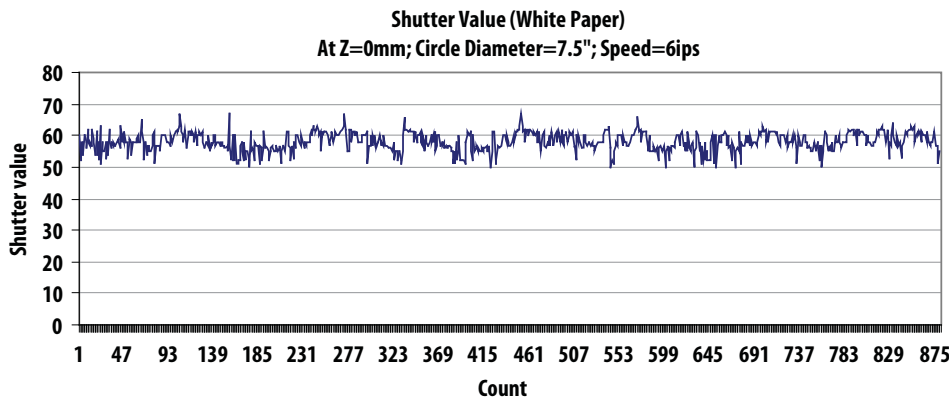


Figure 24. Shutter Values at 800dpi (White Paper)

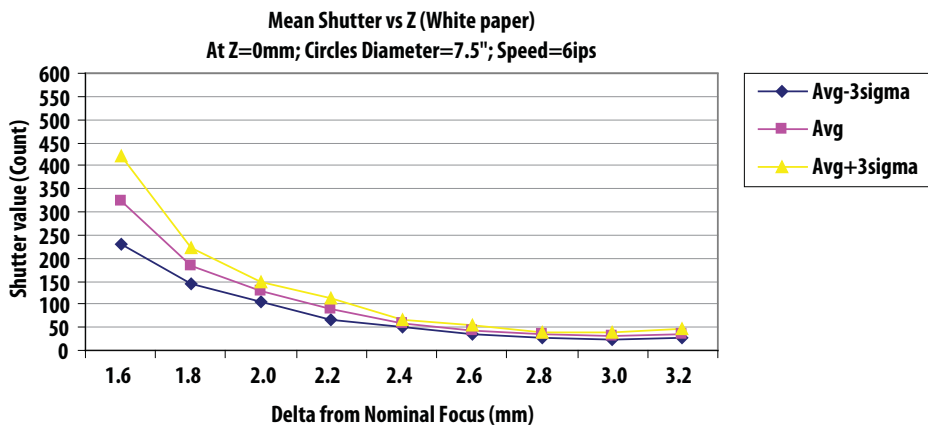


Figure 25. Mean Shutter vs. Z (White Paper)

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ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Maximum_Pixel

Address: 0x09

Access: Read

Reset Value: 0xd0

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MP ₇ | MP ₆ | MP ₅ | MP ₄ | MP ₃ | MP ₂ | MP ₁ | MP ₀ |

Data Type: Eight-bit number.

USAGE: Maximum Pixel value in current frame. Minimum value = 0, maximum value = 254. The maximum pixel value can vary with every frame.

Pixel_Sum

Address: 0x0a

Access: Read

Reset Value: 0x80

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | AP ₇ | AP ₆ | AP ₅ | AP ₄ | AP ₃ | AP ₂ | AP ₁ | AP ₀ |

Data Type: High 8 bits of an unsigned 16-bit integer.

USAGE: This register is used to find the average pixel value. It reports the upper eight bits of a 18-bit counter, which sums all pixels in the current frame. It may be described as the full sum divided by 1024. To find the average pixel value, use the following formula:

$$\text{Average Pixel} = \text{Register Value} * 1024/676 = \text{Register Value} * 1.515$$

The maximum register value is 167. The minimum is 0. The pixel sum value can change on every frame.

Minimum_Pixel

Address: 0x0b

Access: Read

Reset Value: 0x00

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | MP ₇ | MP ₆ | MP ₅ | MP ₄ | MP ₃ | MP ₂ | MP ₁ | MP ₀ |

Data Type: Eight-bit number.

USAGE: Minimum Pixel value in current frame. Minimum value = 0, maximum value = 254. The minimum pixel value can vary with every frame.

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ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

CRC0 Address: 0x0c

Access: Read Reset Value: 0x00

| | | | | | | | | |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CRC0 ₇ | CRC0 ₆ | CRC0 ₅ | CRC0 ₄ | CRC0 ₃ | CRC0 ₂ | CRC0 ₁ | CRC0 ₀ |

Data Type: Eight-bit number.

USAGE: Register 0x0c reports the first byte of the system self test results. Value = F4.

CRC1 Address: 0x0d

Access: Read Reset Value: 0x00

| | | | | | | | | |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CRC1 ₇ | CRC1 ₆ | CRC1 ₅ | CRC1 ₄ | CRC1 ₃ | CRC1 ₂ | CRC1 ₁ | CRC1 ₀ |

Data Type: Eight-bit number.

USAGE: Register 0x0d reports the second byte of the system self test results. Value = 54.

CRC2 Address: 0x0e

Access: Read Reset Value: 0x00

| | | | | | | | | |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CRC2 ₇ | CRC2 ₆ | CRC2 ₅ | CRC2 ₄ | CRC2 ₃ | CRC2 ₂ | CRC2 ₁ | CRC2 ₀ |

Data Type: Eight-bit number.

USAGE: Register 0x0e reports the third byte of the system self test results. Value = 6D.

CRC3 Address: 0x0f

Access: Read Reset Value: 0x00

| | | | | | | | | |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | CRC3 ₇ | CRC3 ₆ | CRC3 ₅ | CRC3 ₄ | CRC3 ₃ | CRC3 ₂ | CRC3 ₁ | CRC3 ₀ |

Data Type: Eight-bit number.

USAGE: Register 0x0f reports the fourth byte of the system self test results. Value = EB.

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Self_Test **Address: 0x10**

Access: Write

Reset Value: NA

| | | | | | | | | |
|-------|----------|----------|----------|----------|----------|----------|----------|--------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | TESTEN |

Data Type: Bit field

USAGE: Before performing system self test, reset the chip. Then, set the TESTEN bit in register 0x10 to start the system self test. The test takes 250ms. During this time, do not write or read through the SPI port. Results are available in the CRC0-3 registers. After self-test, reset the chip again to start normal operation.

| Field Name | Description |
|------------|---|
| TESTEN | Enable System Self Test 0 = Disabled 1 = Enable |

Reserved **Address: 0x11**

Configuration2_bits **Address: 0x12**

Access: Read/Write

Reset Value: 0x28

| | | | | | | | | |
|-------|---|------------------|------------------|----------|----------|----------|----------|----------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | 0 | RES ₁ | RES ₀ | Reserved | Reserved | Reserved | Reserved | Reserved |

Data Type: Bit field

USAGE: Register 0x12 allows the user to change the configuration of the sensor. The RES bit allows selection between 400, 800, 1200 and 1600 cpi resolution.

| Field Name | Description |
|------------|---|
| RES[1:0] | Sets resolution 00 = 400 01 = 800 10 = 1200 11 = 1600 |

Reserved **Address: 0x1b**

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LASER_CTRL0

Address: 0x1a

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|--------|--------|----------|----------|------------------|------------------|------------------|---------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Range1 | Range0 | Reserved | Reserved | CAL ₂ | CAL ₁ | CAL ₀ | Force_Disable |

Data Type: Bit field

USAGE: This register is used to control the laser drive. Bits 7 and 6 require complement values in register 0x1F. If the registers do not contain complementary values for these bits, the laser is turned off and the LP_VALID bit in the MOTION register is set to 0. The registers may be written in any order after the power ON reset.

| Field Name | Description |
|--------------------|---|
| Range[1:0] | Rbin Settings 00= Laser current range from approximately 0.9mA to 3mA 01= Laser current range from approximately 2mA to 5mA 11 = Laser current range from approximately 4mA to 10mA 10 = Invalid setting, LPVALID will be set and laser will off. |
| CAL ₂₋₀ | Laser calibration mode - Write 101b to bits [3,2,1] to set the laser to continuous ON (CW) mode. - Write 000b to exit laser calibration mode, all other values are not recommended. Reading the Motion register (0x02 or 0x42) will reset the value to 000b and exit calibration mode. |
| Force_Disable | LASER force disabled 0 = LASER_NEN functions as normal 1 = LASER_NEN output is high. |

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LSRPWR_CFG0**Address: 0x1c**

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | LP ₇ | LP ₆ | LP ₅ | LP ₄ | LP ₃ | LP ₂ | LP ₁ | LP ₀ |

Data Type: 8 Bit unsigned

USAGE: This register is used to set the laser current. It is to be used together with register 0x1D, where register 0x1D contains the complement of register 0x1C. If the registers do not contain complementary values, the laser is turned off and the LP_VALID bit in the MOTION register is set to 0. The registers may be written in any order after the power ON reset.

| Field Name | Description |
|------------|--|
| LP7 – LP0 | Controls the 8-bit DAC for adjusting laser current. One step is equivalent to $(1/384)*100\% = 0.26\%$ drop of relative laser current. Refer to the table below for examples of relative laser current settings. |

| LP7 - LP3 | LP2 | LP1 | LP0 | Relative Laser Current |
|-----------|-----|-----|-----|------------------------|
| 00000 | 0 | 0 | 0 | 33.59% |
| 00000 | 0 | 0 | 1 | 33.85% |
| 00000 | 0 | 1 | 0 | 34.11% |
| : : | : | : | : | : : |
| 11111 | 1 | 0 | 1 | 99.48% |
| 11111 | 1 | 1 | 0 | 99.74% |
| 11111 | 1 | 1 | 1 | 100% |

LSRPWR_CFG1**Address: 0x1d**

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | LPC ₇ | LPC ₆ | LPC ₅ | LPC ₄ | LPC ₃ | LPC ₂ | LPC ₁ | LPC ₀ |

Data Type: 8 Bit unsigned

USAGE: The value in this register must be a complement of register 0x1C for laser current to be as programmed, otherwise the laser is turned off and the LP_VALID bit in the MOTION register is set to 0. Registers 0x1C and 0x1D may be written in any order after power ON reset.

Reserved**Address: 0x1e**

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LASER_CTRL1 **Address: 0x1f**

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|----------|----------|----------|----------|----------|----------|----------|----------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Range_C1 | Range_CO | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |

Data Type: 8 Bit unsigned

USAGE: Bits 7 and 6 of this register must be the complement of the corresponding bits in register 0x1A for the VCSEL control to be as programmed, otherwise the laser turned is off and the LP_VALID bit in the MOTION register is set to 0. Registers 0x1A and 0x1F may be written in any order after power ON reset.

Reserved **Address: 0x20-0x2d**

Observation **Address: 0x2e**

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|----------|----------|----------|------------------|------------------|------------------|------------------|------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | Reserved | Reserved | OBS ₄ | OBS ₃ | OBS ₂ | OBS ₁ | OBS ₀ |

Data Type: Bit field

USAGE: Register 0x2e provides bits that are set every frame. It can be used during EFT/B testing to check that the chip is running correctly. Writing anything to this register will clear the bits. Wait for at least one frame before reading the register.

| Field Name | Description |
|--------------------|-----------------|
| OBS ₄₋₀ | Set every frame |

Reserved **Address: 0x2f-0x34, 0x36-0x39**

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Pixel_Grab

Address: 0x35

Access: Read/Write

Reset Value: 0x00

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | PD ₇ | PD ₆ | PD ₅ | PD ₄ | PD ₃ | PD ₂ | PD ₁ | PD ₀ |

Data Type: 8 Bit Word

USAGE: For test purposes, the sensor will read out the contents of the pixel array, one pixel per frame. To start a pixel grab, write anything to this register to reset the pointer to pixel 0,0. Then read the PIXRDY bit in the Motion register. When the PIXRDY bit is set, there is valid data in this register to read out. After the data in this register is read, the pointer will automatically increment to the next pixel. Reading may continue indefinitely; once a complete frame's worth of pixels has been read, PIXFIRST will be set to high to indicate the start of the first pixel and the address pointer will start at the beginning location again.

| | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---------------|
| 25 | 51 | 77 | 103 | 129 | 155 | 181 | 207 | 233 | 259 | 285 | 311 | 337 | 363 | 389 | 415 | 441 | 467 | 493 | 519 | 545 | 571 | 597 | 623 | 649 | 675 | Last Pixel |
| 24 | 50 | 76 | 102 | 128 | 154 | 180 | 206 | 232 | 258 | 284 | 310 | 336 | 362 | 388 | 414 | 440 | 466 | 492 | 518 | 544 | 570 | 596 | 622 | 648 | 674 | |
| 23 | 49 | 75 | 101 | 127 | 153 | 179 | 205 | 231 | 257 | 283 | 309 | 335 | 361 | 387 | 413 | 439 | 465 | 491 | 517 | 543 | 569 | 595 | 621 | 647 | 673 | |
| 22 | 48 | 74 | 100 | 126 | 152 | 178 | 204 | 230 | 256 | 282 | 308 | 334 | 360 | 386 | 412 | 438 | 464 | 490 | 516 | 542 | 568 | 594 | 620 | 646 | 672 | |
| 21 | 47 | 73 | 99 | 125 | 151 | 177 | 203 | 229 | 255 | 281 | 307 | 333 | 359 | 385 | 411 | 437 | 463 | 489 | 515 | 541 | 567 | 593 | 619 | 645 | 671 | |
| 20 | 46 | 72 | 98 | 124 | 150 | 176 | 202 | 228 | 254 | 280 | 306 | 332 | 358 | 384 | 410 | 436 | 462 | 488 | 514 | 540 | 566 | 592 | 618 | 644 | 670 | |
| 19 | 45 | 71 | 97 | 123 | 149 | 175 | 201 | 227 | 253 | 279 | 305 | 331 | 357 | 383 | 409 | 435 | 461 | 487 | 513 | 539 | 565 | 591 | 617 | 643 | 669 | |
| 18 | 44 | 70 | 96 | 122 | 148 | 174 | 200 | 226 | 252 | 278 | 304 | 330 | 356 | 382 | 408 | 434 | 460 | 486 | 512 | 538 | 564 | 590 | 616 | 642 | 668 | |
| 17 | 43 | 69 | 95 | 121 | 147 | 173 | 199 | 225 | 251 | 277 | 303 | 329 | 355 | 381 | 407 | 433 | 459 | 485 | 511 | 537 | 563 | 589 | 615 | 641 | 667 | |
| 16 | 42 | 68 | 94 | 120 | 146 | 172 | 198 | 224 | 250 | 276 | 302 | 328 | 354 | 380 | 406 | 432 | 458 | 484 | 510 | 536 | 562 | 588 | 614 | 640 | 666 | |
| 15 | 41 | 67 | 93 | 119 | 145 | 171 | 197 | 223 | 249 | 275 | 301 | 327 | 353 | 379 | 405 | 431 | 457 | 483 | 509 | 535 | 561 | 587 | 613 | 639 | 665 | |
| 14 | 40 | 66 | 92 | 118 | 144 | 170 | 196 | 222 | 248 | 274 | 300 | 326 | 352 | 378 | 404 | 430 | 456 | 482 | 508 | 534 | 560 | 586 | 612 | 638 | 664 | |
| 13 | 39 | 65 | 91 | 117 | 143 | 169 | 195 | 221 | 247 | 273 | 299 | 325 | 351 | 377 | 403 | 429 | 455 | 481 | 507 | 533 | 559 | 585 | 611 | 637 | 663 | |
| 12 | 38 | 64 | 90 | 116 | 142 | 168 | 194 | 220 | 246 | 272 | 298 | 324 | 350 | 376 | 402 | 428 | 454 | 480 | 506 | 532 | 558 | 584 | 610 | 636 | 662 | |
| 11 | 37 | 63 | 89 | 115 | 141 | 167 | 193 | 219 | 245 | 271 | 297 | 323 | 349 | 375 | 401 | 427 | 453 | 479 | 505 | 531 | 557 | 583 | 609 | 635 | 661 | |
| 10 | 36 | 62 | 88 | 114 | 140 | 166 | 192 | 218 | 244 | 270 | 296 | 322 | 348 | 374 | 400 | 426 | 452 | 478 | 504 | 530 | 556 | 582 | 608 | 634 | 660 | |
| 9 | 35 | 61 | 87 | 113 | 139 | 165 | 191 | 217 | 243 | 269 | 295 | 321 | 347 | 373 | 399 | 425 | 451 | 477 | 503 | 529 | 555 | 581 | 607 | 633 | 659 | |
| 8 | 34 | 60 | 86 | 112 | 138 | 164 | 190 | 216 | 242 | 268 | 294 | 320 | 346 | 372 | 398 | 424 | 450 | 476 | 502 | 528 | 554 | 580 | 606 | 632 | 658 | |
| 7 | 33 | 59 | 85 | 111 | 137 | 163 | 189 | 215 | 241 | 267 | 293 | 319 | 345 | 371 | 397 | 423 | 449 | 475 | 501 | 527 | 553 | 579 | 605 | 631 | 657 | |
| 6 | 32 | 58 | 84 | 110 | 136 | 162 | 188 | 214 | 240 | 266 | 292 | 318 | 344 | 370 | 396 | 422 | 448 | 474 | 500 | 526 | 552 | 578 | 604 | 630 | 656 | |
| 5 | 31 | 57 | 83 | 109 | 135 | 161 | 187 | 213 | 239 | 265 | 291 | 317 | 343 | 369 | 395 | 421 | 447 | 473 | 499 | 525 | 551 | 577 | 603 | 629 | 655 | |
| 4 | 30 | 56 | 82 | 108 | 134 | 160 | 186 | 212 | 238 | 264 | 290 | 316 | 342 | 368 | 394 | 420 | 446 | 472 | 498 | 524 | 550 | 576 | 602 | 628 | 654 | |
| 3 | 29 | 55 | 81 | 107 | 133 | 159 | 185 | 211 | 237 | 263 | 289 | 315 | 341 | 367 | 393 | 419 | 445 | 471 | 497 | 523 | 549 | 575 | 601 | 627 | 653 | |
| 2 | 28 | 54 | 80 | 106 | 132 | 158 | 184 | 210 | 236 | 262 | 288 | 314 | 340 | 366 | 392 | 418 | 444 | 470 | 496 | 522 | 548 | 574 | 600 | 626 | 652 | |
| 1 | 27 | 53 | 79 | 105 | 131 | 157 | 183 | 209 | 235 | 261 | 287 | 313 | 339 | 365 | 391 | 417 | 443 | 469 | 495 | 521 | 547 | 573 | 599 | 625 | 651 | |
| 0 | 26 | 52 | 78 | 104 | 130 | 156 | 182 | 208 | 234 | 260 | 286 | 312 | 338 | 364 | 390 | 416 | 442 | 468 | 494 | 520 | 546 | 572 | 598 | 624 | 650 | |

First pixel

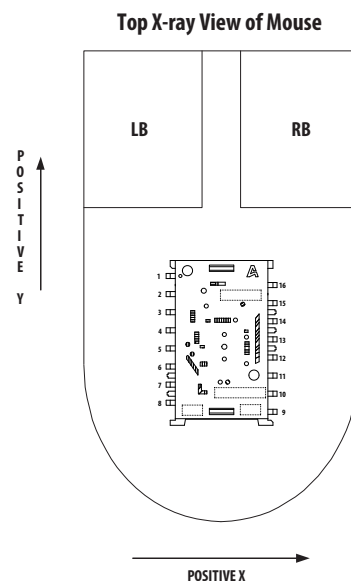


Figure 26. Pixel Address Map (sensor looking on the navigation surface through the lens)

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H_RESOLUTION**Address: 0x36**

Access: Read/Write

Reset Value: 0x04

| | | | | | | | | |
|-------|----------|----------|----------|----------|--------|--------|--------|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | Reserved | Reserved | H_RES_EN | H_RES2 | H_RES1 | H_RES0 | 0 |

Data Type : Bit field

USAGE : This register is used to set the resolution configuration of sensor up to 2000cpi. For resolution setting at 1600cpi and below, configuration via Configuration_Bits register, 0x12 is still effective when H_RES_EN bit is set to zero.

| Field Name | Description |
|------------|--|
| H_RES_EN | 0 = Resolution setting will follow the value as per configuration in Configuration_Bits register, 0x12 1 = Enabled high resolution up to 2000cpi. Resolution setting will follow the configuration as per H_RES2-0 bits in this register and setting in register 0x12 will be ignored. |
| H_RES2-0 | Resolution in count per inch (cpi) 001 = 400 010 = 800 011 = 1200 100 = 1600 101 = 2000 |
| Bit-0 | Must be zero value |

POWER_UP_RESET**Address: 0x3a**

Access: Write

Reset Value: NA

| | | | | | | | | |
|-------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | RST ₇ | RST ₆ | RST ₅ | RST ₄ | RST ₃ | RST ₂ | RST ₁ | RST ₀ |

Data Type: 8 Bit integer

USAGE: Write 0x5a to this register to reset the chip. All settings will revert to default values. Reset is required after recovering from shutdown mode.

SHUTDOWN**Address: 0x3b**

Access: Write Only

Reset Value: NA

| | | | | | | | | |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | SD ₇ | SD ₆ | SD ₅ | SD ₄ | SD ₃ | SD ₂ | SD ₁ | SD ₀ |

Data Type: 8 Bit integer

USAGE: Write 0xe7 to set the chip to shutdown mode, use POWER_UP_RESET register (address 0x3a) to power up the chip.

Reserved**Address: 0x3c**

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ADNS-7550 Integrated Molded Lead-Frame DIP Sensor

Shut_thr Address: 0x3d

Access: Read/Write

Reset Value: 0x56

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|-----------------------|----------|
| Field | Shut_thr ₇ | Shut_thr ₆ | Shut_thr ₅ | Shut_thr ₄ | Shut_thr ₃ | Shut_thr ₂ | Shut_thr ₁ | Reserved |

Data Type: 7 Bit number

USAGE: Threshold defines the Shutter value when lifted runaway happens.

Sensor will suspect lifted runaway happens and suppress motion if (Shutter > Shut_thr[7:1]*32).

Inverse_Revision_ID Address: 0x3e

Access: Read

Reset Value: 0xfc

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Field | NRID ₇ | NRID ₆ | NRID ₅ | NRID ₄ | NRID ₃ | NRID ₂ | NRID ₁ | NRID ₀ |

Data Type: Inverse 8-Bit unsigned integer

USAGE: This value is the inverse of the Revision_ID. It can be used to test the SPI port.

Inverse_Product_ID Address: 0x3f

Access: Write Only

Reset Value: 0xcd

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|-------------------|
| Field | NPID ₇ | NPID ₆ | NPID ₅ | NPID ₄ | NPID ₃ | NPID ₂ | NPID ₁ | NPID ₀ |

Data Type: Inverse 8-Bit unsigned integer

USAGE: This value is the inverse of the Product_ID. It can be used to test the SPI port.

Motion_Burst Address: 0x42

Access: Read

Reset Value: 0x00

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| Field | MB ₇ | MB ₆ | MB ₅ | MB ₄ | MB ₃ | MB ₂ | MB ₁ | MB ₀ |

Data Type: Various

USAGE: Read from this register to activate burst mode. The sensor will return the data in the Motion register, Delta_X_L, Delta_Y_L, Delta_XY_H, Squal, Shutter_Upper, Shutter_Lower and Maximum_Pixel. Reading the first 3 bytes clears the motion data. The read may be terminated anytime after Delta_X is read.