Three-Channel, Isolated Micropower Management Unit with Seven Digital Isolators

Data Sheet

ADP1031

FEATURES

- Wide input supply voltage range: 4.5 V to 60 V
- Integrated flyback power switch
- Generates isolated, independent bipolar outputs and factory programmable buck output
  - V_{OUT1}: 21 V, 24 V or 6 V to 28 V
  - V_{OUT2}: 5.15 V, 5.0 V, or 3.3 V
  - V_{OUT3}: −24 V to −5 V
- Uses a 1:1 ratio transformer for simplified transformer design
- Peak current limiting and OVP for flyback, buck, and inverting regulators
- Precision enable input and power-good output
- Adjustable switching frequency via SYNC input
- Internal compensation and soft start control per regulator
- High speed, low propagation delay, SPI signal isolation channels
- Three, 100 kbps general-purpose isolated data channels
- 9 mm × 7 mm LFCSP form factor enables small overall solution size
- −40°C to +125°C operating junction temperature range
- Conforms to CISPR11 Class B radiated emission limits
- Safety and regulatory approvals (pending)
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A
    - 300 V rms basic insulation between slave, master, and field power domains (IEC 61010-1, pending)
  - VDE certificate of conformity
    - DIN V VDE 0884-10 (VDE 0884-10):2006-12
    - V_{IORM} = 565 V_{PEAK}

APPLICATIONS

- Industrial automation and process control
- Instrumentation and data acquisition systems
- Data and power isolation

GENERAL DESCRIPTION

The ADP1031 is a high performance, isolated micropower management unit (PMU) that combines an isolated flyback dc-to-dc regulator, an inverting dc-to-dc regulator, and a buck dc-to-dc regulator, providing three isolated power rails. Additionally, the ADP1031 contains four, high speed, serial peripheral interface (SPI) isolation channels and three general-purpose isolators for channel to channel applications where low power dissipation and small solution size is required.

TYPICAL APPLICATION CIRCUIT

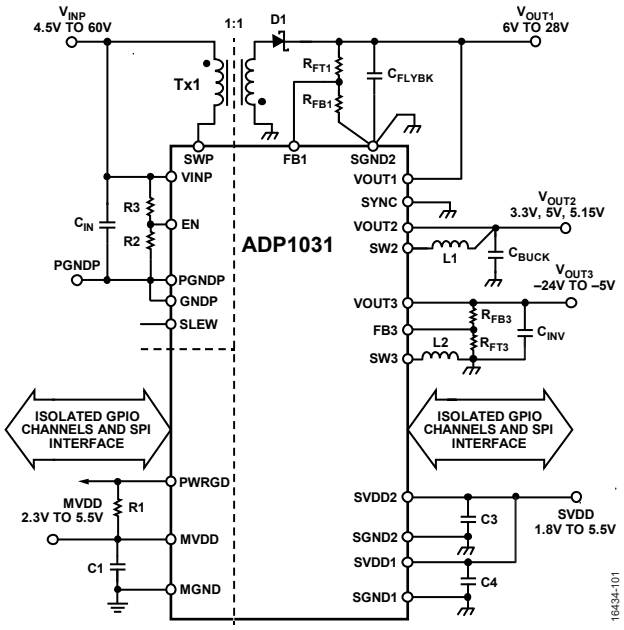

Figure 1.

Operating over an input voltage range of +4.5 V to +60 V, the ADP1031 generates isolated output voltages of +6 V to +28 V (adjustable version) or+ 21 V and +24 V (fixed versions) for V_{OUT1}, factory programmable voltages of +5.15 V, +5.0 V, or +3.3 V for V_{OUT2}, and an adjustable output voltages of −24 V to −5 V for V_{OUT3}.

By default, the ADP1031 flyback regulator operates at a 250 kHz switching frequency and the buck and inverting regulators operate at 125 kHz. All three regulators are phase shifted relative to each other to reduce electromagnetic interference (EMI). The ADP1031 can be driven by an external oscillator in the range of 350 kHz to 750 kHz to ease noise filtering in sensitive applications.

The digital isolators integrated in the ADP1031 use Analog Devices, Inc., *i*Coupler® chip scale transformer technology, optimized for low power and low radiated emissions.

The ADP1031 is available in a 9 mm × 7 mm, 41-lead LFCSP and is rated for a −40°C to +125°C operating junction temperature range.

COMPANION PRODUCTS

Analog Output DAC: AD5758
Precision Data Acquisition Subsystem: AD7768-1
Additional companion products on the ADP1031 product page

Rev. 0 **Document Feedback**

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REVISION HISTORY

1/2019—Revision 0: Initial Version

SPECIFICATIONS

VINP voltage (V_{INP}) = 24 V, MVDD voltage (V_{MVDD}) = 3.3 V, SVDDx voltage (V_{SVDDx}) = 3.3 V, VOUT1 voltage (V_{OUT1}) = 24 V, VOUT2 voltage (V_{OUT2}) = 5.15 V, VOUT3 voltage (V_{OUT3}) = −15 V, and T_A = 25°C for typical specifications. Minimum and maximum specification apply over the entire operating range of 4.5 V ≤ V_{INP} ≤ 60 V, 2.3 V ≤ V_{MVDD} ≤ 5.5 V, 1.8 V ≤ V_{SVDDx} ≤ 5.5 V, and −40°C ≤ T_J ≤ +125°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
INPUT SUPPLY VOLTAGE RANGE						
VINP	V_{INP}	4.5		60	V	
MVDD	V_{MVDD}	2.3		5.5	V	
SVDDx	V_{SVDDx}	1.8		5.5	V	Applies to SVDD1 and SVDD2
OUTPUT POWER AND EFFICIENCY						Transformer = 750316743
Total Output Power			1720		mW	V_{OUT1} current (I_{OUT1}) = 70 mA, V_{OUT2} current (I_{OUT2}) = 7 mA, V_{OUT3} current (I_{OUT3}) = −0.3 mA
			520		mW	I_{OUT1} = 20 mA, I_{OUT2} = 7 mA, I_{OUT3} = −0.3 mA
Efficiency			88.8		%	I_{OUT1} = 70 mA, I_{OUT2} = 7 mA, I_{OUT3} = −0.3 mA
			84.8		%	I_{OUT1} = 20 mA, I_{OUT2} = 7 mA, I_{OUT3} = −0.3 mA
Power Dissipation			216.5		mW	I_{OUT1} = 70 mA, I_{OUT2} = 7 mA, I_{OUT3} = −0.3 mA
			93.1		mW	I_{OUT1} = 20 mA, I_{OUT2} = 7 mA, I_{OUT3} = −0.3 mA
QUIESCENT CURRENT						
VINP						
Operating Current	I_{Q_VINP}		1.77		mA	Normal operation, V_{OUT1}, V_{OUT2}, V_{OUT3} = no load
Shutdown Current	I_{SHDN_VINP}		125	175	µA	EN voltage (V_{EN}) = 0 V
MVDD						
SPI Active Mode	$I_{Q\_MVDD\ (SPI\_ACTIVE)}$		4.1	6.5	mA	V_{Ix}[1] = logic low, $\overline{MSS}$ = logic low
			9.2	14	mA	V_{Ix}[1] = logic high, $\overline{MSS}$ = logic low
SPI Low Power Mode	$I_{Q\_MVDD\ (SPI\_LOWPWR)}$		1.6	2.5	mA	V_{Ix}[1] = logic low, $\overline{MSS}$ = logic high
			1.6	2.5	mA	V_{Ix}[1] = logic high, $\overline{MSS}$ = logic high
SVDD1						
SPI Active Mode	$I_{Q\_SVDD1\ (SPI\_ACTIVE)}$		1.8	2.7	mA	V_{Ix}[1] = logic low, $\overline{SSS}$ = logic low
			5.7	8.6	mA	V_{Ix}[1] = logic high, $\overline{SSS}$ = logic low
SPI Low Power Mode	$I_{Q\_SVDD1\ (SPI\_LOWPWR)}$		1.8	2.7	mA	V_{Ix}[1] = logic low, $\overline{SSS}$ = logic high
			1.8	2.7	mA	V_{Ix}[1] = logic high, $\overline{SSS}$ = logic high
SVDD2	I_{Q_SVDD2}		39	85	µA	V_{Ix}[1] = logic low
			2	2.5	mA	V_{Ix}[1] = logic high
UVLO						
VINP						Relative to PGNDP
Rising Threshold	$V_{UVLO\_FLYBACK\ (RISE)}$		4.44	4.49	V	
Falling Threshold	$V_{UVLO\_FLYBACK\ (FALL)}$	4.29	4.34		V	
Hysteresis			100		mV	
MVDD						Relative to MGND
Rising Threshold	$V_{UVLO\_MVDD\ (RISE)}$		2.14	2.28	V	
Falling Threshold	$V_{UVLO\_MVDD\ (FALL)}$	1.9	2		V	
Hysteresis			140		mV	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
THERMAL SHUTDOWN						
Threshold	T_{SHDN}		150		°C	
Hysteresis	T_{HYS}		15		°C	
PRECISION ENABLE						
Rising Input Threshold	V_{EN_RISING}	1.10	1.135	1.20	V	
Input Hysteresis	V_{EN_HYST}		100		mV	
Leakage Current			0.03	0.5	µA	$V_{EN} = V_{INP}$
POWER GOOD						
Power-Good Threshold						
Flyback Regulator						
Lower Limit	$V_{PG\_FLYBACK\_LL}$	87.5	90	92.5	%	Fixed and adjustable output versions
Upper Limit	$V_{PG\_FYLBACK\_UL}$	107.5	110	112.5	%	Fixed and adjustable output versions
Buck Regulator						
Lower Limit	$V_{PG\_BUCK\_LL}$	87.5	90	92.5	%	
Upper Limit	$V_{PG\_BUCK\_UL}$	107.5	110	112.5	%	
Inverting Regulator						
Lower Limit	$V_{PG\_INVERTER\_LL}$	87.5	90	92.5	%	
Upper Limit	$V_{PG\_INVERTER\_UL}$	107.5	110	112.5	%	
Glitch Rejection			1.36		µs	Glitch of ±15% of the typical output
Output Voltage						
Logic High	V_{PWRGD_OH}	V_{MVDD} − 0.4			V	PWRGD current (I_{PWRGD}) = −1 mA
Logic Low	V_{PWRGD_OL}			0.4	V	I_{PWRGD} = 1 mA
SLEW						
Voltage Level Threshold						
Slow Slew Rate				0.8	V	
Normal Slew Rate		2			V	
Input Current						
Slow Slew Rate		−10			µA	Slew voltage (V_{SLEW}) = 0 V to 0.8 V
Normal Slew Rate				10	µA	V_{SLEW} = 2 V to V_{INP}
Fast Slew Rate		−1		+1	µA	SLEW pin not connected
CLOCK SYNCHRONIZATION						
SYNC Input						
Input Clock						
Range	f_{SYNC}	350		750	kHz	
Minimum On Pulse Width	$t_{SYNC\_MIN\_ON}$	100			ns	
Minimum Off Pulse Width	$t_{SYNC\_MIN\_OFF}$	150			ns	
High Logic	$V_{H\ (SYNC)}$	1.3			V	
Low Logic	$V_{L\ (SYNC)}$			0.4	V	
Leakage Current		−1	0.005	1	µA	SYNC voltage (V_{SYNC}) = V_{SVDDx}
FLYBACK REGULATOR						
Output Voltage Range	$V_{OUT1\ (ADJ)}$	6		28	V	ADP1031ACPZ-1, ADP1031ACPZ-2, and ADP1031ACPZ-3
	$V_{OUT1\ (FIXED)}$		24		V	ADP1031ACPZ-4
	$V_{OUT1\ (FIXED)}$		21		V	ADP1031ACPZ-5
Output Voltage Accuracy		−1.5		+1.5	%	Fixed output options

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Feedback Voltage	V_{FB1}		0.8		V	
Feedback Voltage Accuracy		−1.5		+1.5	%	Adjustable output options
Feedback Bias Current	I_{FB1}			0.05	µA	
Load Regulation	$(\Delta V_{FB1}/V_{FB1})/\Delta I_{OUT1}$		−0.0005		%/mA	I_{OUT1} = 4 mA to 24 mA, I_{OUT2} = 10 mA, I_{OUT3} = −1 mA
Line Regulation	$(\Delta V_{OUT1}/V_{OUT1})/\Delta V_{INP}$		0.0003		%/V	V_{INP} = 16 V to 32 V, I_{OUT1} = 20 mA, I_{OUT2} = 10 mA, I_{OUT3} = −1 mA
Power Field Effect Transistor (FET) On Resistance	$R_{ON\ (FLYBACK)}$		3		Ω	SWP current (I_{SWP}) = 100 mA
Current-Limit Threshold	$I_{LIM\ (FLYBACK)}$	280	300	320	mA	
SWP Leakage Current			0.03	0.5	µA	SWP voltage (V_{SWP}) = 60 V
SWP Capacitance	C_{SWP}		50		pF	
Switching Frequency	$f_{SW\ (FLYBACK)}$	235	250	265	kHz	SYNC = low or high
			$f_{SYNC}/2$		kHz	SYNC = external clock
Minimum On Time			425		ns	
Minimum Off Time			220		ns	
Soft Start Timer	$t_{SS\ (FLYBACK)}$		8		ms	
Severe Overvoltage Threshold	$SOVP_{FLYBACK}$	29.4	30	30.6	V	Flyback regulator stops switching until the overvoltage is removed
Severe Overvoltage Hysteresis	$SOVP_{FLYBACK\_HYST}$		500		mV	
BUCK REGULATOR						
Output Voltage	V_{OUT2}		5.15		V	ADP1031ACPZ-1, ADP1031ACPZ-4, and ADP1031ACPZ-5
			5.0		V	ADP1031ACPZ-2
			3.3		V	ADP1031ACPZ-3
Output Voltage Accuracy		−1.5		+1.5	%	I_{OUT2} = 10 mA, applies to all models
Load Regulation	$(\Delta V_{OUT2}/V_{OUT2})/\Delta I_{OUT2}$		−0.0005		%/mA	I_{OUT2} = 2 mA to 50 mA
Line Regulation	$(\Delta V_{OUT2}/V_{OUT2})/\Delta V_{OUT1}$		0.0004		%/V	V_{OUT1} = 6 V to 28 V, I_{OUT2} = 7 mA
Power FET On Resistance	$R_{ON\_NFET\ (BUCK)}$		1		Ω	SW2 current (I_{SW2}) = 100 mA
	$R_{ON\_PFET\ (BUCK)}$		2.5		Ω	I_{SW2} = 100 mA
Current-Limit Threshold	$I_{LIM\ (BUCK)}$	280	300	320	mA	
SW2 Leakage Current						
P Type Metal-Oxide Semiconductor (PMOS)			0.03	0.5	µA	V_{SW2} = 0 V
N Type Metal-Oxide Semiconductor (NMOS)			0.03	0.5	µA	V_{SW2} = 28 V
Switching Frequency	$f_{SW\ (BUCK)}$	117.5	125	132.5	kHz	SYNC = low or high
			$f_{SYNC}/4$		kHz	SYNC = external clock
Minimum On Time			200		ns	
Soft Start Timer	$t_{SS\ (BUCK)}$		8		ms	
Active Pull-Down Resistor	$R_{PD\ (BUCK)}$		1.7		kΩ	1.23 V < V_{OUT1} < 4.5 V
INVERTING REGULATOR						
Output Voltage Range	V_{OUT3}	−24		−5	V	
Feedback Voltage	V_{FB3}		0.8		V	In reference to V_{OUT3}
Feedback Voltage Accuracy		−1.5		+1.5	%	Adjustable output option
Feedback Bias Current	I_{FB3}			0.05	µA	
Load Regulation	$(\Delta V_{FB3}/V_{FB3})/\Delta I_{OUT3}$		−0.01		%/mA	I_{OUT3} = 1 mA to 15 mA
Line Regulation	$(\Delta V_{OUT3}/V_{OUT3})/\Delta V_{OUT1}$		0.0005		%/V	V_{OUT1} = 6 V to 28 V, I_{OUT3} = −15 mA
Power FET On Resistance	$R_{ON\_NFET\ (INVERTER)}$		1.45		Ω	SW3 current (I_{SW3}) = 100 mA
	$R_{ON\_PFET\ (INVERTER)}$		2.2		Ω	I_{SW3} = 100 mA
Current-Limit Threshold	$I_{LIM\ (INVERTER)}$	280	300	320	mA	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SW3 Leakage Current						
PMOS			0.03	0.5	μA	V_{SW3} = −24 V
NMOS			0.03	0.5	μA	V_{SW3} = 24 V
Switching Frequency	$f_{SW\ (INVERTER)}$	117.5	125	132.5	kHz	SYNC = low or high
			$f_{SYNC}/4$		kHz	SYNC = external clock
Minimum On Time			178		ns	
Soft Start Timer	$t_{SS\ (INVERTER)}$		8		ms	
Active Pull-Down Resistor	$R_{PD\ (INVERTER)}$		350		Ω	1.23 V < V_{OUT1} < 4.5 V
ISOLATORS, DC SPECIFICATIONS						
MCK, $\overline{MSS}$, MO, SO, MGPI1, MGPI2, SGPI3						
Input Threshold						
Logic High	V_{IH}	0.7 × V_{xVDD}			V	V_{xVDD} = V_{MVDD} or V_{SVDDx}
Logic Low	V_{IL}			0.3 × V_{xVDD}	V	V_{xVDD} = V_{MVDD} or V_{SVDDx}
Input Current	I_I	−1		+1	μA	0 V ≤ V_{INPUT} ≤ V_{xVDD}
SCK, $\overline{SSS}$, SI, MI						
Output Voltage						
Logic High	V_{OH}	V_{xVDD} − 0.1			V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{xVDD} − 0.4			V	I_{Ox}[2] = −2 mA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}			0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.15	0.4	V	I_{Ox}[2] = 2 mA, V_{Ix} = V_{IxL}[4]
SGPO1, SGPO2, MGPO3						
Output Voltage						
Logic High	V_{OH}	V_{xVDD} − 0.1			V	I_{Ox}[2] = −20 μA, V_{Ix} = V_{IxH}[3]
		V_{xVDD} − 0.4			V	I_{Ox}[2] = −500 μA, V_{Ix} = V_{IxH}[3]
Logic Low	V_{OL}			0.1	V	I_{Ox}[2] = 20 μA, V_{Ix} = V_{IxL}[4]
			0.15	0.4	V	I_{Ox}[2] = 500 μA, V_{Ix} = V_{IxL}[4]
SCK, SI, MI						
Tristate Leakage		−1	0.01	1	μA	$\overline{MSS}$ = logic high
		−1	0.01	1	μA	V_{Ox}[5] = V_{xVDD}
ISOLATORS, SWITCHING SPECIFICATION						
MCK, $\overline{MSS}$, MO, SO						
SPI Clock Rate	SPI_{MCK}			16.6	MHz	
Latency			100	125	ns	Delay from $\overline{MSS}$ going low to the first data out is valid
Input Pulse Width	t_{PW}	17			ns	Within PWD limit
Input Pulse Width Distortion	t_{PWD}		0.25	6.5	ns	$\lvert t_{PLH} - t_{PHL} \rvert$
Channel Matching						
Codirectional	t_{PSKCD}		0.5	5.5	ns	
Opposing Direction	t_{PSKOD}		0.5	4	ns	

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Propagation Delay	t_{PHL}, t_{PLH}					50% input to 50% output
			7	11	ns	V_{MVDD} = 5 V, V_{SVDD1} = 5 V
			7	12	ns	V_{MVDD} = 3.3V, V_{SVDD1} = 5 V
			7	15	ns	V_{MVDD} = 3.3 V, V_{SVDD1} = 3.3 V
			8.5	12	ns	V_{MVDD} = 2.3 V, V_{SVDD1} = 1.8 V
Jitter			620		ps p-p	V_{MVDD} = 5 V, V_{SVDD1} = 5 V
			100		ps rms	V_{MVDD} = 5 V, V_{SVDD1} = 5 V
			440		ps p-p	V_{MVDD} = 3.3 V, V_{SVDD1} = 5 V
			80		ps rms	V_{MVDD} = 3.3 V, V_{SVDD1} = 5 V
			290		ps p-p	V_{MVDD} = 3.3 V, V_{SVDD1} = 3.3 V
			60		ps rms	V_{MVDD} = 3.3 V, V_{SVDD1} = 3.3 V
			410		ps p-p	V_{MVDD} = 2.3 V, V_{SVDD1} = 1.8 V
			110		ps rms	V_{MVDD} = 2.3 V, V_{SVDD1} = 1.8 V
MGPI1, MGPI2, SGPI3						
Data Rate				100	kbps	
Input Pulse Width	t_{PW}	10			µs	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}			14	µs	50% input to 50% output
Jitter				19.5	µs	
ISOLATORS AC SPECIFICATIONS						
General-Purpose Input/Output (GPIO)						
Output Rise Time/Fall Time	t_R/t_F		2.5		ns	10% to 90%
SPI						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity[6]	|CM|		100		kV/µs	

[1] V_{Ix} is the Channel x logic input, where Channel x can be MCK, MO, SO, MGPI1, MGPI2, or MGPI3.
[2] I_{Ox} is the output current of the pin.
[3] V_{IxH} is the input side, logic high.
[4] V_{IxL} is the input side, logic low.
[5] V_{Ox} is the voltage where the output is pulled.
[6] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining VOUT > 0.8 MVDD and/or SVDDx. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

REGULATORY INFORMATION

See Table 8 and the Insulation Lifetime section for the recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 2. Safety Certifications

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized Under UL 1577 Component Recognition Program	Approved under CSA Component Acceptance Notice 5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
2500 V rms Single Protection	CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: basic insulation at 300 V rms (424 V_{PEAK})	Basic insulation, 565 V_{PEAK}
	CSA 61010-1-12 and IEC 61010-1 third edition: basic insulation at 300 V rms mains, 300 V rms (424 V_{PEAK}) secondary	

ELECTROMAGNECTIC COMPATIBILITY

Table 3.

Regulatory Body	Standard	Comment
SGS-CCSR	CISPR11 Class B	Tested using the system board with the AD5758

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)				
Field Power Domain to Master Domain		2.15	mm min	Measured from field power pins and pads to master pins and pads, shortest distance through air
Field Power Domain to Slave Domain		2.15	mm min	Measured from field power pins and pads to slave pins and pads, shortest distance through air
Master Domain to Slave Domain		2.15	mm min	Measured from master pins and pads to slave pins and pads, shortest distance through air
Minimum External Tracking (Creepage)				
Field Power Domain to Master Domain		2.15	mm min	Measured from field power pins and pads to master pins and pads, shortest distance path along body
Field Power Domain to Slave Domain		2.15	mm min	Measured from field power pins and pads to slave pins and pads, shortest distance path along body
Master Domain to Slave Domain		2.15	mm min	Measured from master pins and pads to slave pins and pads, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		18	µm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303, Part 1
Material Group		II		Material group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

Table 5.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to III	
For Rated Mains Voltage ≤ 300 V rms			I to II	
For Rated Mains Voltage ≤ 400 V rms			I to I	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	565	V_{PEAK}
Input to Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1060	V_{PEAK}
Input to Output Test Voltage, Method A				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	847	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC		678	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	3537	V_{PEAK}
Surge Isolation Voltage	V_{PEAK} = 12.8 kV, 1.2 µs rise time, 50 µs, 50% fall time	V_{IOSM}	4000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Maximum Junction Temperature		T_S	150	°C
Total Power Dissipation at 25°C		P_S	2.48	W
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

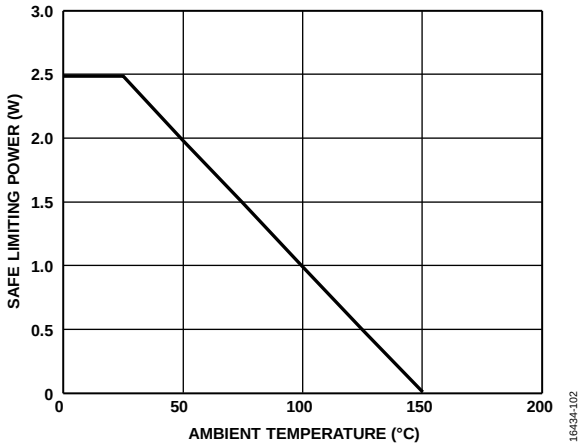


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per DIN V VDE V 0884-10

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VINP to PGNDP	61 V
SWP to VINP	VINP + 70 V or 110 V, whichever is lower
SLEW to GNDP	−0.3 V to VINP + 0.3 V
EN to GNDP	−0.3 V to +61 V
VOUT1 to SGND2	35 V
FB1 to SGND2	−0.3 V to VOUT1 + 0.3 V
VOUT1 to VOUT3	61 V
SW2 to SGND2	−0.3 V to VOUT1 + 0.3 V
VOUT2 to SGND2	6 V
SW3 to SGND2	VOUT3 − 0.3 V to VOUT1 + 0.3 V
VOUT3 to SGND2	−26 V to +0.3 V
FB3 to VOUT3	+3.3 V to −0.3 V
SVDD1 to SGND1	6.0 V
SVDD2 to SGND2	6.0 V
$\overline{SSS}$, SCK, SI, SO to SGND1	−0.3 V to SVDD1 + 0.3 V
SGPO1, SGPO2, SGPI3 to SGND2	−0.3 V to SVDD2 + 0.3 V
SYNC to SGND2	−0.3 V to +6 V
MVDD to MGND	6.0 V
$\overline{MSS}$, MCK, MO, MI to MGND	−0.3 V to MVDD + 0.3 V
MGPI1, MGPI2, MGPO3 to MGND	−0.3 V to MVDD + 0.3 V
PWRGD to MGND	−0.3 V to MVDD + 0.3 V
Common-Mode Transients	±100 kV/µs
Operating Junction Temperature Range[1]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature	JEDEC industry standard
Soldering Conditions	JEDEC J-STD-020

[1] Power dissipated on chip must be derated to keep the junction temperature below 125°C.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is measured at the top of the package and is independent of the PCB. The Ψ_{JT} value is appropriate for calculating junction to case temperature in the application.

Table 7. Thermal Resistance

Package Type[1, 2, 3, 4]	θ_{JA}	θ_{JC}	Ψ_{JT}	Unit
CP-41-1	50.4	33.1	25	°C/W

[1] 9 mm × 7 mm LFCSP with omitted pins for isolation purposes.
[2] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with 19 thermal vias. See JEDEC JESD-51.
[3] Case temperature was measured at the center of the package.
[4] Board temperature was measured near Pin 1.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 8. Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
60 Hz AC Voltage	300 V rms	20-year lifetime at 0.1% failure rate, zero average voltage
DC Voltage	424 V_{PEAK}	Limited by the creepage of the package, Pollution Degree 2, Material Group II[2, 3]

[1] See the Insulation Lifetime section for more details.
[2] Other pollution degree and material group requirements yield a different limit.
[3] Some system level standards allow components to use the printed wiring board (PWB) creepage values. The supported dc voltage may be higher for those standards.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

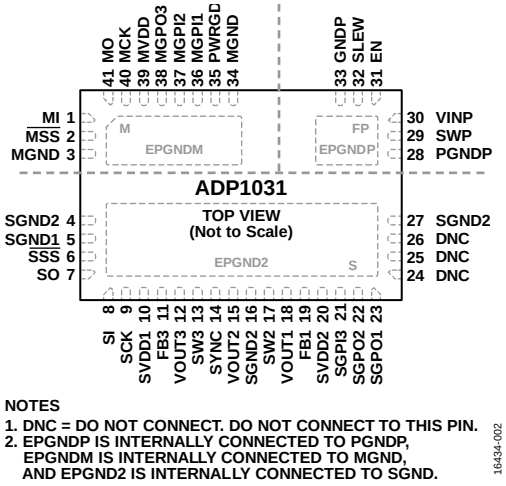


Figure 3. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Isolation Domain	Direction	Description
1	MI	Master	Output	SPI Data Output from the Slave MI and SO Line. This pin is paired with SO. On the slave domain, SO drives this pin.
2	$\overline{\text{MSS}}$	Master	Input	SPI Slave Select Input from the Master Controller. This pin is paired with $\overline{\text{SSS}}$. On the slave domain, this pin drives $\overline{\text{SSS}}$. This signal uses an active low logic.
3	MGND	Master	Return	Master Domain Signal Ground Connection.
4	SGND2	Slave	Return	Slave Domain Ground Connection. This pin can be left unconnected.
5	SGND1	Slave	Return	Slave Domain SPI Isolator Ground.
6	$\overline{\text{SSS}}$	Slave	Output	SPI Slave Select Output. This pin is paired with $\overline{\text{MSS}}$. On the master domain, $\overline{\text{MSS}}$ drives this pin.
7	SO	Slave	Input	SPI Data Input Going to the Master MI and SO Line. This pin is paired with MI. On the master domain, this pin drives MI.
8	SI	Slave	Output	SPI Data Output from the Master MO and SI Line. This pin is paired with MO. On the master domain, MO drives this pin.
9	SCK	Slave	Output	SPI Clock Output from the Master. This pin is paired with MCK. On the master domain, MCK drives this pin.
10	SVDD1	Slave	Power	SPI Isolator Power Supply. Connect a 100 nF decoupling capacitor from SVDD1 to SGND1.
11	FB3	Slave	Not applicable	Inverting Regulator Feedback Pin.
12	VOUT3	Slave	Power	Inverting Regulator Output.
13	SW3	Slave	Not applicable	Inverting Regulator Switch Node.
14	SYNC	Slave	Input	SYNC Pin. To synchronize the switching frequency, connect the SYNC pin to an external clock at twice the required switching frequency. Do not leave this pin floating. Connect a 100 kΩ pull-down resistor to SGND2.
15	VOUT2	Slave	Power	Buck Regulator Output Pin.
16	SGND2	Slave	Return	Slave Power Ground. Ground return for inverting and buck regulator output capacitors.
17	SW2	Slave	Not applicable	Buck Regulator Switch Node.
18	VOUT1	Slave	Power	Flyback Regulator Output Pin.
19	FB1	Slave		Feedback Node for the Flyback Regulator.
20	SVDD2	Slave	Power	GPIO Isolators Power Supply. Connect a 100 nF decoupling capacitor from SVDD2 to SGND2.

Pin No.	Mnemonic	Isolation Domain	Direction	Description
21	SGPI3	Slave	Input	General-Purpose Input 3. This pin is paired with MGPO3.
22	SGPO2	Slave	Output	General-Purpose Output 2. This pin is paired with MGPI2.
23	SGPO1	Slave	Output	General-Purpose Output 1. This pin is paired with MGPI1.
24	DNC	Slave	Not applicable	Do Not Connect. Do not connect to this pin.
25	DNC	Slave	Not applicable	Do Not Connect. Do not connect to this pin.
26	DNC	Slave	Not applicable	Do Not Connect. Do not connect to this pin.
27	SGND2	Slave	Return	Slave Domain Ground Connection. This pin can be left unconnected.
28	PGNDP	Field power	Return	Ground Return for Flyback Regulator Power Supply.
29	SWP	Field power	Not applicable	Flyback Regulator Switching Node. Primary side transformer connection.
30	VINP	Field power	Power	Flyback Regulator Supply Voltage. Connect a minimum of 3.3 µF capacitor from VINP to PGNDP.
31	EN	Field power	Input	Precision Enable. Compare the EN pin to an internal precision reference to enable the flyback regulator output.
32	SLEW	Field power	Input	Flyback Regulator Slew Rate Control. The SLEW pin sets the slew rate for the SWP driver. For the fastest slew rate (best efficiency), leave the SLEW pin open. For the normal slew rate, connect the SLEW pin to VINP. For the slowest slew rate (best EMI performance), connect the SLEW pin to GNDP.
33	GNDP	Field power	Return	Field Power Signal Ground Connection.
34	MGND	Master	Return	Master Domain Power Ground Connection.
35	PWRGD	Master	Return	Power Good. This pin indicates when the secondary side supplies are within their programmed range.
36	MGPI1	Master	Input	General-Purpose Input 1. This pin is paired with SGPO1.
37	MGPI2	Master	Input	General-Purpose Input 2. This pin is paired with SGPO2.
38	MGPO3	Master	Output	General-Purpose Output 3. This pin is paired with SGPI3.
39	MVDD	Master	Power	Master Domain Power. Connect a 100 nF decoupling capacitor from MVDD to MGND.
40	MCK	Master	Input	SPI Clock Input from the Master Controller. Paired with SCK. On the slave domain, this pin drives SCK.
41	MO	Master	Input	SPI Data Input Going to Slave MO and SI Line. Paired with SI. On the slave domain, this pin drives SI.
	EPGNDP	Field power	Return	PGNDP Exposed Pad. This pad is internally connected to PGNDP.
	EPGNDM	Master	Return	MGND Exposed Pad. This pad is internally connected to MGND.
	EPGND2	Slave	Return	SGND Exposed Pad. This pad is internally connected to SGND.

TYPICAL PERFORMANCE CHARACTERISTICS

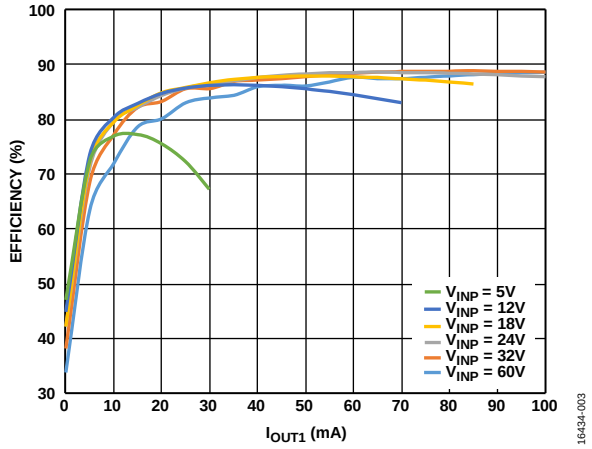


Figure 4. Overall Efficiency at Various Input Voltages, T_A = +25°C, V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, Using a Würth Elektronik 750316743 Transformer

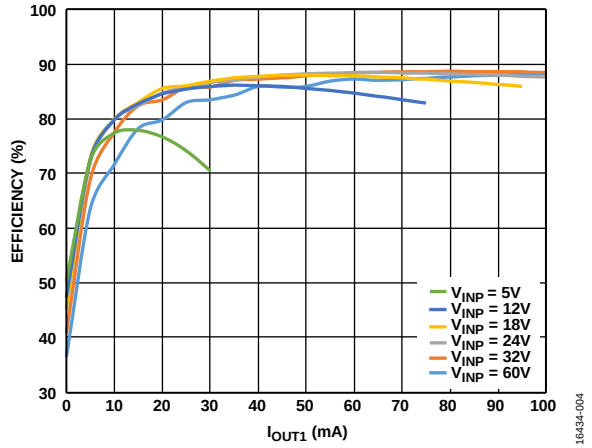


Figure 5. Overall Efficiency at Various Input Voltages, T_A = +25°C, V_{OUT1} = +21 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, Using a Würth Elektronik 750316743 Transformer

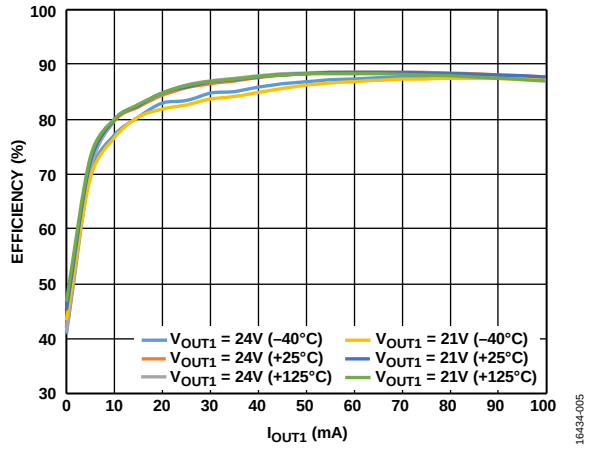


Figure 6. Overall Efficiency across Temperature, V_{INP} = +24 V, V_{OUT1} = +21 V and V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, Using a Würth Elektronik 750316743 Transformer

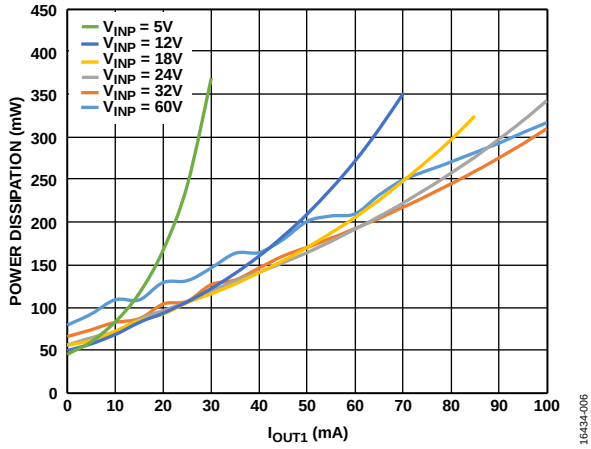


Figure 7. Power Dissipation at Various Input Voltages, T_A = +25°C, V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, T Using a Würth Elektronik 750316743 Transformer

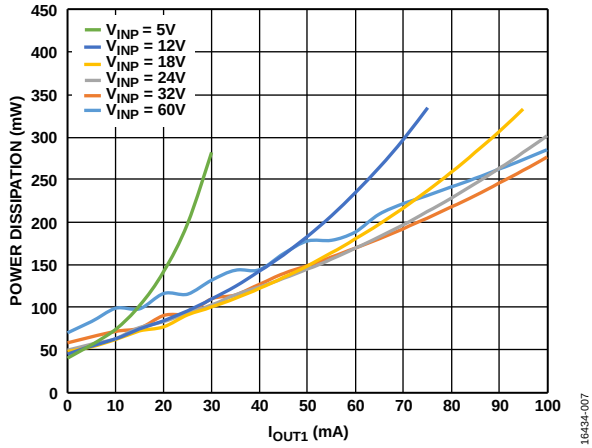


Figure 8. Power Dissipation at Various Input Voltages, T_A = +25°C, V_{OUT1} = +21 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, Using a Würth Elektronik 750316743 Transformer

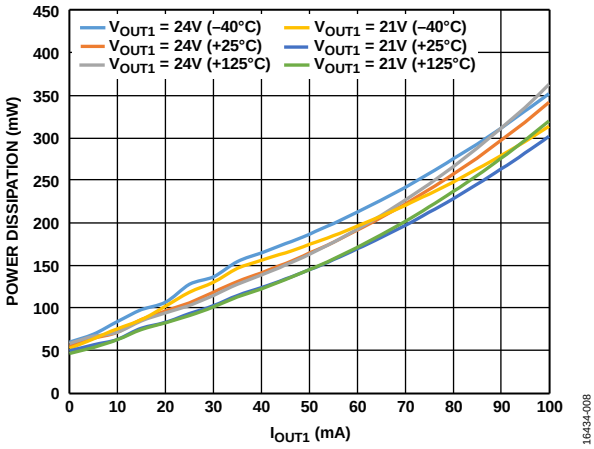


Figure 9. Power Dissipation across Temperature, V_{INP} = +24 V, V_{OUT1} = +21 V and V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA, Using a Würth Elektronik 750316743 Transformer

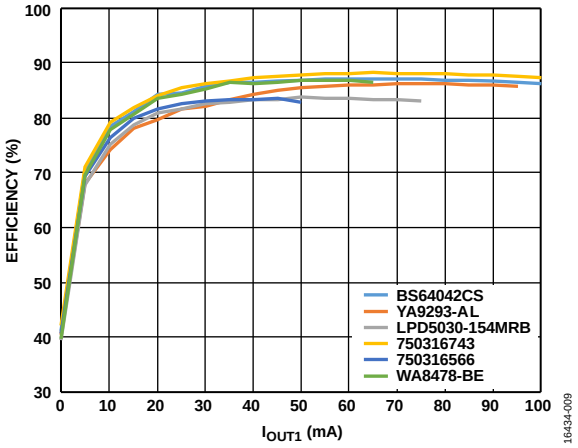


Figure 10. Overall Efficiency using Various Transformers, T_A = +25°C, V_{INP} = +24 V, V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

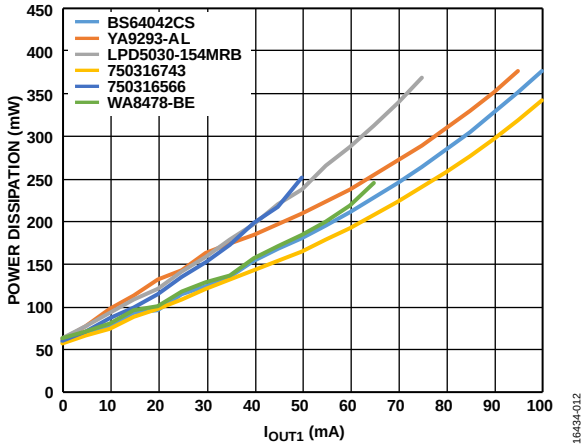


Figure 13. Power Dissipation using Various Transformers, T_A = +25°C, V_{INP} = +24 V, V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

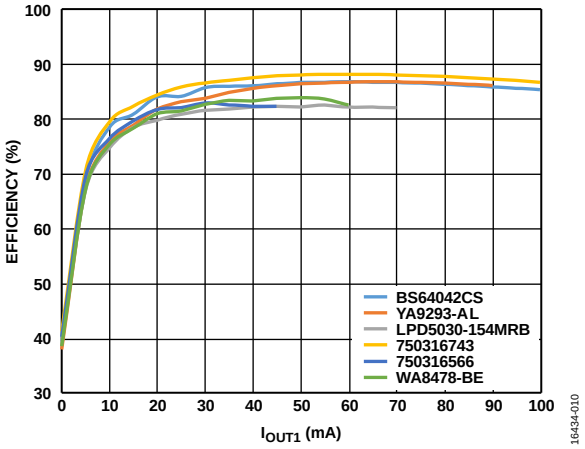


Figure 11. Overall Efficiency using Various Transformers, T_A = +125°C, V_{INP} = +24 V, V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

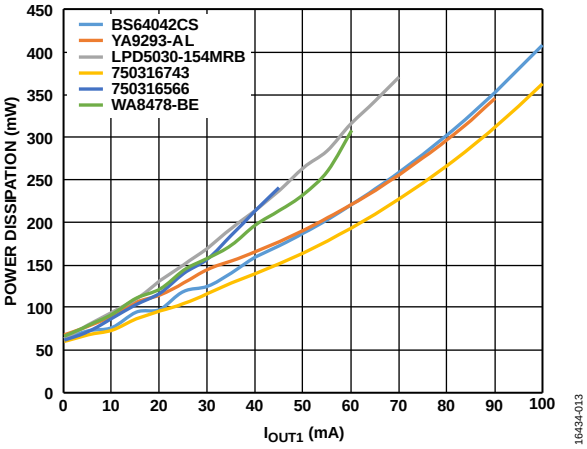


Figure 14. Power Dissipation using Various Transformers, T_A = +125°C, V_{INP} = +24 V, V_{OUT1} = +24 V, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

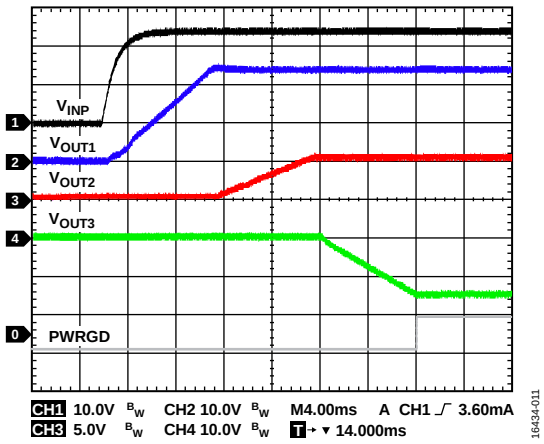


Figure 12. Power-Up Sequence at VINP Rising, T_A = +25°C, V_{INP} = +24 V, V_{OUT1} = +24 V, I_{OUT1} = +20 mA, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

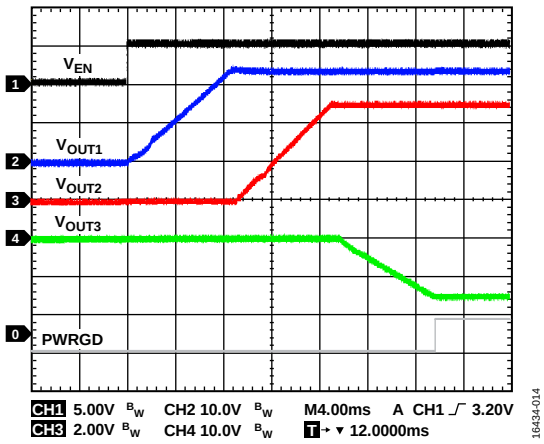


Figure 15. Power-Up Sequence at EN Rising, T_A = +25°C, V_{INP} = +24 V, V_{OUT1} = +24 V, I_{OUT1} = +20 mA, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

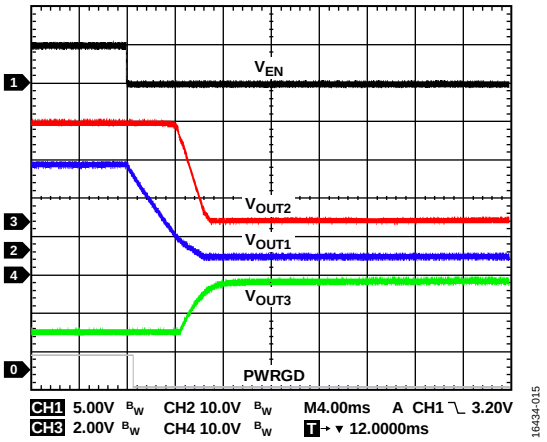


Figure 16. Shutdown Sequence, T_A = +25°C, V_{INP} = +24 V, V_{OUT1} = +24 V, I_{OUT1} = +20 mA, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

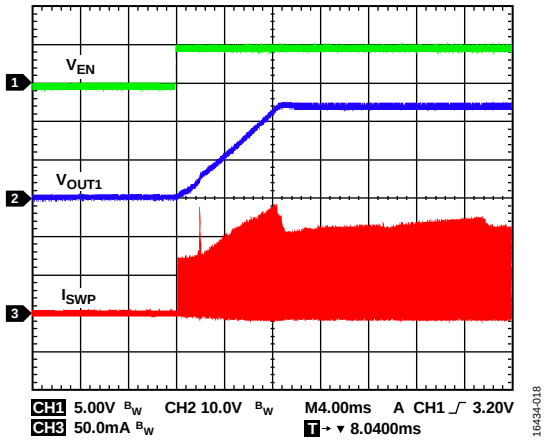


Figure 19. Inrush Current, T_A = +25°C, V_{INP} = +24 V, V_{OUT1} = +24 V, I_{OUT1} = +20 mA, V_{OUT2} = +5.15 V, I_{OUT2} = +7 mA, V_{OUT3} = −15 V, I_{OUT3} = −0.3 mA

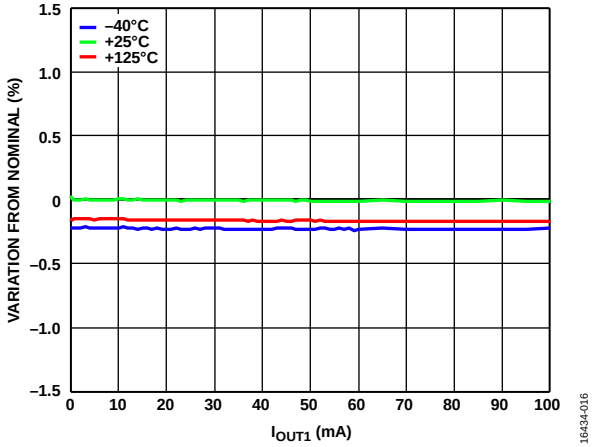


Figure 17. Flyback Regulator Load Regulation Across Temperature, V_{INP} = 24 V, V_{OUT1} = 24 V, Nominal = V_{OUT1} at 20 mA Load

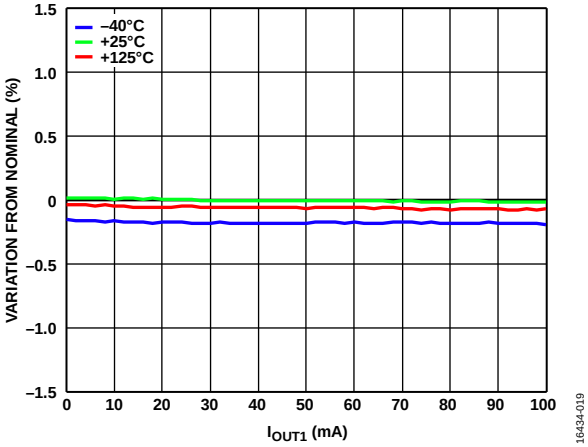


Figure 20. Flyback Regulator Load Regulation Across Temperature, V_{INP} = 24 V, V_{OUT1} = 21 V, Nominal = V_{OUT1} at 20 mA Load

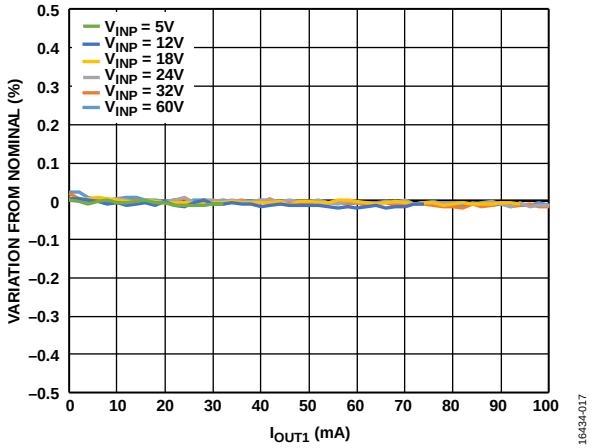


Figure 18. Flyback Regulator Load Regulation at Various Input Voltages, T_A = 25°C, V_{OUT1} = 24 V, Nominal = V_{OUT1} at 20 mA Load

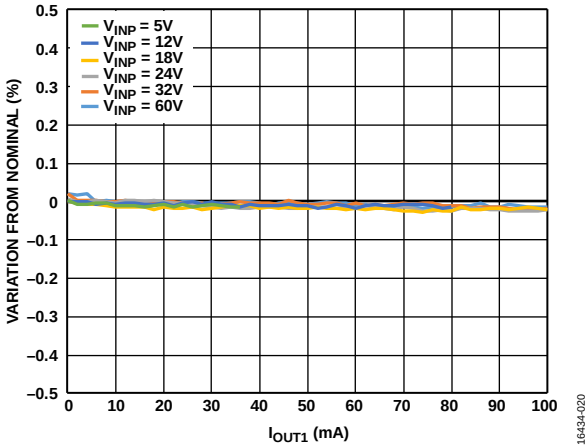


Figure 21. Flyback Regulator Load Regulation at Various Input Voltages, T_A = 25°C, V_{OUT1} = 21 V, Nominal = V_{OUT1} at 20 mA Load

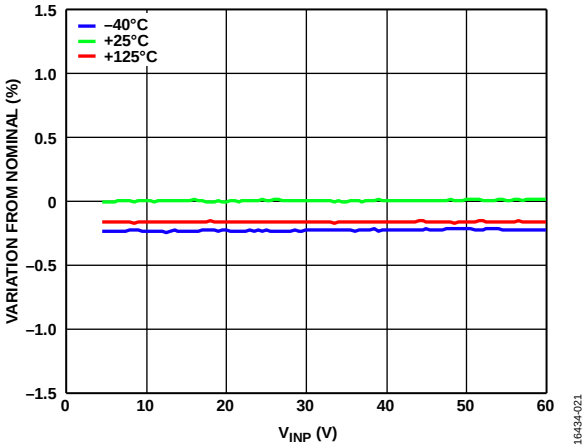


Figure 22. Flyback Regulator Line Regulation Across Temperature, V_{OUT1} = 24 V, I_{OUT1} = 20 mA, Nominal = V_{OUT1} with V_{INP} = 24 V

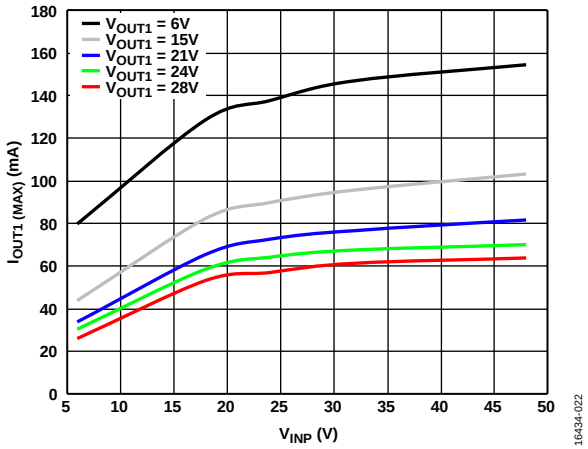


Figure 23. Flyback Regulator Maximum Output Current at Various Output Voltage, T_A = 25°C, Using a Würth Elektronik 750316743 Transformer, Based on Target of 70% $I_{LIM\ (FLYBACK)}$

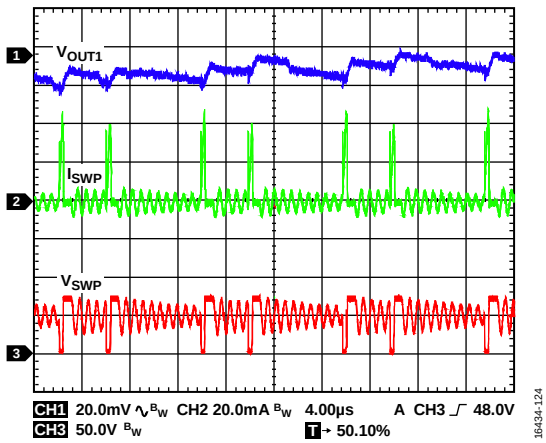


Figure 24. Flyback Regulator Pulse Skipping Operation Showing Inductor Current (I_{SWP}), Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{INP} = 48 V, V_{OUT1} = 24 V, I_{OUT1} = 1 mA

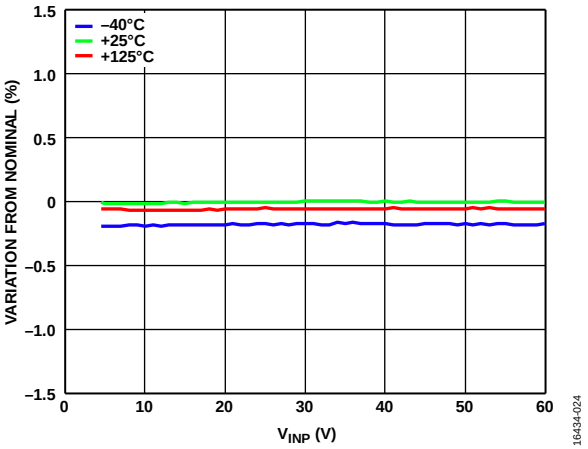


Figure 25. Flyback Regulator Line Regulation Across Temperature, V_{OUT1} = 21 V, I_{OUT1} = 20 mA, Nominal = V_{OUT1} with V_{INP} = 24 V

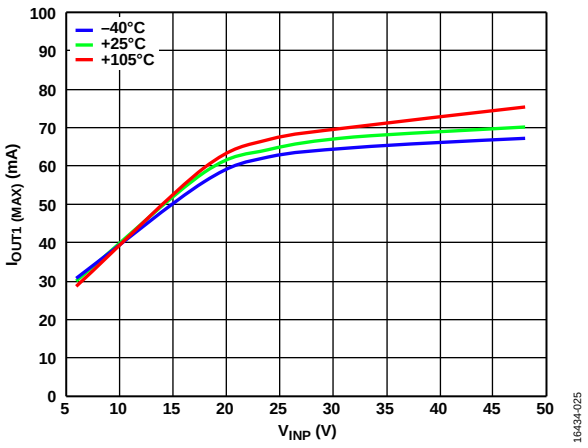


Figure 26. Flyback Regulator Maximum Output Current across Temperature, V_{OUT1} = 24 V, Using a Würth Elektronik 750316743 Transformer, Based on Target of 70% $I_{LIM\ (FLYBACK)}$

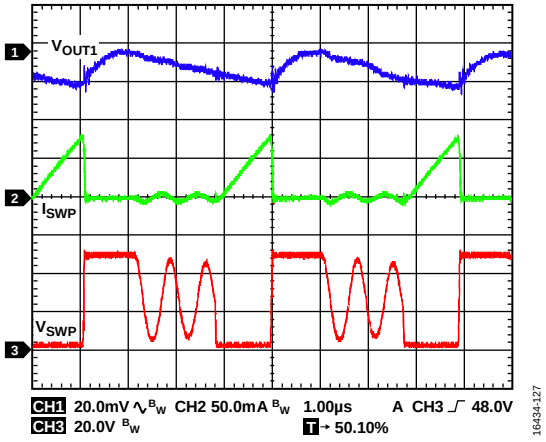


Figure 27. Flyback Regulator Discontinuous Conduction Mode Operation Showing I_{SWP}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{INP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 10 mA

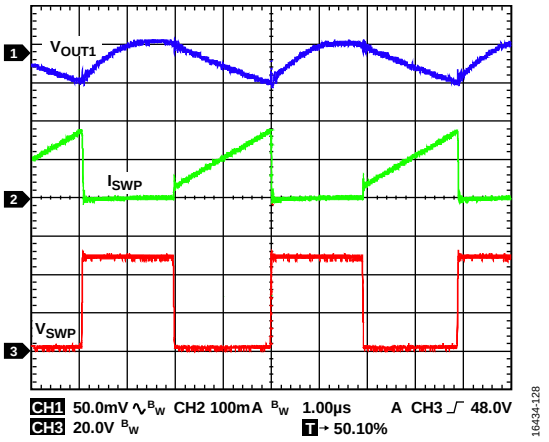


Figure 28. Flyback Regulator Continuous Conduction Mode Operation Showing I_{SWP}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{INP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 50 mA

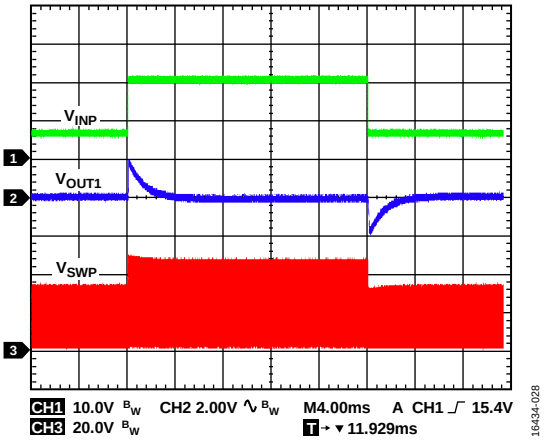


Figure 29. Flyback Regulator Line Transient Response, V_{INP} = 6 V to 20 V Step, V_{OUT1} = 24 V, I_{OUT1} = 20 mA, T_A = 25°C

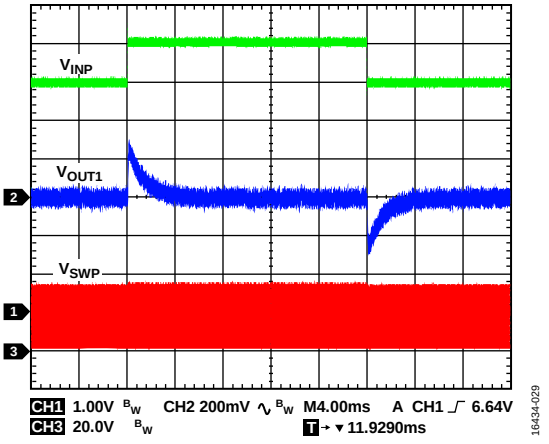


Figure 30. Flyback Regulator Line Transient Response, V_{INP} = 6 V to 7 V Step, V_{OUT1} = 24 V, I_{OUT1} = 20 mA, T_A = 25°C

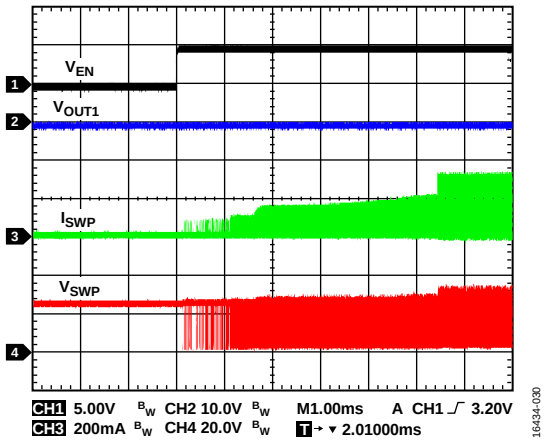


Figure 31. Flyback Regulator Short-Circuit Current Limit During Startup, V_{INP} = 24 V, V_{OUT1} = SGND2, T_A = 25°C

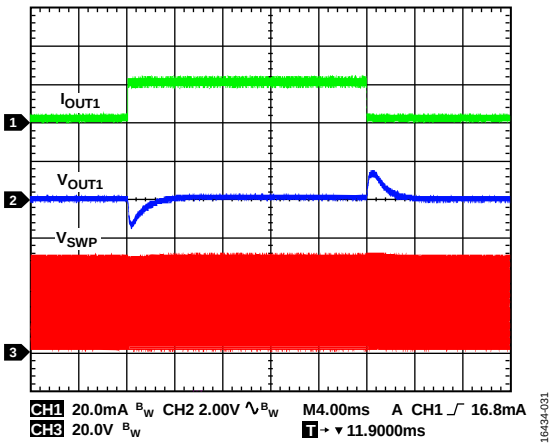


Figure 32. Flyback Regulator Load Transient Response, V_{INP} = 24 V, V_{OUT1} = 24 V, I_{OUT1} = 1 mA to 20 mA Step, T_A = 25°C

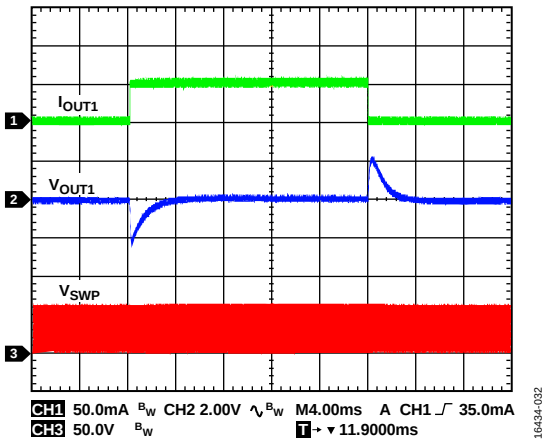


Figure 33. Flyback Regulator Load Transient Response, V_{INP} = 32 V, V_{OUT1} = 24 V, I_{OUT1} = 1 mA to 50 mA Step, T_A = 25°C

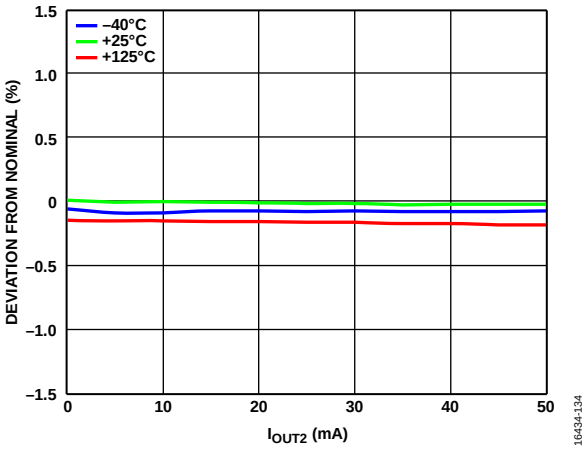


Figure 34. Buck Regulator Load Regulation Across Temperature, V_{OUT1} = 24 V, V_{OUT2} = 5.15 V, Nominal = V_{OUT2} at 10 mA I_{OUT2}

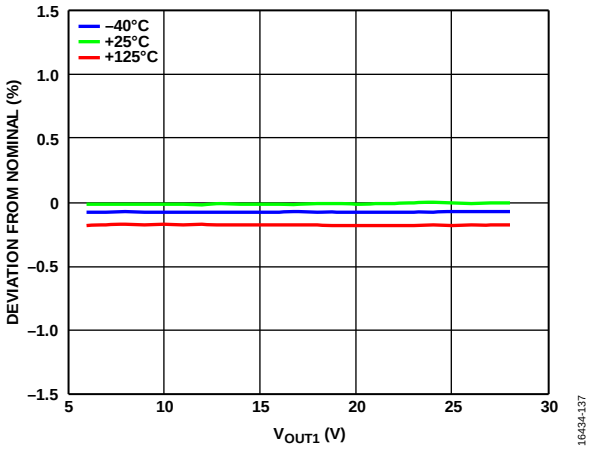


Figure 37. Buck Regulator Line Regulation Across Temperature, V_{OUT2} = 5.15 V, I_{OUT2} = 7 mA, Nominal = V_{OUT2} at 24 V_{OUT1}

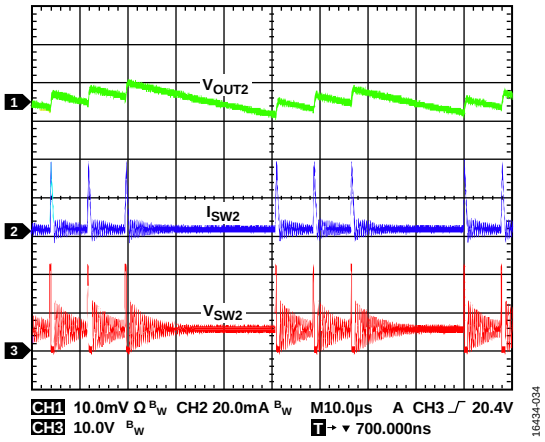


Figure 35. Buck Regulator Pulse Skipping Operation Showing Inductor Current 2 (I_{L2}), Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 24 V, V_{OUT2} = 5.15 V, I_{OUT2} = 0.3 mA

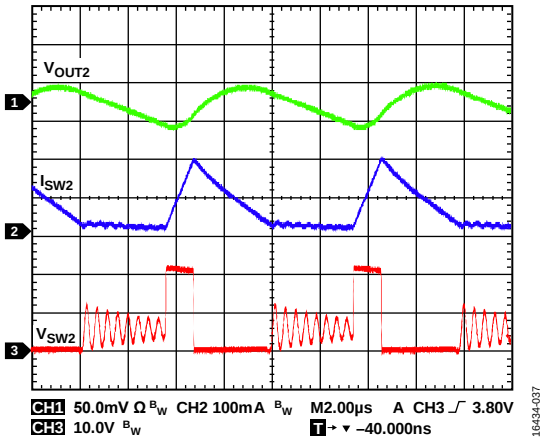


Figure 38. Buck Regulator Discontinuous Conduction Mode Operation Showing I_{L2}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 21 V, V_{OUT2} = 5.15 V, I_{OUT2} = 50 mA

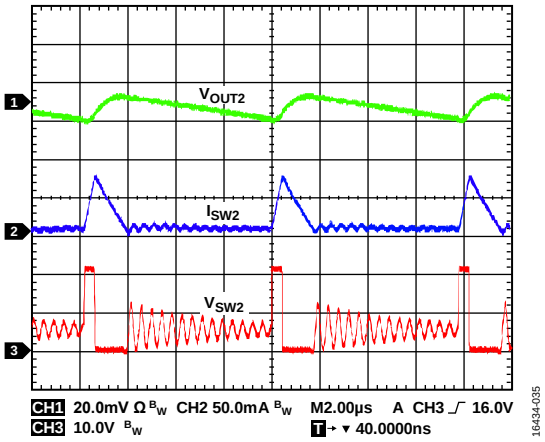


Figure 36. Buck Regulator Discontinuous Conduction Mode Operation Showing I_{L2}, Switch Node Voltage, and Output Ripple, T_A = 25°C, V_{OUT1} = 21 V, V_{OUT2} = 5.15 V, I_{OUT2} = 7 mA

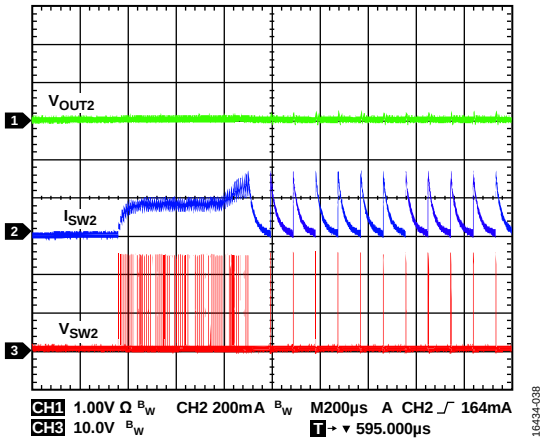


Figure 39. Buck Regulator Short-Circuit Current Limit During Startup, V_{OUT1} = 24 V, V_{OUT2} = SGND2, T_A = 25°C

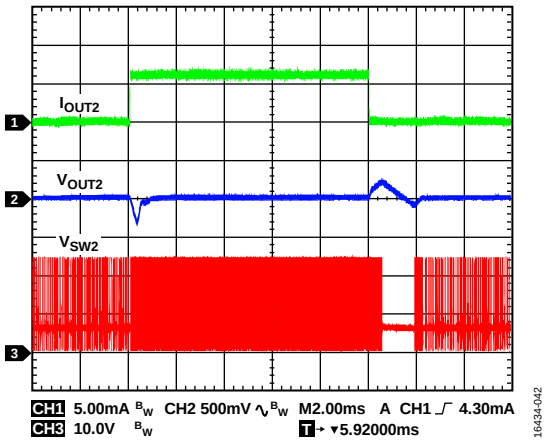


Figure 40. Buck Regulator Load Transient Response, V_{OUT1} = 24 V, V_{OUT2} = 5.15 V, I_{OUT2} = 0.3 mA to 7 mA Step, T_A = 25°C

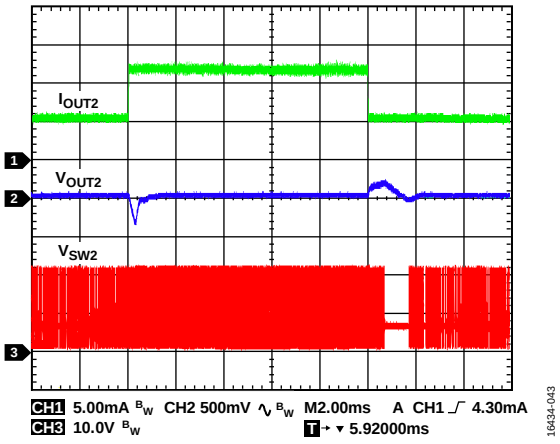


Figure 43. Buck Regulator Load Transient Response, V_{OUT1} = 21 V, V_{OUT2} = 5.15 V, I_{OUT2} = 0.3 mA to 7 mA Step, T_A = 25°C

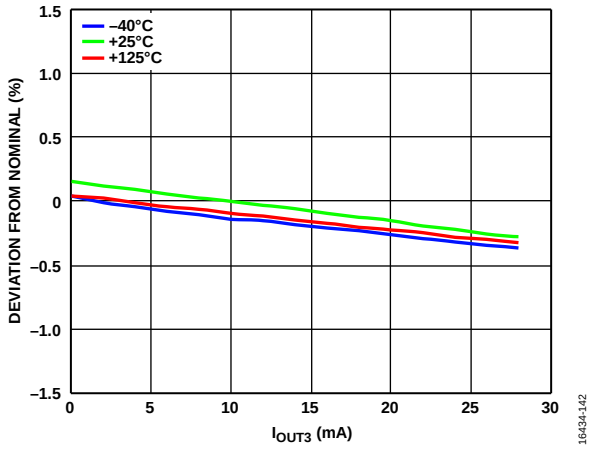


Figure 41. Inverting Regulator Load Regulation Across Temperature, V_{OUT1} = +24 V, V_{OUT3} = −15 V, Nominal = V_{OUT3} at −7 mA I_{OUT3}

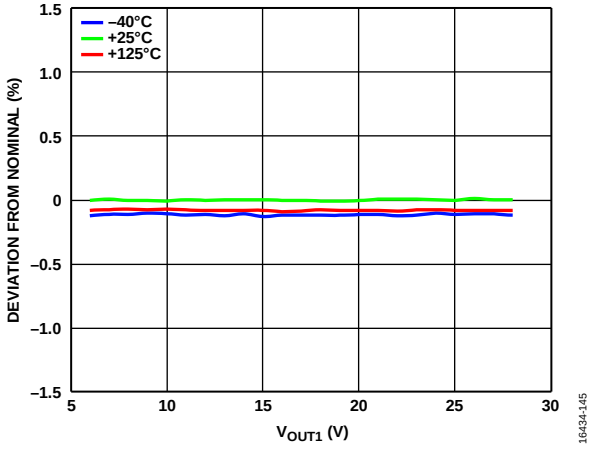


Figure 44. Inverting Regulator Line Regulation Across Temperature, V_{OUT3} = −15 V, I_{OUT3} = −7 mA, Nominal = V_{OUT3} at +24 V_{OUT1}

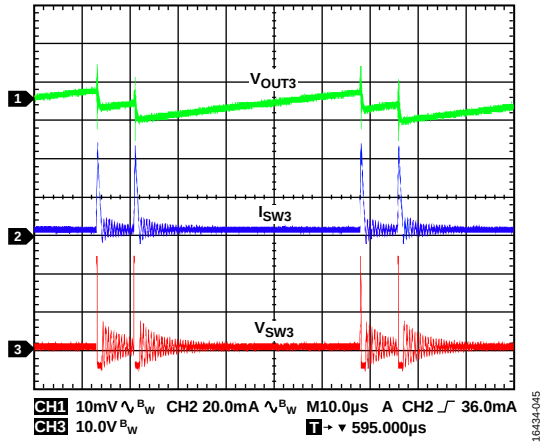


Figure 42. Inverting Regulator Pulse Skipping Operation Showing Inductor Current (I_{L3}), Switch Node Voltage, and Output Ripple, T_A = +25°C, V_{OUT1} = +24 V, V_{OUT3} = −6 V, I_{OUT3} = −0.3 mA

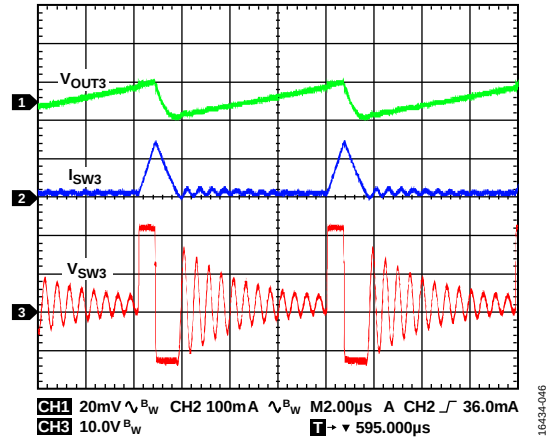


Figure 45. Inverting Regulator Discontinuous Conduction Operation Showing I_{L3}, Switch Node Voltage, and Output Ripple, T_A = +25°C, V_{OUT1} = +24 V, V_{OUT3} = −15 V, I_{OUT3} = −7 mA

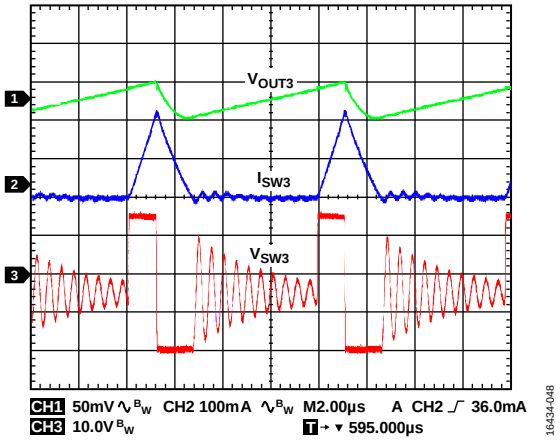


Figure 46. Inverting Regulator Discontinuous Conduction Operation Showing I_{L3}, Switch Node Voltage, and Output Ripple, T_A = +25°C, V_{OUT1} = +24 V, V_{OUT3} = −15 V, I_{OUT3} = −20 mA

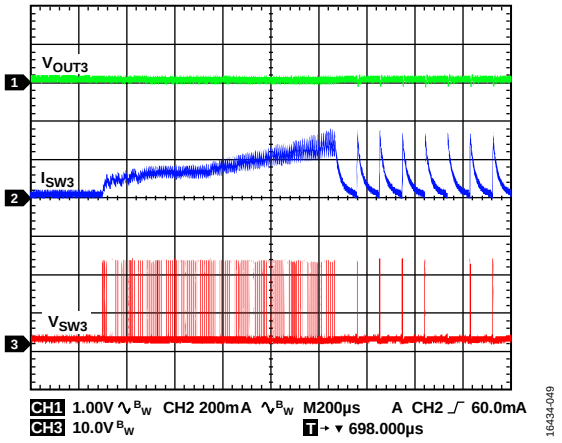


Figure 49. Inverting Regulator Short-Circuit Current Limit During Startup, V_{OUT1} = +24 V, V_{OUT3} = SGND2, T_A = +25°C

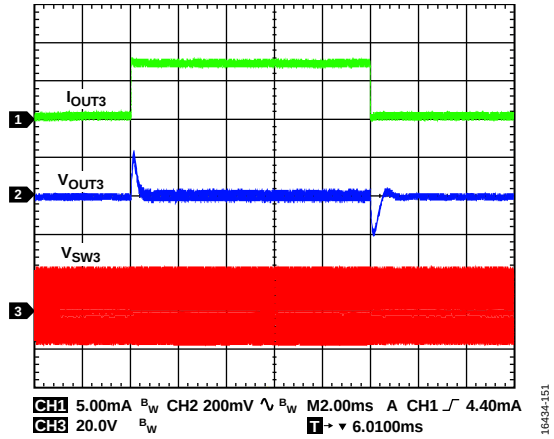


Figure 47. Inverting Regulator Load Transient Response, V_{OUT1} = +24 V, V_{OUT3} = −15 V, I_{OUT2} = −0.3 mA to −7 mA Step, T_A = +25°C

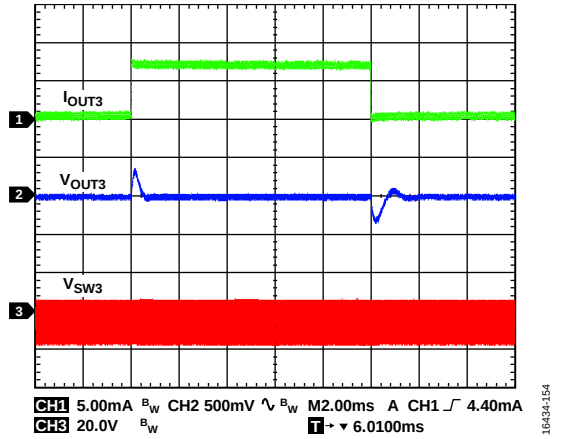


Figure 50. Inverting Regulator Load Transient Response, V_{OUT1} = +6 V, V_{OUT3} = −15 V, I_{OUT2} = −0.3 mA to −7 mA Step, T_A = +25°C

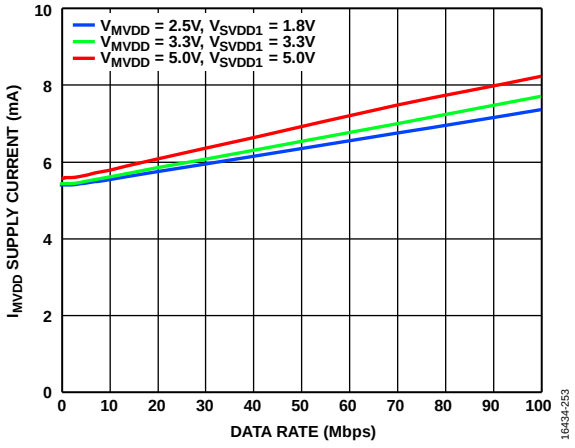


Figure 48. I_{MVDD} Supply Current per SPI Input vs. Data Rate at Various Supply Voltages, $\overline{MSS}$ Is Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

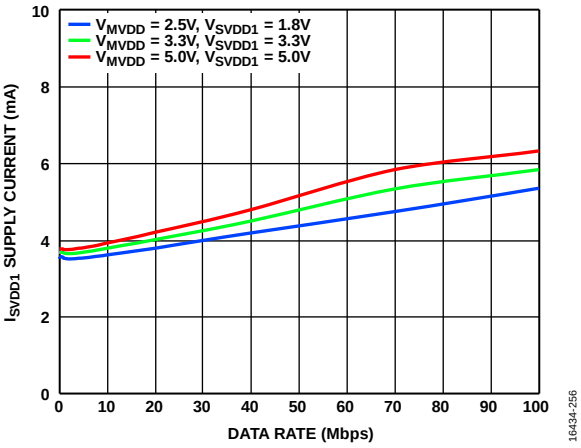


Figure 51. I_{SVDD1} Supply Current per SPI Input vs. Data Rate at Various Supply Voltages, $\overline{SSS}$ Is Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

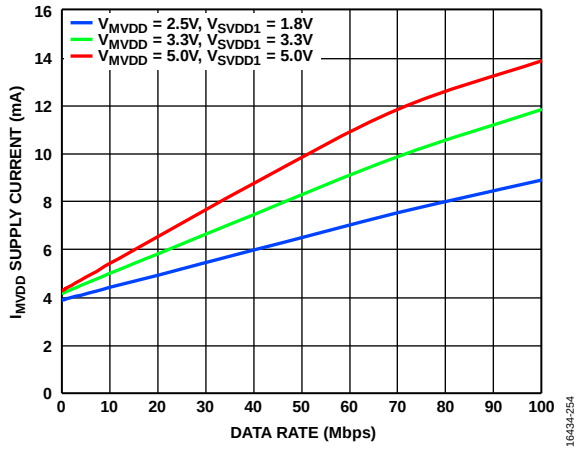


Figure 52. I_{MVDD} Supply Current per SPI Output vs. Data Rate at Various Supply Voltages, $\overline{MSS}$ Is Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

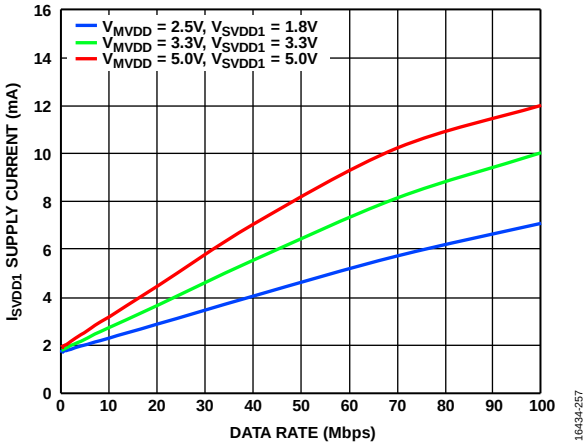


Figure 55. I_{SVDD1} Supply Current vs. Data Rate at Various Supply Voltages, $\overline{SSS}$ Is Low, Clock Signal Applied on Single SPI Channel, Other Input Channels Tied Low

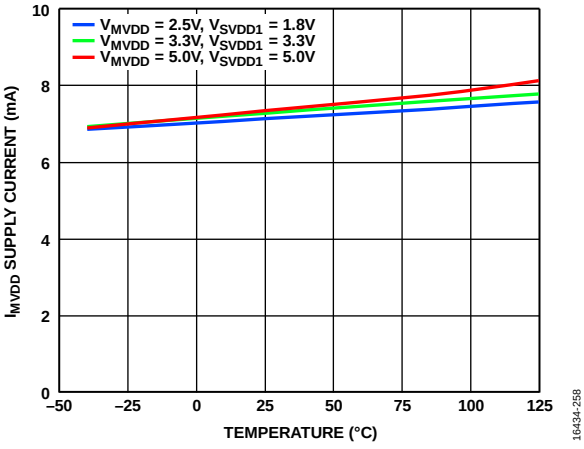


Figure 53. I_{MVDD} Supply Current vs. Temperature at Various Supply Voltages, $\overline{MSS}$ Is Low, Data Rate = 10 Mbps on All SPI Channels

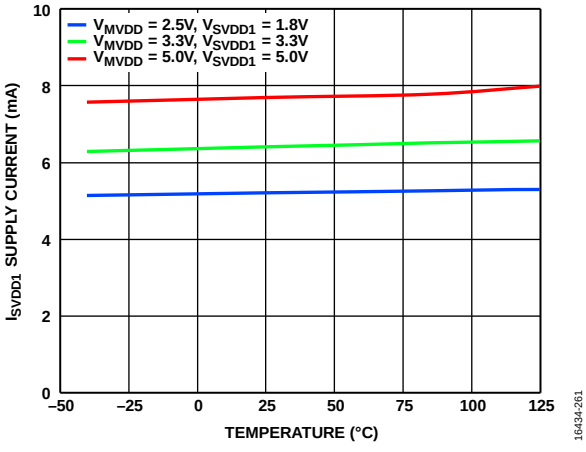


Figure 56. I_{SVDD1} Supply Current vs. Temperature at Various Supply Voltages, $\overline{SSS}$ Is Low, Data Rate = 10 Mbps on All SPI Channels

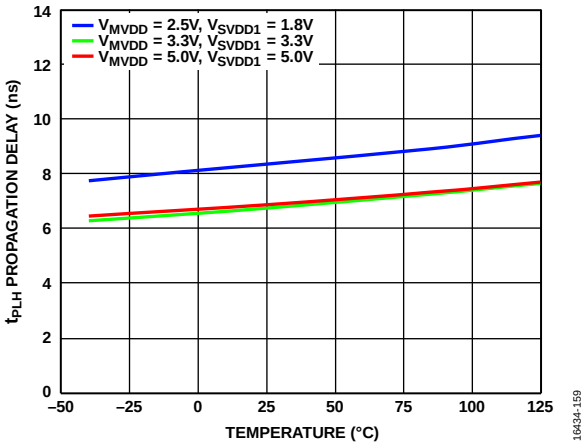


Figure 54. SPI Channels t_{PLH} Propagation Delay vs. Temperature at Various Supply Voltages

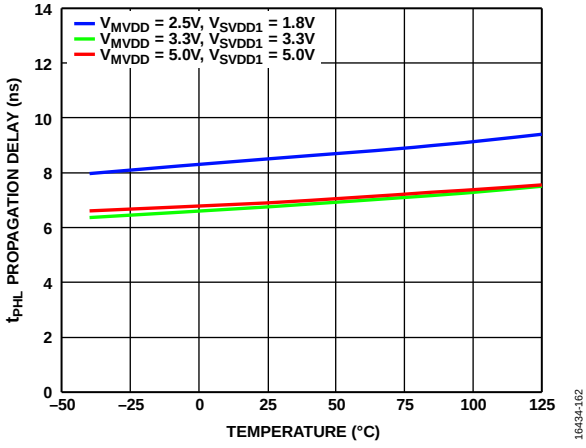


Figure 57. SPI Channels t_{PHL} Propagation Delay vs. Temperature at Various Supply Voltages

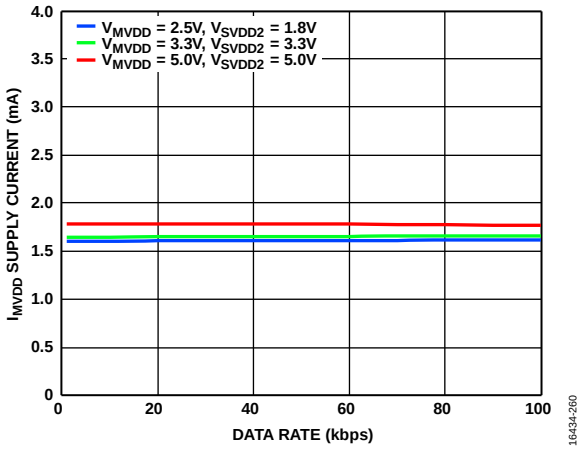


Figure 58. I_{MVDD} Supply Current vs. Data Rate on All GPIO Channels at Various Supply Voltages, $\overline{MSS}$ Is High

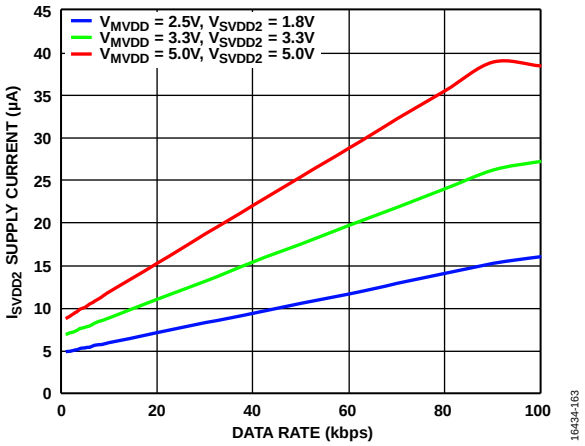


Figure 61. I_{SVDD2} Supply Current vs. Data Rate on All GPIO Channels at Various Supply Voltages, $\overline{MSS}$ Is High

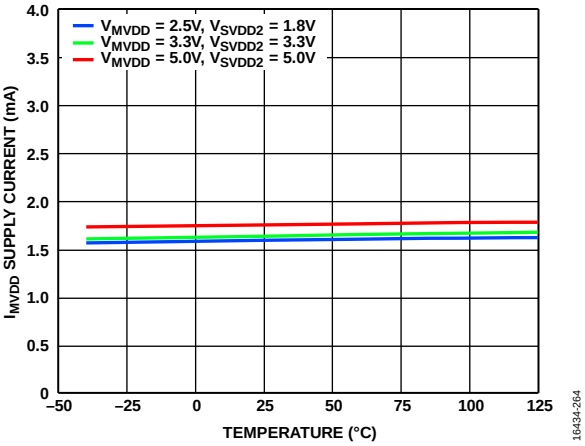


Figure 59. I_{MVDD} Supply Current vs. Temperature at Various Supply Voltages, $\overline{MSS}$ Is Low, Data Rate = 40 kbps on All GPIO Channels

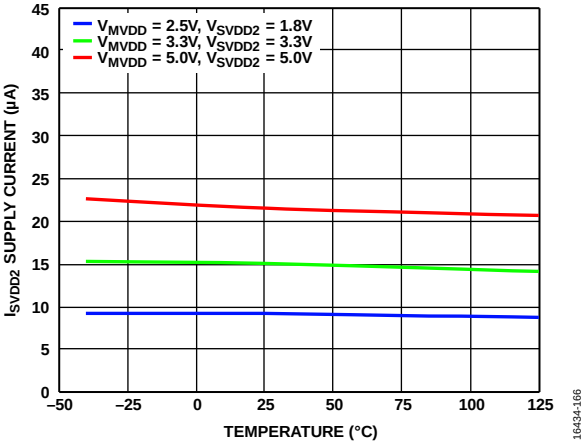


Figure 62. I_{SVDD2} Supply Current vs. Temperature at Various Supply Voltages, $\overline{SSS}$ Is Low, Data Rate = 40 kbps on All GPIO Channels

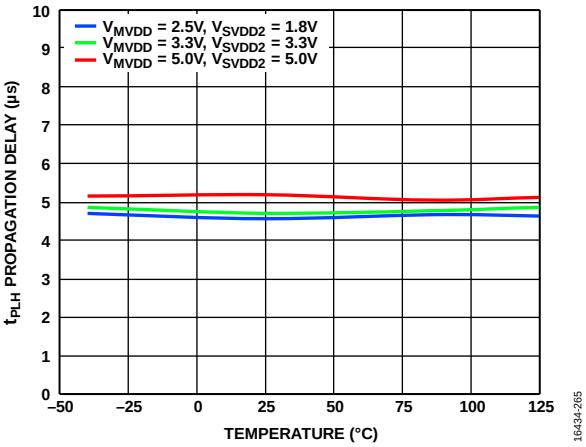


Figure 60. GPIO Channels t_{PLH} Propagation Delay vs. Temperature at Various Supply Voltages

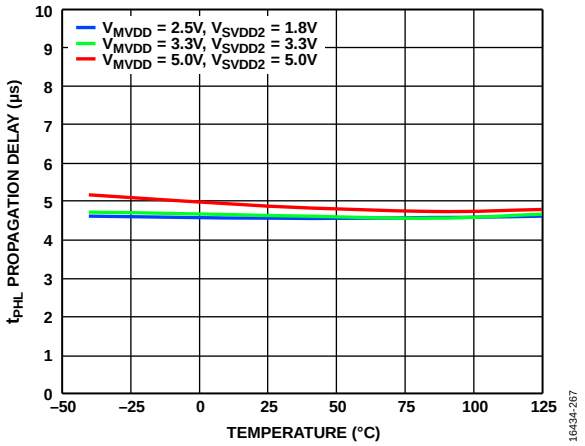


Figure 63. GPIO Channels t_{PHL} Propagation Delay vs. Temperature at Various Supply Voltages

THEORY OF OPERATION

The ADP1031 is a high performance, isolated micro PMU that combines an isolated flyback regulator, an inverting regulator, and a buck regulator, providing three isolated power rails. Additionally, the ADP1031 includes seven low power digital isolators in a 41-lead LFCSP package for channel to channel isolated applications where power dissipation and board space are at a premium.

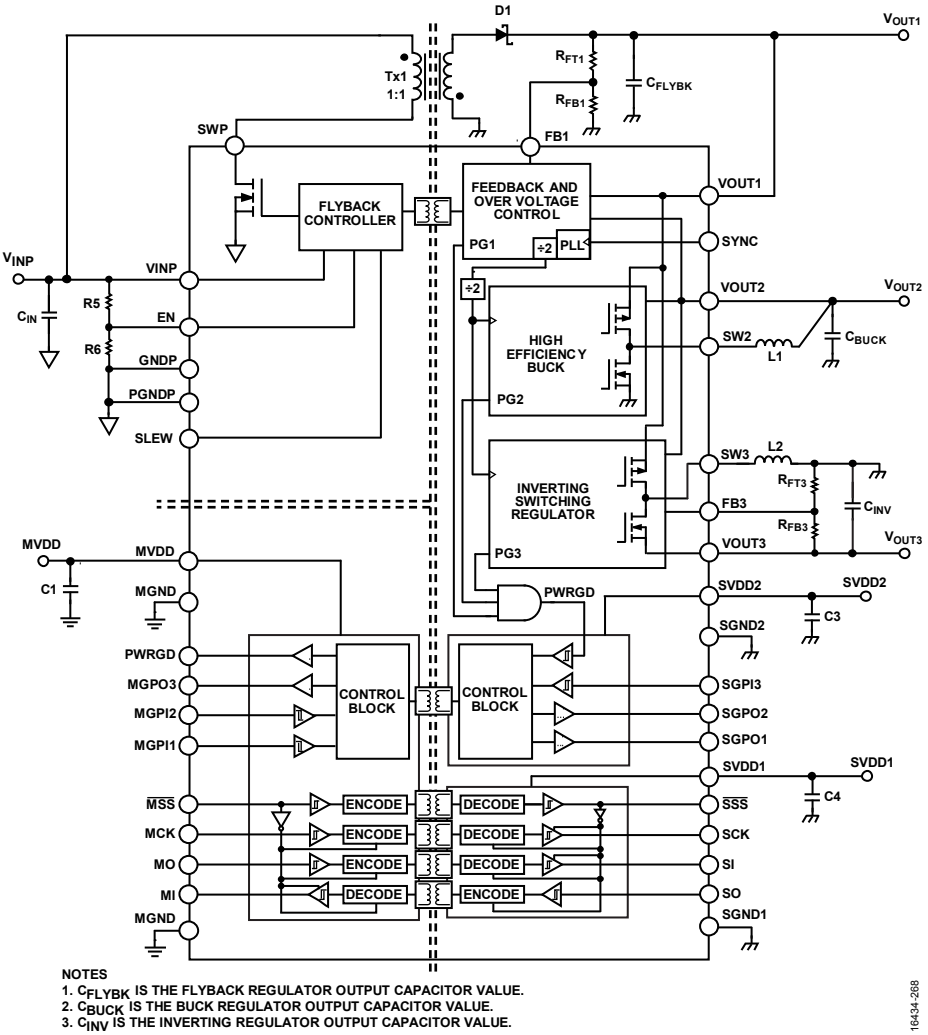


Figure 64. Simplified Block Diagram

FLYBACK REGULATOR

Flyback Regulator Operation

The flyback regulator in the ADP1031 generates an isolated output supply rail that can be programmed from 6 V to 28 V for the adjustable output version or 21 V and 24 V for the factory programmable fixed output versions. The flyback regulator adopts current mode control, resulting in a fast inner current controlled loop that regulates the peak inductor current and a slower outer loop via an isolated *i*Coupler channel that adjusts the current controlled loop to define a regulated output voltage. When the high voltage switch is on, the diode on the secondary side of the transformer is reverse biased, which causes an increase in the current in the primary inductance of the transformer and is stored as energy. When the switch turns off, the diode becomes forward biased and energy stored in the transformer is transferred to the load.

Traditionally, in an isolated flyback regulator, a discrete opto-coupler is used in the feedback path to transmit the signal from the secondary side to the primary side. However, the current transfer ratio (CTR) of the optocouplers degrades over time and over temperature. Therefore, the optocoupler must be replaced every 5 years to 10 years. The ADP1031 eliminates the use of an optocoupler and the associated problems by integrating Analog Devices *i*Coupler technology for feedback, thus reducing system cost, PCB area, and complexity while improving system reliability without the issue of CTR degradation.

A flyback transformer with a single primary and secondary winding is used. This configuration is possible because *i*Coupler technology is used to send an isolated control signal to the primary side controller so that a primary sense winding is not required. In addition, because the secondary and tertiary rails are generated using high efficiency switching regulators, extra secondary windings are not required. This approach offers a number of advantages over an alternative multiwinding solution, such as the following:

- A smaller transformer solution size due to a lower number of turns required on the core and a fewer number of pins.
- Each output can be independently set—the multitap approach requires a custom multitap transformer for different output voltage combinations.
- Outputs are more accurate because the outputs do not rely on the discrete ratios between the transformer windings.
- Output accuracy is unaffected by load changes on each rail.

Power Saving Mode (PSM)

During light load operation, the regulators can skip pulses to maintain output voltage regulation. Therefore, no minimum load is required. Skipping pulses increases the device efficiency but results in larger output ripple.

Flyback Undervoltage Lockout (UVLO)

The UVLO circuitry monitors the VINP pin voltage level. If the input voltage drops below the $V_{UVLO\_FLYBACK\ (FALL)}$ threshold, the flyback regulator turns off. After the VINP pin voltage rises above the $V_{UVLO\_FLYBACK\ (RISE)}$ threshold, the soft start period initiates, and the flyback regulator enables.

Flyback Regulator Precision Enable Control

The flyback regulator in the ADP1031 features a precision enable circuit with an accurate reference voltage. If the voltage at the EN pin rises above the V_{EN_RISING} threshold, the flyback regulator soft start period initiates, and the regulator enables. If the EN pin voltage falls below the $V_{EN\_RISING} - V_{EN\_HYST}$ threshold, the flyback regulator turns off.

Flyback Regulator Soft Start

The flyback regulator includes a soft start function that limits the inrush current from the supply and ramps up the output voltage in a controlled manner. The flyback regulator soft start period initiates when the voltage at the EN pin rises above the V_{EN_RISING} threshold.

Flyback Slew Rate Control

The flyback regulator employs programmable output driver slew rate control circuitry. This circuitry adjusts the slew rate of the switching node as shown in Figure 65, where lower EMI and reduced ringing can be achieved at slightly lower efficiency operation and vice versa. To program the slew rate, connect the SLEW pin to the VINP pin for normal mode, to the GNDP pin for slow mode, or leave it open for fast mode.

Note that slew rate control causes a trade-off between efficiency and low EMI.

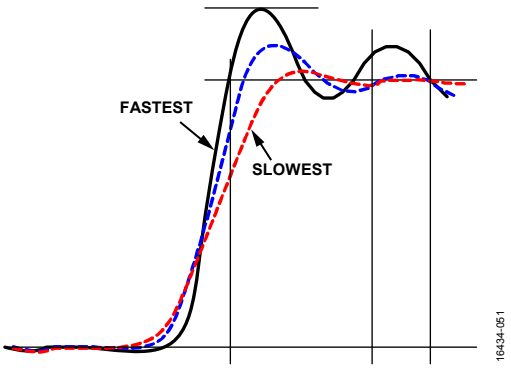


Figure 65. Switching Node at Various Slew Rate Settings

Table 10. Slew Rate Settings

SLEW Pin Connection	Slew Rate	Comment
GNDP	Slow	Lowest EMI
VINP	Normal	Optimized efficiency and EMI
Unconnected	Fast	Highest efficiency

Flyback Regulator Overcurrent Protection

The flyback regulator features a current-limit function that senses the forward current in the switching metal-oxide semiconductor field effect transistor (MOSFET) on a cycle by cycle basis. If the current exceeds the $I_{LIM\ (FLYBACK)}$ threshold, the switch turns off.

Flyback Regulator Overvoltage Protection

The flyback regulator of the ADP1031 implements a number of OVP methods to detect and prevent an overvoltage condition on the flyback regulator output, such as the following:

- If the voltage on the FB1 pin exceeds V_{FB1} by 10% for the adjustable output version, or the VOUT1 pin exceeds the factory programmed V_{OUT1} by 10% for the fixed output version, an OVP fault will be detected, which prevents the flyback regulator switch from turning on. The flyback regulator primary switch stays off until the OVP condition is no longer present.
- If communication across the isolation barrier from the secondary controller to the primary controller fails, the flyback regulator shuts down and a new soft start power-up cycle initiates.
- If the voltage on the output of the flyback regulator exceeds the severe overvoltage threshold ($SOVP_{FLYBACK}$), the primary controller does not turn on the primary side switch. The flyback regulator primary switch stays off until the voltage on the VOUT1 pin falls below the $SOVP_{FLYBACK} - SOVP_{FLYBACK\_HYST}$ threshold.

BUCK REGULATOR

Buck Regulator Operation

The step-down, dc-to-dc (or buck) regulator in the ADP1031 uses a current mode controlled scheme, operating at a fixed frequency set by an internal oscillator. Current mode uses a fast inner current-controlled loop to regulate peak inductor current and a slower outer loop to adjust the current loop to regulate the output voltage. At the start of each oscillator cycle, the high-side MOSFET switch turns on, applying the input voltage to one end of the inductor, which normally causes the buck regulator inductor current (I_{L_BUCK}) to increase until the current sense signal crosses the peak inductor current threshold that turns off the MOSFET switch. The error amplifier output sets this threshold. During the high-side MOSFET off time, the inductor current declines through the low-side MOSFET switch until either the next oscillator clock pulse starts a new cycle that results in continuous conduction mode (CCM) operation, or the inductor current reaches zero, the low-side MOSFET switch is turned off, and the control system waits for the next oscillator clock pulse to start a new cycle, resulting in discontinuous mode (DCM) operation. Under light load conditions, the regulator can skip pulses to maintain regulation and increase power conversion efficiency.

Buck Regulator UVLO

The step-down regulator of theADP1031 features an internal undervoltage lockout circuit that monitors the input voltage to the regulator or VOUT1. If the voltage at VOUT1 drops below the internal threshold level of 4.5 V, the regulator turns off. If the output at VOUT1 rises above the internal threshold, the regulator soft start period initiates, and the regulator enables.

Buck Regulator Soft Start

The step-down regulator in the ADP1031 includes soft start circuitry that ramps the output voltage in a controlled manner during start-up, thereby limiting the inrush current.

Buck Regulator Current-Limit Protection

The step-down regulator in the ADP1031 includes a current-limit protection circuit to limit the amount of forward current through the high-side MOSFET switch. The inductor peak current is monitored cycle by cycle to detect an overload condition. When the overload condition occurs, the current-limit protection limits the peak inductor current to $I_{LIM\ (BUCK)}$, resulting in a drop in the output voltage.

Buck Regulator OVP

The step-down regulator of the ADP1031 features an OVP circuit that monitors the output voltage. If the voltage on the VOUT2 pin exceeds the nominal output voltage by 10%, the step-down, dc-to-dc regulator stops switching until the voltage falls below the threshold again.

Buck Regulator Active Pull-Down Resistor

The buck regulator has an active pull-down resistor that discharges the output capacitor when the output of VOUT1 is between 1.23 V and 4.5 V. The pull-down resistor connects between VOUT2 and SGND2.

INVERTING REGULATOR

Inverting Regulator Operation

The inverting, dc-to-dc regulator in the ADP1031 uses a current mode controlled scheme, operating at a fixed frequency set by an internal oscillator. Current mode uses a fast inner current controlled loop to regulate the peak inductor current and a slower outer loop to adjust the current loop to regulate the output voltage. At the start of each oscillator cycle, the high-side MOSFET switch turns on, applying the input voltage to one end of the inductor, which normally causes the inverting regulator inductor current ($I_{INV\_INDUCTOR}$) to increase until the current sense signal crosses the peak inductor current threshold that turns off the MOSFET switch. The error amplifier output sets this threshold. During the high-side MOSFET off time, the inductor current declines through the low-side MOSFET switch until either the next oscillator clock pulse starts a new cycle, which results in CCM operation, or the inductor current reaches zero, the low-side MOSFET switch is turned off, and the control system waits for the next oscillator clock pulse to start a new cycle, resulting in DCM operation. Under light load conditions, the regulator can skip pulses to maintain regulation and increase power conversion efficiency.

Inverting Regulator UVLO

The inverting, dc-to-dc regulator of the ADP1031 features an internal UVLO circuit that monitors the input voltage to the regulator or VOUT1. If the voltage at VOUT1 drops below the internal threshold level of 4.5 V, the regulator turns off. If the output of VOUT1 rises above the internal threshold, the regulator soft start period initiates, and the regulator enables.

Inverting Regulator Soft Start

The inverting, dc-to-dc regulator in the ADP1031 includes soft start circuitry that ramps the output voltage in a controlled manner during startup, thereby limiting the inrush current.

Inverting Regulator Current-Limit Protection

The inverting, dc-to-dc regulator in the ADP1031 includes a current-limit protection circuit to limit the amount of forward current through the high-side MOSFET switch. The inductor peak current is monitored cycle by cycle to detect an overload condition. When the overload condition occurs, the current-limit protection limits the peak inductor current to $I_{LIM\ (INVERTER)}$, resulting in a drop in the output voltage.

Inverting Regulator OVP

The inverting, dc-to-dc regulator of the ADP1031 features an OVP circuit that monitors the voltage on the FB3 pin. If the voltage on this pin falls below V_{FB3} by 10%, the inverting regulator stops switching until the voltage rises above the threshold again.

Inverting Regulator Active Pull-Down Resistor

The inverting regulator has an active pull-down resistor that discharges the output capacitor when the output of VOUT1 is between 1.23 V and 4.5 V. The pull-down resistor connects between VOUT3 and SGND2.

POWER GOOD

The ADP1031 provides a push pull, power-good output to indicate when the three isolated output voltage rails are valid. The PWRGD pin pulls high when the voltages on the three supplies are within the respective power-good threshold limits.

POWER-UP SEQUENCE

The power-up sequence is as follows (see Figure 66):

1. The flyback regulator powers up first (see 1 in Figure 66).
2. When VOUT1 rises above the lower power-good threshold ($V_{PG\_FLYBACK\_LL}$), the buck regulator turns on (see 2 in Figure 66).
3. When the buck regulator output (VOUT2) rises above the lower power-good threshold ($V_{PG\_BUCK\_LL}$), the inverting regulator turns on (see 3 in Figure 66).
4. PWRGD is driven high when the inverting regulator output (VOUT3) is below the power-good threshold, $V_{PG\_INVERTER\_LL}$ (see 4 in Figure 66).
5. If any of the three analog supplies move outside the power-good threshold ranges, PWRGD drives low after a short deglitch delay (see 5 in Figure 66).

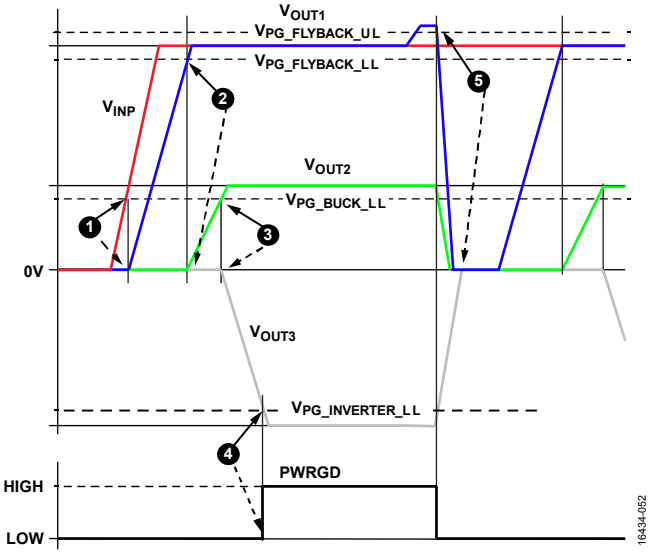


Figure 66. Power-Up Sequencing and PWRGD

OSCILLATOR AND SYNCHRONIZATION

A phase-locked loop (PLL)-based oscillator generates the internal clock for the flyback, buck, and inverter regulators and offers an internally generated frequency or external clock synchronization. Connect the SYNC pin as describe in Table 11 to configure the switching frequency. For external synchronization, connect the SYNC pin to a suitable clock source. The PLL locks to an input clock within the range specified by f_{SYNC}.

Table 11. Sync Pin Functionality

	Switching Frequency (f_{SW})		
SYNC Pin State, f_{SYNC}	**Flyback**	**Buck**	**Inverter**
Low or High	250 kHz	125 kHz	125 kHz
350 kHz to 750 kHz	$f_{SYNC} \div 2$	$f_{SYNC} \div 4$	$f_{SYNC} \div 4$

THERMAL SHUTDOWN

If the ADP1031 junction temperature rises above T_{SHDN}, the thermal shutdown circuit turns the flyback regulator off. Extreme junction temperatures can be the result of prolonged high current operation, poor circuit board design, and/or high ambient temperatures. When thermal shutdown occurs, hysteresis is included so that the ADP1031 does not return to operation until the on-chip temperature drops below $T_{SHDN} - T_{HYS}$. When resuming from thermal shutdown, the ADP1031 performs a soft start.

DATA ISOLATION

High Speed SPI Channels

The ADP1031 has four high speed channels. The first three, CLK, MI/SO, and MO/SI (the slash indicates the connection of the input and output forming a datapath across the isolator that corresponds to an SPI bus signal) are optimized for low propagation delay. With a maximum propagation delay of 15 ns, the ADP1031 supports read and write clock rates up to 16.6 MHz in the standard 4-wire SPI. However, the total round trip delay of the system determines the maximum clock rate and is less than that value.

The relationship between the SPI signal paths, the ADP1031 pin mnemonics, and the data directions are detailed in Table 12.

Table 12. Correspondence of the Pin Mnemonics to the SPI Signal Path Names

SPI Signal Path	Master Side	Data Direction	Slave Side
CLK	MCK	→	SCK
MO/SI	MO	→	SI
MI/SO	MI	←	SO
$\overline{SS}$	$\overline{MSS}$	→	$\overline{SSS}$

The datapaths are SPI mode agnostic. The CLK and MO/SI SPI datapaths are optimized for propagation delay and channel to channel matching. The MI/SO SPI datapath is optimized for propagation delay. The device does not synchronize to the clock channels. Therefore, there are no constraints on the clock polarity or timing with respect to the data lines.

$\overline{SS}$ (slave select bar) is an active low signal. To save power in a multichannel system, $\overline{SS}$ puts the other SPI isolator channels in a low power state when the channels are not in use ($\overline{SS}$ = high), and these channels are only active when required, which is when $\overline{SS}$ is low. The clock and data channels are gated to the $\overline{SS}$ as shown in Figure 67. However, this power saving mode adds 100 ns of latency. This latency is the time required for the internal circuitry to wake up from the low power state and to start transmitting data to the isolation barrier. Conversely, the latency is the delay from the falling edge of $\overline{MSS}$ to the first clock edge or data edge that appears on the slave side, as shown in Figure 68.

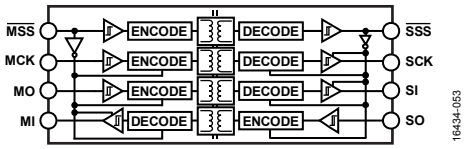


Figure 67. iCoupler Gating

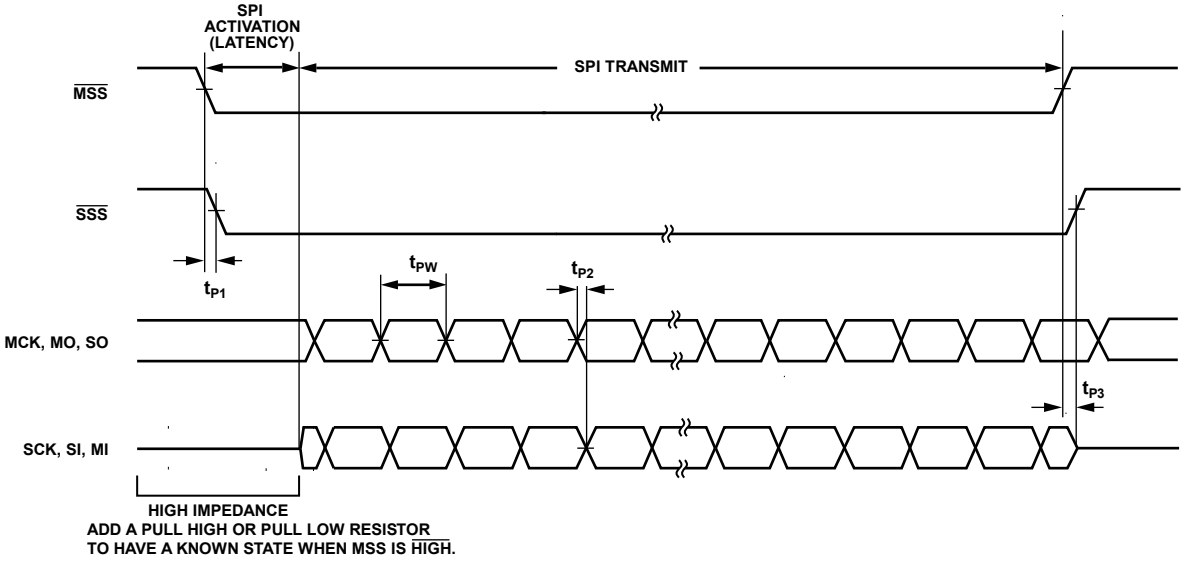


Figure 68. SPI Isolators Timing Diagram

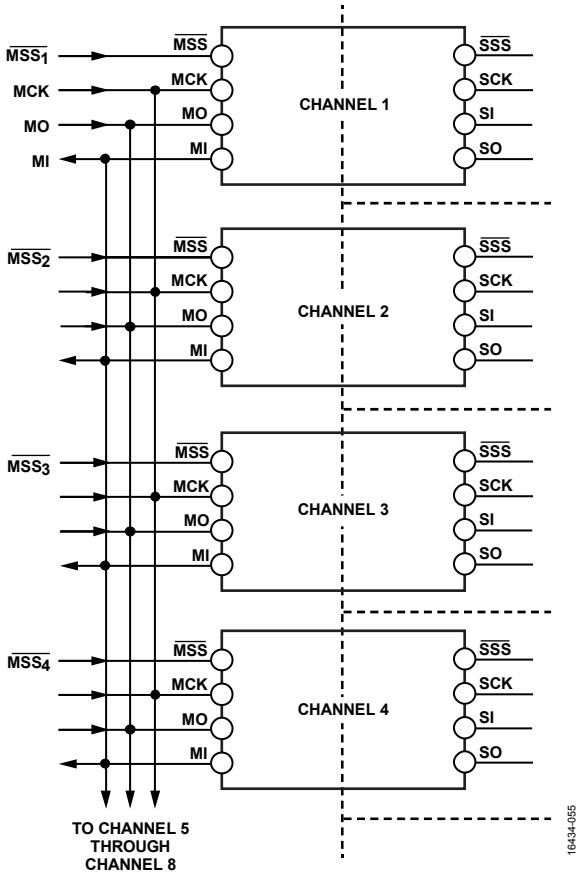


Figure 69. Multichannel SPI Muxing Scheme

The MI, SCK, and SI outputs are also tristated when $\overline{\text{MSS}}$ is high (see Table 13) to allow a more flexible design and to avoid the requirement for external multiplexing of MI in a multichannel system. Figure 69 shows how the SPI busses from multiple ADP1031 devices can be connected together.

Table 13. SPI $\overline{\text{MSS}}$ Gating

Parameter	$\overline{\text{MSS}}$ High	$\overline{\text{MSS}}$ Low
$\overline{\text{SSS}}$	High	Low
SCK	Tristate	MCK
SI	Tristate	MO
MI	Tristate	SO

Connect a pull-up or pull-down resistor to MI, SCK, and SI to pull these pins to the desired logic state when $\overline{\text{MSS}}$ is high.

GPIO Data Channels

The general-purpose data channels are provided as space-saving isolated datapaths where timing is not critical. The dc value of all low speed general-purpose inputs, on a given side of the device, are sampled simultaneously, packetized, and shifted across a single isolation coil. The process is then reversed by reading the inputs on the opposite side of the device, packetizing the inputs and sending these inputs back for similar processing. Because of the sampled nature of this process, the general-purpose data channels exhibit a sampling uncertainty that resembles 19.5 µs peak jitter.

For proper operation of the GPIO channels, refer to Table 14. Power both MVDD and SVDD2 within the specified input voltage range for these pins.

Table 14. Truth Table for GPIO Channels

MVDD State	SVDD2 State	xGPIx	MGPOx	SGPOx	Test Conditions/Comments
Unpowered	Powered	Don't care	Low	Low	During startup
Powered	Unpowered	Don't care	Low	Low	During startup
Powered	Powered	High	High	High	Normal operation
Powered	Powered	Low	Low	Low	Normal operation
Powered	Powered to Unpowered	Don't care	Hold	Low	Hold means that the current state of the outputs are preserved
Powered to Unpowered	Powered	Don't care	Low	Hold	Hold means that the current state of the outputs are preserved

APPLICATIONS INFORMATION

COMPONENT SELECTION

Feedback Resistors

The ADP1031 provides an adjustable output voltage for both flyback and inverting regulators. An external resistor divider sets the output voltage where the divider output must equal the appropriate feedback reference voltage, V_{FB1} or V_{FB3}. To limit the output voltage accuracy degradation due to the feedback bias current, ensure that the current through the divider is at least 10 times I_{FB1} or I_{FB3}. The recommended R_{FB1} and R_{FB3} values are in the range of 50 kΩ to 250 kΩ to minimize the output voltage error due to the bias current and to lessen the power dissipation across the feedback resistors. The external feedback resistors are not required for the fixed output versions because the feedback resistors are already inside the chip.

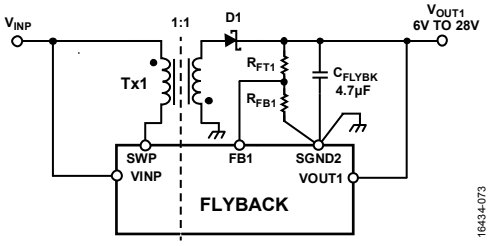


Figure 70. Flyback Regulator Output Voltage Setting

Set the positive output for the flyback regulator by

$$V_{OUT1} = V_{FB1} \times (1 + (R_{FT1}/R_{FB1}))$$

where:
V_{OUT1} is the flyback output voltage.
V_{FB1} is the flyback feedback voltage.
R_{FT1} is the feedback resistor from VOUT1 to FB1.
R_{FB1} is the feedback resistor from FB1 to SGND2.

Conversely, calculate the value of the top resistor for the target V_{OUT1} by:

$$R_{FT1} = R_{FB1} \times ((V_{OUT1}/V_{FB1}) - 1)$$

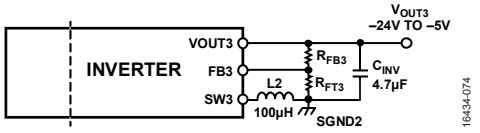


Figure 71. Inverting Regulator Output Voltage Setting

Set the negative output for the inverting regulator by

$$V_{OUT3} = V_{FB3} \times (1 + (R_{FT3}/R_{FB3}))$$

where:
V_{OUT3} is the inverting regulator output voltage (negative sign disregarded).
V_{FB3} is the inverting regulator feedback voltage in reference to VOUT3.
R_{FT3} is the feedback resistor from FB3 to SGND2.
R_{FB3} is the feedback resistor from VOUT3 to FB3.

As with the flyback regulator, calculate the value of the top resistor for the target V_{OUT3} by the following equation:

$$R_{FT3} = R_{FB3} \times ((V_{OUT3}/V_{FB3}) - 1)$$

Table 15. Recommended Feedback Resistor Values

Desired Output Voltage (V)	Flyback/Inverting Regulator		
	R_{FT1}/R_{FT3} (MΩ)	R_{FB1}/R_{FB3} (kΩ)	Calculated Output Voltage (V)
±6	0.715	110	±6.000
±9	1.24	121	±8.998
±12	1.54	110	±12.000
±15	2.15	121	±15.015
±24	3.48	120	±24.000
+28	3.4	100	+28.000

Capacitor Selection

Higher output capacitor values reduce the output voltage ripple and improve the load transient response. When choosing this value, it is also important to account for the loss of capacitance due to the output voltage dc bias.

Ceramic capacitors are manufactured with a variety of dielectrics, each with a different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with voltage ratings of 25 V to 50 V (depending on output) are recommended for best performance. Y5V and Z5U dielectrics are not recommended for use with any dc-to-dc converter because of their poor temperature and dc bias characteristics.

Calculate the worst case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage using the following equation:

$$C_{EFFECTIVE} = C_{NOMINAL} \times (1 - TEMPCO) \times (1 - DCBIASCO) \times (1 - Tolerance)$$

where:
$C_{EFFECTIVE}$ is the effective capacitance at the operating voltage.
$C_{NOMINAL}$ is the nominal capacitance shown in this data sheet.
TEMPCO is the worst case capacitor temperature coefficient.
DCBIASCO is the dc bias derating at the output voltage.
Tolerance is the worst case component tolerance.

To guarantee the performance of the device, it is imperative to evaluate the effects of dc bias, temperature, and tolerances on the behavior of the capacitors for each application.

Capacitors with lower effective series resistance (ESR) and effective series inductance (ESL) are preferred to minimize voltage ripple.

FLYBACK REGULATOR COMPONENTS SELECTION

Input Capacitor

An input capacitor must be placed between the VINP pin and ground. Ceramic capacitors greater than or equal to 3.3 µF over temperature and voltage are recommended. The input capacitor reduces the input voltage ripple caused by the switching current. Place the input capacitor as close as possible to the VINP and PGNDP pins to reduce input voltage spikes. The voltage rating of the input capacitor must be greater than the maximum input voltage.

Output Capacitor

Higher output capacitor values reduce the output voltage ripple and improve load transient response. When choosing this value, it is also important to account for the loss of capacitance due to the output voltage dc bias. A 4.7 µF capacitor is recommended as a balance between performance and size.

Ripple Current vs. Capacitor Value

The output capacitor value must be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. Use the following equation to calculate the output capacitance:

$$C_{OUT} = (L_{PRI} \times I_{SWP}^2)/(2 \times V_{OUT1} \times \Delta V_{OUT1})$$

where:
C_{OUT} is the capacitance of the flyback output capacitor.
L_{PRI} is the primary inductance of the transformer.
I_{SWP} is the peak switch current.
V_{OUT1} is the flyback regulator output voltage.
ΔV_{OUT1} is the allowable flyback regulator output ripple.

Schottky Diode

A Schottky diode with low junction capacitance is recommended for D1. At higher output voltages and especially at higher switching frequencies, the junction capacitance is a significant contributor to efficiency. Choose an output diode with a forward current rating (I_F) that is greater than the maximum load requirement and with a reverse voltage rating (V_R) that is greater than the summation of the maximum supply voltage ($V_{INP\ (MAX)}$) and the maximum output voltage ($V_{OUT1\ (MAX)}$).

Transformer

The transformer used with the ADP1031 is an important component within the system, in terms of efficiency and maximum output power capability. Analog Devices worked with a number of leading magnetic component suppliers to develop a number of transformer designs for use with the ADP1031. These designs are listed in Table 16. A number of factors must be taken into account when designing a transformer for use with the ADP1031.

Turn Ratio

The ADP1031 requires the use of a transformer with a primary to secondary turn ratio of 1:1 to start up properly.

Primary Inductance

The ADP1031 operates with a transformer with an inductance in the 80 µH to 560 µH range. However, it is recommended to choose an inductance value that results in the flyback output voltage (VOUT1) divided by the transformer primary inductance being less than or equal to 140,000 to maintain control loop stability.

$$V_{OUT1}/L_{PRI} \leq 140{,}000$$

where:
V_{OUT1} is the flyback regulator output voltage.
L_{PRI} is the primary side inductance of the transformer.

Using a transformer at the lower end of the inductance range may result in a smaller transformer but also reduces the output power capabilities due to larger ac ripple current through the transformer. Conversely, operating at higher inductance can result in higher output power at the expense of a potentially larger transformer.

Flyback Transformer Saturation Current

Do not exceed the saturation current of the transformer in operation or this may lead to much higher losses and overall lower system efficiency. Choose a transformer with a saturation current rating that is greater than the expected peak switch current (I_{SWP}) across line and load conditions.

Series Winding Resistance

In power loss sensitive applications, keep the series resistance of the primary and secondary windings as low as possible to improve overall efficiency.

Leakage Inductance and Clamping Circuits

When choosing a transformer to operate with the ADP1031, minimize transformer leakage inductance. Leakage inductance causes a voltage spike to appear on the SWP node when the flyback regulator switch is off due to energy storage in the leakage inductance that is not transferred to the output. The voltage spike is more prominent at higher load currents and increases with higher leakage inductance. It is important to keep the voltage spikes lower than the voltage rating of the flyback switch that drives the SWP pin. Margin must be built in to any design to avoid exceeding this limit if no clamp or snubber circuit is used to protect the flyback switch.

To estimate the leading voltage spike at the SWP pin when the switch turns off, use the following equation:

$$V_{PEAK} = I_{PEAK} \times (L_{LEAK}/(C_P + C_{SWP}))^{1/2} + V_{INP} + V_{OUT1} + V_D$$

where:
V_{PEAK} is the voltage spike amplitude.
I_{PEAK} is the peak current on the flyback switch.
L_{LEAK} is the leakage inductance of the transformer.
C_P is the parasitic capacitance of the transformer.
C_{SWP} is the capacitance on the flyback switch.
V_{INP} is the input supply voltage.
V_{OUT1} is the output voltage of the flyback regulator.
V_D is the forward voltage drop across the rectifier diode.

A snubber or clamp circuit can protect the flyback switch for cases where the leakage inductance is too high for application conditions. Two common types of clamping circuit are the resistor, capacitor, diode clamp shown in Figure 72 and the diode Zener diode clamp shown in Figure 73. The resistor, capacitor, diode clamp quickly dampens the voltage spike and provides improved EMI performance, and the diode Zener diode clamp can be used when the clamping level must be consistent and well defined. The diode Zener diode clamp has slightly higher power efficiency over the resistor, capacitor, diode clamp. However, the cost of the diode Zener diode clamp solution is typically higher than the resistor, capacitor, diode solution.

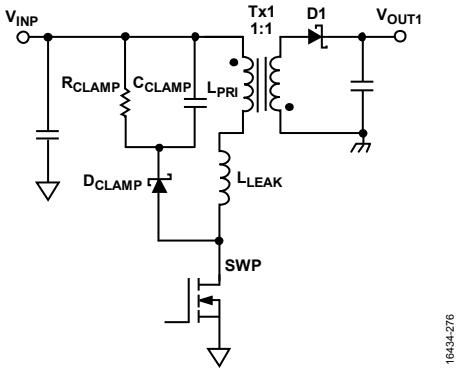


Figure 72. Resistor, Capacitor, Diode Clamp

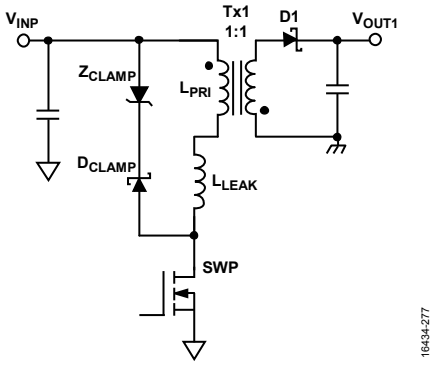


Figure 73. Diode Zener Diode Clamp

Clamping Resistor

To calculate the clamping resistor (R_{CLAMP}) value, the clamping voltage (V_{CLAMP}) must be determined. The clamping voltage is the voltage on which any voltage spike that occurs on the flyback switch is clamped. Choose a clamping voltage (V_{CLAMP}) that provides sufficient margin between the SWP maximum voltage rating (SWP_{VMAX}) specified in the Absolute Maximum Ratings section and that also is greater than the summation of the maximum input supply ($V_{INP\,(MAX)}$) and the maximum flyback output voltage ($V_{OUT1\,(MAX)}$) of the application as given by

$$SWP_{VMAX} > V_{INP\,(MAX)} + V_{CLAMP} > V_{INP\,(MAX)} + V_{OUT1\,(MAX)}$$

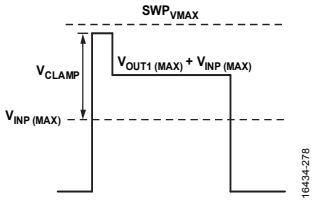


Figure 74. Clamping Waveform

Use the following equation to calculate the value of the clamping resistor for a given V_{CLAMP} value:

$$R_{CLAMP} = (2 \times V_{CLAMP} \times (V_{CLAMP} - V_{OUT1}))/(L_{LEAK} \times I_{PEAK}^2 \times f_{SW})$$

where:
R_{CLAMP} is the value of the clamping resistor.
V_{CLAMP} is the clamping voltage.
V_{OUT1} is the output voltage of the flyback regulator.
L_{LEAK} is the leakage inductance of the transformer.
I_{PEAK} is the peak current on the flyback switch.
f_{SW} is the switching frequency of the flyback regulator.

To calculate the power dissipation across the snubber resistor, use the following equation:

$$P_{RCLAMP} = (V_{CLAMP})^2/(R_{CLAMP})$$

where P_{RCLAMP} is the power dissipation across R_{CLAMP}. Choose R_{CLAMP} with power rating of about twice this value to have margin.

Clamping Capacitor

The clamping capacitor (C_{CLAMP}) is used to minimize the voltage ripple level (V_{RIPPLE}) superimposed in V_{CLAMP}. Calculate the clamping capacitor by using the following equation for the desired V_{RIPPLE} level and the calculated R_{CLAMP}:

$$C_{CLAMP} = V_{CLAMP}/(V_{RIPPLE} \times f_{SW} \times R_{CLAMP})$$

where:
C_{CLAMP} is the value of the clamping capacitor.
V_{CLAMP} is the clamping voltage.
V_{RIPPLE} is the voltage ripple superimposed in V_{CLAMP}. A V_{RIPPLE} of about 5% to 10% of V_{CLAMP} is reasonable.
f_{SW} is the switching frequency of the flyback regulator.
R_{CLAMP} is the value of the clamping resistor.

Clamping Diode

Schottky diodes are typically the best choice. However, fast recovery diodes can also be used. The diode reverse voltage rating must be higher than the maximum SWP pin voltage rating.

Diode Zener Diode Clamp

A Zener diode can replace the resistor, capacitor (RC) network on the resistor, capacitor, diode clamp when the clamping level must be consistent and well defined. Choose the Zener diode breakdown voltage to balance power loss and switch voltage protection. Calculate the Zener voltage by using the following equation:

$$V_{ZENER\ (MAX)} \leq SWP_{VMAX} - V_{INP\ (MAX)}$$

where:
$V_{ZENER\ (MAX)}$ is the maximum Zener diode breakdown voltage or the Zener voltage, which can be the same as the clamping voltage, V_{CLAMP}.
SWP_{VMAX} is the absolute maximum rating of the SWP pin.
$V_{INP\ (MAX)}$ is the maximum input supply voltage.

The power loss in the clamp determines the power requirement for the Zener diode. Use the following equation to calculate the Zener diode power dissipation:

$$P_{ZENER} = (V_{ZENER} \times L_{LEAK} \times I_{PEAK}^2 \times f_{SW})/(2 \times (V_{ZENER} - V_{OUT1}))$$

where:
P_{ZENER} is the Zener diode power dissipation. Choose a Zener diode with power rating higher than the calculated value.
V_{ZENER} is the Zener diode breakdown voltage or the Zener voltage.
L_{LEAK} is the leakage inductance of the transformer.
I_{PEAK} is the peak current on the flyback switch.
f_{SW} is the switching frequency of the flyback regulator.
V_{OUT1} is the output voltage of the flyback regulator.

Ripple Current (I_{AC}) vs. Inductance

Calculate the ripple current by first determining the duty cycle in continuous conduction mode.

$$D_{CCM} = (V_{OUT1} + V_D)/(V_{OUT1} + V_D + V_{INP})$$

where:
D_{CCM} is the duty cycle of the flyback switch.
V_{OUT1} is the output voltage of the flyback regulator.
V_D is the forward voltage drop across the rectifier diode.
V_{INP} is the input supply voltage.

Then, from the duty cycle, calculate the I_{AC} in the flyback switch and transformer primary.

$$I_{AC} = (V_{INP} \times D_{CCM})/(f_{SW} \times L_{PRI})$$

where:
I_{AC} is the ripple current through the primary side of the transformer and flyback switch.
V_{INP} is the input supply voltage.
D_{CCM} is the duty cycle of the flyback switch.
f_{SW} is the switching frequency of the flyback regulator.
L_{PRI} is the primary side inductance of the transformer.

Maximum Output Current Calculation

The maximum output power and current that can be achieved from the flyback output depends on a number of variables within the regulator. These variables include the transformer choice, the operating frequency, and the rectifier diode choice. The flyback regulator output is the supply to the buck regulator that drives V_{OUT2} and the inverting regulator that drives V_{OUT3}. Determine the maximum output power capability by

$$P_{VOUT1\ (MAX)} = 0.5 \times (I_{PEAK}^2 - (I_{PEAK} - I_{AC}/2)^2) \times L_{PRI} \times f_{SW} \times \eta$$

where:
$P_{VOUT1\ (MAX)}$ is the maximum output power from V_{OUT1}.
I_{PEAK} is the peak current on the flyback switch.
I_{AC} is the ripple current through the primary side of the transformer and flyback switch.
L_{PRI} is the primary side inductance of the transformer.
f_{SW} is the switching frequency of the flyback regulator.
η is the expected efficiency of the flyback regulator.

The lower limit of the flyback current-limit threshold, $I_{LIM\ (FLYBACK)}$, limits the maximum I_{PEAK}. However, it is not recommended to operate at this level to avoid unwanted current-limit events due to variation in transformer inductance, efficiency, flyback switching frequency, and rectifier diode forward voltage drop. If the load on the flyback causes the current limit to trip, the output voltage may not regulate as expected. It is recommended to choose a peak operating current with built in margin for the variations mentioned or to calculate the maximum output power or output load using the worst case transformer inductance, efficiency, diode forward voltage drop, and flyback switching frequency.

Calculate the maximum load current on V_{OUT1} by

$$I_{VOUT1\ (MAX)} = P_{VOUT1\ (MAX)}/V_{OUT1}$$

where:
$I_{VOUT1\ (MAX)}$ is the maximum output current from V_{OUT1}.
$P_{VOUT1\ (MAX)}$ is the maximum output power from V_{OUT1}.
V_{OUT1} is the output voltage of the flyback regulator.

BUCK REGULATOR COMPONENTS SELECTION

Inductor

The value of the inductor for the ADP1031 buck regulator affects the efficiency and the output voltage ripple. Larger value inductors typically improve efficiency. However, for a given package size, as load increases, the dc resistance (DCR) and core losses eventually have an increasing negative impact on efficiency. Using a smaller value inductor reduces output voltage ripple but can decrease the overall efficiency due to increased switching losses.

Output Capacitor

The output capacitor selection affects the output ripple voltage, load step transient, and the loop stability of the regulator. A 4.7 µF capacitor is recommended as a balance between performance and size, but a larger capacitor can be used to reduce output ripple.

INVERTING REGULATOR COMPONENT SELECTION

Inductor

The value of the inductor for the ADP1031 inverting regulator affects the efficiency and output voltage ripple. Larger value inductors typically improve efficiency. However, for a given package size, as load increases, the DCR and core losses eventually have an increasing negative impact on efficiency. Using a smaller value inductor reduces output voltage ripple but can decrease the overall efficiency due to increased switching losses.

Output Capacitor

The output capacitor selection affects the output ripple voltage, load step transient, and the loop stability of the regulator. A minimum of 4.7 µF capacitor is recommended to maintain stability across VOUT1 and output load.

Inverting Regulator Stability

The ADP1031 inverting regulator uses internal compensation and operates with an inductance of 100 µH and a typical capacitance of 4.7 µF. Using different component values may result in instability of VOUT3, particularly if lower capacitance and smaller inductor values are used. Consult the factory for guidance. Operating the inverter with the recommended inductor and output capacitor, the output is stable from no load to a 15 mA load for any output from −24 V to −5 V. When increasing the load beyond 15 mA, it is recommended to use a larger output capacitor to stabilize the feedback loop, particularly for lower output voltages.

Table 16. Transformer Selection

Part Number	Manufacturer	Turns Ratio[1]	Primary		Saturation Current[2] (mA)	Isolation Voltage[3] (V rms)	Isolation Type	Size, Length × Width × Height, (mm)
			Inductance (µH)	Resistance (Ω)				
750316743	Würth Elektronik	1:1	280	1.1	250	2000	Basic	8.26 × 8.6 × 9.65
750316566	Würth Elektronik	1:1	150	1.65	220	2000	Basic	7.0 × 6.91 × 7.8
WA8478-BE	Coilcraft	1:1	275	1.2	150	2250	Basic	7.25 × 7.85 × 7.0
YA9293-AL	Coilcraft	1:1	300	1.15	250	2250	Reinforced	10 × 12.07 × 5.97
BS64042CS	Bourns	1:1	270	1.4	400	2200	Basic	10.5 × 9.8 × 11.0
LPD5030-154MRB	Coilcraft	1:1	150	2.43	430	Not applicable	Functional	4.8 × 4.8 × 2.9

[1] Turns ratio between the primary and secondary coils.
[2] 20% drop from initial.
[3] 1 minute duration.

Table 17. Buck Regulator and Inverting Regulator Recommended Inductors

Part Number	Manufacturer	Inductance (µH)	DC Resistance (Ω)	Saturation Current[1] (mA)	Size, Length × Width × Height, (mm)
744043101	Würth Elektronik	100	0.55	290	4.8 × 4.8 × 2.8
XFL3012-104MEB	Coilcraft	100	2.63	280	3.2 × 3.2 × 1.3
LQH3NPN101MMEL	Murata	100	1.59	260	3 × 3 × 1.4
SRN3015-101M	Bourns	100	2.92	270	3 × 3 × 1.5
SRU2016-101Y	Bourns	100	4.9	150	2.8 × 2.8 × 1.65
XFL2006-104MEB	Coilcraft	100	11.1	115	2 × 2 × 0.6

[1] 30% drop in inductance.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADP1031.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 8 summarize the peak voltage for 20 years of service life for a bipolar ac operating condition. In many cases, the approved working voltage is higher than the 20 year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The ADP1031 insulation lifetime depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 75, Figure 76, and Figure 77 shows these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products yet to meet the 20-year operating lifetime recommended by Analog Devices for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 20-year service life. Treat any cross insulation voltage waveform that does not conform to Figure 76 or Figure 77 as a bipolar ac waveform, and limit the peak voltage to the 20-year lifetime voltage value listed in Table 8.

The voltage presented in Figure 76 is shown as sinusoidal for illustration purposes only. The voltage represents any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

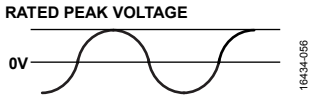


Figure 75. Bipolar AC Waveform

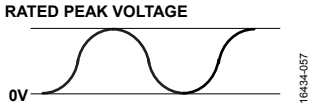


Figure 76. Unipolar AC Waveform

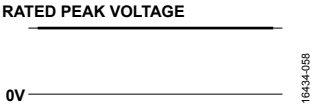


Figure 77. DC Waveform

THERMAL ANALYSIS

For the purpose of thermal analysis, the ADP1031 die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} values from Table 7. The value of θ_{JA} is based on measurements taken with the devices mounted on a JEDEC standard, 4-layer board with fine width traces and still air. Under normal operating conditions, the ADP1031 operates at a full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout Considerations section decreases thermal resistance to the PCB, allowing increased thermal margins in high ambient temperatures. Each switching regulator in the ADP1031 has a thermal shutdown circuit that turns off the dc-to-dc converter and the outputs when a die temperature of approximately 150°C is reached. When the die cools below approximately 135°C, the ADP1031 dc-to-dc converter outputs turn on again.

TYPICAL APPLICATION CIRCUIT

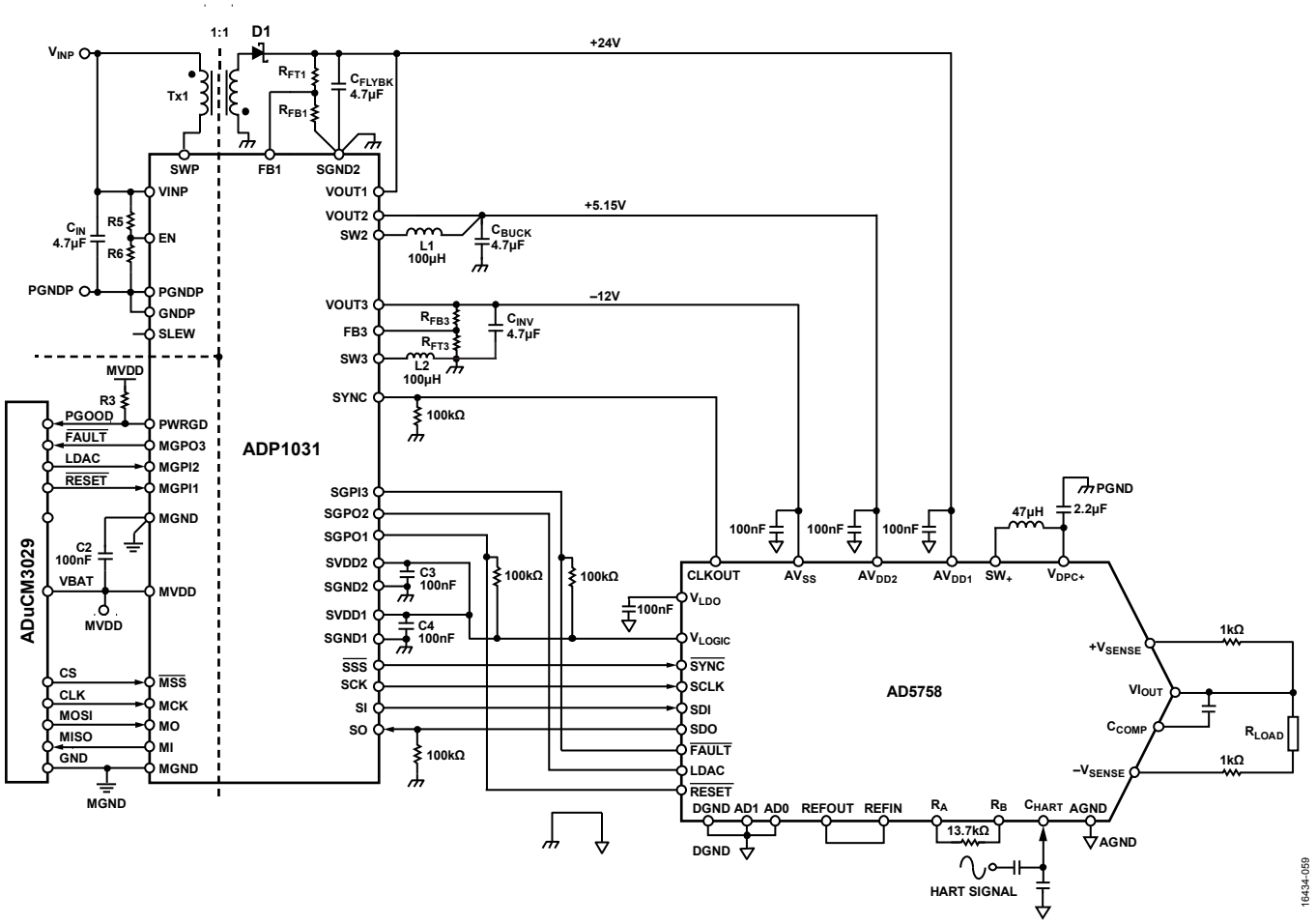


Figure 78. Typical Application Circuit for the ADP1031 Using the AD5758

PCB LAYOUT CONSIDERATIONS

To achieve optimum efficiency, proper regulation, strong stability, and low noise, a well designed PCB layout is required. Follow these guidelines when designing PCBs:

- Keep the input bypass capacitor, C_{IN}, close to the VINP pin and the PGNDP pin.
- Keep the high current switching paths as short as possible. These paths include the connections between the following:
  - C_{IN}, VINP, the primary winding of the transformer, and PGNDP
  - VOUT1, C_{FLYBK}, Diode 1 (D1), the secondary winding of the transformer, and SGND2
  - VOUT2, SW2, Inductance 1 (L1), C_{BUCK}, and SGND2
  - VOUT3, SW3, Inductance 2 (L2), C_{INV}, and SGND2
- Keep high current traces as short and wide as possible to minimize parasitic series inductance, which causes spiking and EMI.
- Avoid routing high impedance traces near any node connected to the SWP, SW2, and SW3 pins or near the L1 and L2 inductors or the T1 transformer to prevent radiated switching noise injection.
- Place the feedback resistors as close to the FB1 and FB3 pins as possible to prevent high frequency switching noise injection.
- To minimize EMI, place the MVDD decoupling capacitor (C1) as close to the MVDD pin (Pin 39) and the MGND pin (Pin 3).
- To minimize EMI, place the SVDD1 decoupling capacitor (C3) as close to the SVDD1 pin (Pin 10) and the SGND1 pin (Pin 5), and place the SVDD2 decoupling capacitor (C7) as close to the SVDD2 pin (Pin 20) and the SGND2 pin (Pin 16).

Figure 79 shows a suggested top layer layout for the ADP1031.

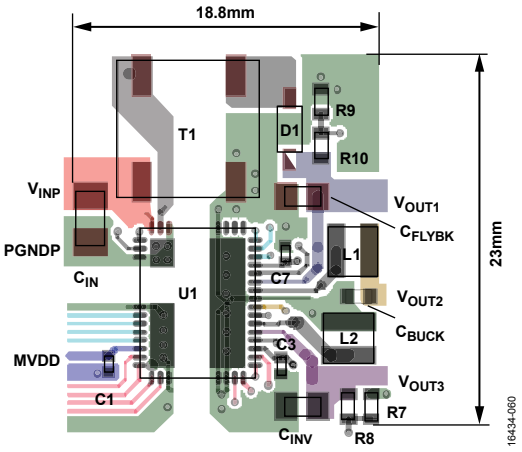
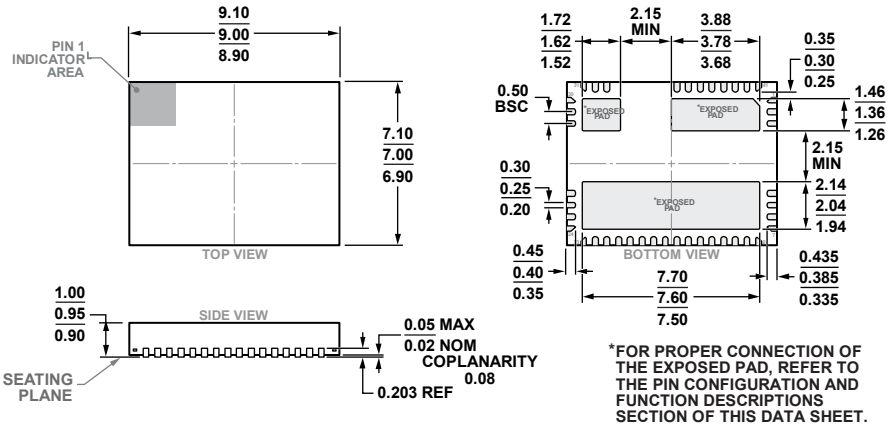


Figure 79. Suggested Top Layer Layout

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220

Figure 80. 41-Lead Lead Frame Chip Scale Package [LFCSP]
9 mm × 7 mm Body and 0.95 mm Package Height
(CP-41-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	VOUT1[2]	VOUT2	VOUT3	Temperature Range	Package Description	Package Option
ADP1031ACPZ-1-R7	Adjustable	5.15 V	Adjustable	−40°C to +125°C	41-Lead LFCSP	CP-41-1
ADP1031ACPZ-2-R7	Adjustable	5 V	Adjustable	−40°C to +125°C	41-Lead LFCSP	CP-41-1
ADP1031ACPZ-3-R7	Adjustable	3.3 V	Adjustable	−40°C to +125°C	41-Lead LFCSP	CP-41-1
ADP1031ACPZ-4-R7	24 V	5.15 V	Adjustable	−40°C to +125°C	41-Lead LFCSP	CP-41-1
ADP1031ACPZ-5-R7	21 V	5.15 V	Adjustable	−40°C to +125°C	41-Lead LFCSP	CP-41-1
ADP1031CP-1-EVALZ	Adjustable	5.15 V	Adjustable		Evaluation Board for the ADP1031ACPZ-1	
ADP1031CP-2-EVALZ	Adjustable	5.15 V	Adjustable		Evaluation Board for the ADP1031ACPZ-2	
ADP1031CP-3-EVALZ	Adjustable	5.15 V	Adjustable		Evaluation Board for the ADP1031ACPZ-3	
ADP1031CP-4-EVALZ	24 V	5.15 V	Adjustable		Evaluation Board for the ADP1031ACPZ-4	
ADP1031CP-5-EVALZ	21 V	5.15 V	Adjustable		Evaluation Board for the ADP1031ACPZ-5	

[1] Z = RoHS Compliant Part.
[2] For other VOUT1 voltage options, contact Analog Devices local sales representatives for additional information.