PPG Optical Sensor Module with Integrated Red/IR Emitters and AFE

Data Sheet **ADPD144RI**

FEATURES

- 2.8 mm × 5.0 mm module with integrated optical components
  - 660 nm LED, 880 nm IR LED, and photodiode
- Fully integrated AFE, ADC, LED drivers, and timing core
- Custom optical package for use under a glass window
- Programmable 2-channel, 8.5 mA to 370 mA LED drivers
- Provision to use external LED emitters
- Low power
- Specifically designed for ultralow direct optical reflections
- Independent AFE settings per channel
- I²C data and control interface
- Burst accumulator enabling 20 bits per sample period
- Sample to sample accumulator enabling up to 27 bits per data read
- 16-bit or 32-bit register or FIFO readout per channel

APPLICATIONS

- Optical heart rate monitoring
- Reflective SpO2 measurement

GENERAL DESCRIPTION

The ADPD144RI is a highly integrated, photometric front end optimized for photoplethysmography (PPG) detection of blood oxygenation (SpO2) by synchronous detection in red and infrared wavelengths. Synchronous measurement allows rejection of both dc and ac ambient light interference with extremely low power consumption.

The module combines highly efficient, light emitting diode (LED) emitters and a sensitive 4-channel, deep diffusion photodiode (PD1 to PD4) with a custom application specific integrated circuit (ASIC) in a compact package that provides optical isolation between the integrated LED emitters and the detection photodiodes to improve through tissue, signal-to-noise ratio (SNR).

The ASIC consists of a 4-channel analog front end (AFE) with two independently configurable datapaths with separate gain and filter settings, a 14-bit analog-to-digital converter (ADC) with a burst accumulator, two flexible, independently configurable, LED drivers, and a digital control block. The digital control block provides AFE and LED timing, signal processing, and communication. Data output and functional configuration occur over a 1.8 V I²C interface.

FUNCTIONAL BLOCK DIAGRAM

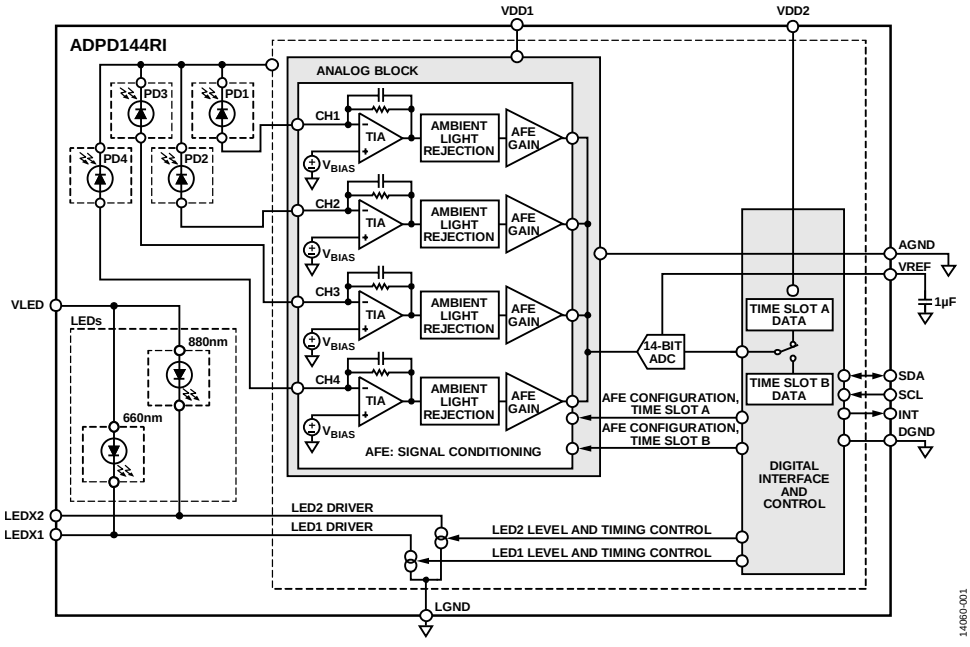

Figure 1.

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REVISION HISTORY

2/2019—Revision A: Initial Version

SPECIFICATIONS

The voltage applied at the VDD1 pin and VDD2 pin (V_{DD}) = 1.8 V and T_A = −40°C to +85°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY CURRENT		VDD1, VDD2 = 1.8 V				
Peak Supply Current	IV_{DD_PEAK}	4-channel operation		9.3		mA
Standby Mode Current	$IV_{DD\_STANDBY}$			3.5		µA
Average Supply Current	IV_{DD_AVG}	See the Calculating the Total Power Consumption section				µA
Supply Current		LED offset = 25 µs, LED period = 19 µs, LED peak current = 25 mA, 4 channels active				
1 Pulse		100 Hz data rate, Time Slot A only		106		µA
		100 Hz data rate, Time Slot B only		94		µA
		100 Hz data rate, Time Slot A and Time Slot B		151		µA
10 Pulses		100 Hz data rate, Time Slot A only		258		µA
		100 Hz data rate, Time Slot B only		246		µA
		100 Hz data rate, Time Slot A and Time Slot B		455		µA
LED SUPPLY VOLTAGE (V_{LED}) CURRENT						
Average Supply Current						
V_{LED}	I_{LED_AVG}	See the Calculating the Total Power Consumption section				
V_{LED} Supply Current, Average		Peak LED current = 100 mA, LED pulse width = 3 µs				
1 Pulse		50 Hz data rate		15		µA
		100 Hz data rate		30		µA
		200 Hz data rate		60		µA
10 Pulses		50 Hz data rate		150		µA
		100 Hz data rate		300		µA
		200 Hz data rate		600		µA

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SATURATION ILLUMINANCE[1]	Blackbody color temperature (T = 5800 K)[2]				
Direct Illumination	Transimpedance amplifier (TIA) gain = 25 kΩ		48		kLux
	TIA gain = 50 kΩ		24		kLux
	TIA gain = 100 kΩ		10		kLux
	TIA gain = 200 kΩ		4		kLux
Through Skin	TIA gain = 25 kΩ		140		kLux
	TIA gain = 50 kΩ		70		kLux
	TIA gain = 100 kΩ		31		kLux
	TIA gain = 200 kΩ		12		kLux
DATA ACQUISITION					
ADC Resolution	Single pulse		14		Bits
Sample Width	64 pulses to 255 pulses		20		Bits
Output Data Width	64 pulses to 255 pulses, 128 samples averaged		27		Bits
Sampling Frequency (f_{SAMPLE})					
Lowest Setting	Adjustable via Register 0x12 setting (see Table 18)	0.122			Hz
Highest Setting	Time Slot B only, one pulse per sample, sleep time = 200 µs			3.48	kHz
Minimum Sleep Time (t_{SLEEP_MIN})	Minimum sleep time required between samples		200		µs

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LEDs					
LED Peak Current Setting	Adjustable via Register 0x23 through Register 0x25 settings (see Table 14)	8.5		370	mA
Dominant Wavelength					
Red LED (LED1)	Forward current of the diode (I_F) = 20 mA		660		nm
Infrared (IR) LED (LED2)	I_F = 100 mA		880		nm
Radiant Flux	Red LED, I_F = 20 mA at 25°C	9			mW
	IR LED, I_F = 100 mA at 25°C	33			mW
PHOTODIODE[3]					
Responsivity	Wavelength, λ = 660 nm (Channel 1, Channel 2, Channel 3)		0.36		A/W
	Wavelength, λ = 660 nm (Channel 4)		0.31		A/W
	Wavelength, λ = 880 nm (Channel 1, Channel 2, Channel 3)		0.25		A/W
	Wavelength, λ = 880 nm (Channel 4)		0.28		A/W
Active Area					
Individual Photodiodes	Per channel		0.3		mm^2
Total Active Area			1.2		mm^2
POWER SUPPLY VOLTAGES	The ADPD144RI does not require a specific power-up sequence				
V_{DD}	Applied at the VDD1 pin and VDD2 pin	1.7	1.8	1.9	V
V_{LED}[4, 5]	Applied at the VLED pin	3	3.5	4.3	V
Power Supply Rejection Ratio (PSRR)	V_{DD} = 1.8 V		−37		dB
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] Saturation illuminance refers to the amount of light that saturates the analog signal path. Actual results may vary by factors of up to 2× from the typical specifications. As a point of reference, Air Mass 1.5 (AM1.5) sunlight (brightest sunlight) produces 100 kLux.
[2] Blackbody color temperature (T = 5800 K) approximates solar radiation (sunlight).
[3] The photodiode layout is shown in Figure 11.
[4] V_{LED} must be sufficient to source the maximum I_F required and to keep the internal driver and current sink compliance voltage at least 0.2 V above LGND. For the integrated LEDs, this voltage appears at the LEDX1 and LEDX2 pins.
[5] See Figure 8 for the current limitation at the minimum V_{LED}.

I²C DIGITAL INPUT/OUTPUT SPECIFICATIONS

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LOGIC INPUTS (SCL, SDA)						
Input Voltage						
High Level	V_{IH}		0.7 × V_{DD}		3.6	V
Low Level	V_{IL}				0.3 × V_{DD}	V
Input Current						
High Level	I_{IH}		−10		+10	µA
Low Level	I_{IL}		−10		+10	µA
Input Capacitance	C_{IN}			10		pF
LOGIC OUTPUTS						
INT Output Voltage						
High Level	V_{OH}	2 mA high level output current	V_{DD} − 0.5			V
Low Level	V_{OL}	2 mA low level output current			0.5	V
SDA Output						
Low Level Voltage	V_{OL1}	2 mA low level output current			0.2 × V_{DD}	V
Low Level Current	I_{OL}	V_{OL1} = 0.6 V	6			mA

I²C TIMING SPECIFICATIONS

Table 4.

Parameter[1, 2]	Description	Min	Typ	Max	Unit
f_{SCL}	SCL frequency		400		kHz
t_1	SCL minimum pulse width high	600			ns
t_2	SCL minimum pulse width low	1300			ns
t_3	Start condition hold time	600			ns
t_4	Start condition setup time	600			ns
t_5	SDA setup time	100			ns
t_6	SCL and SDA rise time			1000	ns
t_7	SCL and SDA fall time			300	ns
t_8	Stop condition setup time	600			ns

[1] Guaranteed by design.
[2] See Figure 2.

Timing Diagram

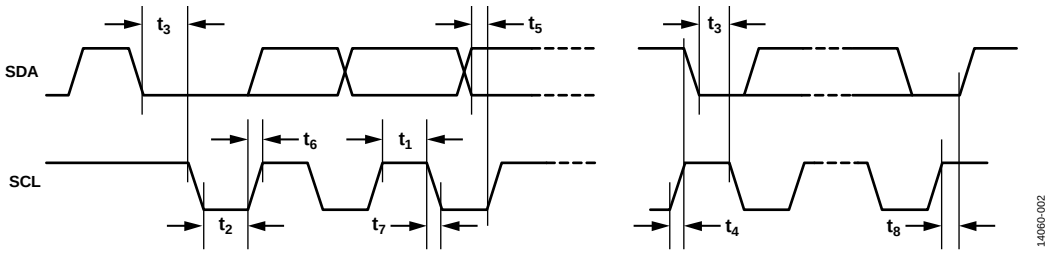

Figure 2. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VDD1, VDD2 to AGND	−0.3 V to +2.2 V
VDD1, VDD2 to DGND	−0.3 V to +2.2 V
INT to DGND	−0.3 V to +2.2V
LEDX1, LEDX2 to LGND	−0.3 V to +3.6 V
SCL to DGND	−0.3 V to +3.6 V
SDA to DGND	−0.3 V to +3.6 V
VLED to LGND[1]	−0.3 V to +4.3 V
ESD	
Human Body Model (HBM)	3000 V
Charged Device Model (CDM)	1250 V
Machine Model (MM)	100 V
Solder Reflow (Pb-Free)	
Peak Temperature	260 (+0/−5)°C
Time at Peak Temperature	<30 sec
Temperature Range	
Powered	−40°C to +85°C
Storage	−40°C to +105°C
Junction Temperature	105°C

[1] The absolute maximum voltage allowable between VLED and LGND is the voltage that causes the LEDX1 pin and the LED2X pin to reach or exceed their absolute maximum voltage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is necessary in a packaged IC to predict reliability and is a measure of the ability of the package to remove heat from the die. This device is a module with three separate die mounted to a substrate. Therefore, it is not possible to have one number describe the θ_{JA} of the entire assembly because the two die types used within this module have different thermal profiles, which is why a separate θ_{JA} is given for each die type in Table 6.

Table 6. Thermal Resistance

Package Type[1]	Supply Pins	θ_{JA}	Unit
CE-12-2			
ASIC	VDD1, VDD2	56	°C/W
LED1, LED2	VLED	156	°C/W

[1] Thermal impedance simulated values are based on JEDEC 2s2p and two thermal vias. See JEDEC JESD-51.

RECOMMENDED SOLDERING PROFILE

Figure 3 and Table 7 provide details about the recommended soldering profile.

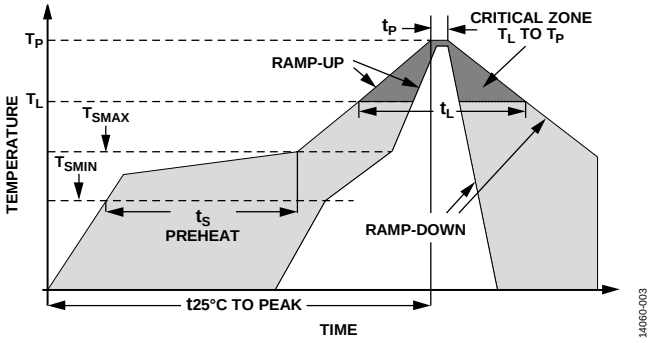

Figure 3. Recommended Soldering Profile

Table 7. Recommended Soldering Profile

Profile Feature	Conditions (Pb-Free)
Average Ramp Rate (T_L to T_P)	2°C/sec maximum
Preheat	
Minimum Temperature (T_{SMIN})	150°C
Maximum Temperature (T_{SMAX})	200°C
Time, T_{SMIN} to T_{SMAX} (t_S)	60 sec to 120 sec
T_{SMAX} to T_L Ramp-Up Rate	2°C/sec maximum
Time Maintained Above Liquidous Temperature	
Liquidous Temperature (T_L)	217°C
Time (t_L)	60 sec to 150 sec
Peak Temperature (T_P)	+260°C (+0/−5)°C
Time Within 5°C of Actual Peak Temperature (t_P)	<30 sec
Ramp-Down Rate	3°C/sec maximum
Time from 25°C ($t_{25°C}$) to Peak Temperature	8 minutes maximum

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

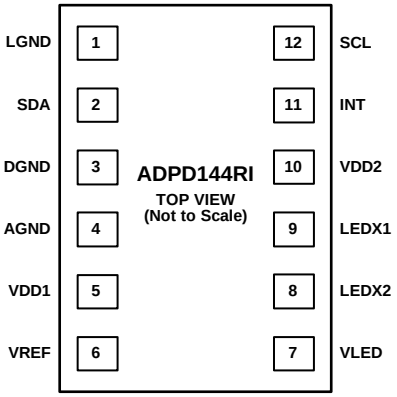

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	LGND	Supply	LED Ground.
2	SDA	Digital input and output	Serial Address and Data.
3	DGND	Supply	Digital Ground.
4	AGND	Supply	Analog Ground.
5	VDD1	Supply	1.8 V Supply Input.
6	VREF	Analog reference	Voltage Reference. Bypass with a 0.7 µF to 4 µF capacitor to AGND. Recommended value is 1 µF.
7	VLED	Supply	Integrated LEDs Anode Supply Voltage.
8	LEDX2	Analog output	External LED2 Cathode. Do not connect this pin unless driving external LEDs.
9	LEDX1	Analog output	External LED1 Cathode. Do not connect this pin unless driving external LEDs.
10	VDD2	Supply	1.8 V Supply Input.
11	INT	Digital input and output	Interrupt Input and Output.
12	SCL	Digital input	Serial Clock for I^2C Communication.

TYPICAL PERFORMANCE CHARACTERISTICS

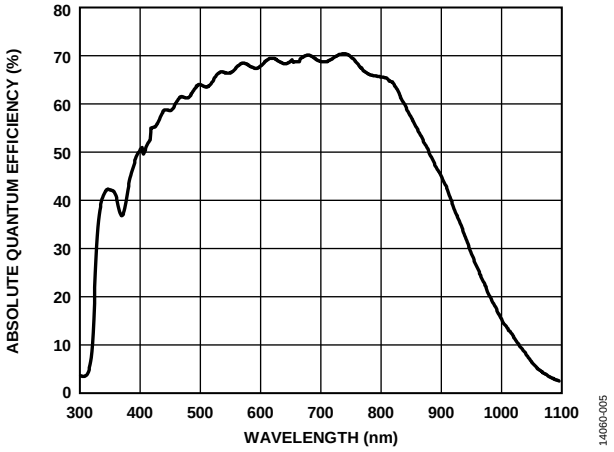

Figure 5. Photodiode Quantum Efficiency

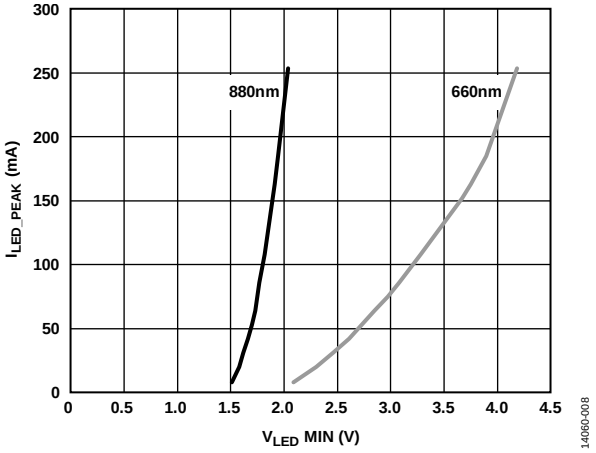

Figure 8. Maximum Achievable LED Current (I_{LED_PEAK}) vs. Minimum V_{LED}

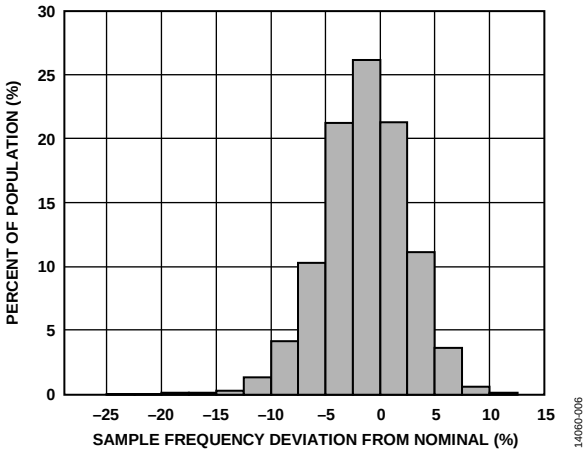

Figure 6. 32 kHz Clock Frequency Distribution
(Default Settings, Before User Calibration: Register 0x4B = 0x2612)

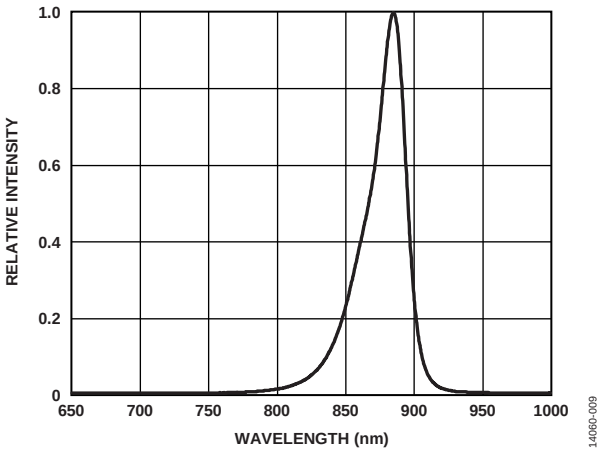

Figure 9. Spectral Output of LED2 (880 nm LED)

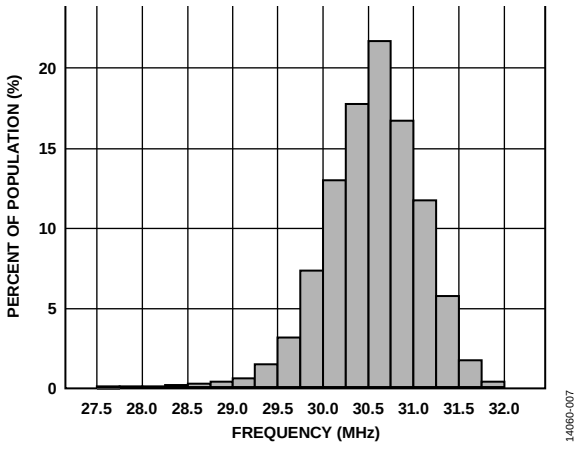

Figure 7. 32 MHz Clock Frequency Distribution
(Default Settings, Before User Calibration: Register 0x4D = 0x425E)

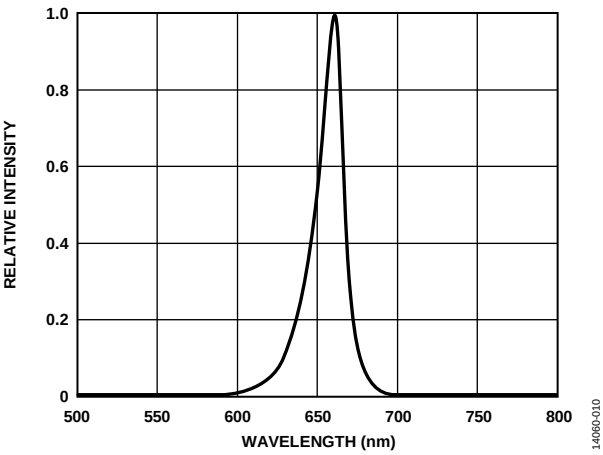

Figure 10. Spectral Output of LED1 (660 nm LED)

THEORY OF OPERATION

INTRODUCTION

The ADPD144RI is a highly integrated, optical module designed for reflective PPG measurements. The module combines red and infrared LED emitters, a four segment optical detector, and a mixed signal, photometric front end with digital control and signal processing in a compact device for optical measurements.

The ADPD144RI uses synchronous detection of optical pulses to improve the rejection of ambient light while also using much less operating power than nonsynchronous architectures. The integrated LED emitters produce light pulses synchronous with the active sampling period of the AFE. The AFE comprises a programmable TIA, a band-pass filter and an integrator. The processed analog signals are digitized by a 14-bit ADC and summed by the 20-bit burst accumulator. Four channels of simultaneous sampling are matrixed into two independent time slots (one for each LED wavelength). The number of pulses per sample is adjustable and accumulation and averaging can be applied to multiple samples to increase the dynamic range to 27 bits.

A high speed I²C interface allows data to be read from output registers directly or through a first in, first out (FIFO) buffer. Configuration control of the ADPD144RI is provided through the I²C interface.

OPTICAL COMPONENTS

Photodiode

The ADPD144RI integrates a 1.2 mm² deep-junction photodiode optimized for red and infrared sensitivity. The optical sensing area is segmented into four physical photodiodes. These diodes are multiplexed into two or four separate optical channels within the analog signal processing block. Data processing is performed on each channel independently, and output data is reported in sets of four 16-bit or 32-bit registers (one per optical channel) or summed into a single register, depending on programmed output data format.

LEDs

The ADPD144RI module contains two LED emitters at the optimum 660 nm red (LED1) and 880 nm IR (LED2) wavelengths for measurement of blood oxygenation (SpO2). A common anode connection to VLED supplies both integrated LEDs while the cathode of each LED is connected to a programmable current sink. The use of current sinks to pulse the LEDs allows a single supply voltage to power LEDs with different forward voltage requirements automatically compensating for the different forward voltages required by different LED families. When using the integrated LEDs, do not connect the LEDX1 and LEDX2 pins.

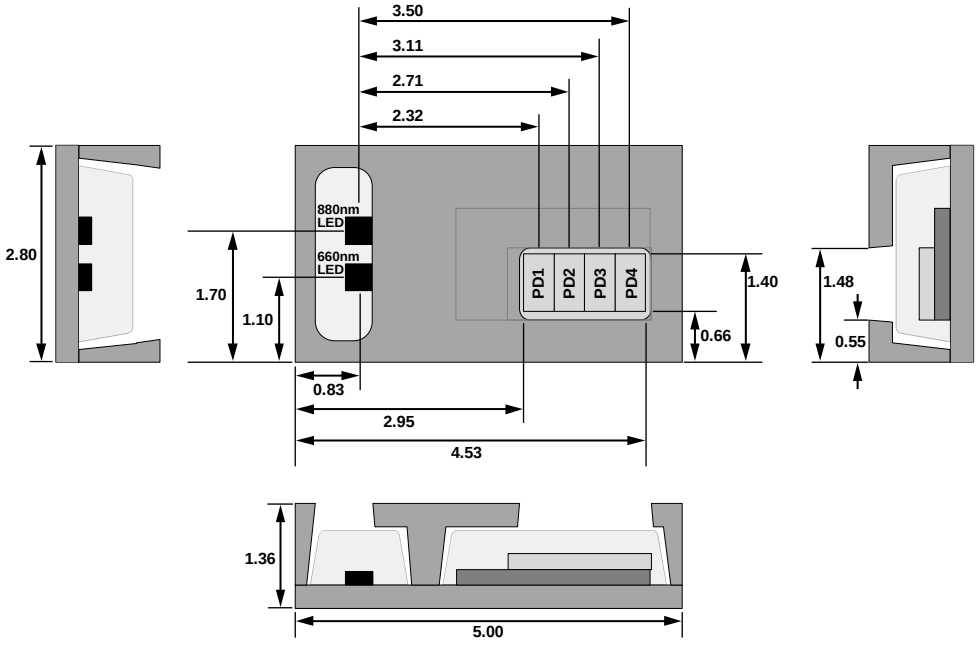

Figure 11. Optical Component Locations

SAMPLING OPERATION

The ADPD144RI samples bursts of synchronous pulses in two independent time slots, Time Slot A and Time Slot B, which occur sequentially within a sample period. The entire signal path from LED stimulation to data capture and processing is executed during each time slot. Time Slot A and Time Slot B feature separate datapaths that can be configured with independent settings for the LED driver, AFE setup, and the resulting data. In a typical Sp02 application, the red and IR emitters are assigned to different time slots, allowing each wavelength independent calibration.

Each time slot can contain 1 to 255 pulses. The energy from each pulse is collected, and the total energy minus ambient light is sampled by the ADC. A burst accumulator sums the pulse energies into a 20-bit value. The number of pulses in each time slot is set in the top octet of Register 0x31 for Time Slot A and Register 0x36 for Time Slot B. Each time slot is considered a discrete sample and the combined Time Slot A and Time Slot B, when both are used, is considered a sampling period. Flexibility in pulse number and emitter power allows the designer to choose the best balance of sampling rate, sensitivity, and power consumption for the application.

PULSE TIMING

The pulse timing for each time slot is programmed in Register 0x30, Register 0x31, Register 0x35, and Register 0x36. Sampling starts with the pulse delay, which is the time from the acquisition start to the rising edge of the first pulse. Time Slot A and Time Slot B operate in sequence for every sampling period in which these slots are both enabled.

To calculate sample timing use the following equation:

Pulse Offset + (*Pulse Count* × *Pulse Period*) + *Processing Time* (1)

where:
Pulse Offset is the delay before the first pulse in each sample.
Pulse Count is the total number of pulses within a time slot.
Pulse Period is the time from the start of one pulse to the start of the subsequent pulse.
Processing Time is the time for the burst accumulator to sum the pulse energy and place the data on the internal bus.

The following timing calculations use the configuration detailed in Table 12.

Register 0x31 = 0x0320, Register 0x31 = 0x0818, Pulse Offset A = 25 µs, Pulse Width A = 3 µs, Pulse Period A = 19 µs, and Pulse Count A = 8.

Time Slot A (t_A) = 25 µs + 8 × 19 µs + 68 µs = 245 µs

Register 0x31 = 0x0320, Register 0x31 = 0x0818, Pulse Offset B = 25 µs, Pulse Width B = 3 µs, Pulse Period B = 19 µs, and Pulse count B = 8.

Time Slot B (t_B) = 25 µs + 8 × 19 µs + 20 µs = 197 µs

Processing time for Time Slot A (t_1) is fixed at 68 µs and Time Slot B (t_2) is fixed at 20 µs.

Note that n_A is the number of pulses for Time Slot A, and n_B is the number of pulses for Time Slot B.

The minimum sleep time (t_{SLEEP_MIN}) between samples is 200 µs but can be longer depending on the f_{SAMPLE}, see Register 0x12, Bits[15:0].

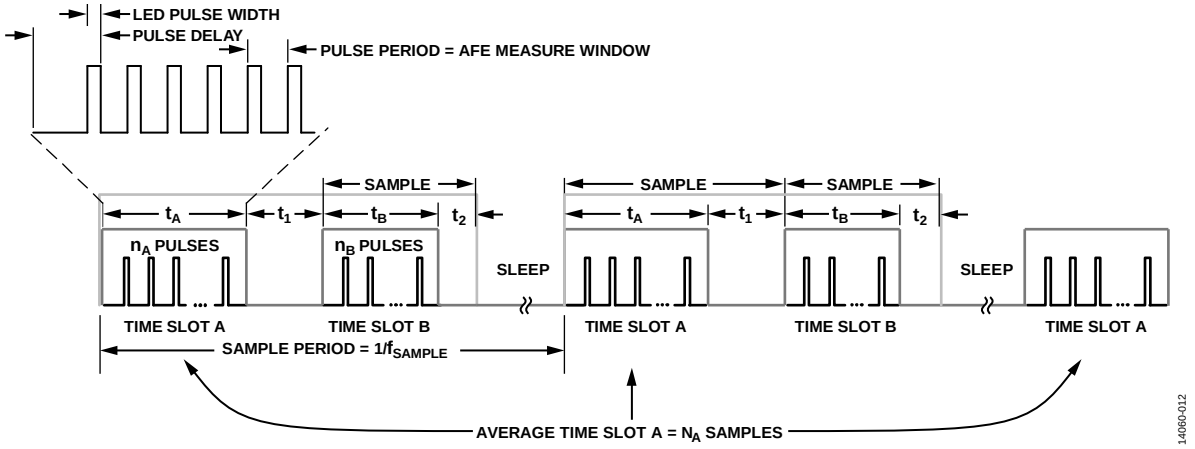

Figure 12. Time Slot Timing Diagram

Table 9. Recommended AFE and LED Timing Configuration

Register Name	Address	Recommended Setting
SLOTA_LEDMODE	0x30	0x0319
SLOTB_LEDMODE	0x35	0x0319
SLOTA_AFEMODE	0x39	0x21F3
SLOTB_AFEMODE	0x3B	0x21F3

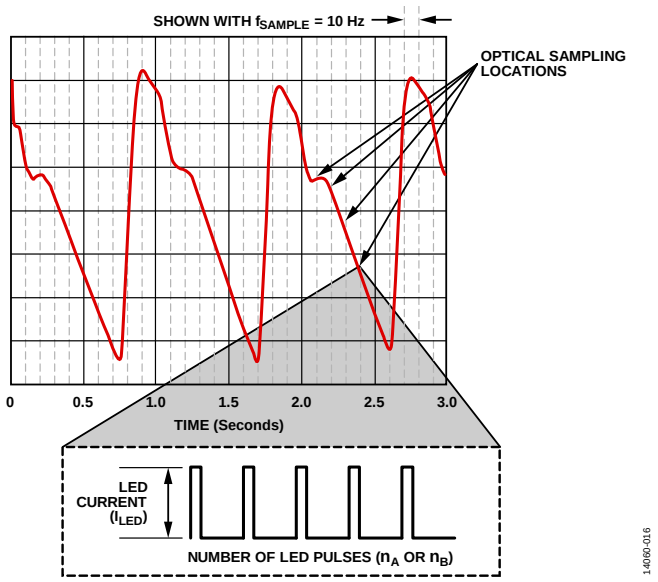

Figure 13. Example of a PPG Signal Sampled at a Data Rate of 10 Hz Using Five Pulses per Sample

TIME SLOT SWITCH

Two different input configurations can be used with the four-segment optical detector. The photodiodes can be assigned to their own AFE channel to increase dynamic range or can be summed to reduce noise. Photodiode outputs are assigned depending on the settings of Register 0x14 (see Figure 14). Both configurations are available and can be set independently for Time Slot A and Time Slot B.

See Table 10 for the time slot switch register settings. For situations requiring high dynamic range where all four channels are needed, configure the channels such that each of the photodetector segments is routed to its own channel. For lower light conditions, the two pairs of the segments can each be summed into a single channel as shown in Figure 14. Using only half of the amplifiers increases the signal to noise ratio by approximately a factor of √2 but sacrifices saturation headroom.

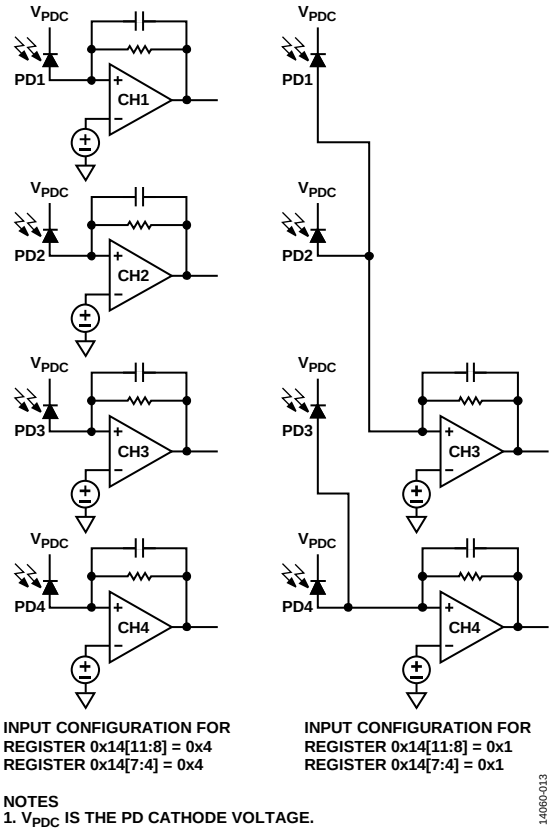

Figure 14. Input Configurations

Table 10. Time Slot Switch (Register 0x14)

Address	Bits	Name	Description
0x14	[11:8]	SLOTB_PD_SEL	Selects connection of PD1, PD2, PD3, or PD4 for Time Slot B, as shown in Figure 14. 0x1: Channel 3 and Channel 4 are connected during Time Slot B. 0x4: Channel 1, Channel 2, Channel 3, and Channel 4 are connected during Time Slot B. Other: reserved.
	[7:4]	SLOTA_PD_SEL	Selects connection of PD1, PD2, PD3, or PD4 for Time Slot A, as shown in Figure 14. 0x1: Channel 3 and Channel 4 are connected during Time Slot A. 0x4: Channel 1, Channel 2, Channel 3, and Channel 4 are connected during Time Slot A. Other: reserved.

STATE MACHINE OPERATION

During each time slot, the ADPD144RI operates according to a state machine. The state machine operates in the following sequence (see Figure 15).

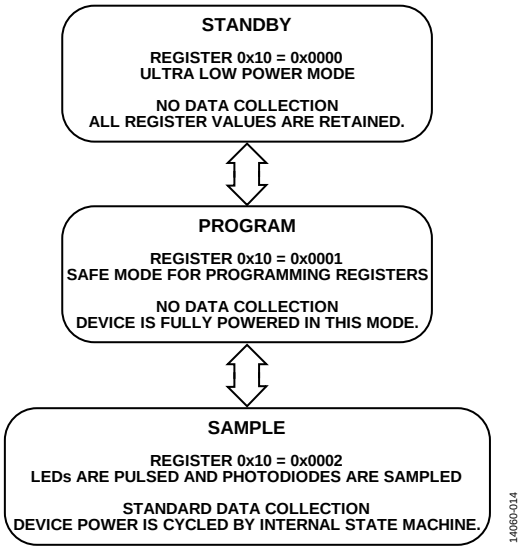

Figure 15. State Machine Operation Flowchart

The ADPD144RI operates in one of three modes: standby, program, and sample.

Standby mode is a power saving mode in which no data collection occurs. All register values are retained in this mode. To place the device in standby mode, write 0x0 to Register 0x10, Bits[1:0]. The device powers up in standby mode.

Program mode is used for programming registers. Always cycle the ADPD144RI through program mode when writing registers or changing modes. Because no power cycling occurs in this mode, the device may consume higher current in program mode than in normal operation. To place the device in program mode, write 0x1 to Register 0x10, Bits[1:0].

In normal operation (sample mode), the ADPD144RI pulses light and collects data. Power consumption in this mode depends on the pulse count and data rate. To place the device in sample mode, write 0x2 to Register 0x10, Bits[1:0].

SAMPLE MODE OPERATION AND DATA FLOW

In sample mode, the ADPD144RI follows a specific pattern that is set up by the state machine. This pattern is shown in the corresponding data flow diagram in Figure 16. The pattern is as follows:

1. LED pulse and sample. The ADPD144RI pulses an LED emitter. The response of a photodiode or photodiodes to the reflected light is measured by the ADPD144RI. Each data sample is constructed from the sum of n individual pulses, where n_{PULSE} is user configurable between 1 and 255.
2. Intersample averaging. If desired, the logic can average N-samples, from 2 to 128 in powers of 2, to produce output data. New output data is saved to the output registers every N samples.
3. Data read. The host processor reads the converted results from the data register or the FIFO.
4. Repeat. The sequence has a few different loops that enable different types of averaging while keeping both time slots close in time relative to each other.

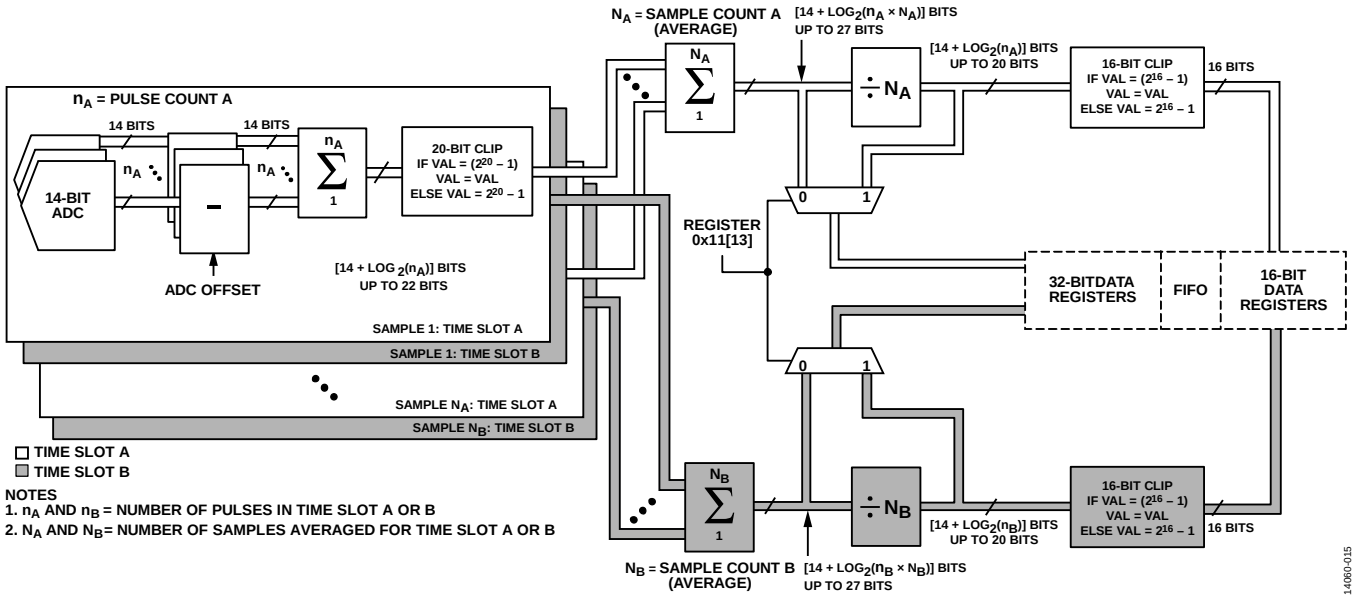

Figure 16. ADPD144RI Data Flow

ADJUSTABLE SAMPLING FREQUENCY

Register 0x12 sets a divider from the 32 kHz clock that determines the sampling frequency of the ADPD144RI. The maximum sampling frequency ($f_{SAMPLE, MAX}$) is determined by the sample periods for Time Slot A and Time Slot B plus the minimum sleep time.

$$f_{SAMPLE, MAX} = 1/(t_A + t_1 + t_B + t_2 + t_{SLEEP\_MIN}) \quad (2)$$

where t_{SLEEP_MIN} is the minimum sleep time required between samples.

See the Pulse Timing section for the definitions of t_A, t_1, t_B, and t_2.

If a given time slot is not in use, elements from that time slot do not factor into the calculation. For example, if Time Slot A is not in use, t_A and t_1 do not add to the sampling period, and the maximum sampling frequency is calculated as follows:

$$f_{SAMPLE, MAX} = 1/(t_B + t_2 + t_{SLEEP\_MIN}) \quad (3)$$

External Sync for Sampling

The ADPD144RI provides an option to use an external sync signal to trigger the sampling periods. This external sample sync signal is provided on the INT pin. This functionality is controlled by Register 0x4F, Bits[2:1]. When enabled, a rising edge on the selected input specifies when the next sample cycle occurs. When triggered, there is a delay of one to two internal sampling clock (32 kHz) cycles, and then the normal start-up sequence occurs. This sequence is the same as if the normal sample timer provided the trigger. To enable the external sync signal feature, use the following procedure:

1. Write 0x1 to Register 0x10 to enter program mode.
2. Write 1 to Register 0x4F, Bit 2 to select the external sync using the INT pin. Enable the INT pin input buffer by writing 1 to Register 0x4F, Bit 1.
3. Write 0x4000 to Register 0x38.
4. Write 0x0002 to Register 0x10 to start the sampling operations.
5. Apply the external sync signal on the INT pin at the desired rate (sampling occurs at that rate). As with normal sampling operations, read the data using the FIFO or the data registers.

The maximum frequency constraints ($f_{SAMPLE, MAX}$) still apply when externally triggering the sample function.

LED Pulse and Sample

At each sampling period, the selected LED driver drives a series of LED pulses in each time slot as shown in Figure 13. The magnitude, duration, and number of pulses are programmable over the I²C interface. Each LED pulse coincides with a sensing period of the AFE. During the AFE sensing period, the charge acquired on the photodiode from ambient light is subtracted from the photodiode charge of the synchronous LED pulse. The combined signals effectively null the contribution of ambient light.

During each pulse period, the photodiode output is integrated and converted to a digital value by the 14-bit ADC. Each subsequent conversion within a time slot is summed with the previous result. Up to 255 pulse values from the ADC can be summed in an individual time slot up to a maximum of 20 bits.

LED DRIVER OPERATION

Integrated LEDs

The ADPD144RI features integrated 660 nm (LED1) and 880 nm (LED2) LED emitters optimized for SpO2 measurement. The anodes of the integrated LEDs require connection to a power supply via the VLED pin, which allows flexibility of the supply voltage for the LEDs as well as decoupling. A capacitor (C_{VLED}), placed close to the VLED pin, provides additional pulse current to the LEDs in pulse mode. Without this capacitor, output impedance of the LED supply can adversely affect the pulsed performance of the LEDs. Selection of the correct C_{VLED} value is covered in the Determining CVLED section.

The LEDX1 and LEDX2 pins are external connections to the LED drivers and cannot be connected when using the integrated LED emitters. It is not possible to combine integrated and external LEDs.

External LEDs

External LEDs can be driven for applications beyond SpO2 or for use in transmission PPG. Leaving the VLED pin unconnected effectively disables the integrated LED emitters on the ADPD144RI. The external LED anodes require connection to an external LED supply, V_{XLED}. The cathodes of the external LEDs are connected to the LEDX1 and LEDX2 pins.

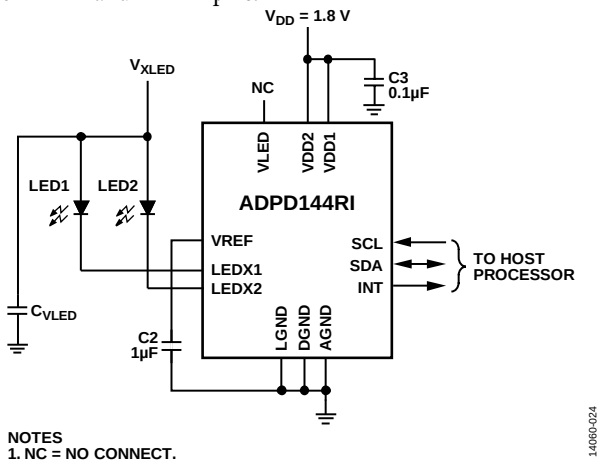

Figure 17. Connection of External LEDs

The ADPD144RI LED drivers are pulsed current sinks, which allows programming of the LED pulse currents without concern for LED supply voltage or LED technology as long as the LEDX1 and LEDX2 voltages stay within the working envelope of the current sinks, 0.2 V > 3.6 V above LGND. Below 0.2 V, the LED driver performance cannot be guaranteed. The LED drivers have an absolute maximum voltage rating of 3.6 V. Any voltage exposure over this rating affects the reliability of the device operation and, in certain circumstances, causes the device to completely cease proper operation.

The voltage that is presented to the LEDX1 and LEDX2 pins when using the external LEDs is the V_{XLED} supply voltage minus the forward voltage drop across the diode plus the voltage drop of any resistance in line with the LED. The operating forward voltage for an LED depends on the type and technology of the LED and varies only a small amount over the operating range of the LED. Forward voltage is typically 1.3 V for an 880 nm LED1 and 1.8 V for a 660 nm LED2, while shorter wavelengths operate at higher forward voltages. Voltage drop across any resistance in series with the LED varies with instantaneous current and must be considered when calculating the voltage at LEDX1 and LEDX2. Even though the average current through the LED is small, the pulsed current is high enough to be affected by series resistance, and care in the layout to reduce series inductance and resistance in the circuit path between the V_{XLED} supply through the external LED and into the LEDX1 and LEDX2 driver pins is recommended.

Multiple Sample Averaging and Accumulation

The ADPD144RI digital processing block can provide sample accumulation and averaging to increase signal resolution and improve signal noise shaping.

As shown in Figure 16, pulses acquired by the AFE (n_A or n_B) are summed and clipped to 20-bit samples at the output of the burst accumulator. The effective gain and dynamic range of the AFE can be further extended to 27 bits by summing multiple samples (N_A or N_B) in the sample accumulator at the expense of the effective sampling rate.

The 27-bit values are padded up to 32-bit words and can be read out directly by using the 32-bit output registers or the 32-bit FIFO configuration. New data is written to the registers at the rate of f_{SAMPLE}/N every N^{th} sample. The 16-bit registers remain active during 32-bit sample accumulation. Data from the sample accumulator is decimated and clipped to prevent overrun of the 16-bit output registers. Sample averaging can be used to integrate the noise while maintaining 16-bit resolution.

Writing 0 to Register 0x11, Bit 13 places the digital decimation filter into the datapath of the 32-bit registers. This provides 20-bit average data to the 32-bit registers. When using the averaging feature, samples can be averaged by powers of 2. The user can select from 2, 4, 8 … up to 128 samples to be averaged.

Data Read

The host processor reads output data from the ADPD144RI, via the I^2C protocol, from the data registers or from the FIFO. New output data is made available every N samples, where N is the user configured averaging factor. The averaging factors for Time Slot A and Time Slot B are configurable independently of each other. If the time slots are the same, both time slots can be configured to save data to the FIFO. If the two averaging factors are different, only one time slot can save data to the FIFO. Data from the other time slot can be read from the output registers.

The data read operations are described in more detail in the Reading Data section.

I²C SERIAL INTERFACE

The ADPD144RI supports an I²C serial interface via the SDA (data) pin and the SCL (clock) pin. All internal registers are accessed through the I²C interface.

The ADPD144RI conforms to the UM10204 I²C-Bus Specification and User Manual, Rev. 05—9 October 2012, available from NXP Semiconductors. The ADPD144RI supports fast mode (400 kbps) data transfer. Register read and write operations are supported, as shown in Figure 18. Figure 2 shows the timing diagram for the I²C interface. The 7-bit I²C slave address for the device is 0x64.

Figure 18 illustrates the ADPD144RI I²C write and read operations. Single word and multiword read operations are supported. For a single register read, the host sends a no acknowledge (NACK) after the second data byte is read and a new register address is needed for each access.

For multiword operations, each pair of data bytes is followed by an acknowledge (ACK) from the host until the last byte of the last word is read. The host indicates the last read word by sending a NACK. When reading from the FIFO (Register 0x60), the data is automatically advanced to the next word in the FIFO, and the space is freed. When reading from other registers, the register address is automatically advanced to the next register, allowing the user to read without readdressing each register and thereby reducing the amount of overhead required to read multiple registers. This auto-increment does not apply to the register that precedes the FIFO, Register 0x5F, or the last data register, Register 0x7F.

All register writes are single word only and require 16 bits (one word) of data.

Table 11. Definitions of I²C Terminology

Term	Description
SCL	Serial clock.
SDA	Serial address and data.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by a master. The ADPD144RI operates as a slave device.
Start (S)	A high to low transition on the SDA line while SCL is high. All transactions begin with a start condition.
Start (Sr)	A repeated start condition.
Stop (P)	A low to high transition on the SDA line while SCL is high. A stop condition terminates all transactions.
ACK	During the acknowledge (ACK) or no acknowledge (NACK) clock pulse, the SDA line is pulled low and remains low.
NACK	During the ACK or NACK clock pulse, the SDA line remains high.
Slave Address	After a start (S), a 7-bit slave address is sent, which is followed by a data direction bit (read or write).
Read (R)	A 1 indicates a request for data.
Write (W)	A 0 indicates a transmission.

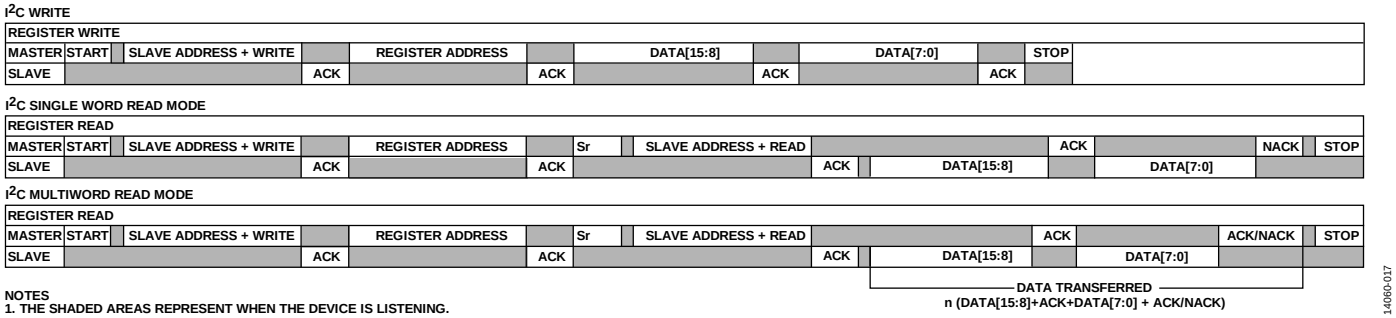

Figure 18. I²C Write and Read Operations

APPLICATIONS INFORMATION

TYPICAL CONNECTION DIAGRAM

Figure 19 illustrates the recommended connection diagram for the ADPD144RI. The 1.8 V I²C communication lines, SCL and SDA, along with the INT line, connect to a system microprocessor or sensor hub. A level translator may be necessary if the I²C lines from the microprocessor are not 1.8 V logic.

Provide the 1.8 V supply, tied to VDD1 and VDD2. Use standard regulator circuits according to the peak current requirements specified in Table 1 and calculated in the Calculating the Total Power Consumption section.

For best noise performance, connect AGND, DGND, and LGND together at a large conductive surface such as a ground plane, ground pour, or large ground trace.

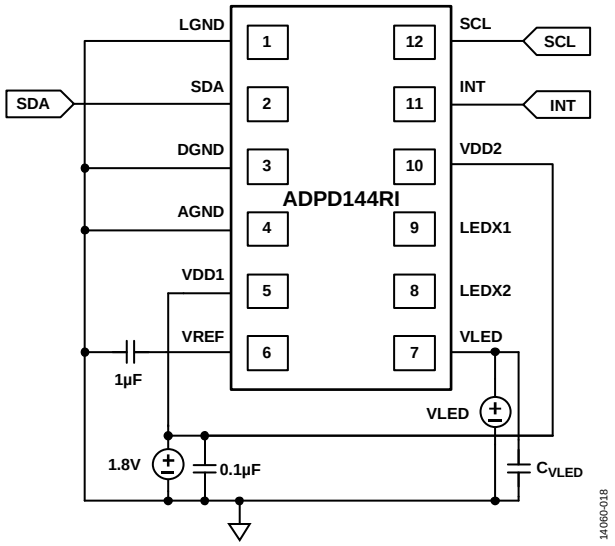

Figure 19. Connection Diagram

LAND PATTERN

Figure 20 shows the recommended PCB footprint (land pattern). Table 7 and Figure 3 provide the recommended soldering profile.

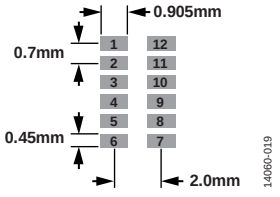

Figure 20. Land Pattern

RECOMMENDED START-UP SEQUENCE

The ADPD144RI does not require a particular power-up sequence. The device powers up in standby mode (Register 0x10 = 0x0000).

From standby mode, to begin measurement, initiate the ADPD144RI as follows:

1. Write 0x0001 to Register 0x10 to force the device into program mode.
2. Registers must be written while the device is in program mode. Registers may be written in any order.
3. Set SAMPLE_CLK, Register 0x4B, Bit 7 (CLK32K_EN) to start the sample clock (32 kHz clock). This step must be done only once after power-up of the device. However, writing to the bit more than once does not cause a problem.
4. Write 0x0002 to Register 0x10 to force the device to normal operation.

The ADPD144RI is now sampling and data can be read from the output register and/or FIFO depending on set configuration.

To place the ADPD144RI into standby mode:

1. Write 0x0001 to Register 0x10 to force the device into program mode.
2. If desired, write registers in any order while the device is in program mode.
3. Write 0x00FF to Register 0x00 to clear all interrupts. If desired, clear the FIFO as well by setting DATA_ACCESS_CTL, Register 0x5F, Bit 0 (FIFO_ACCESS_ENA) and writing 0x80FF to Register 0x00. Reset Register 0x5F, Bit 0 back to 0 when this step is complete.
4. Write 0x0000 to Register 0x10 to force the device into standby mode.
5. This step is optional. For absolute minimum standby power consumption, disable the 32 kHz clock by setting SAMPLE_CLK, Register 0x4B, Bit 7 (CLK32K_EN) to 0. This must be written when the device is in standby mode (Register 0x10 = 0x0).

The ADPD144RI is now in standby mode.

Warning: if 0 is written to Register 0x4B, Bit 7 (CLK32K_EN) while in program mode or normal mode, the device is unable to transition into any other mode, including standby mode. As a result, the power consumption in what appears to be standby mode is greatly elevated. Due to the low current draw of the 32 kHz clock while in operation, it is recommended, from an ease of use perspective, to keep the 32 kHz clock running after the clock is turned on.

READING DATA

The ADPD144RI provides multiple methods for accessing the sample data. Each time slot can be independently configured to provide data access using the FIFO or the data registers. Interrupt signaling is also available to simplify timely data access. The FIFO is available to loosen the system timing requirements for data accesses.

Reading Data Using the FIFO

The ADPD144RI includes a 128-byte FIFO memory buffer that can be configured to store data from either or both time slots. Register 0x11 selects the kind of data from each time slot to be written to the FIFO. Note that both time slots can be enabled to use the FIFO, but only if the output data rate of the time slots is the same.

$$Output\ Data\ Rate = f_{SAMPLE}/N_X \quad (4)$$

where:
N_X is the averaging factor for each time slot (N_A for Time Slot A and N_B for Time Slot B). $N_A = N_B$ must be true to store data from both time slots in the FIFO.

Data packets are written to the FIFO at the output data rate. A data packet for the FIFO consists of a complete sample for each enabled time slot. Data for each photodiode channel can be stored as either 16 or 32 bits. Each time slot can store 2, 4, 8, or 16 bytes of data per sample, depending on the mode and data format. To ensure that data packets are intact, new data is only written to the FIFO if there is sufficient space for a complete packet. Any new data that arrives when there is not enough space is lost. The FIFO continues to store data when sufficient space exists. Always read FIFO data in complete packets to ensure that data packets remain intact.

The number of bytes currently stored in the FIFO is available in Register 0x00, Bits[15:8]. A dedicated FIFO interrupt is also available and automatically generates when a specified amount of data is written to the FIFO.

To read data from the FIFO using an interrupt-based method, use the following procedure:

1. In program mode, configure time slots as required.
2. Set data format for each time slot in Register 0x11.
3. Set FIFO_THRESH in Register 0x06, Bits[13:8] to the interrupt threshold. A recommended value for this is the number of
   16-bit words in a data packet, minus 1. Setting FIFO_THRESH generates an interrupt when there is at least one complete packet in the FIFO.
4. Enable the FIFO interrupt by writing a 0 to FIFO_INT_MASK in Register 0x01, Bit 8. Configure the interrupt pin (INT) by writing the appropriate value to the bits in Register 0x02.
5. Enter normal operation mode by setting Register 0x10 to 0x2.
6. When an interrupt occurs, complete the following steps:
   a. There is no requirement to read the FIFO_SAMPLES register because the interrupt is generated only if there is one or more full packet. Optionally, the interrupt routine can check for the presence of more than one available packet by reading this register.
   b. Write 1 to FIFO_ACCESS_ENA, Register 0x5F, Bit 0 twice in two consecutive write operations.
   c. Read a complete packet using one or more multiword accesses using Register 0x60. Reading the FIFO automatically frees the space for new samples.
   d. Write 0 to FIFO_ACCESS_ENA, Register 0x5F, Bit 0.

The interrupt automatically clears when enough data is read from the FIFO to bring the data level below the threshold.

To read data from the FIFO in a polling method, use the following procedure:

1. In program mode, set the configuration of the time slots as desired for operation.
2. Write Register 0x11 with the desired data format for each time slot.
3. Enter normal operation mode by setting Register 0x10 to 0x02.

Next, begin the polling operations using the following procedure:

1. Wait for the polling interval to expire.
2. Read the FIFO_SAMPLES bits (Register 0x00, Bits[15:8]).
3. If FIFO_SAMPLES ≥ the packet size, read a packet using the following steps:
   a. Write 1 to FIFO_ACCESS_ENA, Register 0x5F, Bit 0 twice in two consecutive write operations.
   b. Read a complete packet using one or more multiword accesses via Register 0x60. Reading the FIFO automatically frees the space for new samples.
   c. Write 0 to FIFO_ACCESS_ENA, Register 0x5F, Bit 0.
   d. Repeat Step 1.

When a mode change is required, or any other disruption to normal sampling is necessary, the FIFO must be cleared. Use the following procedure to clear the state and empty the FIFO:

1. Enter program mode by setting Register 0x10 to 0x1.
2. Write 1 to FIFO_ACCESS_ENA, Register 0x5F, Bit 0 twice in two consecutive write operations.
3. Write 1 to Register 0x00, Bit 15.
4. Write 0 to FIFO_ACCESS_ENA, Register 0x5F, Bit 0.

Reading Data from Registers Using Interrupts

The latest sample data is always available in the data registers and is updated simultaneously at the end of each time slot. The data value for each photodiode channel is available as a 16-bit value in Register 0x64 through Register 0x67 for Time Slot A, and Register 0x68 through Register 0x6B for Time Slot B. If allowed to reach their maximum value, Register 0x64 through Register 0x6B clip. If Register 0x64 through Register 0x6B saturate, the unsaturated (up to 27 bits) values for each channel are available in Register 0x70 through Register 0x77 for Time Slot A and Register 0x78 through Register 0x7F for Time Slot B. Sample interrupts are available to indicate when the registers are updated and can be read. To use the interrupt for a given time slot, use the following procedure:

1. Enable the sample interrupt by writing a 0 to the appropriate bit in Register 0x01. To enable the interrupt for Time Slot A, write 0 to Bit 5. To enable the interrupt for Time Slot B, write 0 to Bit 6. Either or both interrupts can be set. An interrupt is generated when the data registers are updated.
2. Configure the INT pin by writing the appropriate value to the bits in Register 0x02.
3. The interrupt handler must perform the following:
   a. Read Register 0x00 and observe Bit 5 or Bit 6 to confirm which interrupt has occurred. This step is not required if only one interrupt is in use.
   b. Read the data registers before the next sample can be written. The system must have an interrupt latency and service time that is short enough to respond before the next data update, based on the output data rate.
   c. Write a 1 to Bit 5 or Bit 6 in Register 0x00 to clear the interrupt.

If both time slots are in use, it is possible to use only the Time Slot B interrupt to signal when all registers can be read. It is recommended to use the multiword read to transfer the data from the data registers.

Reading Data from Registers Without Interrupts

If the system interrupt response is not fast or predictable enough to use the interrupt method, or if the INT pin is not used, it is possible to obtain reliable data access by using the data hold mechanism. To guarantee that the data read from the registers is from the same sample time, it is necessary to prevent the update of samples while reading the current values.

The method for performing register reads without interrupt timing is as follows:

1. Write a 1 to SLOTA_DATA_HOLD or SLOTB_DATA_HOLD bits, Register 0x5F, Bit 1 and Bit 2, respectively, for the time slot requiring access (both time slots can be accessed). This write prevents sample updates.
2. Read the registers as desired.
3. Write a 0 to the SLOTA_DATA_HOLD or SLOTB_DATA_HOLD bits, Register 0x5F, Bit 1 and Bit 2, respectively. Sample updates are allowed again.

Because a new sample may arrive while the reads are occurring, this method prevents the new sample from partially overwriting the data being read.

CLOCKS AND TIMING CALIBRATION

The ADPD144RI uses two internal time bases. A 32 kHz clock provides master timing for the state machine, sets the sample timing, and determines the output data rate. A separate 32 MHz clock controls the digital processing engine of the ASIC. Both clocks are internally generated and exhibit device to device variation of approximately 10% (typical).

Both clocks can be calibrated to provide accurate timing for applications that require precise timing reference.

Calibrating the 32 kHz Clock

The 32 kHz clock provides the coarse timing reference for sampling time and output data rate. For applications where an accurate time reference is important, such as heart rate measurements, calibrate the 32 kHz clock. To calibrate the clock, take the following steps:

1. Set the sampling frequency to the highest the system can handle, such as 2000 Hz. Because the 32 kHz clock controls sample timing, its frequency is readily accessible via the INT pin. Configure the interrupt by writing 0xC0FF to Register 0x02 and set the interrupt to occur at the sampling frequency by writing 0 to Register 0x01, Bit 5. Monitor the INT pin. The INT pin then pulses at 1/4 the sample frequency.
2. If the monitored interrupt frequency × 4 is less than the set sampling frequency, increase the CLK32K_ADJUST bits, Register 0x4B, Bits[5:0]. If the monitored interrupt frequency × 4 is larger than the set sampling frequency, decrease the CLK32K_ADJUST bits.

Repeat Step 2 until the monitored interrupt signal frequency is close enough to the set sampling frequency. Note that the resolution of the 32 kHz clock adjust is 0.6 kHz per LSB.

Calibrating the 32 MHz Clock

The 32 MHz clock calibrates items associated with fine timing within a sample period, such as LED pulse width and spacing. Only calibrate the 32 MHz clock after the 32 kHz clock is calibrated. To calibrate the 32 MHz clock, take the following steps:

1. Write 0x1 to Register 0x5F, Bit 0 (FIFO_ACCESS_ENA).
2. Enable the CLK_RATIO calculation by writing 0x1 to Register 0x50, Bit 5 (CLK32M_CAL_EN). This function counts the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. With this function enabled, this cycle value is stored in Register 0x0A, Bits[11:0], and nominally this ratio is 0x7D0.
3. Calculate the 32 MHz clock error as follows:

$$Clock\ Error = 32\ MHz \times (1 - CLK\_RATIO/2000) \quad (5)$$

4. Adjust the frequency by setting Bits[7:0] in Register 0x4D per the following equation:

$$CLK32M\_ADJUST = Clock\ Error/109\ kHz \quad (6)$$

5. Write 0x0 to Register 0x50, Bit 5 (CLK32M_CAL_EN) to reset the CLK_RATIO function.

Repeat Step 2 through Step 5 until the desired accuracy is achieved.

Write 0x0 to Register 0x5F, Bit 0 and set the INT pin back to the mode desired for normal operation.

DETERMINING C_{VLED}

The synchronous excitation of the ADPD144RI LED emitters is provided by pulsed current sinks. A pulsed signal greatly reduces the average power requirement of the V_{LED} supply but requires that the V_{LED} supply provide a high dynamic current to satisfy the pulse current. Output impedance, PCB trace resistance and parasitic inductances affect the ability to supply the instantaneous current necessary to maintain the forward voltage across the LED. The C_{VLED} capacitor provides a local, low impedance current source that reduces the dynamic requirements on the V_{LED} supply.

A properly sized C_{VLED} typically has a sufficient storage capacity to prevent the forward voltage on the LED from dropping less than the minimum voltage required for the maximum pulse current. To calculate the recommended minimum value for the C_{VLED}, use the following equation:

$$C_{VLED} = \frac{t_{LED\_PULSE} \times I_{F\_PEAK}}{V_{LED\_MIN} - (V_{F\_PEAK} + 0.2)} \quad (7)$$

where:

C_{VLED} is the minimum size of capacitor in Farads.
t_{LED_PULSE} is the LED pulse width.
I_{F_PEAK} is the maximum forward-bias current on the LED used in operating the device.
V_{LED_MIN} is the voltage from the V_{LED} supply under I_{F_PEAK}.
V_{F_PEAK} is the maximum forward-bias voltage required on the LED to achieve I_{F_PEAK}.

Figure 8 shows the LED forward-bias voltage drop vs. the LED driver current settings for the integrated LED emitters. To determine the C_{VLED} value, determine the peak forward-bias voltage, V_{F_PEAK} of the LED in operation. For example, the 660 nm LED requires a forward voltage (V_F) of approximately 3.5 V to drive a forward current (I_F) of 150 mA. If 150 mA is the highest power used in the design, V_{F_PEAK} = 3.5 V.

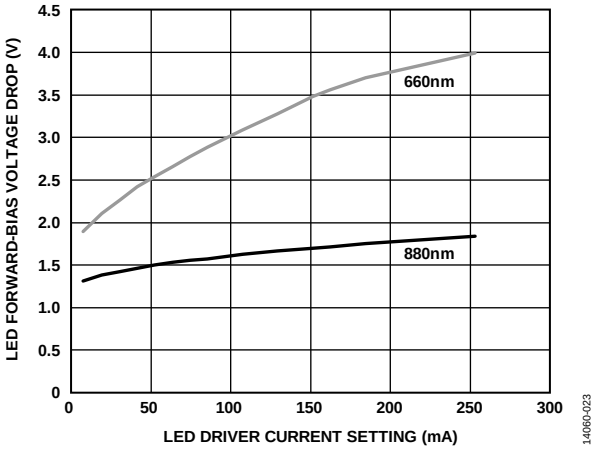

Figure 21. LED Forward-Bias Voltage Drop vs. LED Driver Current Setting for the Integrated LED Emitters

The numerator of the C_{VLED} equation sets up the total discharge amount in coulombs from the bypass capacitor to satisfy a single programmed LED pulse at the maximum current. The denominator represents the difference between the lowest voltage from the V_{LED} supply and the LED required voltage plus the 0.2 V compliance necessary for the driver.

For a typical ADPD144RI example, assume that the lowest value for the V_{LED} supply is 4.0 V and that the peak current is 150 mA for the 660 nm LED (LED1). The minimum value for C_{VLED} is then equal to 1.5 µF.

$$C_{VLED} = (3 \times 10^{-6} \times 0.150)/(4.0 - (3.5 + 0.2)) = 1.5\ \mu F \quad (8)$$

In addition, consider the effect of V_{LED} output impedance and parasitic impedance from the traces. As shown in Equation 8, as the supply voltage drops close to the minimum required anode voltage, the demands on C_{VLED} become greater, forcing the capacitor value higher. Therefore, adding margin on C_{VLED} is strongly recommended. It is also recommended to place C_{VLED} close to the VLED pin to optimize optical pulse quality.

DETERMINING THE AVERAGE LED CURRENT

When the ADPD144RI drives an LED, the ADPD144RI drives the LED in a series of short pulses. Figure 22 shows the typical ADPD144RI configuration of a LED pulse burst sequence. In this sequence, the LED pulse width, t_{LED_PULSE}, is 3 µs, and the LED pulse period, t_{LED_PERIOD}, is 19 µs. The goal of C_{VLED} is to buffer the LED between individual pulses. In the worst case scenario, where the pulse train shown in Figure 22 is a continuous sequence of short pulses, the V_{LED} supply must supply the average current. Therefore, calculate $I_{LED\_AVERAGE}$ as follows:

$$I_{LED\_AVERAGE} = (t_{LED\_PULSE}/t_{LED\_PERIOD}) \times I_{LED\_PEAK} \quad (9)$$

where:
$I_{LED\_AVERAGE}$ is the average current needed, per pulse, from the V_{LED} supply, and $I_{LED\_AVERAGE}$ is also the V_{LED} supply current rating.
I_{LED_PEAK} is the peak current setting of the LED.

For the numbers shown in Figure 22, $I_{LED\_AVERAGE} = 3/19 \times I_{LED\_PEAK}$. For typical LED timing, the average V_{LED} supply current is 3/19 × 250 mA = 39.4 mA, indicating that the V_{LED} supply must support a dc current of 40 mA.

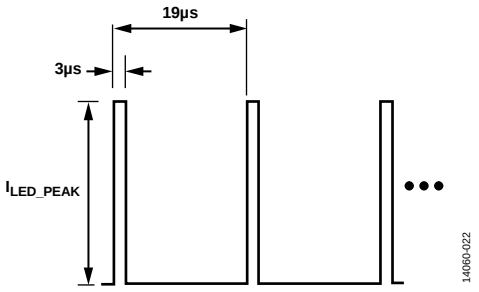

Figure 22. Typical Configuration of a LED Pulse Burst Sequence

CALCULATING THE TOTAL POWER CONSUMPTION

The current consumption of the ADPD144RI depends on the user selected operating configuration, as described in the following equations.

Total Power Consumption

To calculate the total power consumption, use the following equation:

$$Total\ Power = I_{VDD\_AVG} \times I_{LEDA\_AVG} \times V_{LEDA} + I_{LEDB\_AVG} \times V_{LEDB} \quad (10)$$

See the following sections for the definitions of these variables.

Average V_{DD} Supply Current

To calculate the average V_{DD} supply current, use the following equation:

$$I_{VDD\_AVG} = DR \times ((I_{AFE\_A} \times t_{SLOTA}) + (I_{AFE\_B} \times t_{SLOTB}) + Q_{PROC}) + I_{VDD\_STANDBY} \quad (11)$$

where:
DR is the data rate in Hz.
Q_{PROC} is an average charge associated with a processing time. $Q_{PROC} = 0.64 \times 10^{-3}$ mC for Time Slot A enabled), 0.51×10^{-3} mC for Time Slot B enabled, and 0.69×10^{-3} mC for Time Slot A and Time Slot B enabled.
$I_{VDD\_STANDBY} = 3.5 \times 10^{-3}$ mA.

$$I_{AFE\_x}\ (\text{mA}) = 8.9 + (LEDx_{PEAK} - 25)/225 \quad (12)$$

$$t_{SLOTx}\ (\text{sec}) = LEDx\_OFFSET + LEDx\_PERIOD \times PULSE\_COUNT \quad (13)$$

where:
$LEDx_{PEAK}$ is the coarse LED current setting in Register 0x23 and Register 0x24, Bits[3:0], respectively, expressed in mA.
LEDx_OFFSET is the pulse start time offset expressed in seconds.
LEDx_PERIOD is the pulse period expressed in seconds.
PULSE_COUNT is the number of pulses.

Note that if either Time Slot A or Time Slot B is disabled, $I_{AFE\_x} = 0$ for that respective time slot.

Average V_{LEDA} Supply Current

To calculate the average V_{LED} supply current (I_{LEDA_AVG}) for Time Slot A, use the following equation:

$$I_{LEDA\_AVG} = (SLOTA\_LED\_WIDTH/1 \times 10^{6}) \times LEDA_{PEAK} \times DR \times PULSE\_COUNT \quad (14)$$

where:
SLOTA_LED_WIDTH is the width of the LED pulse assigned to Time Slot A.
$LEDA_{PEAK}$ is $LED1_{PEAK}$ or $LED2_{PEAK}$, expressed in mA, for whichever LED is selected for Time Slot A.

Average V_{LEDB} Supply Current

To calculate the average V_{LED} supply current (I_{LEDB_AVG}) for Time Slot B, use the following equation:

$$I_{LEDB\_AVG} = (SLOTB\_LED\_WIDTH/1 \times 10^{6}) \times LEDB_{PEAK} \times DR \times PULSE\_COUNT \quad (15)$$

where:
SLOTB_LED_WIDTH is the width of the LED pulse assigned to Time Slot B.
$LEDB_{PEAK}$ is $LED1_{PEAK}$ or $LED2_{PEAK}$, expressed in mA, for whichever LED is selected for Time Slot B.

OPTIMIZING SNR PER WATT

The ADPD144RI offers a variety of parameters that the user can adjust to achieve the best signal. One of the key goals of system performance is to obtain the best system SNR for the lowest total power, which is often referred to as optimizing SNR per watt. In systems where SNR is the primary design goal and power is a secondary concern, there may be a configuration that achieves the same SNR for an overall lower system power.

Optimizing for Peak SNR

The first step in optimizing for peak SNR is to find a TIA gain and LED level that gives the best performance where the number of LED pulses remains constant. It is important to note that the SNR improves as a square root of the number of pulses averaged together, whereas LED power consumed is directly proportional to the number of LED pulses. For every doubling of the LED pulse count, there is a doubling of the LED power consumed and a 3 dB SNR improvement. As a result, avoid any change in the gain configuration that provides less than 3 dB of improvement for a 2× power penalty. Any TIA gain configuration that provides more than 3 dB of improvement for a 2× power penalty is recommended. If peak SNR is the goal and there is no issue saturating the photodiode with LED current at any gain, the 50,000 TIA gain setting is an optimal choice. After the SNR per pulse per channel is optimized, the user can then increase the number of pulses to achieve the desired system SNR.

Optimizing SNR per Watt in a Signal Limited System

In practice, optimizing for peak SNR is not always practical. One scenario in which the PPG signal has a poor SNR is the signal limited regime. In this scenario, the LED current reaches an upper limit before the desired dc return level is achieved.

Tuning in this case starts where the peak SNR tuning stops. The starting point is nominally a 50,000 gain, as long as the lowest LED current setting of 8 mA does not saturate the photodiode and the 50,000 gain provides enough protection against intense background light. In these cases, use a 25,000 gain as the starting point.

The goal of the tuning process is to bring the dc return signal to a specific ADC range, such as 50% or 60%. The ADC range choice is a function of the margin of headroom needed to prevent saturation as the dc level fluctuates over time. The SNR of the PPG waveform is always some percentage of the dc level. If the target level cannot be achieved at the base gain, increase the gain and repeat the procedure. The tuning system may need to place an upper limit on the gain to prevent saturation from ambient signals.

Tuning the Pulse Count

After the LED peak current and TIA gain are optimized, increasing the number of pulses per sample increases the SNR by the square root of the number of pulses. There are two ways to increase the pulse count. The pulse count registers (Register 0x31, Bits[15:8], and Register 0x36, Bits[15:8]) change the number of pulses per internal sample. Register 0x15, Bits[6:4] and Bits[10:8], controls the number of internal samples that are averaged together before the data is sent to the output. Therefore, the number of pulses per sample is the pulse count register multiplied by the number of subsequent samples being averaged. In general, the internal sampling rate increases as the number of internal sample averages increase to maintain the desired output data rate. The SNR per watt is most optimal with pulse count values of 16 or less. Above pulse count values of 16, the square root relationship does not hold in the pulse count register. However, this relationship continues to hold when averaged between samples using Register 0x15.

Note that increasing the LED peak current increases SNR almost directly proportional to LED power, whereas increasing the number of pulses by a factor of n_{PULSE} results in only a nominal $\sqrt{(n_{PULSE})}$ increase in SNR.

When using the sample sum and average function (Register 0x15), the output data rate decreases by the number of summed samples. To maintain a static output data rate, increase the sample frequency (Register 0x12) by the same factor as that selected in Register 0x15. For example, for a 100 Hz output data rate and a sample sum and average of four samples, set the sample frequency to 400 Hz.

TIA ADC Mode

The device can be placed in TIA ADC mode, which ties the TIA directly to the ADC, bypassing the analog ambient light rejection block. TIA ADC mode provides a relative measure of the amount of background light present at the input of the device. This mode only measures dc light and does not measure the light returned from the LED pulse. To enter TIA ADC mode, write 0xB065 to Register 0x45 and write 0x0000 to the ADC offset registers, Register 0x18 through Register 0x21. Increasing light causes a decrease in the output values because the TIA is an inverting stage. The data registers then read a relative amount of dc light. On this device, use TIA ADC mode only as a relative measurement. This test looks for devices that have a high resistance between inputs due to solder flux because this resistance manifests itself as an elevated dc current.

MECHANICAL CONSIDERATIONS FOR COVERING THE ADPD144RI

In some applications, it may be necessary to cover the ADPD144RI to protect the device from moisture. The ADPD144RI is designed with this necessity in mind. The unique cross section of the device, as shown in Figure 11, prevents light from going directly from the LED to the detector even with a reasonably thick window. The window thickness must be less than 1 mm.

SAMPLE SETUP FILE SpO2

The following sequence of register writes configures the device for optimal reading of the SpO2 levels in reflectance mode using the integrated 660 nm (LED1) and 880 nm (LED2) LED emitters. In this setup, all four photodiodes are connected to Channel 3 and Channel 4 for best SNR. Eight LED pulses per slot and eight samples per average. The optical data rate is set to 100 data reads per second for Time Slot A and Time Slot B. Unwritten registers are set to their default values at power up and stay that way unless written to.

Figure 23 shows the reflectance PPG taken when using the example setup file detailed in Table 12 programmed through Analog Devices, Inc., Wavetool software available on the ADPD144RI product page.

Figure 23. Reflectance PPG Taken Using the Example SpO2 Setup File (see Table 12) Programmed Through Analog Devices Wavetool Software

Table 12. Example SpO2 Setup File

Register	Value	Register Name	Description
0x10	0x0001	Mode	Set this register to 0001 to write to registers.
0x02	0x0005	INT_IO_CTL	Enables the interrupt drive, low active.
0x11	0x30A9	SLOT_EN	If FIFO full drop package, Time Slot A = sample mode, Time Slot B = sample mode, Time Slot A = 32-bit sum, and Time Slot B = 32-bit sum.
0x12	0x000A	F_SAMPLE	Sample rate = 800 Hz.
0x14	0x0116	PD_LED_SELECT	PD1, PD2, PD3, and PD4 into Channel 3 and Channel 4, Time Slot A and Time Slot B active, pulse LED2 Time Slot A, and pulse LED1 Time Slot B. See Figure 14.
0x15	0x0330	NUM_AVG	Average samples for Time Slot A = 8, and average samples for Time Slot B = 8.
0x18	0x3FFF	SLOTA_CH1_OFFSET	16,383 not used.
0x19	0x3FFF	SLOTA_CH2_OFFSET	16,383 not used.
0x1A	0x1FF0	SLOTA_CH3_OFFSET	8,176 half scale.
0x1B	0x1FF0	SLOTA_CH4_OFFSET	8,176 half scale.
0x1E	0x3FFF	SLOTB_CH1_OFFSET	16,383 not used.
0x1F	0x3FFF	SLOTB_CH2_OFFSET	16,383 not used.
0x20	0x1FF0	SLOTB_CH3_OFFSET	8,176 half scale.
0x21	0x1FF0	SLOTB_CH4_OFFSET	8,176 half scale.
0x23	0x3005	ILED1_COARSE	Scale 100% and driver current = 100 mA.
0x24	0x3007	ILED2_COARSE	Scale 100% and driver current = 130 mA.
0x25	0x0207	ILED_FINE	LED1 = 593.75 ns and LED2 = 593.75 ns.
0x30	0x0319	SLOTA_LEDMODE	Pulse Offset A = 25 µs and pulse width = 3 µs.
0x31	0x0813	SLOTA_NUMPULSES	Pulse Period A = 19 µs and Pulse Count A = 8.
0x35	0x0319	SLOTB_LEDMODE	Pulse Offset B = 25 µs and pulse width = 3 µs.
0x36	0x0813	SLOTB_NUMPULSES	Pulse Period B = 19 µs and Pulse Count A = 8.
0x39	0x21F3	SLOTA_AFEMODE	Time Slot A AFE fine offset = 593.75 ns (19 × 31.25 ns), AFE offset = 15 µs, and AFE width = 4 µs.
0x3B	0x21F3	SLOTB_AFEMODE	Time Slot A AFE fine offset = 593.75 ns (19 × 31.25 ns), AFE offset = 15 µs, and AFE width = 4 µs.
0x42	0x1C36	SLOTA_GAIN	Time Slot A TIA = 50,000, band-pass filter = 390 kHz/100 kHz, VREF = 1.265 V, and integrator = 200,000/6.33 pF.
0x44	0x1C36	SLOTB_GAIN	Time Slot B TIA = 50,000, band-pass filter = 390 kHz/100 kHz, VREF = 1.265 V, and integrator = 200,000/6.33 pF.
0x4E	0x0040	ADC_TIMING	The ADC clock only pulses during conversion.
0x10	0x0002	Mode	Set this register to 0002 to run the device.

REGISTER LISTING

Table 13. Register Map

Addr	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W[1]
0x00	Status	[15:8]	FIFO_SAMPLES								0x0000	RW1C
		[7:0]	Reserved	SLOTB_INT	SLOTA_INT	Reserved						
0x01	INT_MASK	[15:8]	Reserved							FIFO_INT_MASK	0x00FF	R/W
		[7:0]	Reserved	SLOTB_INT_MASK	SLOTA_INT_MASK	Reserved						
0x02	INT_IO_CTL	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved					INT_ENA	INT_DRV	INT_POL		
0x06	FIFO_THRESH	[15:8]	Reserved		FIFO_THRESH						0x0000	R/W
		[7:0]	Reserved									
0x08	DEVID	[15:8]	DEV_ID[15:8]								0x0416	R
		[7:0]	DEV_ID[7:0]									
0x0A	CLK_RATIO	[15:8]	Reserved				CLK_RATIO[11:8]				0x0000	R
		[7:0]	CLK_RATIO[7:0]									
0x10	Mode	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved						Mode			
0x11	SLOT_EN	[15:8]	Reserved		RDOUT_MODE	FIFO_OVRN_PREVENT	Reserved			SLOTB_FIFO_MODE[8]	0x1000	R/W
		[7:0]	SLOTB_FIFO_MODE[7:6]		SLOTB_EN	SLOTA_FIFO_MODE[4:2]			Reserved	SLOTA_EN		
0x12	FSAMPLE	[15:8]	FSAMPLE[15:8]								0x0028	R/W
		[7:0]	FSAMPLE[7:0]									
0x14	PD_LED_SELECT	[15:8]	Reserved				SLOTB_PD_SEL[11:8]				0x0541	R/W
		[7:0]	SLOTA_PD_SEL[7:4]				SLOTB_LED_SEL[3:2]		SLOTA_LED_SEL[1:0]			
0x15	NUM_AVG	[15:8]	Reserved					SLOTB_NUM_AVG			0x0600	R/W
		[7:0]	Reserved	SLOTA_NUM_AVG			Reserved					
0x18	SLOTA_CH1_OFFSET	[15:8]	SLOTA_CH1_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH1_OFFSET[7:0]									
0x19	SLOTA_CH2_OFFSET	[15:8]	SLOTA_CH2_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH2_OFFSET[7:0]									
0x1A	SLOTA_CH3_OFFSET	[15:8]	SLOTA_CH3_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH3_OFFSET[7:0]									
0x1B	SLOTA_CH4_OFFSET	[15:8]	SLOTA_CH4_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTA_CH4_OFFSET[7:0]									
0x1E	SLOTB_CH1_OFFSET	[15:8]	SLOTB_CH1_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH1_OFFSET[7:0]									
0x1F	SLOTB_CH2_OFFSET	[15:8]	SLOTB_CH2_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH2_OFFSET[7:0]									
0x20	SLOTB_CH3_OFFSET	[15:8]	SLOTB_CH3_OFFSET[15:8]								0x2000	R/W
		[7:0]	SLOTB_CH3_OFFSET[7:0]									
0x21	SLOTB_CH4_OFFSET	[15:8]	SLOTB_CH4_OFFSET[15:8]								0x2000	RW
		[7:0]	SLOTB_CH4_OFFSET[7:0]									
0x23	ILED1_COARSE	[15:8]	Reserved		ILED1_SCALE	Reserved					0x3000	R/W
		[7:0]	Reserved				ILED1_COARSE					
0x24	ILED2_COARSE	[15:8]	Reserved		ILED2_SCALE	Reserved					0x3000	R/W
		[7:0]	Reserved				ILED2_COARSE					
0x25	ILED_FINE	[15:8]	Reserved					ILED2_FINE[10:8]			0x630C	R/W
		[7:0]	ILED2_FINE[7:6]		Reserved	ILED1_FINE						
0x30	SLOTA_LEDMODE	[15:8]	SLOTA_LEDMODE[15:8]								0x0320	R/W
		[7:0]	SLOTA_LEDMODE[7:0]									
0x31	SLOTA_NUMPULSES	[15:8]	SLOTA_NUMPULSES								0x0818	R/W
		[7:0]	Reserved (write 0x13)									

Addr	Name	Bits	Bit 15 / Bit 7	Bit 14 / Bit 6	Bit 13 / Bit 5	Bit 12 / Bit 4	Bit 11 / Bit 3	Bit 10 / Bit 2	Bit 9 / Bit 1	Bit 8 / Bit 0	Reset	R/W[1]
0x34	LED_DISABLE	[15:8]	Reserved						SLOTB_LED_DIS	SLOTA_LED_DIS	0x0000	R/W
		[7:0]	Reserved									
0x35	SLOTB_LEDMODE	[15:8]	SLOTB_LEDMODE[15:8]								0x0320	R/W
		[7:0]	SLOTB_LEDMODE[7:0]									
0x36	SLOTB_NUMPULSES	[15:8]	SLOTB_NUMPULSES								0x0818	R/W
		[7:0]	Reserved (write 0x13)									
0x38	EXT_SYNC_STARTUP	[15:8]	Reserved	EXT_SYNC_ENA	Reserved						0x0000	R/W
		[7:0]	Reserved									
0x39	SLOTA_AFEMODE	[15:8]	SLOTA_AFEMODE[15:8]								0x22FC	R/W
		[7:0]	SLOTA_AFEMODE[7:0]									
0x3B	SLOTB_AFEMODE	[15:8]	SLOTB_AFEMODE[15:8]								0x22FC	R/W
		[7:0]	SLOTB_AFEMODE[7:0]									
0x42	SLOTA_GAIN	[15:8]	Reserved								0x1C38	R/W
		[7:0]	Reserved	SLOTA_TIA_IND_EN	Reserved (write 0x03)		Reserved (write 0x1)		SLOTA_TIA_GAIN			
0x43	SLOTA_AFE_CON	[15:8]	SLOTA_AFE_CON[15:8]								0xADA5	R/W
		[7:0]	SLOTA_AFE_CON[7:0]									
0x44	SLOTB_GAIN	[15:8]	Reserved								0x1C38	R/W
		[7:0]	Reserved	SLOTB_TIA_IND_EN	Reserved (write 0x03)		Reserved (write 0x1)		SLOTB_TIA_GAIN			
0x45	SLOTB_AFE_CON	[15:8]	SLOTB_AFE_CON[15:8]								0xADA5	R/W
		[7:0]	SLOTB_AFE_CON[7:0]									
0x4B	SAMPLE_CLK	[15:8]	Reserved								0x2612	R/W
		[7:0]	CLK32K_EN	Reserved	CLK32K_ADJUST							
0x4D	CLK32M_ADJUST	[15:8]	Reserved								0x425E	R/W
		[7:0]	CLK32M_ADJUST									
0x4E	ADC_TIMING	[15:8]	ADC_TIMING[15:8]								0x0060	R/W
		[7:0]	ADC_TIMING[7:0]									
0x4F	EXT_SYNC_SEL	[15:8]	Reserved								0x2090	R/W
		[7:0]	Reserved					EXT_SYNC_SEL	INT_IE	Reserved		
0x50	CLK32M_CAL_EN	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved		CLK32M_CAL_EN	Reserved						
0x55	TIA_INDEP_GAIN	[15:8]	Reserved				SLOTB_TIA_GAIN_4		SLOTB_TIA_GAIN_3		0x0000	R/W
		[7:0]	SLOTB_TIA_GAIN_2		SLOTA_TIA_GAIN_4		SLOTA_TIA_GAIN_3		SLOTA_TIA_GAIN_2			
0x5F	DATA_ACCESS_CTL	[15:8]	Reserved								0x0000	R/W
		[7:0]	Reserved					SLOTB_DATA_HOLD	SLOTA_DATA_HOLD	FIFO_ACCESS_ENA		
0x60	FIFO_ACCESS	[15:8]	FIFO_DATA[15:8]								0x0000	R
		[7:0]	FIFO_DATA[7:0]									
0x64	SLOTA_PD1_16BIT	[15:8]	SLOTA_PD1_16BIT [15:8]								0x0000	R
		[7:0]	SLOTA_PD1_16BIT [7:0]									
0x65	SLOTA_PD2_16BIT	[15:8]	SLOTA_PD2_16BIT [15:8]								0x0000	R
		[7:0]	SLOTA_PD2_16BIT [7:0]									
0x66	SLOTA_PD3_16BIT	[15:8]	SLOTA_PD3_16BIT [15:8]								0x0000	R
		[7:0]	SLOTA_PD3_16BIT [7:0]									
0x67	SLOTA_PD4_16BIT	[15:8]	SLOTA_PD4_16BIT [15:8]								0x0000	R
		[7:0]	SLOTA_PD4_16BIT [7:0]									
0x68	SLOTB_PD1_16BIT	[15:8]	SLOTB_PD1_16BIT [15:8]								0x0000	R
		[7:0]	SLOTB_PD1_16BIT [7:0]									
0x69	SLOTB_PD2_16BIT	[15:8]	SLOTB_PD2_16BIT [15:8]								0x0000	R
		[7:0]	SLOTB_PD2_16BIT [7:0]									

Addr	Name	Bits	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Reset	R/W[1]
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0		
0x6A	SLOTB_PD3_16BIT	[15:8]	SLOTB_PD3_16BIT [15:8]								0x0000	R
		[7:0]	SLOTB_PD3_16BIT [7:0]									
0x6B	SLOTB_PD4_16BIT	[15:8]	SLOTB_PD4_16BIT [15:8]								0x0000	R
		[7:0]	SLOTB_PD4_16BIT [7:0]									
0x70	A_PD1_LOW	[15:8]	SLOTA_PD1_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_PD1_LOW[7:0]									
0x71	A_PD2_LOW	[15:8]	SLOTA_PD2_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_PD2_LOW[7:0]									
0x72	A_PD3_LOW	[15:8]	SLOTA_PD3_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_PD3_LOW[7:0]									
0x73	A_PD4_LOW	[15:8]	SLOTA_PD4_LOW[15:8]								0x0000	R
		[7:0]	SLOTA_PD4_LOW[7:0]									
0x74	A_PD1_HIGH	[15:8]	SLOTA_PD1_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_PD1_HIGH[7:0]									
0x75	A_PD2_HIGH	[15:8]	SLOTA_PD2_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_PD2_HIGH[7:0]									
0x76	A_PD3_HIGH	[15:8]	SLOTA_PD3_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_PD3_HIGH[7:0]									
0x77	A_PD4_HIGH	[15:8]	SLOTA_PD4_HIGH[15:8]								0x0000	R
		[7:0]	SLOTA_PD4_HIGH[7:0]									
0x78	B_PD1_LOW	[15:8]	SLOTB_PD1_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_PD1_LOW[7:0]									
0x79	B_PD2_LOW	[15:8]	SLOTB_PD2_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_PD2_LOW[7:0]									
0x7A	B_PD3_LOW	[15:8]	SLOTB_PD3_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_PD3_LOW[7:0]									
0x7B	B_PD4_LOW	[15:8]	SLOTB_PD4_LOW[15:8]								0x0000	R
		[7:0]	SLOTB_PD4_LOW[7:0]									
0x7C	B_PD1_HIGH	[15:8]	SLOTB_PD1_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_PD1_HIGH[7:0]									
0x7D	B_PD2_HIGH	[15:8]	SLOTB_PD2_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_PD2_HIGH[7:0]									
0x7E	B_PD3_HIGH	[15:8]	SLOTB_PD3_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_PD3_HIGH[7:0]									
0x7F	B_PD4_HIGH	[15:8]	SLOTB_PD4_HIGH[15:8]								0x0000	R
		[7:0]	SLOTB_PD4_HIGH[7:0]									

[1] RW1C means write 1 to clear.

LED CONTROL REGISTERS

Table 14. LED Control Registers

Address	Data Bit	Default Value	Access	Name	Description
0x14	[15:12]	0x0	R/W	Reserved	Write 0x0 to these bits for proper operation.
	[11:8]	0x5	R/W	SLOTB_PD_SEL	Selects connection of PD1, PD2, PD3, or PD4 for Time Slot B as shown in Figure 14. 0x1: Channel 3 and Channel 4 are connected during Time Slot B. 0x4: Channel 1, Channel 2, Channel 3, and Channel 4 are connected during Time Slot B. Other: reserved.
	[7:4]	0x4	R/W	SLOTA_PD_SEL	Selects connection of PD1, PD2, PD3, or PD4 for Time Slot A as shown in Figure 14. 0x1: Channel 3 and Channel 4 are connected during Time Slot A. 0x4: Channel 1, Channel 2, Channel 3, and Channel 4 are connected during Time Slot A. Other: reserved.
	[3:2]	0x0	R/W	SLOTB_LED_SEL	Time Slot B LED configuration. These bits determine which LED is associated with Time Slot B. 0x0: reserved. 0x1: LEDX1 pulses during Time Slot B. 0x2: LEDX2 pulses during Time Slot B. 0x3: reserved.
	[1:0]	0x1	R/W	SLOTA_LED_SEL	Time Slot A LED configuration. These bits determine which LED is associated with Time Slot A. 0x0: reserved. 0x1: LEDX1 pulses during Time Slot A. 0x2: LEDX2 pulses during Time Slot A. 0x3: reserved.
0x23	[15:14]	0x0	R/W	Reserved	
	13	0x1	R/W	ILED1_SCALE	LEDX1 current scale factor. 1: 100% strength. 0: 40% strength (recommended operation setting). *LEDX1 Current Scale* = 0.4 + 0.6 × *Register 0x23, Bit 13*.
	12	0x1	R/W	Reserved	
	[11:4]	0x0	R/W	Reserved	Write 0x03.
	[3:0]	0x0	R/W	ILED1_COARSE	LEDX1 coarse current setting. Coarse current sink target value of LED1 in standard operation. 0: 25 mA. 1: 40 mA. 2: 55 mA. 3: 70 mA. 4: 85 mA. 5: 100 mA. … 15: 250 mA. $LEDX1_{PEAK} = LEDX1_{COARSE} \times LEDX1_{FINE} \times LEDX1_{SCALE}$ where: $LEDX1_{PEAK}$ is the LEDX1 peak target value (mA). $LEDX1_{COARSE} = 28 + 15.5 \times$ (*Register 0x23, Bits[3:0]*). $LEDX1_{FINE} = 0.71 + 0.024 \times$ (*Register 0x25, Bits[4:0]*). $LEDX1_{SCALE} = 0.4 + 0.6 \times$ (*Register 0x23, Bit 13*).

Address	Data Bit	Default Value	Access	Name	Description
0x24	[15:14]	0x0	R/W	Reserved	
	13	0x1	R/W	ILED2_SCALE	LED2 current scale factor. 1: 100% strength. 0: 40% strength (recommended operation setting). *LED2 Current Scale* = 0.4 + 0.6 × (*Register 0x24, Bit 13*)
	12	0x1	R/W	Reserved	
	[11:4]	0x0	R/W	Reserved	Write 0x03.
	[3:0]	0x0	R/W	ILED2_COARSE	LED2 coarse current setting. Coarse current sink target value of LED2 in standard operation. See Register 0x23, Bits[3:0] for values. $LED2_{PEAK} = LED2_{COARSE} \times LED2_{FINE} \times LED2_{SCALE}$ where: $LED2_{PEAK}$ is the LED2 peak target value (mA). $LED2_{COARSE}$ = 28 + 15.5 × (*Register 0x24, Bits[3:0]*). $LED2_{FINE}$ = 0.71 + 0.024 × (*Register 0x25, Bits[10:6]*). $LED2_{SCALE}$ = 0.4 + 0.6 × (*Register 0x24, Bit 13*).
0x25	[15:11]	0xC	R/W	Reserved	
	[10:6]	0xC	R/W	ILED2_FINE	LED2 fine adjust. Current adjust multiplier for LED2. *LED2 Fine Adjust* = 0.71 + 0.024 × (*Register 0x25, Bits[10:6]*) See Register 0x24, Bits[3:0], for the full LED2 formula.
	5	0x0	R/W	Reserved	
	[4:0]	0xC	R/W	ILED1_FINE	LEDX1 fine adjust. Current adjust multiplier for LEDX1. *LEDX1 Fine Adjust* = 0.71 + 0.024 × (*Register 0x25, Bits[4:0]*) See Register 0x23, Bits[3:0], for the full LEDX1 formula.
0x30	[15:0]	0x0320	R/W	SLOTA_LEDMODE	LED configuration for Time Slot A. Recommended setting: write 0x0319.
0x31	[15:8]	0x08	R/W	SLOTA_NUMPULSES	LED Time Slot A pulse count. n_A: number of LED pulses in Time Slot A, typically LEDX1. A setting of six pulses (0x06) is typical.
	[7:0]	0x18	R/W	Reserved (write 0x13)	Write 0x13.
0x34	[15:10]	0x00	R/W	Reserved	
	9	0x0	R/W	SLOTB_LED_DIS	Time Slot B LED disable. 1: disables the LED that is assigned to Time Slot B. Register 0x34 keeps the drivers active and prevents them from pulsing current to the LEDs. Disabling both LEDs via this register is often used to measure the dark level. Use Register 0x11 instead to enable or disable the actual time slot usage and not the LED only.
	8	0x0	R/W	SLOTA_LED_DIS	Time Slot A LED disable. 1: disables the LED that is assigned to Time Slot A. Use Register 0x11 instead to enable or disable the actual time slot usage and not the LED only.
	[7:0]	0x00	R/W	Reserved	
0x35	[15:0]	0x0320	R/W	SLOTB_LEDMODE	LED configuration for Time Slot B. Recommended setting: write 0x0319.
0x36	[15:8]	0x08	R/W	SLOTB_NUMPULSES	LED Time Slot B pulse count. n_B: number of LED pulses in Time Slot B, typically LED2. A setting of six pulses (0x06) is typical.
	[7:0]	0x18	R/W	Reserved (write 0x13)	Write 0x13.

AFE CONFIGURATION REGISTERS

Table 15. AFE Configuration Registers, Time Slot A

Address	Data Bit	Default Value	Access	Name	Description
0x39	[15:0]	0x22FC	R/W	SLOTA_AFEMODE	AFE configuration for Time Slot A. Recommended setting: write 0x21F4.
0x42	[15:7]	0x038	R/W	Reserved	
	6	0x0	R/W	SLOTA_TIA_IND_EN	Enable Time Slot A TIA gain individual settings. When this bit is enabled, Channel 1 receives the TIA gain from Register 0x42, Bits[1:0], and Channel 2 to Channel 4 receive the settings from Register 0x55, Bits[5:0]. 0: disable TIA gain individual setting. 1: enable TIA gain individual setting.
	[5:4]	0x3	R/W	Reserved	Write 0x03.
	[3:2]	0x2	R/W	Reserved	Write 0x1.
	[1:0]	0x0	R/W	SLOTA_TIA_GAIN	TIA gain for Time Slot A. When SLOTA_TIA_ IND_EN is enabled, this value is for Time Slot A Channel 1 TIA gain. When SLOTA_TIA_IND_EN is disabled, it is for all four Time Slot A channel TIA gain settings. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
0x43	[15:0]	0xADA5	R/W	SLOTA_AFE_CON	AFE connection in Time Slot A. 0xADA5: analog full path mode. 0xB065: TIA ADC mode. Others: reserved.
0x55	[15:12]	0x0	R/W	Reserved	
	[11:10]	0x0	R/W	SLOTB_TIA_GAIN_4	TIA gain for Time Slot B Channel 4. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[9:8]	0x0	R/W	SLOTB_TIA_GAIN_3	TIA gain for Time Slot B Channel 3. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[7:6]	0x0	R/W	SLOTB_TIA_GAIN_2	TIA gain for Time Slot B Channel 2. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[5:4]	0x0	R/W	SLOTA_TIA_GAIN_4	TIA gain for Time Slot A Channel 4. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
	[3:2]	0x0	R/W	SLOTA_TIA_GAIN_3	TIA gain for Time Slot A Channel 3. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.

Address	Data Bit	Default Value	Access	Name	Description
	[1:0]	0x0	R/W	SLOTA_TIA_GAIN_2	TIA gain for Time Slot A Channel 2. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.

Table 16. AFE Configuration Registers, Time Slot B

Address	Data Bit	Default Value	Access	Name	Description
0x3B	[15:0]	0x22FC	R/W	SLOTB_AFEMODE	AFE configuration for Time Slot B. Recommended setting: write 0x21F4.
0x44	[15:7]	0x038	R/W	Reserved	
	6	0x0	R/W	SLOTB_TIA_IND_EN	Enable Time Slot B TIA gain individual settings. When it is enabled, Channel 1 receives the TIA gain from Register 0x44, Bits[1:0], and Channel 2 to Channel 4 receive the settings from Register 0x55, Bits[11:6]. 0: disable TIA gain individual setting. 1: enable TIA gain individual setting.
	[5:4]	0x3	R/W	Reserved	Write 0x03.
	[3:2]	0x2	R/W	Reserved	Write 0x1.
	[1:0]	0x0	R/W	SLOTB_TIA_GAIN	TIA gain for Time Slot B. When SLOTB_TIA_IND_EN is enabled, this value is for Time Slot B Channel 1 TIA gain. When SLOTB_TIA_ IND_EN is disabled, it is for all four Time Slot B Channel TIA gain settings. 0: 200 kΩ. 1: 100 kΩ. 2: 50 kΩ. 3: 25 kΩ.
0x45	[15:0]	0xADA5	R/W	SLOTB_AFE_CON	AFE connection in Time Slot B. 0xADA5: analog full path mode. 0xB065: TIA ADC mode. Others: reserved.

SYSTEM REGISTERS

Table 17. System Registers

Address	Data Bit	Default	Access	Name	Description
0x00	[15:8]	0x00	R/W	FIFO_SAMPLES	FIFO status. Number of available bytes to be read from the FIFO. When comparing this to the FIFO length threshold (Register 0x06, Bits[13:8]), note that the FIFO status value is in bytes and the FIFO length threshold is in words, where one word = two bytes. With the FIFO_ACCESS_ENA bit set, write 1 to Bit 15 of FIFO_SAMPLES to clear the contents of the FIFO.
	7	0x00	R/W	Reserved	
	6	0x00	R/W	SLOTB_INT	Time Slot B interrupt. Describes the type of interrupt event. A 1 indicates an interrupt of a particular event type has occurred. Write a 1 to clear the corresponding interrupt. After clearing the interrupt, the register goes to 0. Writing a 0 to this register has no effect.
	5	0x00	R/W	SLOTA_INT	Time Slot A interrupt. Describes the type of interrupt event. A 1 indicates an interrupt of a particular event type has occurred. Write a 1 to clear the corresponding interrupt. After clearing the interrupt, the register goes to 0. Writing a 0 to this register has no effect.
	[4:0]	0x00	R/W	Reserved	

Address	Data Bit	Default	Access	Name	Description
0x01	[15:9]	0x00	R/W	Reserved	
	8	0x00	R/W	FIFO_INT_MASK	Sends an interrupt when the FIFO data length has exceeded the FIFO length threshold in Register 0x06, Bits[13:8]. A 0 enables the interrupt.
	7	0x1	R/W	Reserved	
	6	0x1	R/W	SLOTB_INT_MASK	Sends an interrupt on the Time Slot B sample. A 0 enables the interrupt.
	5	0x1	R/W	SLOTA_INT_MASK	Sends an interrupt on the Time Slot A sample. A 0 enables the interrupt.
	[4:0]	0x1F	R/W	Reserved	
0x02	[15:3]	0x0000	R/W	Reserved	
	2	0x0	R/W	INT_ENA	INT enable. 0: disable the INT pin. The INT pin floats regardless of interrupt status. The status register (Address 0x00) remains active. 1: enable the INT pin.
	1	0x0	R/W	INT_DRV	INT drive. 0: the INT pin is always driven. 1: the INT pin is driven when the interrupt is asserted. Otherwise, it is left floating and requires a pull-up or pull-down resistor, depending on polarity (operates as open-drain). Use this setting if multiple devices need to share the INT pin.
	0	0x0	R/W	INT_POL	INT polarity. 0: the INT pin is active high. 1: the INT pin is active low.
0x06	[15:14]	0x0	R/W	Reserved	
	[13:8]	0x00	R/W	FIFO_THRESH	FIFO length threshold. An interrupt is generated when the number of data words in the FIFO exceeds the value in FIFO_THRESH. The interrupt pin automatically deasserts when the number of data words available in the FIFO no longer exceeds the value in FIFO_THRESH.
	[7:0]	0x00	R/W	Reserved	
0x08	[15:0]	0x0416	R	DEV_ID	Device ID.
0x0A	[15:12]	0x0	R	Reserved	
	[11:0]	0x000	R	CLK_RATIO	When the CLK32M_CAL_EN bit (Register 0x50, Bit 5) is set, the device calculates the number of 32 MHz clock cycles in two cycles of the 32 kHz clock. The result, nominally 2000 (0x07D0), is stored in the CLK_RATIO bits.
0x10	[15:2]	0x000	R/W	Reserved	
	[1:0]	0x0	R/W	Mode	Determines the operating mode of the ADPD144RI. 0x0: standby. 0x1: program. 0x2: sample.
0x11	[15:14]	0x1	R/W	Reserved	
	13	0x0	R/W	RDOUT_MODE	Readback data mode for extended data registers. 0x0: block sum of N samples. 0x1: block average of N samples.
	12	0x1	R/W	FIFO_OVRN_PREVENT	0x0: wrap around FIFO, overwriting old data with new. 0x1: new data if FIFO is not full (recommended setting).
	[11:9]	0x0	R/W	Reserved	

Address	Data Bit	Default	Access	Name	Description
	[8:6]	0x0	R/W	SLOTB_FIFO_MODE	Time Slot B FIFO data format. 0: no data to FIFO. 1: 16-bit sum of all 4 channels. 2: 32-bit sum of all 4 channels. 4: 4 channels of 16-bit sample data. 6: 4 channels of 32-bit extended sample. Others: reserved. The selected Time Slot B data is saved in the FIFO. Available only if Time Slot A has the same averaging factor, N_{SAMPLE} (Register 0x15, Bits[10:8] = Bits[6:4]), or if Time Slot A is not saving data to the FIFO (Register 0x11, Bits[4:2] = 0).
	5	0x0	R/W	SLOTB_EN	Time Slot B enable. 1: enables Time Slot B.
	[4:2]	0x0	R/W	SLOTA_FIFO_MODE	Time Slot A FIFO data format. 0: no data to FIFO. 1: 16-bit sum of all 4 channels. 2: 32-bit sum of all 4 channels. 4: 4 channels of 16-bit sample data. 6: 4 channels of 32-bit extended sample. Others: reserved.
	1	0x0	R/W	Reserved	Write 0x0.
	0	0x0	R/W	SLOTA_EN	Time Slot A enable. 1: enables Time Slot A.
0x38	15	0x0	R/W	Reserved	
	14	0x0	R/W	EXT_SYNC_ENA	Write 0x1 when EXT_SYNC_SEL (Register 0x4F, Bit 2) is set to 1. Otherwise, write 0x0.
	[13:0]	0x0	R/W	Reserved	
0x4B	[15:8]	0x26	R/W	Reserved	
	7	0x0	R/W	CLK32K_EN	Sample clock power-up. Enables the data sample clock. 0x0: clock disabled. 0x1: normal operation.
	6	0x0	R/W	Reserved	
	[5:0]	0x12	R/W	CLK32K_ADJUST	Data sampling (32 kHz) clock frequency adjust. This register calibrates the sample frequency of the device to achieve high precision on the data rate as defined in Register 0x12. Adjusts the sample master 32 kHz clock by 0.6 kHz per LSB. For a 100 Hz sample rate as defined in Register 0x12, 1 LSB of Register 0x4B, Bits[5:0], is 1.9 Hz. Note that a larger value produces a lower frequency. See the Clocks and Timing Calibration section for more information regarding clock adjustment. 00 0000: maximum frequency. 10 0010: typical center frequency. 11 1111: minimum frequency.
0x4D	[15:8]	0x42	R/W	Reserved	
	[7:0]	0x5E	R/W	CLK32M_ADJUST	Internal timing (32 MHz) clock frequency adjust. This register calibrates the internal clock of the device to achieve precisely timed LED pulses. Adjusts the 32 MHz clock by 109 kHz per LSB. See the Clocks and Timing Calibration section for more information on clock adjustment. 0000 0000: minimum frequency. 0101 1110: default frequency. 1111 1111: maximum frequency.
0x4E	[15:0]	0x0060	R/W	ADC_TIMING	Write 0x0040.

Address	Data Bit	Default	Access	Name	Description
0x4F	[15:3]	0x0412	R/W	Reserved	Write 0x0412.
	2	0x0	R/W	EXT_SYNC_SEL	Sample sync select. 0: use the internal 32 kHz clock with FSAMPLE to select sample timings. 1: use the INT pin to trigger the sample cycle.
	1	0x0	R/W	INT_IE	INT pin input enable.
	0	0x0	R/W	Reserved	Write 0x0.
0x50	[15:6]	0x000	R/W	Reserved	
	5	0x0	R/W	CLK32M_CAL_EN	As part of the 32 MHz clock calibration routine, write 1 to begin the clock ratio calculation. Read the result of this calculation from the CLK_RATIO bits in Register 0x0A. Reset this bit to 0 prior to reinitiating the calculation.
	[4:0]	0x0	R/W	Reserved	

ADC REGISTERS

Table 18. ADC Registers

Address	Data Bits	Default	Access	Name	Description
0x12	[15:0]	0x0028	R/W	FSAMPLE	Sampling frequency: f_{SAMPLE} = 32 kHz/(Register 0x12, Bits[15:0] × 4). For example, 100 Hz = 0x0050, 200 Hz = 0x0028.
0x15	[15:11]	0x0	R/W	Reserved	
	[10:8]	0x6	R/W	SLOTB_NUM_AVG	Sample sum/average for Time Slot B. Specifies the averaging factor, N_B, which is the number of consecutive samples that is summed and averaged after the ADC. Register 0x70 to Register 0x7F hold the data sum. Register 0x64 to Register 0x6B and the data buffer in Register 0x60 hold the data average, which can increase SNR without clipping, in 16-bit registers. The data rate is decimated by the value of the SLOTB_NUMB_AVG bits. 0: 1. 1: 2. 2: 4. 3: 8. 4: 16. 5: 32. 6: 64. 7: 128.
	7	0x0	R/W	Reserved	
	[6:4]	0x0	R/W	SLOTA_NUM_AVG	Sample sum/average for Time Slot A. N_A: same as Bits[10:8] but for Time Slot A. See description in Register 0x15, Bits[10:8].
	[3:0]	0x0	R/W	Reserved	
0x18	[15:0]	0x2000	R/W	SLOTA_CH1_OFFSET	Time Slot A Channel 1 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x19	[15:0]	0x2000	R/W	SLOTA_CH2_OFFSET	Time Slot A Channel 2 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1A	[15:0]	0x2000	R/W	SLOTA_CH3_OFFSET	Time Slot A Channel 3 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1B	[15:0]	0x2000	R/W	SLOTA_CH4_OFFSET	Time Slot A Channel 4 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1E	[15:0]	0x2000	R/W	SLOTB_CH1_OFFSET	Time Slot B Channel 1 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x1F	[15:0]	0x2000	R/W	SLOTB_CH2_OFFSET	Time Slot B Channel 2 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x20	[15:0]	0x2000	R/W	SLOTB_CH3_OFFSET	Time Slot B Channel 3 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.
0x21	[15:0]	0x2000	R/W	SLOTB_CH4_OFFSET	Time Slot B Channel 4 ADC offset. The value to subtract from the raw ADC value. A value of 0x2000 is typical.

DATA REGISTERS

Table 19. Data Registers

Address	Data Bits	Access	Name	Description
0x5F	[15:3]	R/W	Reserved	
	2	R/W	SLOTB_DATA_HOLD	Setting this bit prevents an update of the data registers corresponding to Time Slot B. Set this bit to ensure that unread data registers are not updated, guaranteeing a contiguous set of data from all four photodiode channels.
	1	R/W	SLOTA_DATA_HOLD	Setting this bit prevents an update of the data registers corresponding to Time Slot A. Set this bit to ensure that unread data registers are not updated, guaranteeing a contiguous set of data from all four photodiode channels.
	0	R/W	FIFO_ACCESS_ENA	Set to 1 twice to enable FIFO access. It is necessary to write 1 to the FIFO_ACCESS_ENA bit in two consecutive write operations to read data from the FIFO. For power savings, reset to 0 when FIFO access is complete. This bit also turns on the 32 MHz clock so that calibration can occur.
0x60	[15:0]	R	FIFO_DATA	Next available word in FIFO. Prior to reading this register, set the FIFO_ACCESS_ENA bit (Register 0x5F, Bit 0) twice. Reset this bit to 0 when the FIFO access sequence is complete.
0x64	[15:0]	R	SLOTA_PD1_16BIT	16-bit value of Photodiode 1 in Time Slot A.
0x65	[15:0]	R	SLOTA_PD2_16BIT	16-bit value of Photodiode 2 in Time Slot A.
0x66	[15:0]	R	SLOTA_PD3_16BIT	16-bit value of Photodiode 3 in Time Slot A.
0x67	[15:0]	R	SLOTA_PD4_16BIT	16-bit value of Photodiode 4 in Time Slot A.
0x68	[15:0]	R	SLOTB_PD1_16BIT	16-bit value of Photodiode 1 in Time Slot B.
0x69	[15:0]	R	SLOTB_PD2_16BIT	16-bit value of Photodiode 2 in Time Slot B.
0x6A	[15:0]	R	SLOTB_PD3_16BIT	16-bit value of Photodiode 3 in Time Slot B.
0x6B	[15:0]	R	SLOTB_PD4_16BIT	16-bit value of Photodiode 4 in Time Slot B.
0x70	[15:0]	R	SLOTA_PD1_LOW	Low data-word for Photodiode 1 in Time Slot A.
0x71	[15:0]	R	SLOTA_PD2_LOW	Low data-word for Photodiode 2 in Time Slot A.
0x72	[15:0]	R	SLOTA_PD3_LOW	Low data-word for Photodiode 3 in Time Slot A.
0x73	[15:0]	R	SLOTA_PD4_LOW	Low data-word for Photodiode 4 in Time Slot A.
0x74	[15:0]	R	SLOTA_PD1_HIGH	High data-word for Photodiode 1 in Time Slot A.
0x75	[15:0]	R	SLOTA_PD2_HIGH	High data-word for Photodiode 2 in Time Slot A.
0x76	[15:0]	R	SLOTA_PD3_HIGH	High data-word for Photodiode 3 in Time Slot A.
0x77	[15:0]	R	SLOTA_PD4_HIGH	High data-word for Photodiode 4 in Time Slot A.
0x78	[15:0]	R	SLOTB_PD1_LOW	Low data-word for Photodiode 1 in Time Slot B.
0x79	[15:0]	R	SLOTB_PD2_LOW	Low data-word for Photodiode 2 in Time Slot B.
0x7A	[15:0]	R	SLOTB_PD3_LOW	Low data-word for Photodiode 3 in Time Slot B.
0x7B	[15:0]	R	SLOTB_PD4_LOW	Low data-word for Photodiode 4 in Time Slot B.
0x7C	[15:0]	R	SLOTB_PD1_HIGH	High data-word for Photodiode 1 in Time Slot B.
0x7D	[15:0]	R	SLOTB_PD2_HIGH	High data-word for Photodiode 2 in Time Slot B.
0x7E	[15:0]	R	SLOTB_PD3_HIGH	High data-word for Photodiode 3 in Time Slot B.
0x7F	[15:0]	R	SLOTB_PD4_HIGH	High data-word for Photodiode 4 in Time Slot B.

OUTLINE DIMENSIONS

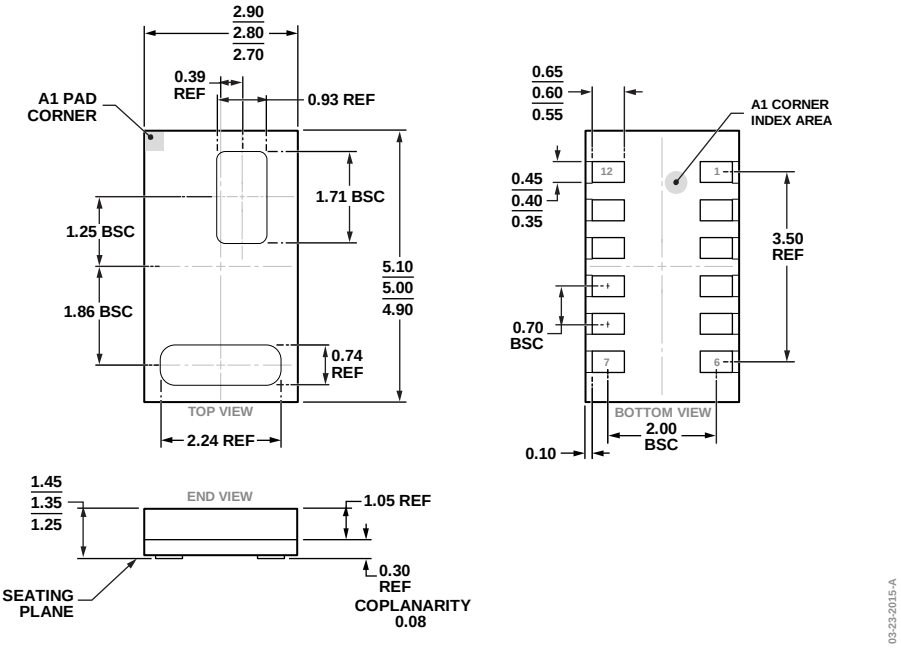

Figure 24. 12-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
2.8 mm × 5.0 mm Body
(CE-12-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
ADPD144RI-ACEZ-RL	−40°C to +85°C	12-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV], 13″Tape and Reel	CE-12-2
ADPD144RI-ACEZ-RL7	−40°C to +85°C	12-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV], 7″Tape and Reel	CE-12-2
EVAL-ADPD144RIZ-SF		Small Form Factor Evaluation Board, Suitable for Earbud and Patch Applications	

[1] Z = RoHS Compliant Part.
[2] To use the EVAL-ADPD144RIZ-SF, the EVAL-ADPDUCZ microcontroller board must also be used.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).