

## Oven-Controlled, Buried Zener, Precision Voltage Reference

### FEATURES

- ▶ LTZ1000-class, ultrastable, 6.6 V, buried Zener reference
- ▶ On-chip, thermally regulated, matched resistor-dividers
- ▶ Precision 5 V output  $\pm 0.25\%$  ( $R_{ISET} = 102 \Omega$ ,  $T_J = 70^\circ\text{C}$ )
- ▶ 5 V output noise (0.1 Hz to 10 Hz): 0.13 ppm p-p
- ▶ Zener, thermal loop op amps, and buffer provided on chip
- ▶ Input voltage range: 9 V to 36 V
- ▶ Hermetic, surface-mount package, [20-terminal LCC](#)
- ▶ Ovenization ensures ultra-low temperature drift

### APPLICATIONS

- ▶ Calibration equipment
- ▶ Benchtop digital multimeters
- ▶ Automated test equipment (ATE)
- ▶ Precision data acquisition systems (DAS)
- ▶ Stationary high-precision measurement devices

### GENERAL DESCRIPTION

The ADR1001 is a fully integrated, ultra-low drift, buried Zener precision voltage reference solution in a single chip. By integrating the entire signal conditioning circuitry required by the LTZ1000 into a single chip, the ADR1001 provides a significant reduction in overall solution area, while simplifying the design process by eliminating the many challenges of building a discrete circuit solution.

### FUNCTIONAL BLOCK DIAGRAM

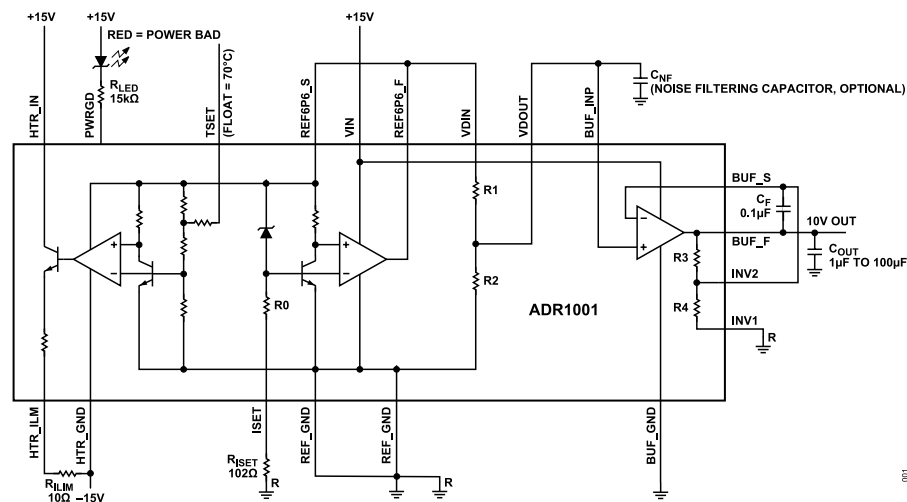


Figure 1. Functional Block Diagram, Including Surrounding Schematic, Showing Split Supply Heater Operation and 10 V Reference Output

The on-chip heater, combined with Analog Devices buried Zener technology, allows the ADR1001 to achieve sub-ppm temperature coefficient performance and single-digit ppm long-term drift performance. Besides providing best-in-class precision in all vectors, the ADR1001 incorporates ease-of-use features to reduce cost and design-in effort. These features include a pin-programmable internal thermostat, resistor-programmable heater current limit, open-collector power-good flag pin, hermetic surface-mount package, and an extra matched resistor pair. By default, the temperature setpoint is  $70^\circ\text{C}$  when no external resistor is connected to the TSET pin, and the internal heater current limit is 100 mA with HTR\_ILIM shorted to HTR\_GND.

The integrated thin-film resistors and on-chip buffer can be used to provide standard output voltage reference values that are compatible with modern precision converters. The ADR1001 divider network and output buffer combination is trimmed to within  $\pm 0.25\%$  initial accuracy. In addition, a pair of matched resistors is also included on-chip, allowing customers to easily generate a negative voltage reference or a gain of 2 with minimal impact to the output accuracy or drift.

The ADR1001 is packaged in a hermetic, ceramic, [20-terminal leadless chip carrier \(LCC\)](#). The surface-mount ceramic package allows customers to eliminate the through-hole component soldering step while still retaining the hermetic seal of a classic through-hole metal can package.

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**REVISION HISTORY****1/2024—Revision 0: Initial Version**

## SPECIFICATIONS

## 6.6 V REFERENCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $T_{\text{SET}} = 70^\circ\text{C}$ ,  $R_{\text{ISET}} = 102\ \Omega$ , unless otherwise noted. All parametrics are extracted within 15 seconds of power-up.

Table 1. 6.6 V Reference Characteristics

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
6.6 V OUTPUT VOLTAGE <sup>1</sup>						
$T_{\text{SET}} = 70^\circ\text{C}$	$V_{6P6\_70C\_R\text{ISET}=102}$	$R_{\text{ISET}} = 102\ \Omega$ ; TSET floating	6.491	6.626	6.702	V
	$V_{6P6\_70C\_R\text{ISET}=470}$	$R_{\text{ISET}} = 470\ \Omega$ ; TSET floating	6.467	6.603	6.679	V
$T_{\text{SET}} = 40^\circ\text{C}$	$V_{6P6\_40C\_R\text{ISET}=102}$	$R_{\text{ISET}} = 102\ \Omega$ ; TSET tied to REF6P6S	6.501	6.631	6.704	V
	$V_{6P6\_40C\_R\text{ISET}=470}$	$R_{\text{ISET}} = 470\ \Omega$ ; TSET tied to REF6P6S	6.478	6.580	6.681	V
$T_{\text{SET}} = 125^\circ\text{C}$	$V_{6P6\_125C\_R\text{ISET}=102}$	$R_{\text{ISET}} = 102\ \Omega$ ; TSET tied to REF_GND	6.467	6.611	6.692	V
	$V_{6P6\_125C\_R\text{ISET}=470}$	$R_{\text{ISET}} = 470\ \Omega$ ; TSET tied to REF_GND	6.439	6.555	6.672	V
$V_{\text{ISET}}$						
$T_{\text{SET}} = 70^\circ\text{C}$	$V_{\text{ISET\_70C\_R\text{ISET}=102}$	Voltage at ISET pin; $R_{\text{ISET}} = 102\ \Omega$ ; TSET floating	434	444	454	mV
	$V_{\text{ISET\_70C\_R\text{ISET}=470}$	Voltage at ISET pin; $R_{\text{ISET}} = 470\ \Omega$ ; TSET floating	462	472	482	mV
$T_{\text{SET}} = 40^\circ\text{C}$	$V_{\text{ISET\_40C\_R\text{ISET}=102}$	Voltage at ISET pin; $R_{\text{ISET}} = 102\ \Omega$ ; TSET tied to REF6P6_S	504	514	526	mV
	$V_{\text{ISET\_40C\_R\text{ISET}=470}$	Voltage at ISET pin; $R_{\text{ISET}} = 470\ \Omega$ ; TSET tied to REF6P6_S	532	542	552	mV
$T_{\text{SET}} = 125^\circ\text{C}$	$V_{\text{ISET\_125C\_R\text{ISET}=102}$	Voltage at ISET pin; $R_{\text{ISET}} = 102\ \Omega$ ; TSET tied to REF_GND	311	321	331	mV
	$V_{\text{ISET\_125C\_R\text{ISET}=470}$	Voltage at ISET pin; $R_{\text{ISET}} = 470\ \Omega$ ; TSET tied to REF_GND	332	342	352	mV
TEMPERATURE COEFFICIENT	$\text{TCV}_{6P6}$	See the <a href="#">Typical Performance Characteristics</a> section				
Unheated TC		Heater off		36		ppm/ $^\circ\text{C}$
Heated TC		$T_{\text{SET}} = 70^\circ\text{C}$		0.2		ppm/ $^\circ\text{C}$
LINE REJECTION	$\Delta V_{6P6}/\Delta V_{\text{IN}}$	$9\ \text{V} < V_{\text{IN}} < 30\ \text{V}$		0.5	2	ppm/V
HEATER LINE REJECTION						
Positive Heater Line Rejection	$\Delta V_{6P6}/\Delta V_{\text{HTR\_IN}}$	$8\ \text{V} < V_{\text{HTR\_IN}} < 30\ \text{V}$	-2	-0.4	+2	ppm/V
Negative Heater Line Rejection	$\Delta V_{6P6}/\Delta V_{\text{HTR\_GND}}$	$-22\ \text{V} < V_{\text{HTR\_GND}} < 0\ \text{V}$	-2	-0.7	+2	ppm/V
LOAD REJECTION (SOURCING ONLY)	$\Delta V_{6P6}/\Delta I_{L\_6P6}$	$\Delta I_{L\_6P6} = 5.65\ \text{mA}$ (in addition to 4.35 mA Zener current to 10 mA total current)		1.8	7	ppm/mA
OUTPUT CURRENT CAPACITY (SOURCING ONLY)	$I_{L\_6P6}$	Includes Zener bias current; guaranteed by load rejection	10			mA
QUIESCENT CURRENT	$I_{\text{Q}}$	Current at $V_{\text{IN}}$ , excluding Zener and heater loads	2.27	2.4	2.5	mA
6.6 V OUTPUT SHORT-CIRCUIT CURRENT LIMIT	$I_{\text{SC\_6P6}}$	Amount of current available to source before PWRGD pulls low; includes Zener bias current	13	14.4	16	mA
OUTPUT-VOLTAGE NOISE						
Low-Frequency Noise	$e_{\text{Np-p\_6P6}}$	0.1 Hz to 10.0 Hz		0.6		$\mu\text{V p-p}$
Spot Noise Density	$e_{\text{N\_6P6}}$	$f = 100\ \text{Hz}$		25		$\text{nV}/\sqrt{\text{Hz}}$
PWRGD OUTPUT LOW VOLTAGE	PWRGD $V_{\text{OL}}$	PWRGD pulled up externally with 10 k $\Omega$ to 5 V	150	200	210	mV
LONG-TERM DRIFT	$\Delta V_{6P6\_LTD}$	See <a href="#">Figure 13</a> and <a href="#">Figure 14</a>				
		200 hours		-3		ppm
		1000 hours		-5		ppm
		2000 hours		-5		ppm

<sup>1</sup> Does not include solder shift.

## SPECIFICATIONS

## HEATER AMPLIFIER ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. All parametrics are extracted within 15 seconds of power-up.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
HEATER SET TEMPERATURE	$T_{J_{TSET\_70C}}$	TSET floating <sup>1</sup>	67	70	73	$^\circ\text{C}$
HEATER SET TEMPERATURE LOW	$T_{J_{TSET\_40C}}$	TSET tied to REF6P6_F <sup>1</sup>		40		$^\circ\text{C}$
HEATER SET TEMPERATURE HIGH	$T_{J_{TSET\_125C}}$	TSET tied to REF_GND <sup>1</sup>		128		$^\circ\text{C}$
HEATER CURRENT LIMIT	$I_{H_{LIM}}$	No external limiter	99	104	110	mA
	$I_{H_{LIM\_10\Omega}}$	10 $\Omega$ external R between HTR_ILIM and HTR_GND, $R_{ISET} = 470 \Omega$	56	58	60	mA
THERMAL RESISTANCE	$\theta_{JA}$	See the <a href="#">Thermal Resistance</a> section		130		$^\circ\text{C/W}$

<sup>1</sup> Refer to the [Setting the ADR1001 Operating Temperature](#) section and [Table 10](#) for more information.

## 5 V OUTPUT AND BUFFER ELECTRICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $T_{SET} = 70^\circ\text{C}$ ; BUF\_INP connected to VDOUT; VDIN connected to REF6P6\_F, REF6P6\_S. All parametrics are extracted within 15 seconds of power-up.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
5 V OUTPUT VOLTAGE <sup>1</sup>		Noninverting input connected to VDOUT				
$T_{SET} = 70^\circ\text{C}$	$V_{5\_70C\_RISET=102\Omega}$	$R_{ISET} = 102 \Omega$ ; TSET floating	4.9875	5.0	5.0125	V
	$V_{5\_70C\_RISET=470\Omega}$	$R_{ISET} = 470 \Omega$ ; TSET floating	4.970	4.986	4.996	V
$T_{SET} = 40^\circ\text{C}$	$V_{5\_40C\_RISET=102\Omega}$	$R_{ISET} = 102 \Omega$ ; TSET tied to REF6P6_S	4.995	5.005	5.017	V
	$V_{5\_40C\_RISET=470\Omega}$	$R_{ISET} = 470 \Omega$ ; TSET tied to REF6P6_S	4.977	4.987	4.999	V
$T_{SET} = 125^\circ\text{C}$	$V_{5\_125C\_RISET=102\Omega}$	$R_{ISET} = 102 \Omega$ ; TSET tied to REF_GND	4.970	4.988	5.006	V
	$V_{5\_125C\_RISET=470\Omega}$	$R_{ISET} = 470 \Omega$ ; TSET tied to REF_GND	4.949	4.970	4.990	V
5 V OUTPUT-VOLTAGE ERROR	$V_{5\_ERR}$	$R_{ISET} = 102 \Omega$ ; TSET floating			$\pm 0.25$	%
SOLDER HEAT RESISTANCE SHIFT	SHR			80		ppm
OUTPUT-VOLTAGE TEMPERATURE COEFFICIENT	$TCV_{OUT}$	Includes heated tempco of 6.6 V reference, voltage divider, and output buffer		0.2		ppm/ $^\circ\text{C}$
LINE REJECTION	$\Delta V_5/\Delta V_{IN}$	9 V < $V_{IN}$ < 30 V	-3	+0.5	+3	ppm/V
HEATER LINE REJECTION						
Positive Heater Line Rejection	$\Delta V_5/\Delta V_{HTR\_IN}$	8 V < $V_{HTR\_IN}$ < 30 V	-3	-0.4	+3	ppm/V
Negative Heater Line Rejection	$\Delta V_5/\Delta V_{HTR\_GND}$	-22 V < $V_{HTR\_GND}$ < 0 V	-2	-0.7	+2	ppm/V
LOAD REJECTION	$\Delta V_5/\Delta I_L$					
Sourcing		0 mA < $I_{OUT}$ < 8 mA	-14	+1	+19	$\mu\text{V}/\text{mA}$
Sinking		-8 mA < $I_{OUT}$ < 0 mA	-14	+4	+18	$\mu\text{V}/\text{mA}$
SHORT-CIRCUIT CURRENT LIMIT	$I_{SC\_5}$					
Sourcing to GND			13	14.7	16	mA
Sinking to $V_{IN} = 15 \text{ V}$			11	12	13	mA
OFFSET VOLTAGE	$V_{OS}$	$V_{CM} = 5 \text{ V}$	-1		+1	mV
INPUT BIAS CURRENT	$I_B$	$V_{CM} = 5 \text{ V}$		2	6	nA
OUTPUT-VOLTAGE NOISE <sup>2</sup>						
Low-Frequency Noise	$e_{Np-p\_5V}$	0.1 Hz to 10.0 Hz		0.7		$\mu\text{V p-p}$
Spot Noise Density	$e_{N\_5V}$	f = 100 Hz		25		nV/ $\sqrt{\text{Hz}}$

## SPECIFICATIONS

Table 3. (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
LONG-TERM DRIFT	$\Delta V_{5\_LTD}$	Includes LTD of 6.6 V reference, voltage divider, and output buffer; see <a href="#">Figure 11</a> and <a href="#">Figure 12</a> 200 hours (early life drift) 1000 hours 2000 hours				
				-2		ppm
				-4		ppm
				-5		ppm
5 V OUTPUT STARTUP STABILIZATION TIME						
±0.25%				0.2		sec
±3 ppm				45		sec

<sup>1</sup> Does not include solder shift.

<sup>2</sup> Dominated by Zener noise.

## SPECIFICATIONS

## VOLTAGE DIVIDER CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise noted;  $T_{\text{SET}} = 70^\circ\text{C}$ , unless otherwise noted. All parametrics are extracted within 15 seconds of power-up.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
V <sub>DOUT</sub> VOLTAGE	V <sub>DOUT</sub>	VDIN connected to REF6P6_F, REF6P6_S, V <sub>DOUT</sub> floating				
$T_{\text{SET}} = 70^\circ\text{C}$	V <sub>DOUT_70C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET floating	4.9875	5.0005	5.0125	V
	V <sub>DOUT_70C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET floating	4.970	4.984	4.996	V
$T_{\text{SET}} = 40^\circ\text{C}$	V <sub>DOUT_40C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET tied to REF6P6_S	4.995	5.005	5.016	V
	V <sub>DOUT_40C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET tied to REF6P6_S	4.977	4.988	4.999	V
$T_{\text{SET}} = 125^\circ\text{C}$	V <sub>DOUT_125C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET tied to REF_GND	4.970	4.988	5.005	V
	V <sub>DOUT_125C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET tied to REF_GND	4.949	4.969	4.990	V
V <sub>DOUT</sub> VOLTAGE ERROR	V <sub>DOUT_ERR</sub>	R <sub>ISET</sub> = 102 Ω; TSET floating			0.25	%
AUXILIARY VOLTAGE DIVIDER						
End-to-End Resistance	R <sub>3</sub> + R <sub>4</sub>		17.784	18.7	19.632	kΩ
Matching	$\Delta R/R$		-0.3	+0.05	+0.3	%
Matching Tempco	$(\Delta R/R)/\Delta T$			<1		ppm/°C
10 V OUTPUT VOLTAGE <sup>1</sup>	V <sub>10</sub>	See Figure 46				
$T_{\text{SET}} = 70^\circ\text{C}$	V <sub>10_70C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET floating	9.975	10.00	10.025	V
	V <sub>10_70C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET floating	9.940	9.966	9.994	V
$T_{\text{SET}} = 40^\circ\text{C}$	V <sub>10_40C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET tied to REF6P6_S	9.989	10.008	10.034	V
	V <sub>10_40C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET tied to REF6P6_S	9.954	9.973	9.998	V
$T_{\text{SET}} = 125^\circ\text{C}$	V <sub>10_125C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET tied to REF_GND	9.942	9.979	10.012	V
	V <sub>10_125C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET tied to REF_GND	9.899	9.944	9.982	V
10 V OUTPUT-VOLTAGE ERROR	V <sub>10_ERR</sub>	R <sub>ISET</sub> = 102 Ω; TSET floating			0.25	%
10 V OUTPUT LINE REJECTION	$\Delta V_{10}/\Delta V_{\text{IN}}$	12 V < V <sub>IN</sub> < 30 V	-2		+2	ppm/V
2.5 V OUTPUT VOLTAGE	V <sub>2P5</sub>	See Figure 48				
$T_{\text{SET}} = 70^\circ\text{C}$	V <sub>2P5_70C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET floating	2.49375	2.5	2.50625	V
	V <sub>2P5_70C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET floating	2.483	2.491	2.497	V
$T_{\text{SET}} = 40^\circ\text{C}$	V <sub>2P5_40C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET tied to REF6P6_S	2.496	2.502	2.508	V
	V <sub>2P5_40C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET tied to REF6P6_S	2.487	2.493	2.499	V
$T_{\text{SET}} = 125^\circ\text{C}$	V <sub>2P5_125C_102Ω</sub>	R <sub>ISET</sub> = 102 Ω; TSET tied to REF_GND	2.484	2.494	2.502	V
	V <sub>2P5_125C_470Ω</sub>	R <sub>ISET</sub> = 470 Ω; TSET tied to REF_GND	2.473	2.485	2.494	V
2.5 V OUTPUT-VOLTAGE ERROR	V <sub>2P5_ERR</sub>	R <sub>ISET</sub> = 102 Ω; TSET floating			0.25	%

<sup>1</sup> Does not include solder shift.

## ABSOLUTE MAXIMUM RATINGS

**Table 5. Absolute Maximum Ratings**

Parameter	Rating
<b>SUPPLY VOLTAGES</b>	
HTR_IN to HTR_GND (Substrate) <sup>1</sup>	8 V to 36 V
VIN to HTR_GND (Substrate) <sup>1</sup>	36 V
VIN to REF_GND	36 V
REF_GND to BUF_GND	-0.3 V to +0.3 V
<b>PRECISION RESISTOR-DIVIDERS</b>	
VDIN to REF_GND	12 V
VDOOUT to REF_GND	8 V
VDOOUT to VDIN	4 V
TSET	(REF_GND - 0.3 V) to (REF6P6_F + 0.3 V)
INV2 to INV1	-0.3 V to +8 V
<b>OUTPUT BUFFER<sup>2</sup></b>	
BUF_INP to BUF_S Maximum Differential	15 V
BUF_INP and BUF_S Maximum Input Current	5 mA
BUF_F to INV2	-0.3 V to +8 V
PWRGD to REF_GND	36 V
<b>TEMPERATURE</b>	
Storage Range	-65°C to +150°C
Operating Range	-40°C to +130°C
Junction Range	-40°C to +130°C
Lead, Soldering (10 sec)	300°C
LATCHUP	100 mA

<sup>1</sup> HTR\_GND must be the lowest potential on the chip to prevent the forward bias of the substrate junction.

<sup>2</sup> BUF\_F cannot go below REF\_GND (inverting function). If a negative reference is desired, see [Figure 47](#).

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

**Table 6. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
E-20-1			
2-Layer JEDEC Board	120	N/A	°C/W
Evaluation Board	140	N/A	°C/W

## ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

## ESD Ratings for the ADR1001

**Table 7. ADR1001, 20-Terminal LCC**

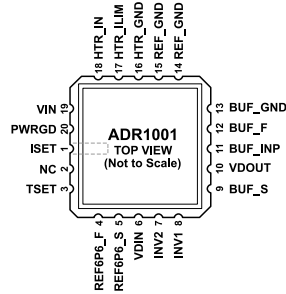
ESD Model	Withstand Threshold (V)	Class
HBM	±2000	2
FICDM	±1000	C3

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

**PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**



NOTES  
 1. NC = NO CONNECT. INTERNALLY CONNECTED. 000

**Figure 2. Pin Configuration**

**Table 8. Pin Function Descriptions**

Pin No.	Mnemonic	Description
1	ISET	Zener Bias Current Set.
2	NC	No Connect. Internally connected. NC can be shorted to REF_GND.
3	TSET	Chip Temperature Set.
4	REF6P6_F	6.6 V Force.
5	REF6P6_S	6.6 V Sense.
6	VDIN	Precision Divider Input.
7	INV2	Inverter Divider Resistor.
8	INV1	Inverter Divider Resistor.
9	BUF_S	Buffer Inverting Input.
10	VDOUT	Precision Divider 5 V Output.
11	BUF_INP	Buffer Noninverting Input.
12	BUF_F	Buffer Force.
13	BUF_GND	Buffer Ground Force.
14, 15	REF_GND	Reference Ground Sense.
16	HTR_GND	Level Shifted Heater Ground.
17	HTR_ILIM	Heater Current Limit.
18	HTR_IN	Heater Power.
19	VIN	Reference Power.
20	PWRGD	Power-Good Status Flag.



TYPICAL PERFORMANCE CHARACTERISTICS

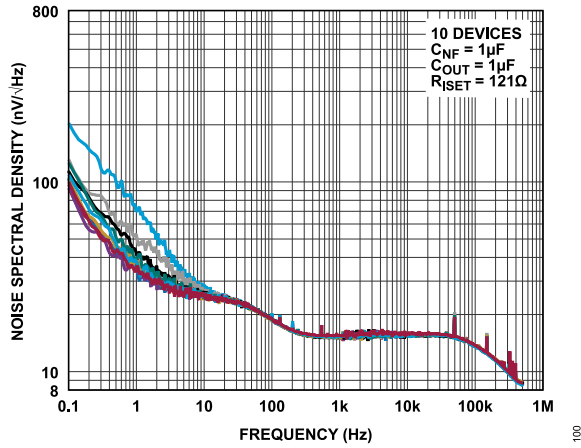


Figure 3. Noise Spectral Density vs. Frequency, 5 V Output

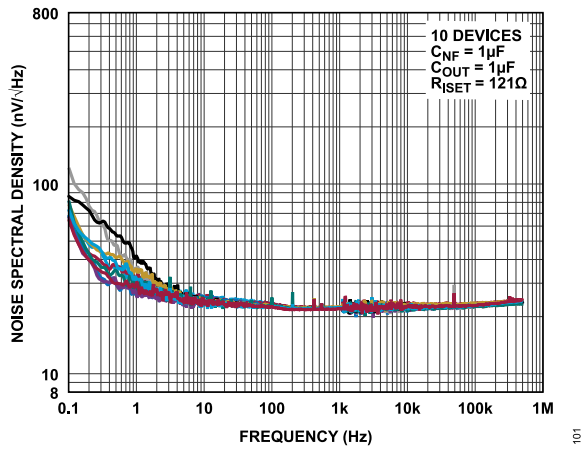


Figure 4. Noise Spectral Density vs. Frequency, 6.6 V Output

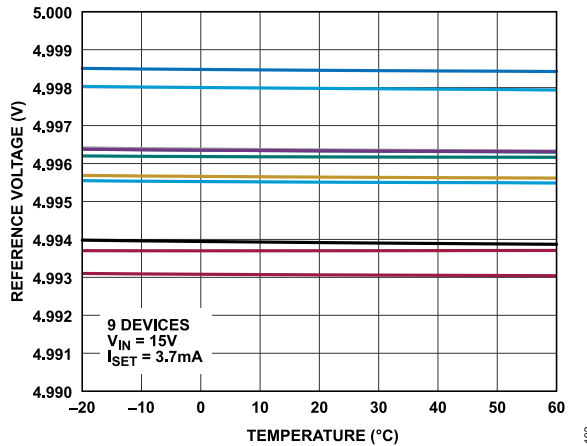


Figure 5. Reference Voltage vs. Temperature, 5 V Output

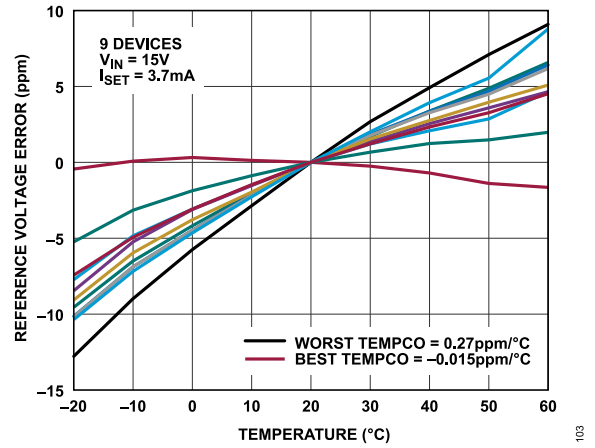


Figure 6. Reference Voltage Error vs. Temperature, 5 V Output, Referred to +20°C

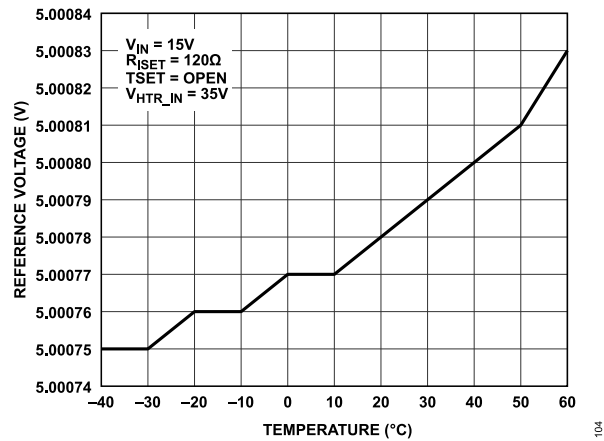


Figure 7. Reference Voltage vs. Temperature, 5 V Output

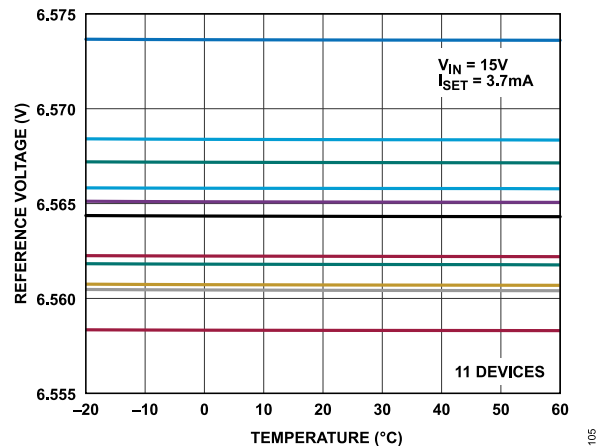


Figure 8. Reference Voltage vs. Temperature, 6.6 V Output

TYPICAL PERFORMANCE CHARACTERISTICS

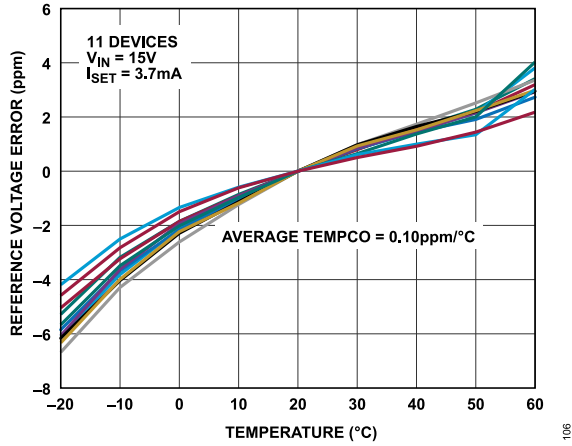


Figure 9. Reference Voltage Error vs. Temperature, 6.6 V Output, Referred to +20°C

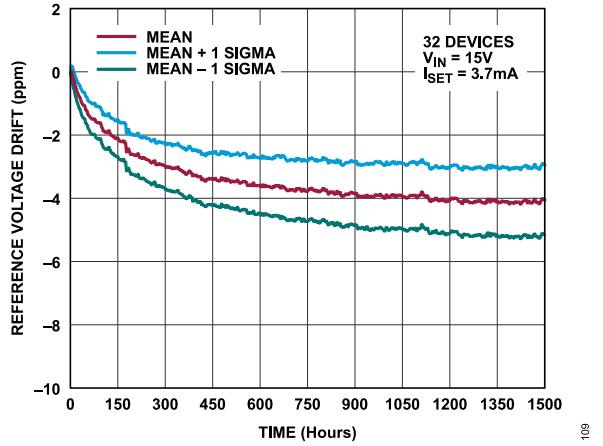


Figure 12. Long-Term Drift, 5 V Output, Mean and Sigmas

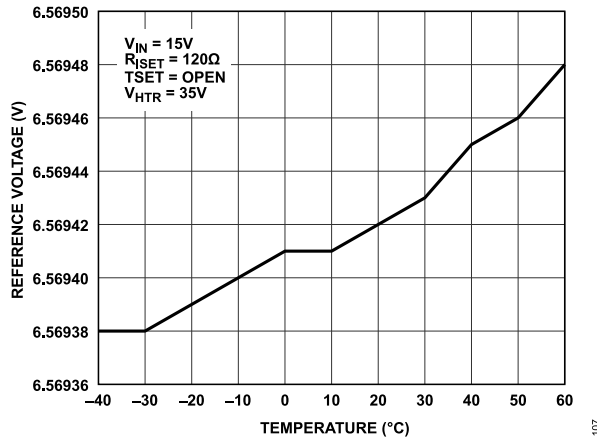


Figure 10. Reference Voltage vs. Temperature, 6.6 V Output

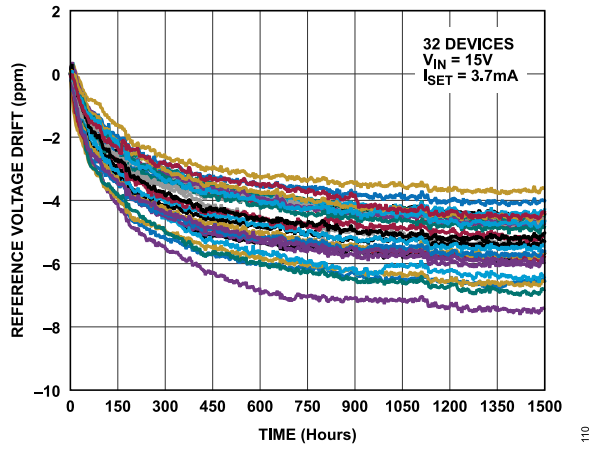


Figure 13. Long-Term Drift, 6.6 V Output

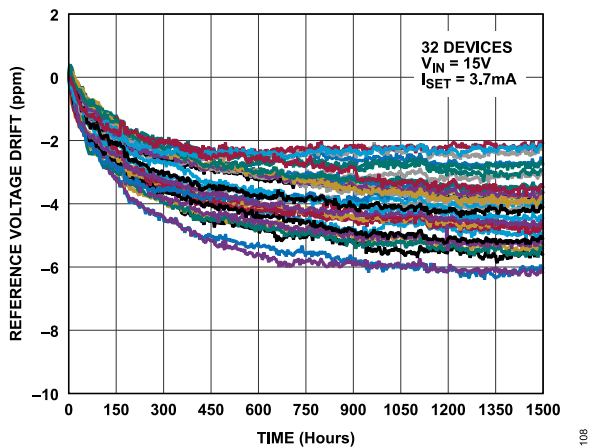


Figure 11. Long-Term Drift, 5 V Output

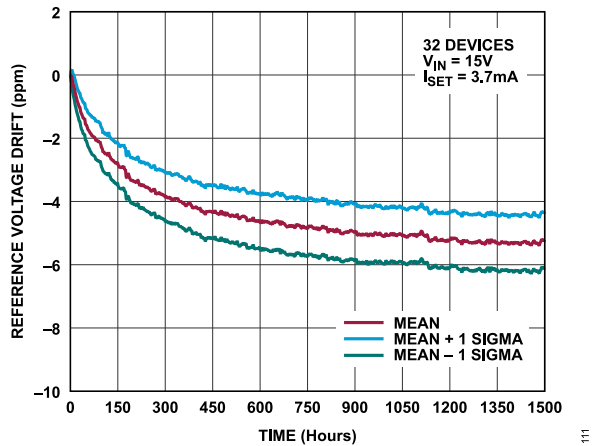


Figure 14. Long-Term Drift, 6.6 V Output, Mean and Sigmas

TYPICAL PERFORMANCE CHARACTERISTICS

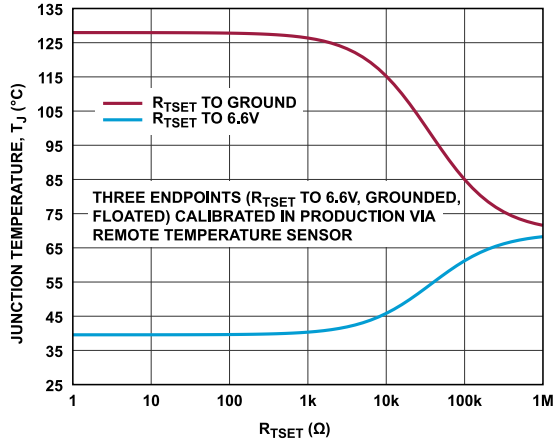


Figure 15. Junction Temperature vs.  $R_{TSET}$  to 6.6 V, Ground, and Floated

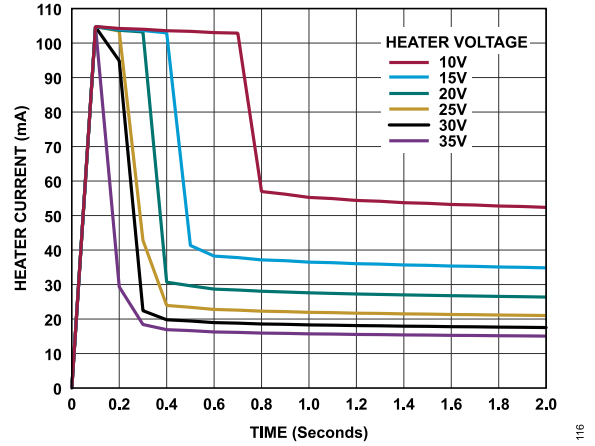


Figure 18. Heater Current vs. Time,  $R_{ILIM} = 0 \Omega$ , First 2 Seconds

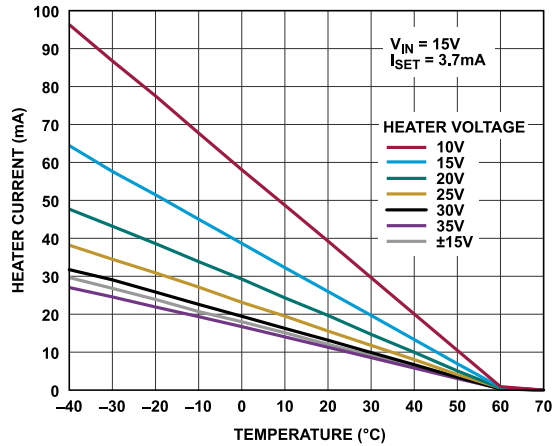


Figure 16. Final Heater Current vs. Temperature

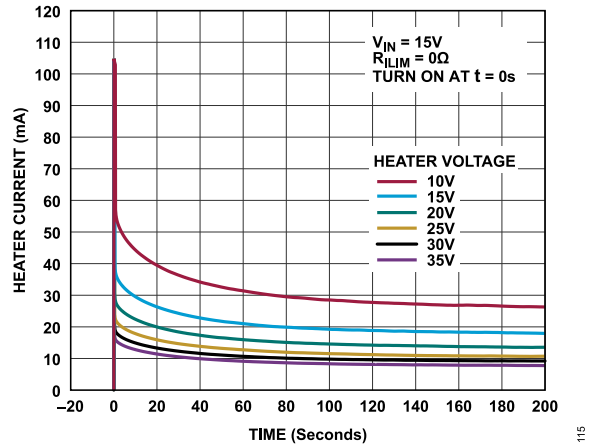


Figure 19. Heater Current vs. Time,  $R_{ILIM} = 0 \Omega$

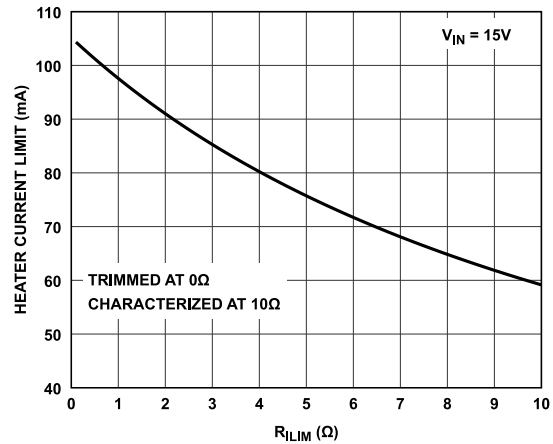


Figure 17. Heater Current Limit vs.  $R_{ILIM}$

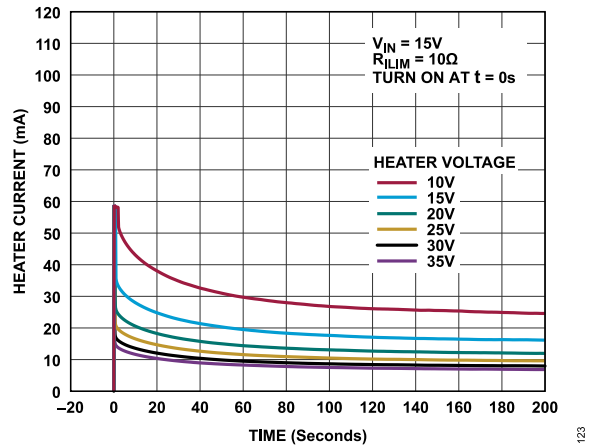


Figure 20. Heater Current vs. Time,  $R_{ILIM} = 10 \Omega$

TYPICAL PERFORMANCE CHARACTERISTICS

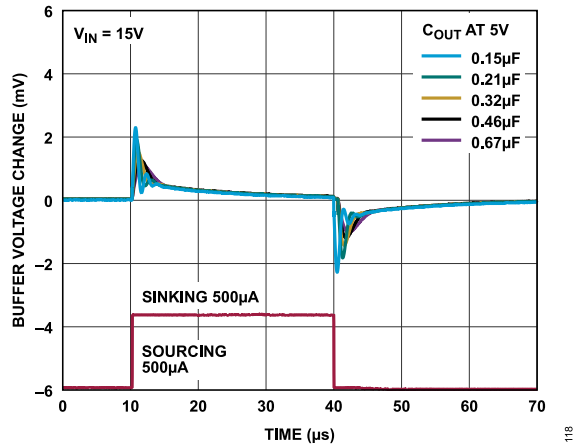


Figure 21. Buffer Output 1 mA Load Step Time Domain Response, Various Small  $C_{OUT}$

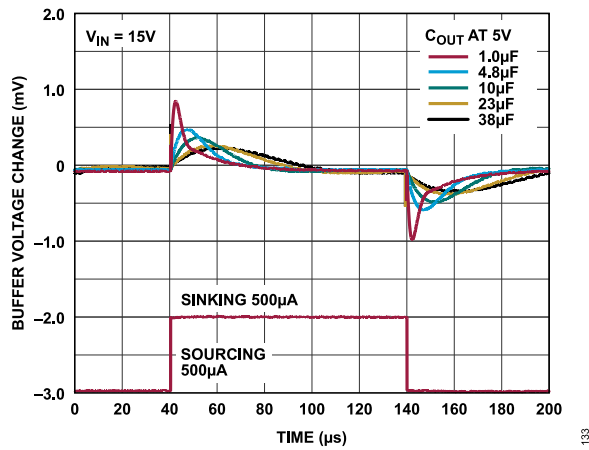


Figure 22. Buffer Output 1 mA Load Step Time Domain Response, Various Larger  $C_{OUT}$

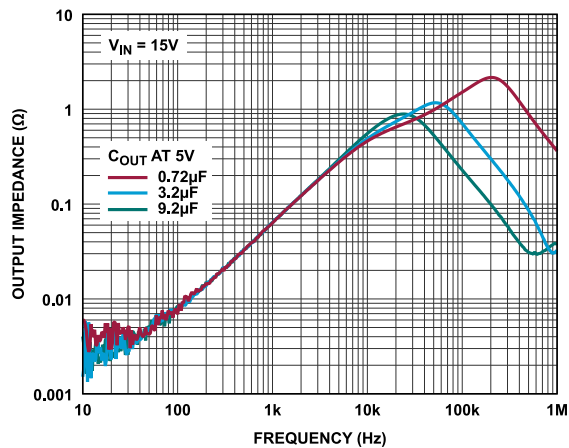


Figure 23. Output Impedance vs. Frequency, Various  $C_{OUT}$

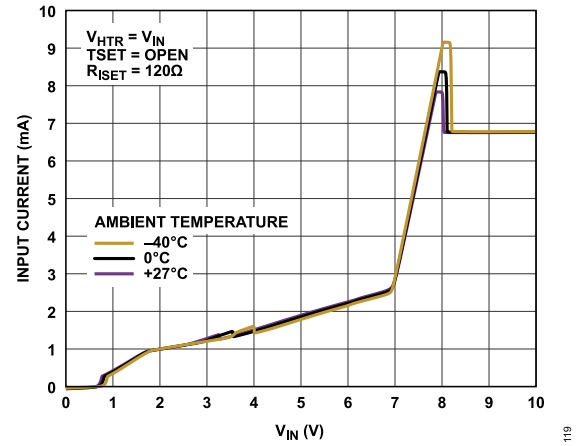


Figure 24. Power-Up Characteristic, Input Current as  $V_{IN}$  Rises

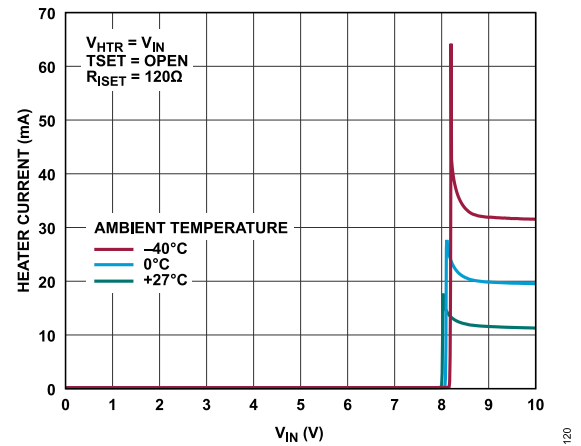


Figure 25. Power-Up Characteristic, Heater Current as  $V_{IN}$  Rises

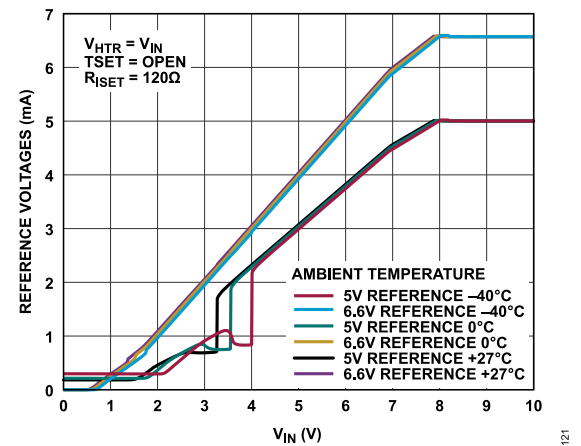


Figure 26. Power-Up Characteristic, Reference Voltages as  $V_{IN}$  Rises

TYPICAL PERFORMANCE CHARACTERISTICS

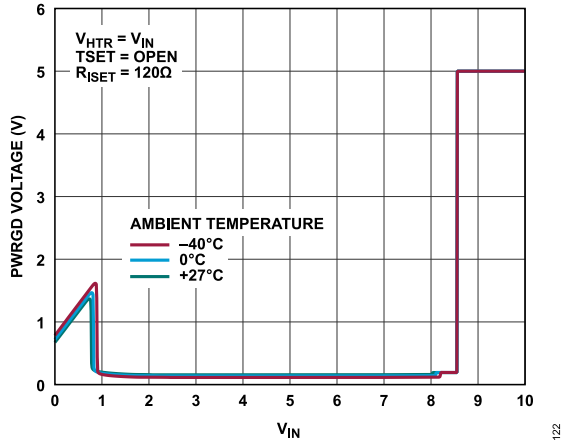


Figure 27. Power-Up Characteristic, PWRGD Pin Voltage as  $V_{IN}$  Rises

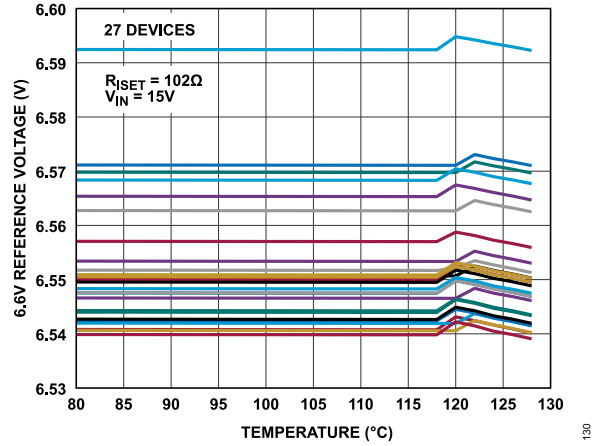


Figure 30. 6.6 V Output in Thermal Deregulation, TSET Pin Shorted to REF6P6, 27 Devices

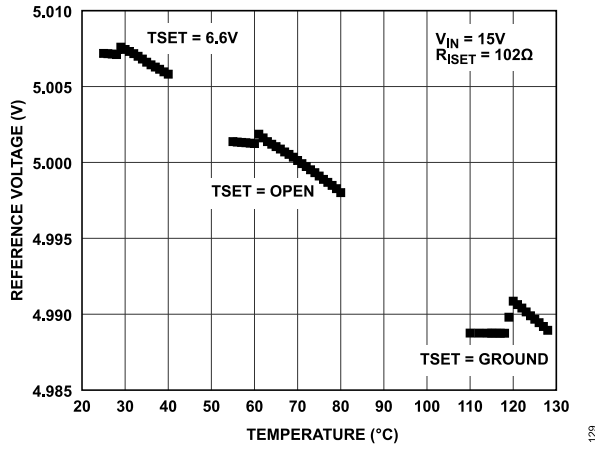


Figure 28. Thermal Deregulation at 3  $V_{TSET}$  Points, 5 V Output

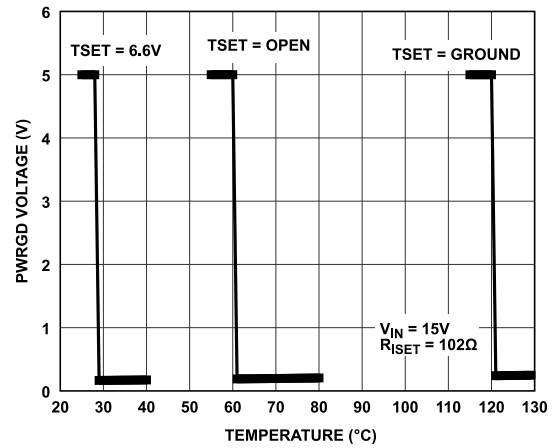


Figure 31. PWRGD Pin Voltage at Thermal Deregulation, 3 TSET Voltages

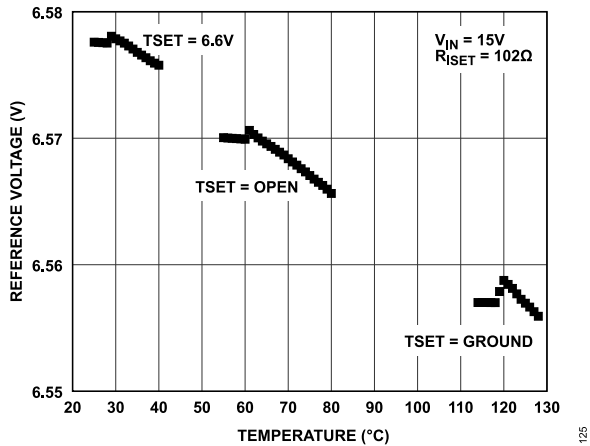


Figure 29. Thermal Deregulation at 3  $V_{TSET}$  Points, 6.6 V Output

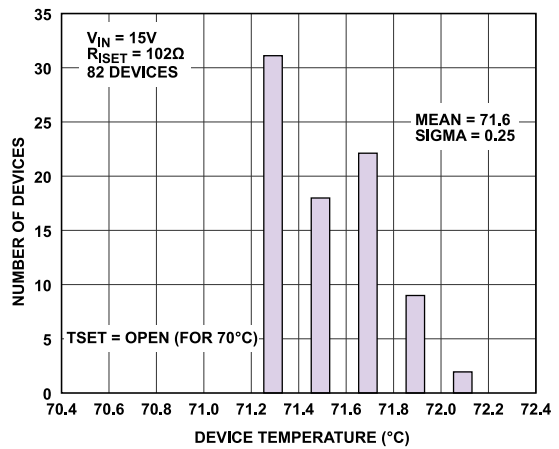


Figure 32. Temperature Set Accuracy, TSET Pin Open

TYPICAL PERFORMANCE CHARACTERISTICS

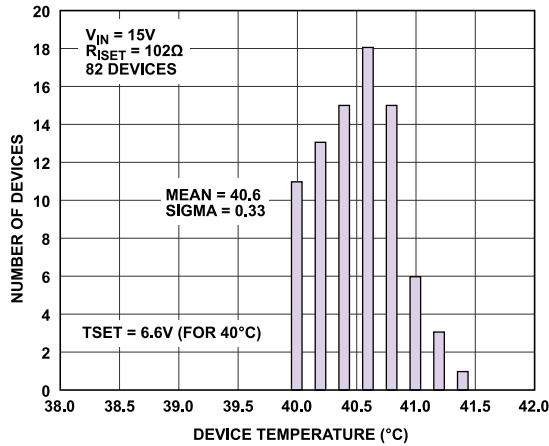


Figure 33. Temperature Set Accuracy, TSET Pin at 6.6 V

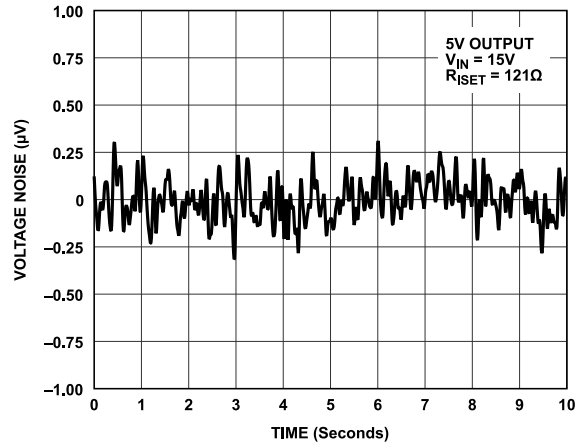


Figure 36. 5 V Output, 0.1 Hz to 10 Hz Peak-to-Peak Noise

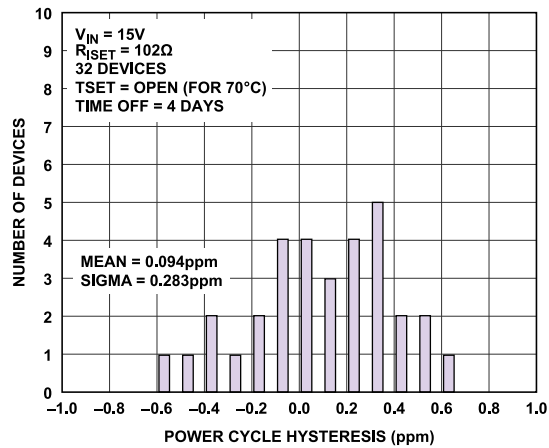


Figure 34. Power Cycle Hysteresis, 5 V Output

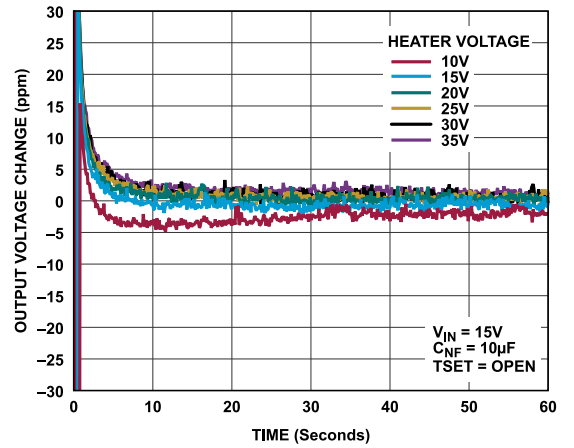


Figure 37. Stabilization Time, Various Heater Voltages, 5 V Output

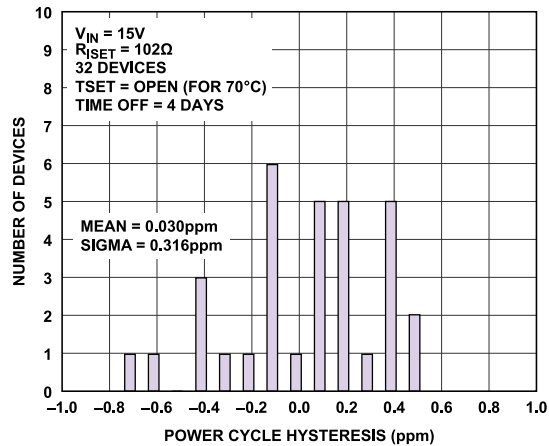


Figure 35. Power Cycle Hysteresis, 6.6 V Output

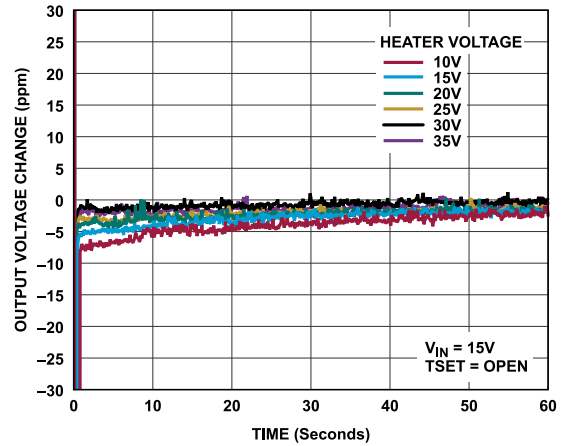


Figure 38. Stabilization Time, Various Heater Voltages, 6.6 V Output

TYPICAL PERFORMANCE CHARACTERISTICS

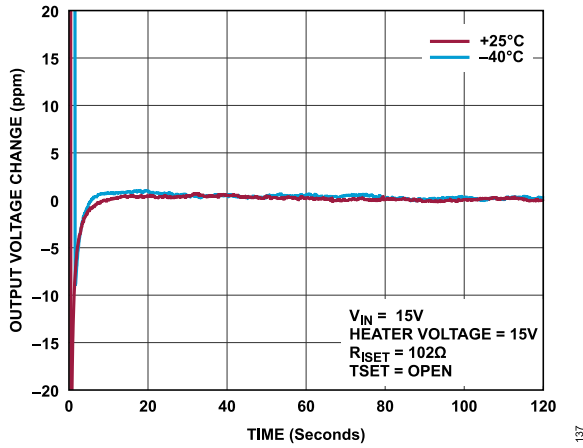


Figure 39. Stabilization Time, Room Temperature and Cold, 5 V Output

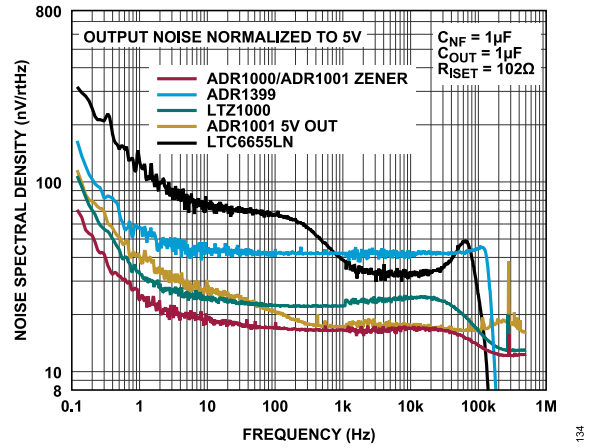


Figure 40. Noise Spectral Density vs. Frequency, Comparing Various Products, Normalized to 5 V Output

## THEORY OF OPERATION

The ADR1001 is a fully integrated, easy-to-implement version of the LTZ1000 (or ADR1000) with the addition of a precision voltage divider and output buffer. This addition allows the ADR1001 to serve a variety of functions, including signal-chain calibrator (full system reference), or standalone 20-bit DAC, or ADC voltage reference. As shown in Figure 1, the ADR1001 is divided into three functions: buried Zener reference loop, a heater with thermostatic control, and a voltage divider and precision output buffer.

### BURIED ZENER REFERENCE LOOP

A stable but inaccurate voltage reference of 6.6 V is created by summing an Analog Devices, Inc., proprietary low-noise buried Zener with a transistor base-emitter voltage ( $V_{BE}$ ) to achieve first-order temperature compensation. Since the buried Zener is the dominant noise source of the ADR1001, the ISET pin allows the user to power-scale the current in the buried Zener to trade off higher power for lower noise, with the thermal noise of the Zener scaling as the inverse square root of the Zener current ( $I_Z$ ). For example, if the spot noise density at 100 Hz is 50 nV/ $\sqrt{\text{Hz}}$  with an  $I_Z$  of 1 mA, adjusting the Zener current to 4 mA lowers the reference noise to approximately 25 nV/ $\sqrt{\text{Hz}}$ .

An internal op amp, in combination with an external resistor at ISET to GND, is used to set the Zener operating current as follows:

$$R_{ISET} = (0.605 \text{ V} - 0.0023 \text{ V/}^\circ\text{C} \times T) / I_Z - 7 \ \Omega \quad (1)$$

where:

$T$  is the heated chip temperature.

$I_Z$  is the desired Zener current.

0.605 V =  $Q1 V_{BE}$  at 0°C.

-0.0023 V/°C =  $Q1 V_{BE}$  temperature drift.

7  $\Omega$  = bulk resistance to Zener anode.

If temperature  $T = +70^\circ\text{C}$ , and  $I_Z = 4 \text{ mA}$ :

$$R_{ISET} = (0.605 \text{ V} - 0.0023 \text{ V/}^\circ\text{C} \times 70^\circ\text{C}) / 4 \text{ mA} - 7 \ \Omega = 104 \ \Omega \quad (2)$$

Note that because the 7  $\Omega$  bulk resistance (see the R0 in Figure 1) schematically appears under Q1 base, it must be included in the calculation of  $I_Z$ .

The 6.6 V reference output has a short-circuit current limit of approximately 10 mA at  $T_{SET} = 70^\circ\text{C}$ , but it should be noted that this output is only intended for Class A biasing of the buried Zener and to aid in thermostatic control (see the [Setting the ADR1001 Operating Temperature](#) section). Thus, the 6.6 V output is not designed to be loaded by a converter or any switch capacitor circuitry, because its maximum capacitive load drive capability is only 1 nF.

### THERMAL REGULATOR

Similar to the ADR1399 and LTZ1000, the ADR1001 uses an on-chip heater to maintain chip temperature fixed at 70°C, regardless of ambient temperature. Using this approach, the ADR1001 can achieve tempcos of less than 0.1 ppm/°C and linear over the thermally regulated range. Figure 41 shows a nominal plot of heater

current vs. ambient temperature. The power dissipation of the heater is proportional to the difference between chip temperature ( $T_{CHIP}$ ) and  $T_A$ .

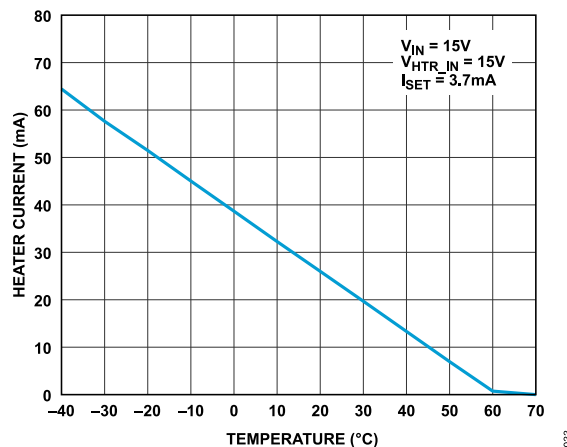


Figure 41. ADR1001 Heater Current vs. Ambient Temperature,  $HTR\_IN = 15 \text{ V}$ ;  $HTR\_GND = 0 \text{ V}$

To calculate the maximum power dissipation required for a given set temperature, use the equation as follows:

$$\text{Power (W)} = T_{RISE} / \theta_{JA} \quad (3)$$

where:

$$T_{RISE} = T_{SET} - T_A$$

$$\theta_{JA} \text{ (nominal)} = 120^\circ\text{C/W}$$

If  $T_A = -40^\circ\text{C}$ ,  $T_{SET} = +70^\circ\text{C}$  (TSET pin floating), and  $\theta_{JA} = +120^\circ\text{C/W}$ ,

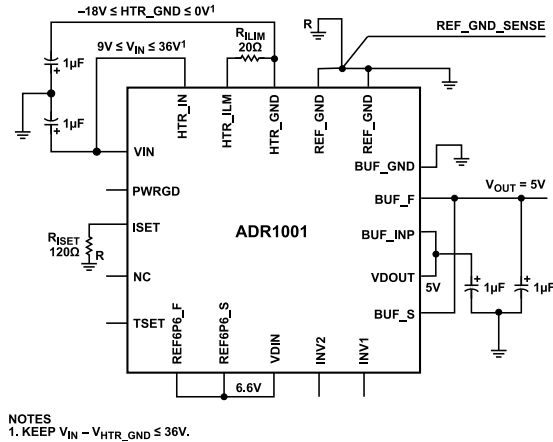
$$\text{Power} = (+70^\circ\text{C} - (-40^\circ\text{C})) / 120^\circ\text{C/W} = 0.92 \text{ W} \quad (4)$$

Note that power dissipation is the product of the voltage applied to the heater transistor ( $V(HTR\_IN) - V(HTR\_GND)$ ) and the current applied via the thermal feedback loop ( $I_{HEATER}$ ). The heater transistor has a built-in current limit of 100 mA. Thus, care must be taken to ensure that maximum  $T_{RISE}$  can be achieved with the voltage and current available to the heater.

If a power budget analysis determines that more power is required to cover the maximum  $T_{RISE}$ , the ADR1001 heater ground can be level shifted to a negative voltage to increase the total available voltage across the heater, thus cutting the heater current requirement for a given  $T_{RISE}$ , as shown in Figure 42.



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**Figure 42. HTR\_ILIM and HTR\_GND Shifted Negatively**

Since the heater current is inversely proportional to heater voltage for a given set temperature, doubling the heater voltage effectively reduces the current requirement in half. Note that the absolute maximum voltage across the heater transistor is 36 V. Therefore, if HTR\_GND is level shifted to -18 V, the HTR\_IN absolute maximum is +18 V.

**HEATER CURRENT LIMITING**

Previous ovenized voltage references do not integrate a current limiter into the thermal regulator. This can be problematic at power-up if the power supply cannot provide the initial current inrush at colder ambient temperatures. If HTR\_ILIM and HTR\_GND are shorted, the ADR1001 limits the heater current to 100 mA. If the heater start-up time is less critical than peak inrush current, a resistor ( $R_{ILIM}$ ) can be placed between HTR\_ILIM and HTR\_GND to further lower the short-circuit current limit. Figure 19 and Figure 20 show the REF6P6 reference start-up delay associated with a 40% reduction in peak heater current.

**SETTING THE ADR1001 OPERATING TEMPERATURE**

The ADR1001 TSET pin allows for programming of the chipset temperature via pin strapping through a resistor ( $R_{TSET}$ ) to REF6P6\_F (to lower the thermostat) or REF\_GND (to raise the thermostat). If TSET is left floating, the thermostat is programmed to a 70°C default set temperature. It is important to note that all ADR1001 absolute accuracy trims are performed at the default set temperature of 70°C and, since the unheated tempco of the 6.6 V reference

is 36 ppm/°C typical, any adjustment to  $T_{CHIP}$  incurs a penalty to absolute accuracy of around 36 ppm/°C of adjustment.

Table 9 shows a list of common values and chipset temperatures. These values are extracted from Figure 15. It is good practice to set  $T_{CHIP}$  to as low of a value as the system can tolerate. This practice not only conserves power, but also helps reduce on-chip gradients that degrade thermally regulated tempco.

**Table 9. Configuring TSET Pin for Desired Chipset Temperature**

Desired Set Temperature	Pin Configuration
40°C	Short to REF6P6_F
60°C	Connect 79 kΩ to REF6P6_F
70°C	Float TSET
90°C	Connect 63 kΩ to REF_GND
110°C	Connect 15.8 kΩ to REF_GND
125°C	Short to REF_GND

It is also important to consider other parasitic dissipators as they can impact at what temperature the ADR1001 loses thermal regulation. For example, as seen in Table 10, with  $R_{ISET} = 102 \Omega$  and  $V_{IN} = 15 V$ , the reference dissipates approximately  $15 V \times 6.74 mA = 95 mW$ . With a  $\theta_{JA} = +120^\circ C/W$ , the reference self-heats approximately 11°C. This means that if the ADR1001 thermostat is set to 70°C, the ADR1001 heater exits thermal regulation at approximately 59°C, as shown in Figure 28, Figure 29, and Figure 31.

The ADR1001 thermostat has been characterized by measuring die temperature through a remote temperature sensor (see Figure 32 and Figure 33) and by direct measure of when the reference thermally deregulates (see Figure 29). Figure 29 shows the 6.6 V reference tempco vs. an ambient temperature sweep for TSET floating, TSET shorted to REF6P6, and TSET shorted to REF\_GND. In all three curves, the inflection point indicates the temperature at which thermal deregulation occurs, including self-heating.

Once the ambient temperature exceeds  $T_{CHIP}$ , the power-good status flag pulls low (see Figure 31), alerting the user that the reference is no longer in thermal regulation. Running the ADR1001 with  $T_{SET} = +125^\circ C$  is not recommended, as diode leakage from ESD protection diodes can adversely impact the noise and long-term drift performance. High  $T_{SET}$  temperatures are intended for a self-burn post solder, although Analog Devices has not thoroughly investigated the efficacy of this approach.

**Table 10. Thermal Deregulation Margins**

Thermal Deregulation (°C)	$\theta_{JA}$ (°C/W)	$I_{VIN}$ (A)	$V_{IN}$ (V)	$T_{MARGIN}$ (°C)	Remote Temp Sensor Error (°C)	Actual Die Temperature (°C)
+28	+120	$+7.30 \times 10^{-3}$	+15	+13.14	-1.72	+39.42
+60	+120	$+6.74 \times 10^{-3}$	+15	+12.13	-1.89	+70.24
+120	+120	$+5.70 \times 10^{-3}$	+15	+10.26	-2.19	+128.07

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### PRECISION VOLTAGE DIVIDER AND OUTPUT BUFFER

The 6.6 V reference output provides an extremely stable buried Zener voltage, but with relatively poor initial accuracy. A 5 V absolute accurate thin film divider is accessible via the VDOOUT and VDIN pins. The divider and buffer offset are trimmed together to 5 V or to  $\pm 0.25\%$  accuracy. The trim is done with a Zener current-set resistor of 102  $\Omega$  and at the default chipset temperature of +70°C.

### POWER GOOD

The ADR1001 provides an open-collector status flag pin that when tied to a given supply via a pull-up resistor alerts the user if one or more fault conditions are present. [Table 11](#) shows the state of the PWRGD pin for a given condition.

**Table 11. PWRGD Pin States**

Condition	PWRGD	Heater Current	Notes
All Clear	High	0 mA < $I_{\text{HEATER}}$ < 100 mA	Heater regulated
$T_{\text{CHIP}}$ Low	Low	100 mA	Have not reached set temperature
$T_{\text{CHIP}}$ High	Low	0 mA	$T_{\text{A}} > T_{\text{CHIP}}$
$V_{\text{IN}}$ Low	Low	Disabled	$V_{\text{IN}} < 9 \text{ V}$
6.6 V $V_{\text{REF}}$ Low	Low	Disabled	Overload on $V_{\text{REF}}$

If no fault conditions are present, the PWRGD pin must read whichever voltage supply the pull-up resistor is tied to. There are a couple of reasons the PWRGD pin is deasserted due to the  $T_{\text{CHIP}}$  low condition:

- ▶ The chip has not completely warmed up. At room temperature, with 15 V on the heater and  $T_{\text{CHIP}}$  of +70°C (thermal regulation completes in about 1 sec).
- ▶ The thermal regulator does not have enough power to reach the programmed set temperature and is therefore in current limit.

If the ambient temperature exceeds the chipset temperature, the current in the heater reaches 0 mA and the PWRGD pin is deasserted. The reference still functions, but with a severely degraded tempco of 36 ppm/°C for  $I_{\text{Z}} = 4 \text{ mA}$ , for example.

### EXTERNAL RESISTOR SENSITIVITY

The ADR1001 integrates most of the resistors required in the [ADR1000](#) applications circuit. However, there are a couple of key components that can still impact the long-term stability of the device. The  $R_{\text{ISET}}$  resistor characteristics are attenuated by a factor of 267 with respect to the 6.6 V reference output. That is, if the  $R_{\text{ISET}}$  value drifts by 10 ppm in the first 1000 hours of operation, that adds  $10 \text{ ppm}/267 = 0.003 \text{ ppm}$  of drift to the 6.6 V reference.

To a much lesser extent, adjusting the ADR1001 thermostat using a TSET resistor also has an impact on long-term stability. For example, a 20 ppm change in an external TSET resistor changes  $T_{\text{CHIP}}$  by approximately 0.0001°C. The typical unheated tempco of the ADR1001 is 36 ppm/°C, and thus the ADR1001 reference

output incurs a  $(0.0001^\circ\text{C} \times 36 \text{ ppm}/^\circ\text{C}) = 0.0036 \text{ ppm}$  change in output voltage. In other words, the TSET resistor characteristic effects on the reference are attenuated by a factor of about 5500.

### CAPACITORS

The ADR1001 VIN and HTR\_IN supply pins should be bypassed with 1  $\mu\text{F}$  or larger capacitors placed as close to the pins as possible. In the event the heater is level-shifted below ground by a negative regulator, the HTR\_GND pin should be bypassed equivalently. The ADR1001 output buffer requires a minimum 0.2  $\mu\text{F}$  of load capacitance placed near BUF\_F for stability. If smaller load step perturbation is required, the part has been tested with up to 38  $\mu\text{F}$  WIMA capacitors (see the 1 mA load step response in [Figure 21](#)). Surface-mount multilayer ceramic capacitors all exhibit a voltage coefficient that reduces the effective capacitance value with applied voltage. If the BUF\_F output capacitor value is chosen close to 0.2  $\mu\text{F}$ , care should be taken that the type and size of capacitor does not exhibit excessive voltage coefficient, as this could cause the output to display excessive ringing during a load step. Refer to the capacitor manufacturer specifications to determine if the desired form factor needs to be upsized to account for the effect of the voltage coefficient.

### NOISE PERFORMANCE

Because the ADR1001 noise is dominated by the buried Zener reference itself, broadband noise can be reduced to a minimum of the buffer input referred noise ( $\sim 15 \text{ nV}/\sqrt{\text{Hz}}$ ) by placing a capacitor to REF\_GND at the VDOOUT-BUF\_INP connection. As shown in [Figure 1](#), this noise filter capacitor forms a low-pass filter with a -3 dB point determined by R1 in parallel with R2 and the noise filter capacitance itself. The R1 and R2 parallel combination has a nominal value of 2.3 k $\Omega$ . However, this value varies slightly from part to part. As shown in [Figure 3](#), the effect of a 2.3 k $\Omega$  + 1  $\mu\text{F}$  low-pass filter can be observed in the ADR1001 5 V output noise spectral density with a -3 dB roll-off occurring at around 70 Hz.

A few precautions must be taken to replicate the noise performance measured in [Figure 3](#) and [Figure 4](#). Dissimilar metal junctions formed at the PCB solder joints create a thermocouple effect, which, when disturbed with an air gradient, create additional low-frequency noise.

The ADR1001 has a typical DC PSRR exceeding 120 dB. However, driving the supplies with a low-noise, high-AC PSRR regulator such as the LTC3045 is still recommended to prevent high-frequency noise from coupling to the output through the supplies.

### ELECTROMECHANICAL STABILITY

The ADR1001 is designed to provide similar mechanical stability performance to the ADR1000 or LTZ1000 but in a more manufacturing-friendly, surface-mount ceramic package. However, because the ADR1001 comes in direct contact with the FR4, utilization of PCB cutouts, as per the ADR1001 evaluation board ([EVAL-ADR1001](#)) and as described in the [AN-82 Application Note Under-](#)

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standing and Applying Voltage References, is highly recommended. Figure 11 and Figure 13 show the long-term drift performance of 32 units. All units were soldered to a PCB with diving board cutouts and drift measurements beginning within 24 hours of solder. Additionally, the use of the ADR1001 in applications that involve high levels of vibration, acceleration, and/or potential for mechanical shock is not recommended.

**SOLDER HEAT RESISTANCE (SHR) SHIFT**

The SHR shift refers to the permanent change in output voltage induced by both mechanical stress and elevated temperature associated with soldering the part to a PCB. After the part undergoes a solder reflow cycle and begins cooling, the materials that comprise the semiconductor device contract at different rates, causing mechanical stress gradients to change. This effect is more pronounced in lead-free soldering processes due to higher reflow temperatures.

The SHR is calculated after three solder reflow cycles to simulate conditions where two reflows are required for assembling a two-sided PCB with surface-mount components, and one additional cycle is required for rework. The reflow cycles use the JEDEC standard reflow temperature profile. Experimental SHR results are shown in Figure 43 and Figure 44. These results show shift due to reflow heat only, not mechanical stress.

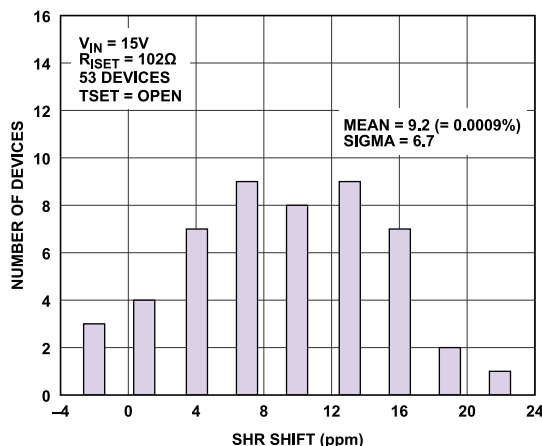


Figure 44. SHR Shift, 6.6 V Output

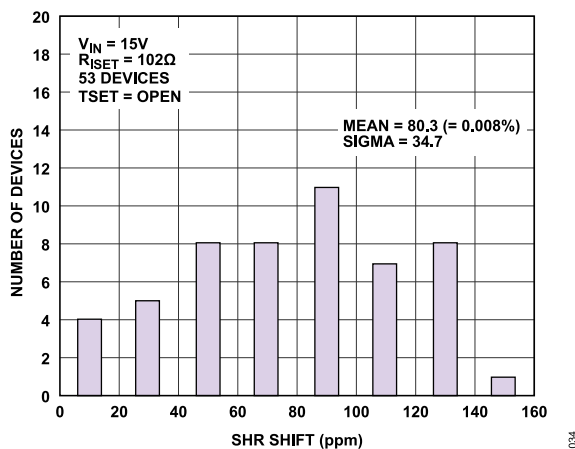


Figure 43. SHR Shift, 5 V Output

APPLICATIONS INFORMATION

BASIC CONNECTIONS

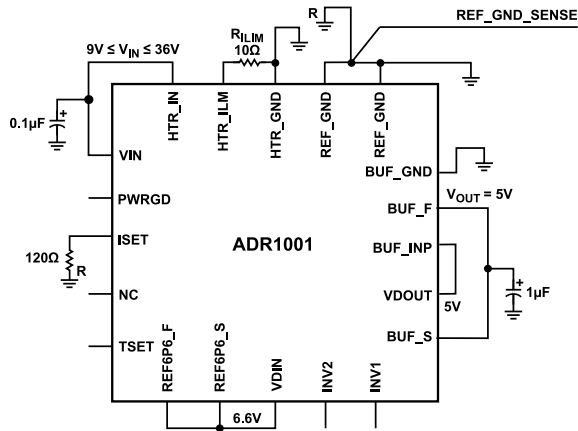


Figure 45. Basic Hookup for 5 V Output

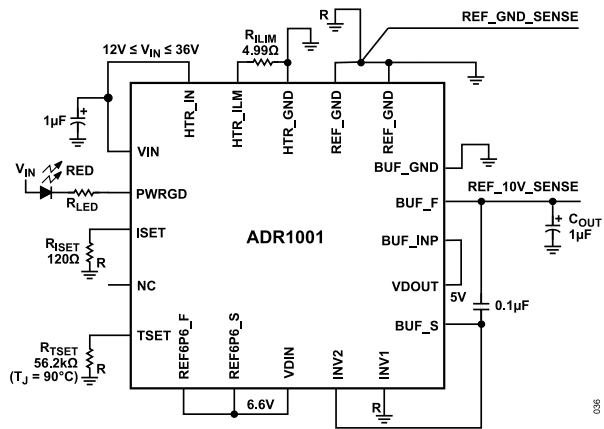
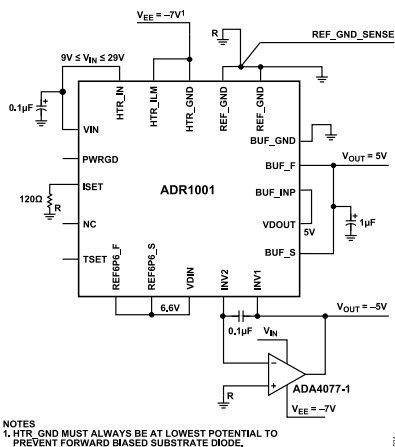


Figure 46. 10 V Ultra-Stable Reference Using On-Chip Matched Resistors



NOTES  
1. HTR\_GND MUST ALWAYS BE AT LOWEST POTENTIAL TO PREVENT FORWARD BIASED SUBSTRATE DIODE.

Figure 47. Bipolar ±5 V DAC Drive Using Internal INV1 and INV2 Resistors and One External Inverting Op Amp

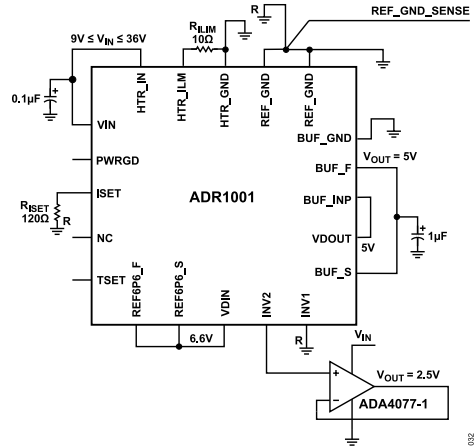


Figure 48. Simultaneous Full 5 V and Half-Scale 2.5 V Reference Outputs Using Internal INV1 and INV2 Resistor-Divider and One External Op Amp Buffer

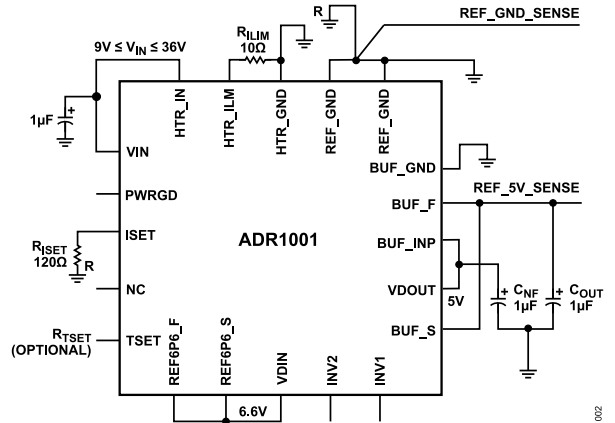


Figure 49. Ultra-Stable 5 V ± 0.25% Reference with 60 mA Inrush Limit

OUTLINE DIMENSIONS

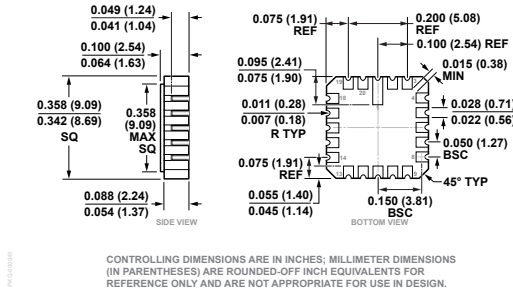


Figure 50. 20-Terminal Ceramic Leadless Chip Carrier [LCC] (E-20-1)  
 Dimensions shown in inches and millimeters

Updated: March 11, 2023

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADR1001AEZ	-40°C to +125°C	20-Lead LCC	E-20-1

<sup>1</sup> Z = RoHS Compliant Part.

EVALUATION BOARDS

Model <sup>1</sup>	Description
ADR1001E-EBZ	Evaluation Board

<sup>1</sup> Z = RoHS Compliant Part.