ADS-1011

10-Bit, 2.5µs Sampling A/D Converter

PRODUCT OVERVIEW

The ADS-1011 is a serial output, low power, 10-bit A/D converter that is rated to withstand up to 30k Rad. Operating from a supply range of 2.7 V to 5.5 V, these 2.5µs successive approximation converters are available in commercial or extended operating temperature grades. The ADS-1011 offers a unique architecture that includes a sample-hold, high speed microprocessor compatible serial data transfer while consuming less than 2mW of power at 50 kHz throughput. These converters are available in a 24-pin LCC hermetically sealed ceramic package. For other package options, contact the factory. Models are available for use in commercial (0 to +70°C), industrial (–40 to +100°C), or Hi-Rel (–55 to +125°C) operating temperature ranges.

FEATURES

- 10-bit resolution
- 2.5µs conversion time
- Less than 2mW @ 50kHz throughput
- Rated to withstand 30k Rad
- Small, 24 pin LCC ceramic package
- +2.7 to +5.5 Vdc operation
- Microprocessor compatible serial interface
- 250kHz throughput
- Hi-Rel model available (–55°C to +125°C)

INPUT/OUTPUT CONNECTIONS			
Pin	FUNCTION	Pin	FUNCTION
1	NC	24	-Vin
2	NC	23	+Vin
3	NC	22	NC
4	NC	21	NC
5	NC	20	CONVST
6	GND	19	NC
7	GND	18	Vdd
8	REF	17	Vdd
9	NC	16	GND
10	NC	15	GND
11	NC	14	NC
12	DOUT	13	SCLK

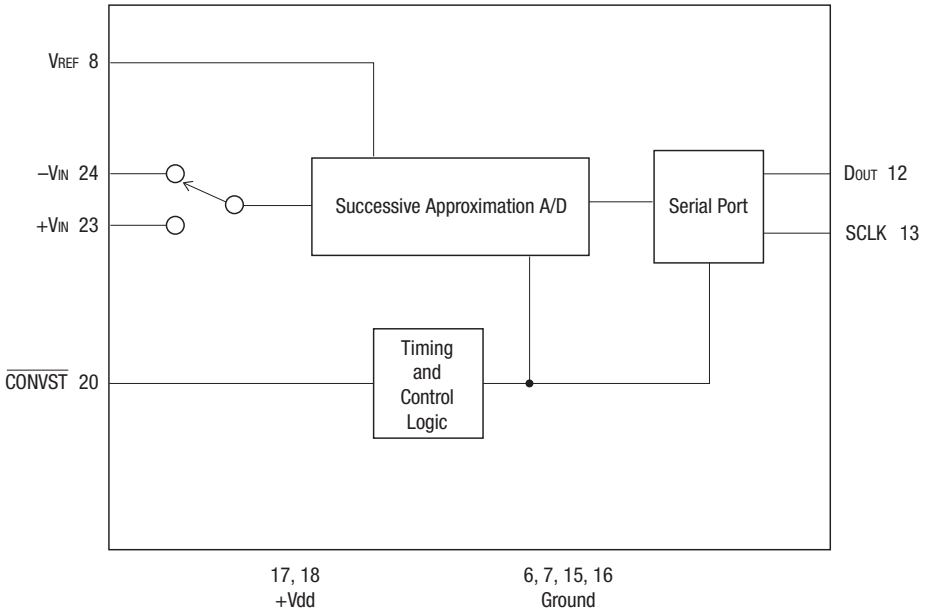


Figure 1. ADS-1011 Block Diagram

ABSOLUTE MAXIMUM RATINGS		
PARAMETERS	**LIMITS**	**UNITS**
Power Supply Voltage (V_{DD})	–0.3 to +7	Volts
Digital Inputs	–0.3 to V_{DD}+0.3	Volts
Analog Input	–0.3 to V_{DD}+0.3	Volts
Reference to GND	–0.3 to V_{DD}+0.3	Volts
Digital Outputs	–0.3 to V_{DD}+0.3	Volts
Lead Temperature (10 sec. max.)	+300	°C
Storage Temperature	–65 to +150	°C

FUNCTIONAL SPECIFICATIONS

(Typical at GND=0V, VREF=V_{DD}, +25°C)

ANALOG INPUT	**MIN.**	**TYP.**	**MAX.**	**UNITS**
Analog Input	0	–	VREF	Volts
Analog Input Capacitance				
Input Capacitance	—	—	15	pF
Input Current	—	—	±	µA
DIGITAL INPUTS				
Logic Levels				
Logic "1"	2.0	—	—	Volts
Logic "0"	—	—	0.4	Volts
Logic Loading				
Logic Loading "1"	—	—	+1	µA
Logic Loading "0"	—	—	-1	µA
DIGITAL OUTPUTS				
Logic Levels				
Logic "1"	2.4	—	—	Volts
Logic "0"	—	—	0.4	Volts
High impedance Leakage Current	—	—	±20	µA
TIMING				
Conversion Time	—	—	2.5	µs
Throughput Rate	—	—	250	kHz
Sample Hold Acquisition Time	—	—	120	nSec
REFERENCE				
Reference Input	1.5	—	V_{DD}	Volts
Input Current	—	—	±5	µA
PERFORMANCE	**MIN.**	**TYP.**	**MAX.**	**UNITS**
No Missing Codes	10	—	—	LSB
Integral Nonlinearity (end-point)	—	—	±1	LSB
Differential Nonlinearity	—	—	±1	LSB
Zero Error	—	—	±2	LSB
Gain Error	—	—	±2	LSB
Dynamic Performance Fin = 20kHz, Fsample = 200 kHz				
Signal-to-Noise (& distortion)	58	60	—	dB
Total Harmonic Distortion	—	65	-64	dB
Peak Harmonics	—	—	-64	dB
Two Tone Intermodulation Distortion (29.5kHz, 30kHz)	—	-67	—	dB

POWER REQUIREMENTS				
Power Supply Range (+VDD)	+2.7	+5.0	+5.5	Volts
Power Supply Current				
250 kHz Throughput Rate	—	—	3.5	mA
Power Dissipation				
At V_{DD} = 5.5V	—	—	20	mW
PHYSICAL/ENVIRONMENTAL				
Operating Temp. Range, Case:				
LC Versions	0	—	+70	°C
LE Versions	–40	—	+100	°C
LM Versions	–55	—	+125	°C
Storage Temp. Range	–65	—	+150	°C
Package Type	LCC 24-pin ceramic LCC			
REFERENCE INPUTS	**MIN.**	**TYP.**	**MAX.**	**UNITS**
VREF Input Voltage Range	1.2	—	VDD	Volts
Input Current	—	—	10	uA
Input Capacitance	—	—	15	pf

TECHNICAL NOTES

The ADS-1011 is a successive approximation A/D with a built-in sample-hold. The analog input voltage is applied between pins Vin+ and Vin-. The Hi to Lo transition of the CONVST command initiates the conversion process. The rising edge of the succeeding SCLK signal will bring out the most significant bit (MSB) of the conversion process. The rising edge of the second SCLK will bring out the next most significant. This process will continue until the 10th SCLK rising edge has brought out the least significant bit (LSB). Note that the rising edge of SCLK can also be used to latch Dout (see fig. 3, timing diagram).

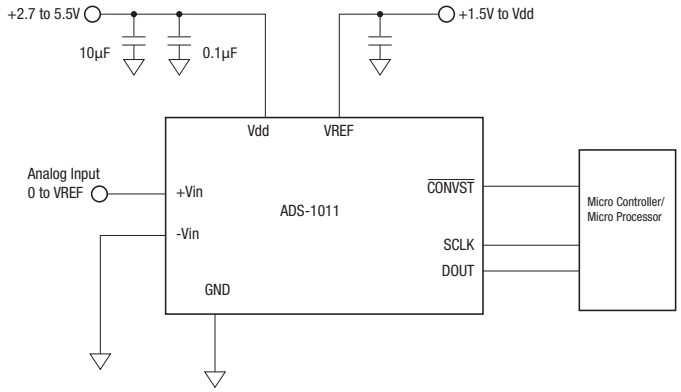


Figure 2. Typical Connection Diagram

Table 1. Timing Parameter

Timing Designation	Description	Parameter
	CONVST Pulsewidth LO	30ns min
	CONVST Pulsewidth HI	30ns min
t_1	CONVST rising edge to SCLK rising edge	10ns min
t_2	SCLK rising edge to Dout data valid	15ns max
t_3	SCLK Pulsewidth HI	40ns min
t_4	SCLK Pulsewidth LO	40ns min
t_5	Data valid after rising edge of SCLK	10ns max
t_6	Data Out HI_Z after falling edge of SCLK	25ns max

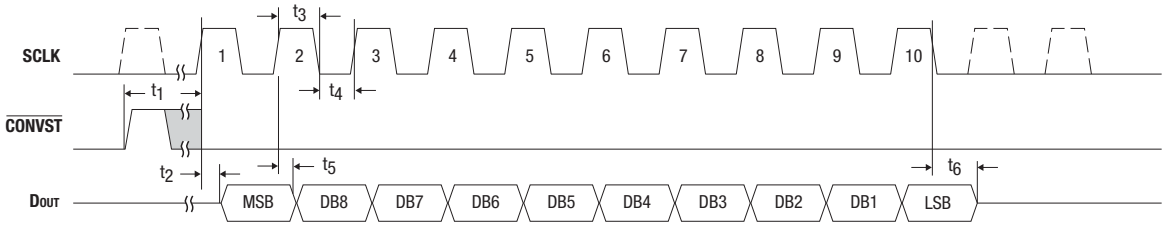
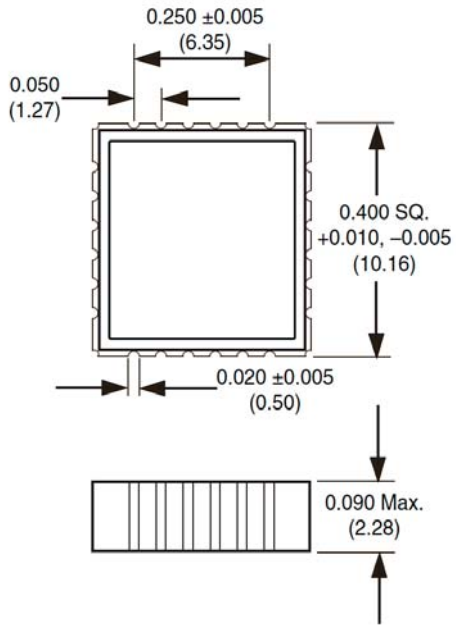


Figure 3. Timing Diagram

MECHNICAL DIMENSIONS

ADS-1011 LCC



ORDERING INFORMATION

MODEL	TEMP. RANGE	PACKAGE	ROHS
ADS-1011LC	0°C to +70°C	24-pin LCC	No
ADS-1011LC-C	0°C to +70°C	24-pin LCC	Yes
ADS-1011LE	–40°C to +100°C	24-pin LCC	No
ADS-1011LE-C	–40°C to +100°C	24-pin LCC	Yes
ADS-1011LM	–55°C to +125°C	24-pin LCC	No
ADS-1011LM-C	–55°C to +125°C	24-pin LCC	Yes

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