



20-Bit Analog-to-Digital Converter For Bridge Sensors

FEATURES

- Complete Front-End for Bridge Sensor
- Onboard PGA with Gain of 64 or 128
- Onboard Oscillator
- RMS Noise:
40nV at 10SPS (G = 128)
88nV at 80SPS (G = 128)
- 18-Bit Noise-Free Resolution
- Selectable 10SPS or 80SPS Data Rates
- Simultaneous 50Hz and 60Hz Rejection at 10SPS
- External Voltage Reference up to 5V for Ratiometric Measurements
- Simple, Pin-Driven Control
- Two-Wire Serial Digital Interface
- Tiny 16-pin TSSOP Package
- Supply Range: 2.7V to 5.3V
- -40°C to $+85^{\circ}\text{C}$ Temperature Range

APPLICATIONS

- Weigh Scales
- Strain Gauges
- Pressure Sensors
- Industrial Process Control

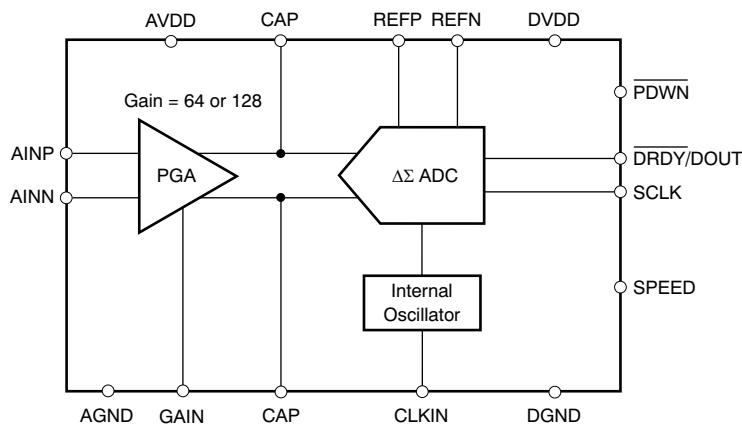
DESCRIPTION

The ADS1230 is a precision 20-bit analog-to-digital converter (ADC). With an onboard low-noise programmable gain amplifier (PGA), onboard oscillator, and precision 20-bit delta-sigma ADC, the ADS1230 provides a complete front-end solution for bridge sensor applications including weigh scales, strain gauges, and pressure sensors.

The low-noise PGA has a gain of 64 or 128, supporting a full-scale differential input of $\pm 39\text{mV}$ or $\pm 19.5\text{mV}$, respectively. The delta-sigma ADC has 20-bit effective resolution and is comprised of a 3rd-order modulator and 4th-order digital filter. Two data rates are supported: 10SPS (with both 50Hz and 60Hz rejection) and 80SPS. The ADS1230 can be clocked by the internal oscillator or an external clock source. Offset calibration is performed on-demand, and the ADS1230 can be put in a low-power standby mode or shut off completely in power-down mode.

All of the features of the ADS1230 are controlled by dedicated pins; there are no digital registers to program. Data are output over an easily-isolated serial interface that connects directly to the MSP430 and other microcontrollers.

The ADS1230 is available in a TSSOP-16 package and is specified from -40°C to $+85^{\circ}\text{C}$.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	ADS1230	UNIT
AVDD to AGND	-0.3 to +6	V
DVDD to DGND	-0.3 to +6	V
AGND to DGND	-0.3 to +0.3	V
Input Current	100, Momentary	mA
	10, Continuous	mA
Analog Input Voltage to AGND	-0.3 to AVDD + 0.3	V
Digital Input Voltage to DGND	-0.3 to DVDD + 0.3	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-60 to +150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $\text{AVDD} = \text{DVDD} = \text{REFP} = +5\text{V}$, $\text{REFN} = \text{AGND}$, and $\text{Gain} = 64$, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1230			UNIT	
		MIN	TYP	MAX		
Analog Inputs						
Full-Scale Input Voltage (AINP – AINN)		$\pm 0.5V_{\text{REF}}/\text{PGA}$			V	
Common-Mode Input Range		AGND + 1.5V		AVDD – 1.5V	V	
Differential Input Current		± 2			nA	
System Performance						
Resolution	No Missing Codes	20			Bits	
Data Rate	Internal Oscillator, SPEED = High	69.5	80	86.4	SPS	
	Internal Oscillator, SPEED = Low	8.68	10	10.8	SPS	
	External Oscillator, SPEED = High	$f_{\text{CLK}}/61,440$			SPS	
	External Oscillator, SPEED = Low	$f_{\text{CLK}}/491,520$			SPS	
Digital Filter Settling Time	Full Settling	4			Conversions	
Integral Nonlinearity (INL)	Differential Input, End-Point Fit, G = 64	± 10			ppm	
	Differential Input, End-Point Fit, G = 128	± 6			ppm	
Input Offset Error ⁽¹⁾		± 3			ppm of FS	
Input Offset Drift		± 10			nV/ $^{\circ}\text{C}$	
Gain Error		± 0.8			%	
Gain Drift		± 4			ppm/ $^{\circ}\text{C}$	
Normal-Mode Rejection ⁽²⁾	Internal Oscillator, $f_{\text{DATA}} = 10\text{SPS}$	90			dB	
	External Oscillator, $f_{\text{DATA}} = 10\text{SPS}$ $f_{\text{IN}} = 50\text{Hz}$ or 60Hz , $\pm 1\text{Hz}$	100			dB	
Common-Mode Rejection	at DC, $\Delta\text{VDD} = 0.1\text{V}$	110			dB	
Input-Referred Noise	$f_{\text{DATA}} = 10\text{SPS}$	53			nV, rms	
	$f_{\text{DATA}} = 80\text{SPS}$	100			nV, rms	
Power-Supply Rejection	at DC, $\Delta\text{VDD} = 0.1\text{V}$	90	100		dB	
Voltage Reference Input						
Voltage Reference Input (V_{REF})	$V_{\text{REF}} = \text{REFP} - \text{REFN}$	1.5	AVDD	AVDD + 0.1V	V	
Negative Reference Input (REFN)		AGND – 0.1		REFP – 1.5	V	
Positive Reference Input (REFP)		REFN + 1.5		AVDD + 0.1	V	
Voltage Reference Input Current		10			nA	
Digital						
Logic Levels	V_{IH}	All digital inputs except CLKIN	0.7 DVDD		DVDD + 0.1	V
		CLKIN	0.7 DVDD		5.1	V
	V_{IL}		DGND		0.2 DVDD	V
	V_{OH}	$I_{\text{OH}} = 1\text{mA}$	DVDD – 0.4			V
V_{OL}	$I_{\text{OL}} = 1\text{mA}$			0.2 DVDD	V	
Input Leakage	$0 < V_{\text{IN}} < \text{DVDD}$				± 10	μA
External Clock Input Frequency (f_{CLKIN})		0.2	4.9152	6	MHz	
Serial Clock Input Frequency (f_{SCLK})					5	MHz

(1) Offset calibration can minimize these errors to the level of noise at any temperature.

(2) Specification is assured by the combination of design and final production test.

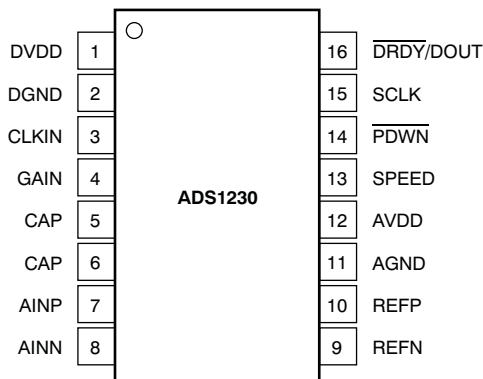
ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, AVDD = DVDD = REFP = +5V, REFN = AGND, and Gain = 64, unless otherwise noted.

PARAMETER	CONDITIONS	ADS1230			UNIT
		MIN	TYP	MAX	
Power Supply					
Power-Supply Voltage (AVDD, DVDD)		2.7		5.3	V
Analog Supply Current	Normal Mode, AVDD = 3V		900	1400	μA
	Normal Mode, AVDD = 5V		900	1400	μA
	Standby Mode		0.1	1	μA
	Power-Down		0.1	1	μA
Digital Supply Current	Normal Mode, DVDD = 3V		60	100	μA
	Normal mode, DVDD = 5V		95	140	μA
	Standby Mode, SCLK = High, DVDD = 3V		45	65	μA
	Standby Mode, SCLK = High, DVDD = 5V		65	80	μA
	Power-Down		0.2		μA
Power Dissipation, Total	Normal Mode, AVDD = DVDD = 3V		2.9	4.5	mW
	Normal Mode, AVDD = DVDD = 5V		5.0	7.7	mW
	Standby Mode, AVDD = DVDD = 5V		0.3	0.4	mW

PIN CONFIGURATION

PW PACKAGE TSSOP-16 (Top View)



PIN DESCRIPTIONS

NAME	TERMINAL	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
DVDD	1	Digital	Digital Power Supply: 2.7V to 5.3V
DGND	2	Digital	Digital Ground
CLKIN	3	Digital/Digital Input	External Clock Input: typically 4.9152MHz. Tie low to activate internal oscillator.
GAIN	4	Digital Input	PGA Gain Select
			GAIN PGA
			0 64 1 128
CAP	5	Analog	Gain Amp Bypass Capacitor Connection
CAP	6	Analog	Gain Amp Bypass Capacitor Connection
AINP	7	Analog Input	Positive Analog Input
AINN	8	Analog Input	Negative Analog Input
REFN	9	Analog Input	Negative Reference Input
REFP	10	Analog Input	Positive Reference Input
AGND	11	Analog	Analog Ground
AVDD	12	Analog	Analog Power Supply, 2.7V to 5.3V
SPEED	13	Digital Input	Data Rate Select:
			SPEED DATA RATE
			0 10SPS 1 80SPS
PDWN	14	Digital Input	Power-Down: Holding this pin low powers down the entire converter and resets the ADC.
SCLK	15	Digital Input	Serial Clock: Clock out data on the rising edge. Also used to initiate Offset Calibration and Sleep modes. See the Offset Calibration , Standby Mode , and Standby Mode with Offset Calibration sections for more details.
DRDY/DOUT	16	Digital Output	Dual-Purpose Output:
			Data Ready: Indicates valid data by going low. Data Output: Outputs data, MSB first, on the first rising edge of SCLK.

NOISE PERFORMANCE

The ADS1230 offers outstanding noise performance. [Table 1](#) summarizes the typical noise performance with inputs shorted externally for different data rates and voltage reference values.

The RMS and Peak-to-Peak noise are referred to the input. The effective number of bits (ENOB) is defined as:

$$\text{ENOB} = \ln(\text{FSR}/\text{RMS noise})/\ln(2)$$

The Noise-Free Bits are defined as:

$$\text{Noise-Free Bits} = \ln(\text{FSR}/\text{Peak-to-Peak Noise})/\ln(2)$$

Where:

$$\text{FSR (Full-Scale Range)} = V_{\text{REF}}/\text{Gain}.$$

Table 1. Noise Performance for $A_{V_{DD}} = 5V$ and $V_{REF} = 5V$

DATA RATE	GAIN	RMS NOISE (nV)	PEAK-TO-PEAK NOISE ⁽¹⁾ (nV)	ENOB (RMS)	NOISE-FREE BITS
10	64	53	290	20.5	18
	128	40	198	19.8	17.5
80	64	100	480	19.5	17.3
	128	88	480	18.7	16.3

(1) Peak-to-peak data are based on direct measurement.

Table 2. Noise Performance for $A_{V_{DD}} = 3V$ and $V_{REF} = 3V$

DATA RATE	GAIN	RMS NOISE (nV)	PEAK-TO-PEAK NOISE ⁽¹⁾ (nV)	ENOB (RMS)	NOISE-FREE BITS
10	64	46	290	20.6	18
	128	49	259	19.6	17.2
80	64	100	576	19.5	17
	128	102	461	18.5	16.3

(1) Peak-to-peak data are based on direct measurement.

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $AVDD = DVDD = REFP = 5\text{V}$, and $REFN = \text{AGND}$, unless otherwise noted.

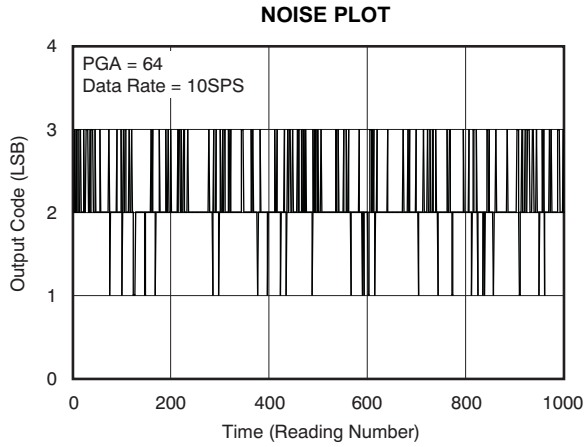


Figure 1.

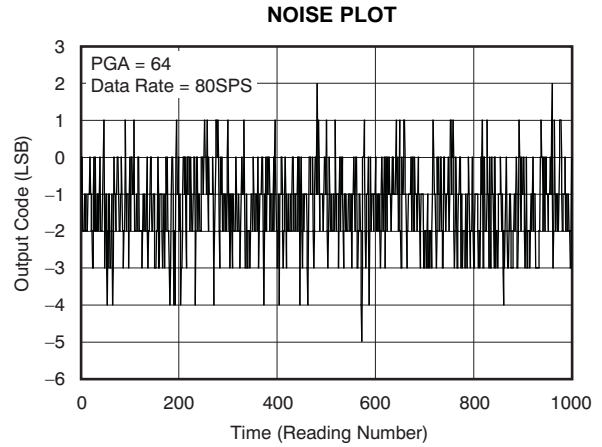


Figure 2.

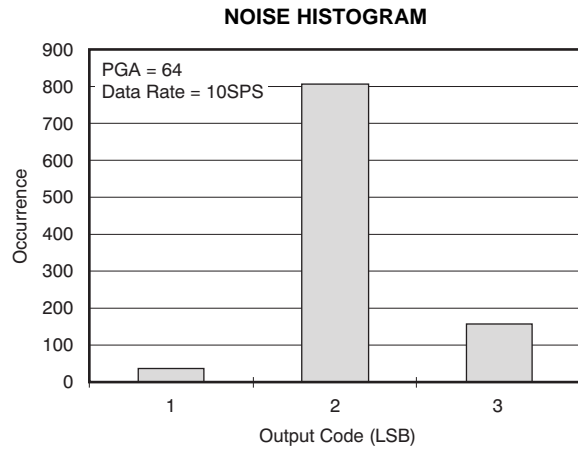


Figure 3.

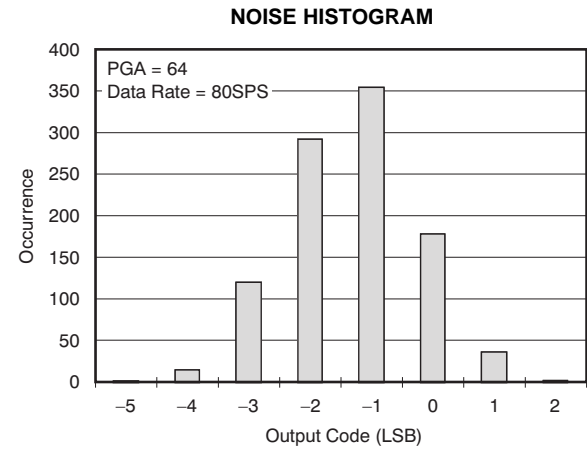


Figure 4.

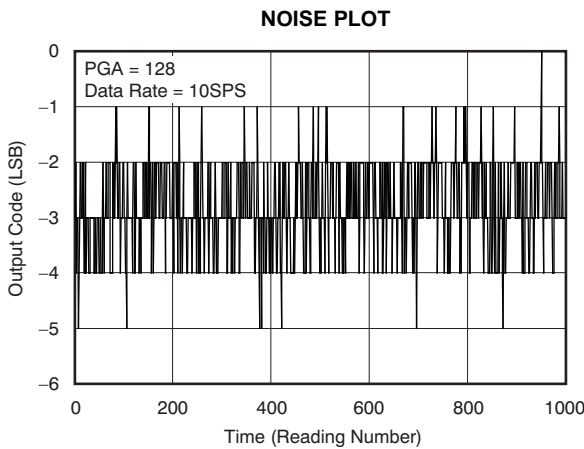


Figure 5.

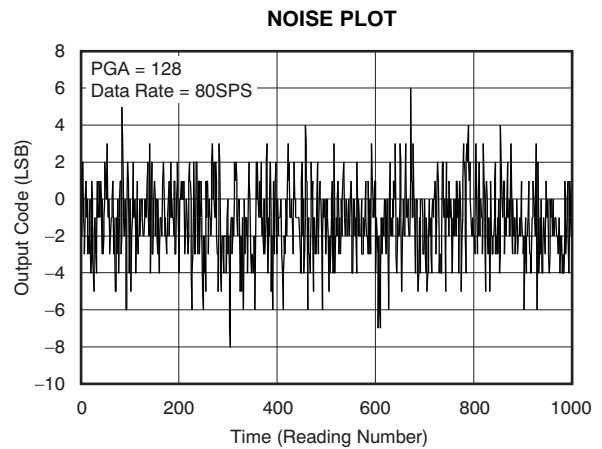


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = DVDD = REFP = 5\text{V}$, and $REFN = \text{AGND}$, unless otherwise noted.

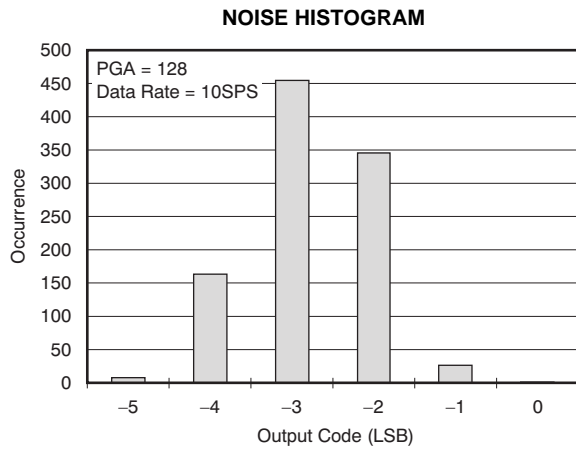


Figure 7.

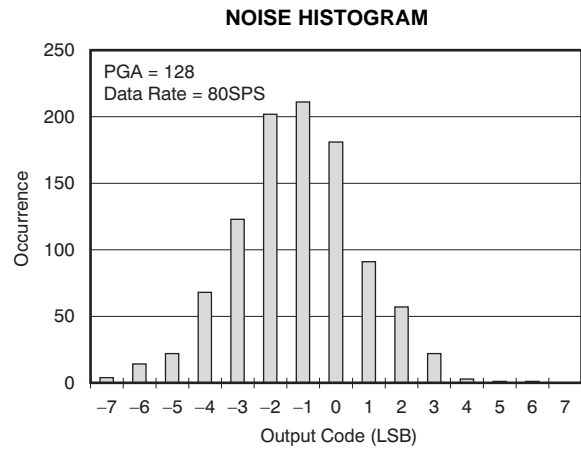


Figure 8.

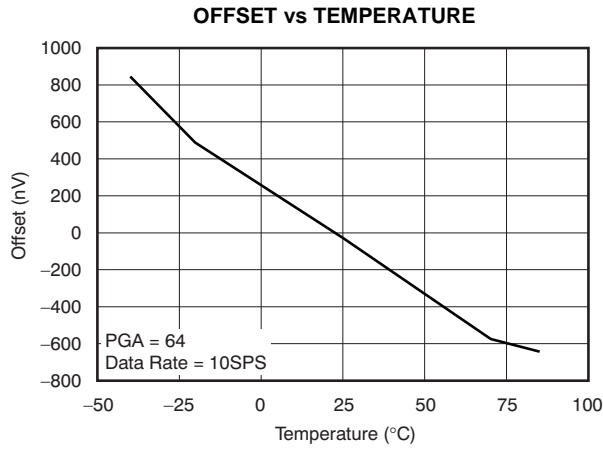


Figure 9.

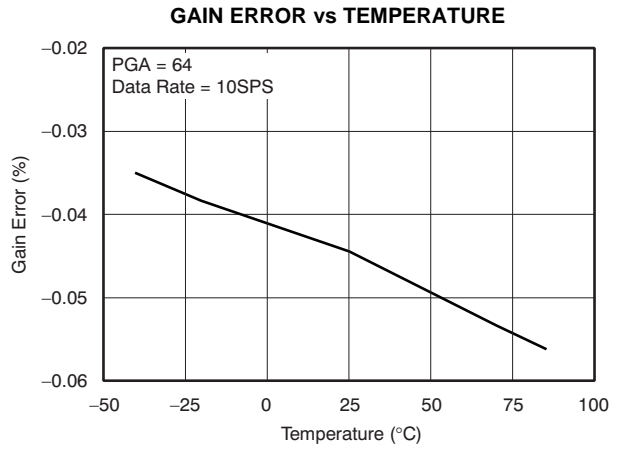


Figure 10.

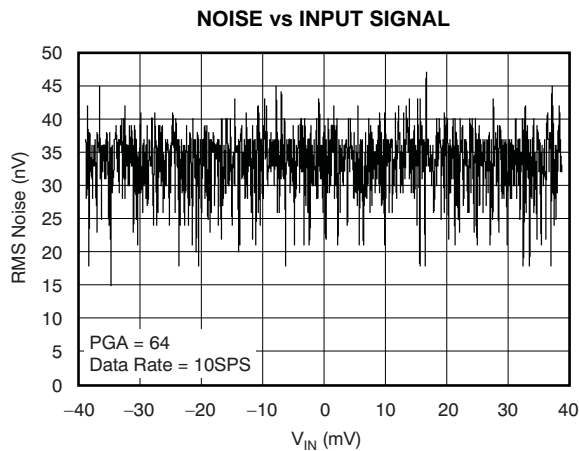


Figure 11.

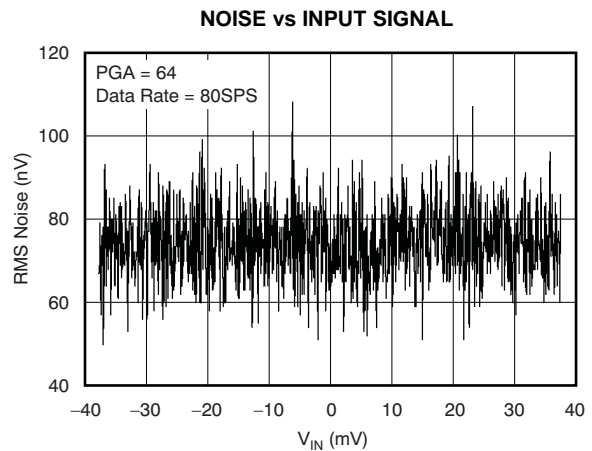


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $AVDD = DVDD = REFP = 5\text{V}$, and $REFN = \text{AGND}$, unless otherwise noted.

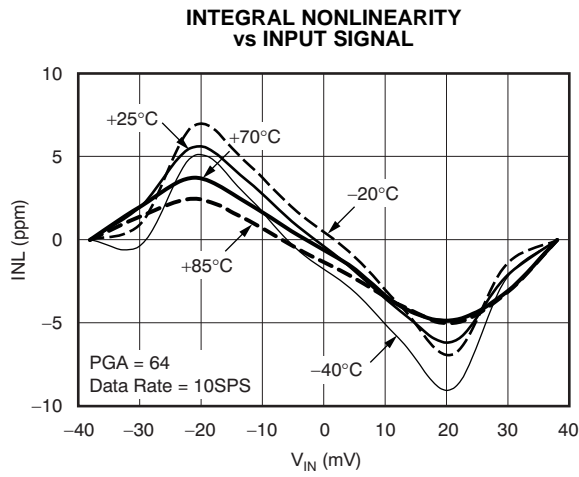


Figure 13.

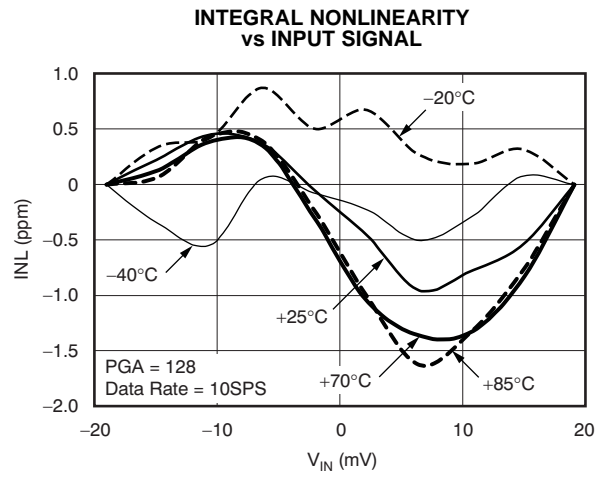


Figure 14.

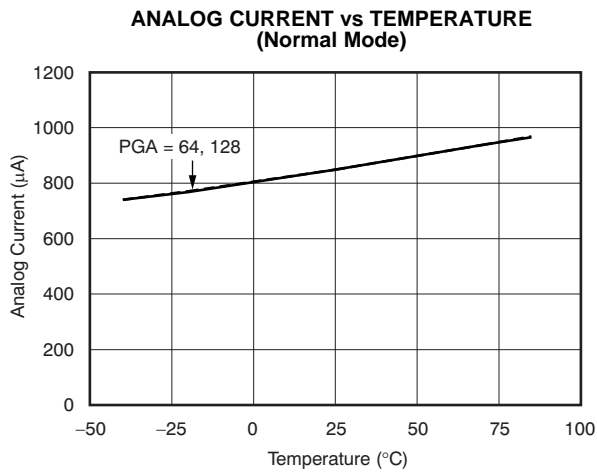


Figure 15.

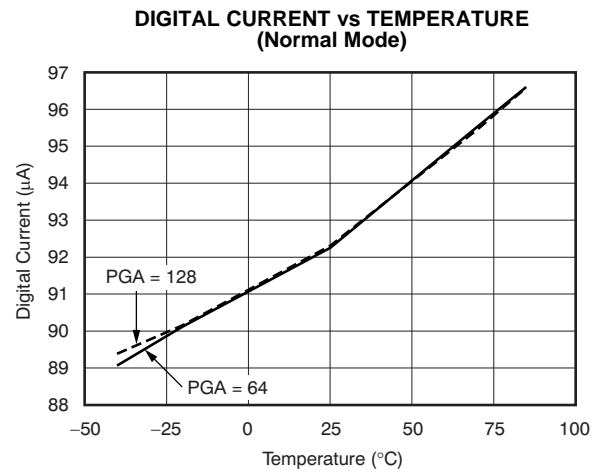


Figure 16.

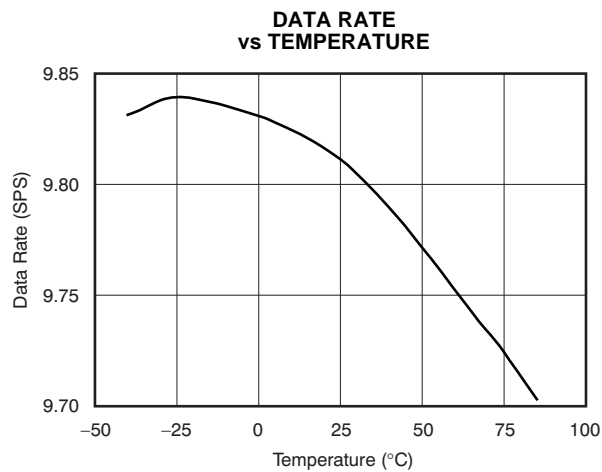


Figure 17.

OVERVIEW

The ADS1230 is a precision, 20-bit ADC that includes a low-noise PGA, internal oscillator, third-order delta-sigma ($\Delta\Sigma$) modulator, and fourth-order digital filter. The ADS1230 provides a complete front-end solution for bridge sensor applications such as weigh scales, strain gauges, and pressure sensors.

Clocking can be supplied by an external clock or by a precision internal oscillator. Data can be output at 10SPS for excellent 50Hz and 60Hz rejection, or at 80SPS when higher speeds are needed. The ADS1230 is easy to configure, and all digital control is accomplished through dedicated pins; there are no registers to program. A simple two-wire serial interface retrieves the data.

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1230 accepts differential input signals, but can also measure unipolar signals. When measuring unipolar (or single-ended signals) with respect to ground, connect the negative input (AINN) to ground and connect the input signal to the positive input (AINP). Note that when the ADS1230 is configured this way, only half of the converter full-scale range is used, since only positive digital output codes are produced.

LOW-NOISE PGA

The ADS1230 features a low-drift, low-noise PGA that provides a complete front-end solution for bridge sensors. A simplified diagram of the PGA is shown in Figure 18. It consists of two chopper-stabilized amplifiers (A1 and A2) and three accurately-matched resistors (R_1 , R_{F1} , and R_{F2}), which construct a differential front-end stage with a gain of 64, followed by gain stage A3 (Gain = 1 or 2). The PGA inputs are equipped with an EMI filter, as shown in Figure 18. The cutoff frequency of the EMI filter is 19.6MHz. By using AVDD as the reference input, the bipolar input ranges from -39mV to $+39\text{mV}$ (Gain = 64) or -19.5mV to $+19.5\text{mV}$ (Gain = 128), and the unipolar input ranges from 0mV to $+39\text{mV}$ (Gain =

64) or 0mV to $+19.5\text{mV}$ (Gain = 128). The inputs of the ADS1230 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry.

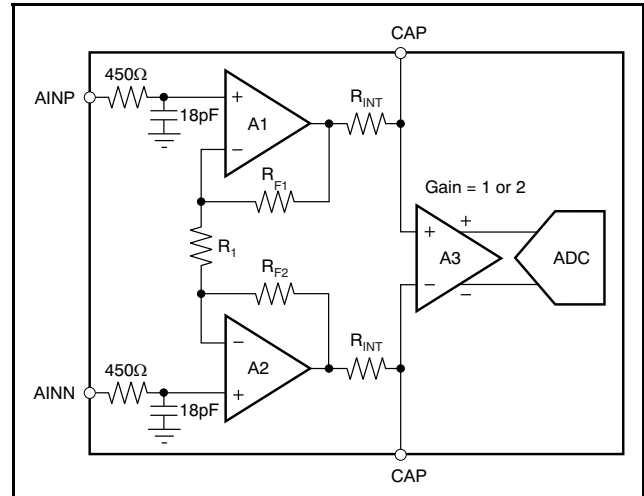


Figure 18. Simplified Diagram of the PGA

Bypass Capacitor

By applying a $0.1\mu\text{F}$ external capacitor (C_{EXT}) across two capacitor pins combined with the internal $2\text{k}\Omega$ resistor R_{INT} (on-chip), a low-pass filter with a corner frequency of 720Hz is created to bandlimit the signal path before the modulator input. This low-pass filter serves two purposes. First, the input signal is bandlimited to prevent aliasing as well as to filter out the high-frequency noise. Second, it attenuates the chopping residue from the amplifier to improve temperature drift performance. It is not required to use high-quality capacitors (such as ceramic or tantalum capacitors) for a general application. However, high-quality capacitors such as poly are recommended for high-linearity applications.

VOLTAGE REFERENCE INPUTS (REFP, REFN)

The voltage reference used by the modulator is generated from the voltage difference between REFP and REFN: $V_{REF} = REFP - REFN$. The reference inputs use a structure similar to that of the analog inputs. In order to increase the reference input impedance, a switching buffer circuitry is used to reduce the input equivalent capacitance. A simplified diagram of the circuitry on the reference inputs is shown in Figure 19. The switches and capacitors can be modeled with an effective impedance of:

$$Z_{EFF} = \frac{1}{2f_{MOD}C_{BUF}}$$

Where:

f_{MOD} = modulator sampling frequency (76.8kHz)

C_{BUF} = input capacitance of the buffer

For the ADS1230:

$$Z_{EFF} = \frac{1}{(2)(76.8kHz)(32.5fF)} = 200M\Omega$$

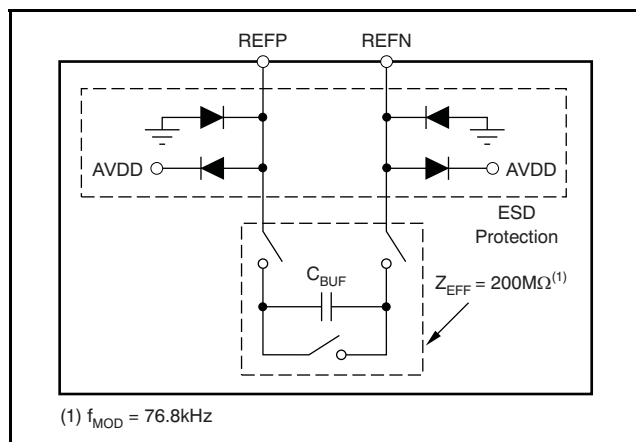


Figure 19. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise, do not exceed AVDD by 100mV:

$$GND - 100mV < (REFP \text{ or } REFN) < AVDD + 100mV$$

CLOCK SOURCES

The ADS1230 can use an external clock source or internal oscillator to accommodate a wide variety of applications. Figure 20 shows the equivalent circuitry of the clock source. The CLK_DETECT block determines whether the crystal oscillator/external clock signal is applied to the CLKIN pin so that the internal oscillator is bypassed or activated. When the CLKIN pin frequency is above ~200kHz, the CLK_DETECT output goes low and shuts down the internal oscillator. When the CLKIN pin frequency is below ~200kHz, the CLK_DETECT output goes high and activates the internal oscillator. It is highly recommended to hard-wire the CLKIN pin to ground when the internal oscillator is chosen.

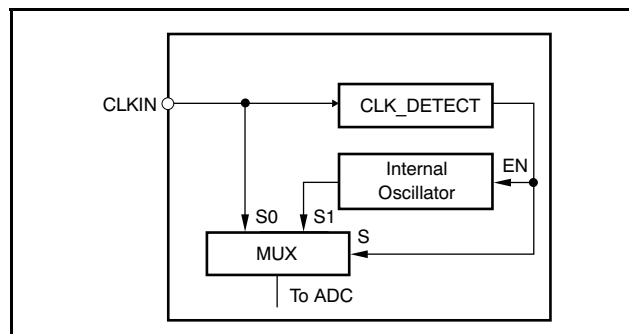


Figure 20. Equivalent Circuitry of the Clock Source

An external clock may be used by driving the CLKIN pin directly. The [Electrical Characteristics table](#) shows the allowable frequency range. The clock input may be driven with 5V logic, regardless of the DVDD or AVDD voltage.

FREQUENCY RESPONSE

The ADS1230 uses a sinc⁴ digital filter with the frequency response ($f_{CLK} = 4.9152\text{MHz}$) shown in Figure 21. The frequency response repeats at multiples of the modulator sampling frequency of 76.8kHz. The overall response is that of a low-pass filter with a -3dB cutoff frequency of 3.32Hz with the SPEED pin tied low (10SPS data rate) and 11.64Hz with the SPEED pin tied high (80SPS data rate).

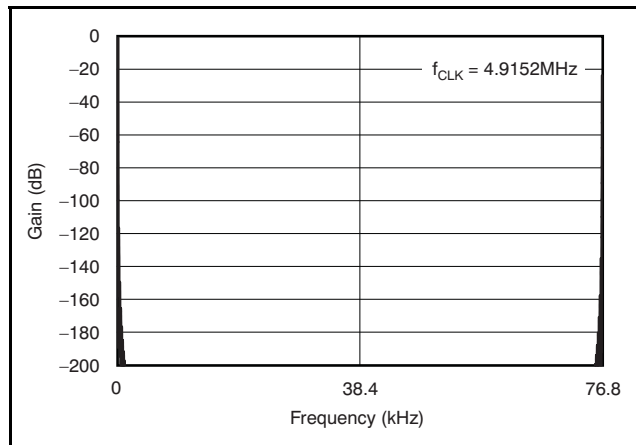


Figure 21. Frequency Response

To help see the response at lower frequencies, Figure 22(a) illustrates the response out to 100Hz, when the data rate = 10SPS. Notice that signals at multiples of 10Hz are rejected, and therefore simultaneous rejection of 50Hz and 60Hz is achieved.

The benefit of using a sinc⁴ filter is that every frequency notch has four zeros on the same location. This response, combined with the low drift internal oscillator, provides an excellent normal-mode rejection of line-cycle interference.

Figure 22(b) shows the same plot, but zooms in on the 50Hz and 60Hz notches with the SPEED pin tied low (10SPS data rate). With only a ±3% variation of the internal oscillator, over 100dB of normal-mode rejection is achieved.

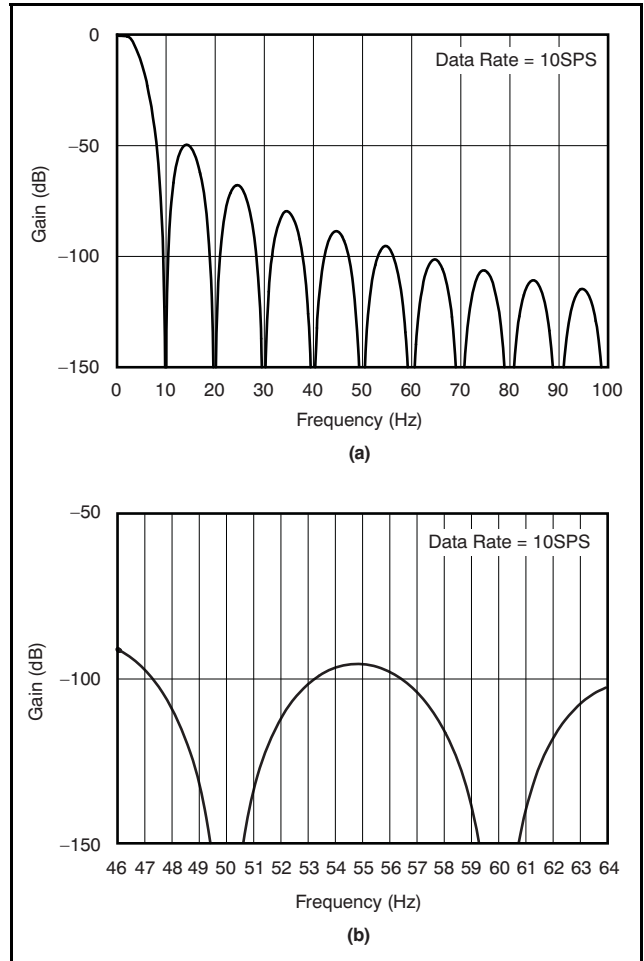


Figure 22. Frequency Response Out To 100Hz

The ADS1230 data rate and frequency response scale directly with clock frequency. For example, if f_{CLK} increases from 4.9152MHz to 6.144MHz when the SPEED pin is tied high, the data rate increases from 80SPS to 100SPS, while notches also increase from 80Hz to 100Hz. Note that these changes are only possible when the external clock source is applied.

SETTLING TIME

In certain instances, large changes in input will require settling time. For example, an external multiplexer in front of the ADS1230 can put large changes in input voltage by simply switching the multiplexer input channels. Abrupt changes in the input will require four data conversion cycles to settle. When continuously converting, five readings may be necessary in order to settle the data. If the change in input occurs in the middle of the first conversion, four more full conversions of the fully-settled input are required to get fully-settled data. Discard the first four readings because they contain only partially-settled data. Figure 23 illustrates the settling time for the ADS1230 in Continuous Conversion mode.

DATA RATE

The ADS1230 data rate is set by the SPEED pin, as shown in Table 3. When SPEED is low, the data rate is nominally 10SPS. This data rate provides the lowest noise, and also has excellent rejection of both 50Hz and 60Hz line-cycle interference. For applications requiring fast data rates, setting SPEED high selects a data rate of nominally 80SPS.

Table 3. Data Rate Settings

SPEED PIN	DATA RATE	
	Internal Oscillator or 4.9152MHz Crystal	External Oscillator
0	10SPS	$f_{CLKIN} / 491,520$
1	80SPS	$f_{CLKIN} / 61,440$

DATA FORMAT

The ADS1230 outputs 20 bits of data in binary two's complement format. The least significant bit (LSB) has a weight of $0.5V_{REF}/(2^{19} - 1)$. The positive full-scale input produces an output code of 7FFFFh and the negative full-scale input produces an output code of 80000h. The output clips at these codes for signals exceeding full-scale. Table 4 summarizes the ideal output codes for different input signals.

The ADS1230 is a 20-bit ADC. After data conversion is completed, applying 20 SCLKs retrieves 20 bits of data (MSB first). However, if the SCLKs continue to be applied after 20 bits of data are retrieved, the DOUT pin outputs four 1s for the 21st through the 24th SCLK, as shown in Figure 24.

Table 4. Ideal Output Code vs Input Signal⁽¹⁾

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT
$\geq +0.5V_{REF}/Gain$	7FFFFh
$(+0.5V_{REF}/Gain)/(2^{19} - 1)$	00001h
0	00000h
$(-0.5V_{REF}/Gain)/(2^{19} - 1)$	FFFFFh
$\leq -0.5V_{REF}/Gain$	80000h

(1) Excludes effects of noise, INL, offset, and gain errors.

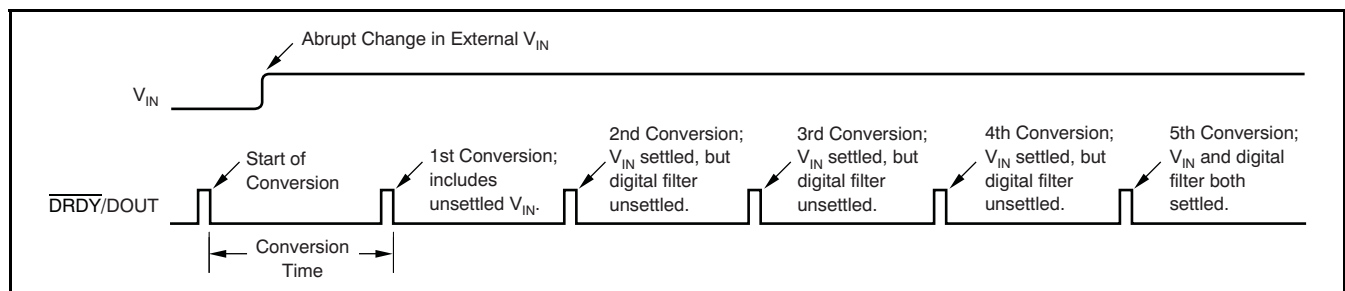


Figure 23. Settling Time in Continuous Conversion Mode

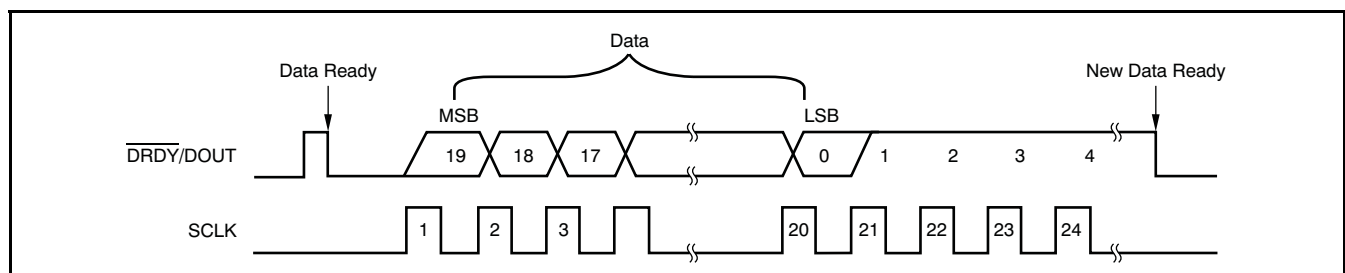


Figure 24. Data Retrieval Format

DATA READY/DATA OUTPUT ($\overline{\text{DRDY}}/\text{DOUT}$)

This digital output pin serves two purposes. First, it indicates when new data are ready by going low. Afterwards, on the first rising edge of SCLK, the $\overline{\text{DRDY}}/\text{DOUT}$ pin changes function and begins outputting the conversion data, most significant bit (MSB) first. Data are shifted out on each subsequent SCLK rising edge. After all 20 bits have been retrieved, the pin can be forced high with an additional SCLK. It then stays high until new data are ready. This configuration is useful when polling on the status of $\overline{\text{DRDY}}/\text{DOUT}$ to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. As with CLK, this input may be driven with 5V logic regardless of the DVDD or AVDD voltage. This input has built-in hysteresis, but care should still be taken to ensure a clean signal. Glitches or slow-rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise and fall times of SCLK are both less than 50ns.

DATA RETRIEVAL

The ADS1230 continuously converts the analog input signal. To retrieve data, wait until $\overline{\text{DRDY}}/\text{DOUT}$ goes low, as shown in [Figure 25](#). After $\overline{\text{DRDY}}/\text{DOUT}$ goes low, begin shifting out the data by applying SCLKs. Data are shifted out MSB first. It is not required to shift out all 20 bits of data, but the data must be retrieved before new data are updated (within t_{CONV}) or else the data will be overwritten. Avoid data retrieval during the update period (t_{UPDATE}). If 24 SCLKs have been applied, $\overline{\text{DRDY}}/\text{DOUT}$ will be high since the last four bits have been appended by '1'. However, if only 20 SCLKs have been applied, $\overline{\text{DRDY}}/\text{DOUT}$ remains at the state of the last bit shifted out until it is taken high (see t_{UPDATE}), indicating that new data are being updated. To avoid having $\overline{\text{DRDY}}/\text{DOUT}$ remain in the state of the last bit, the 21st SCLK can be applied to force $\overline{\text{DRDY}}/\text{DOUT}$ high, as shown in [Figure 26](#). This technique is useful when a host controlling the device is polling $\overline{\text{DRDY}}/\text{DOUT}$ to determine when data are ready.

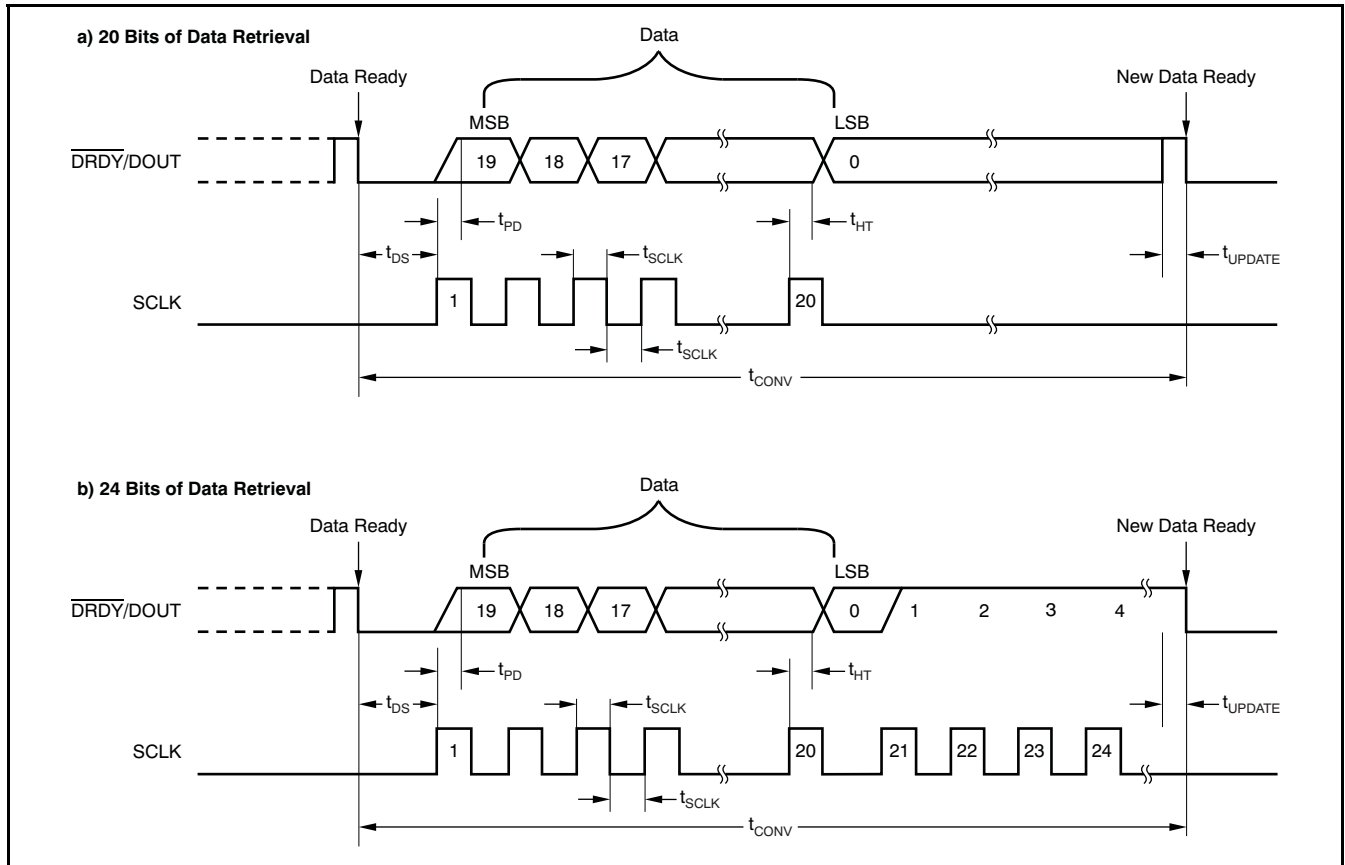


Figure 25. Data Retrieval Timing

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{DS}	DRDY/DOUT low to first SCLK rising edge	0			ns
t_{SCLK}	SCLK positive or negative pulse width	100			ns
t_{PD}	SCLK rising edge to new data bit valid: propagation delay			50	ns
t_{HT}	SCLK rising edge to old data bit valid: hold time	0			ns
$t_{UPDATE}^{(1)}$	Data updating: no readback allowed	39			μ s
$t_{CONV}^{(1)}$	Conversion time (1/data rate)	SPEED = 1	12.5		ms
		SPEED = 0	100		ms

(1) Value given for $f_{CLK} = 4.9152\text{MHz}$. For different f_{CLK} frequencies, scale proportional to CLK period.

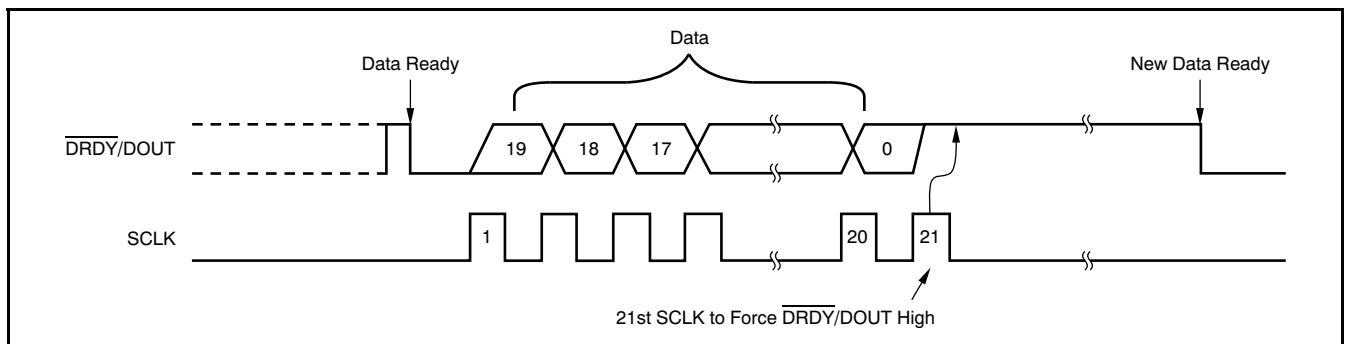


Figure 26. Data Retrieval with DRDY/DOUT Forced High Afterwards

OFFSET CALIBRATION

Offset calibration can be initiated at any time to remove the ADS1230 inherited offset error. To initiate offset calibration, apply at least two additional SCLKs after retrieving 20 bits of data plus four bits of '1'. Figure 27 shows the timing pattern. The 25th SCLK keeps $\overline{\text{DRDY}}/\text{DOUT}$ high. The falling edge of the 26th SCLK begins the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK; however, activity on SCLK should be minimized during offset calibration for best results.

During this time, the analog input pins are disconnected within the ADC and the appropriate signal is applied internally to perform the calibration. When the calibration is completed, $\overline{\text{DRDY}}/\text{DOUT}$ goes low, indicating that new data are ready. The first conversion after a calibration is fully settled and valid for use. The offset calibration takes exactly the same time as specified in (t_{CAL}) immediately after the falling edge of the 26th SCLK.

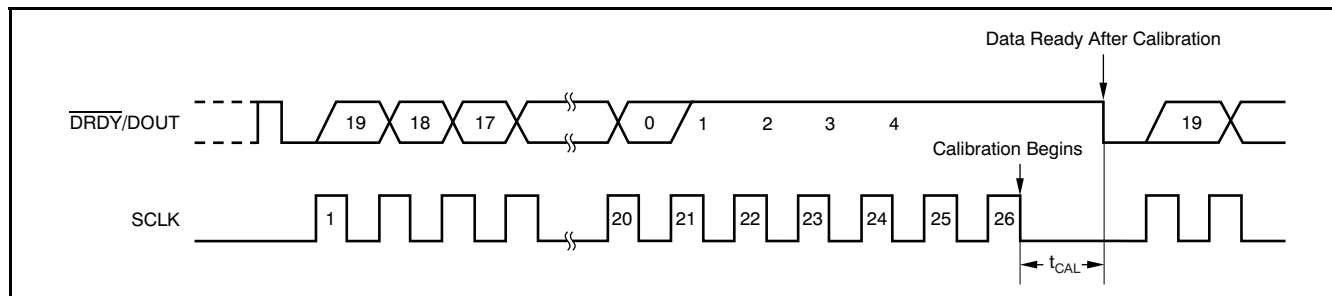


Figure 27. Offset-Calibration Timing

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
$t_{\text{CAL}}^{(1)}$	First data ready after calibration	SPEED = 1	101.28	101.29	ms
		SPEED = 0	801.02	801.03	ms

(1) Value given for $f_{\text{CLK}} = 4.9152\text{MHz}$. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a $\pm 3\%$ variation when an internal oscillator is used.

STANDBY MODE

Standby mode dramatically reduces power consumption by shutting down most of the circuitry. In Standby mode, the entire analog circuitry is powered down and only the clock source circuitry is awake to reduce the wake-up time from the Standby mode. To enter Standby mode, simply hold SCLK high after $\overline{\text{DRDY}}/\text{DOUT}$ goes low; see Figure 28. Standby mode can be initiated at any time during readback; it is not necessary to retrieve all 20 bits of data beforehand.

When t_{STANDBY} has passed with SCLK held high, Standby mode activates. $\overline{\text{DRDY}}/\text{DOUT}$ stays high when Standby mode begins. SCLK must remain high to stay in Standby mode. To exit Standby mode (wakeup), set SCLK low. The first data after exiting Standby mode is valid.

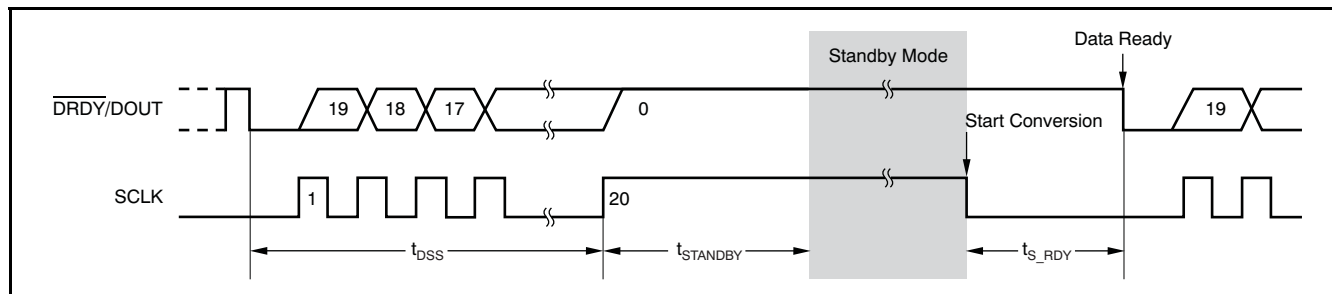


Figure 28. Standby Mode Timing (can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
$t_{\text{DSS}}^{(1)}$	SCLK high after $\overline{\text{DRDY}}/\text{DOUT}$ goes low to activate Standby mode	SPEED = 1	0	12.44	ms
		SPEED = 0	0	99.94	ms
$t_{\text{STANDBY}}^{(1)}$	Standby mode activation time	SPEED = 1	20		μs
		SPEED = 0	20		μs
$t_{\text{S_RDY}}^{(1)}$	Data ready after exiting Standby mode	SPEED = 1	52.51	52.51	ms
		SPEED = 0	401.8	401.8	ms

(1) Value given for $f_{\text{CLK}} = 4.9152\text{MHz}$. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a $\pm 3\%$ variation when an internal oscillator is used.

STANDBY MODE WITH OFFSET-CALIBRATION

Offset-calibration can be set to run immediately after exiting Standby mode. This option is useful when the ADS1230 is put in Standby mode for long periods of time, and offset-calibration is desired afterwards to compensate for temperature or supply voltage changes.

To force an offset-calibration with Standby mode, shift 25 SCLKs and bring the SCLK pin high to enter Standby mode. Offset-calibration then begins after wake-up; [Figure 29](#) shows the appropriate timing. Note the extra time needed after wake-up for calibration before data are ready. The first data after Standby mode with offset-calibration is fully settled and can be used right away.

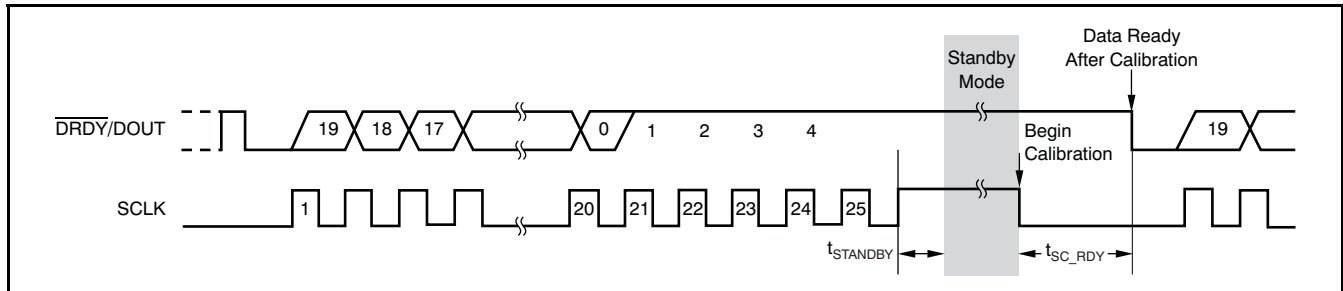


Figure 29. Standby Mode with Offset-Calibration Timing (can be used for single conversions)

SYMBOL	DESCRIPTION		MIN	MAX	UNITS
t _{SC_RDY} ⁽¹⁾	Data ready after exiting Standby mode and calibration	SPEED = 1	103	103	ms
		SPEED = 0	803	803	ms

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

POWER-DOWN MODE

Power-Down mode shuts down the entire ADC circuitry and reduces the total power consumption close to zero. To enter Power-Down mode, simply hold the PDWN pin low. Power-Down mode also resets the entire circuitry to free the ADC circuitry

from locking up to an unknown state. Power-Down mode can be initiated at any time during readback; it is not necessary to retrieve all 20 bits of data beforehand. Figure 30 shows the wake-up timing from Power-Down mode.

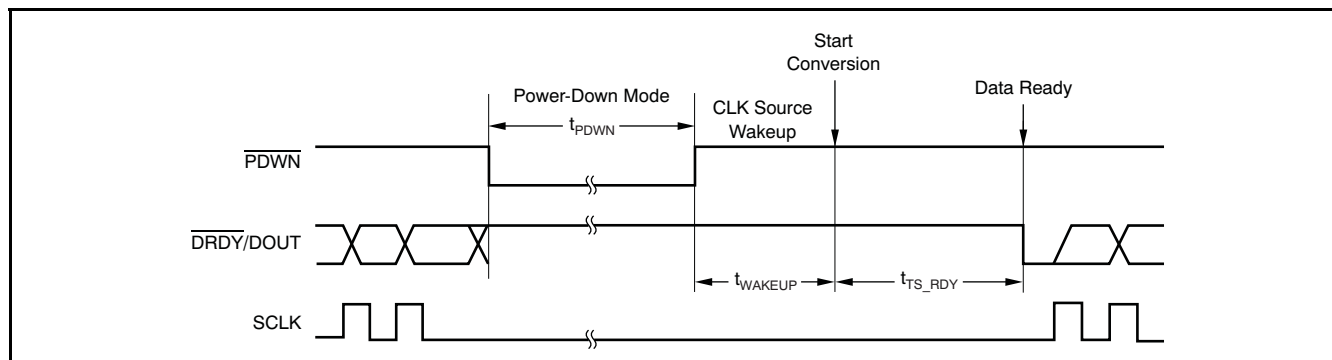


Figure 30. Wake-Up Timing from Power-Down Mode

SYMBOL	DESCRIPTION	MIN	TYP	UNITS
t _{WAKEUP}	Wake-up time after Power-Down mode	Internal clock	7.95	μs
		External clock	0.16	μs
t _{PDWN} ⁽¹⁾	PDWN pulse width	26		μs

(1) Value given for f_{CLK} = 4.9152MHz. For different f_{CLK} frequencies, scale proportional to CLK period. Expect a ±3% variation when an internal oscillator is used.

APPLICATION EXAMPLES

Weigh Scale System

Figure 31 shows a typical ADS1230 hook-up as part of a weigh scale system. In this setup, the ADS1230 is configured at a 10SPS data rate. Note that the internal oscillator is used by grounding the CLKIN pin. The user can also apply a 4.9152MHz clock to the CLKIN pin. For a typical 2mV/V load cell, the maximum output signal is approximately 10mV for a single +5V excitation voltage. The ADS1230 can achieve 17.5 noise-free bits at 10SPS when PGA = 128. With the extra software filtering/averaging (typically done by a microprocessor), an extra bit can be expected.

$$\text{Noise-Free Counts} = (2^{\text{BIT}_{\text{EFF}}}) \left(\frac{\text{FS}_{\text{LC}}}{\text{FS}_{\text{AD}}} \right)$$

Where:

BIT_{EFF} = effective noise-free bits (17.5 + 1 bit from software filtering/averaging)

FS_{LC} = full-scale output of the load cell (10mV)

FS_{AD} = full-scale input of the ADS1230 (39mV, when PGA = 128)

Therefore:

$$\text{Noise-Free Counts} = (2^{(17.5+1)}) \left(\frac{10\text{mV}}{39\text{mV}} \right) = 95,058$$

With +5V supply voltage, 95,058 noise-free counts can be expected from the ADS1230.

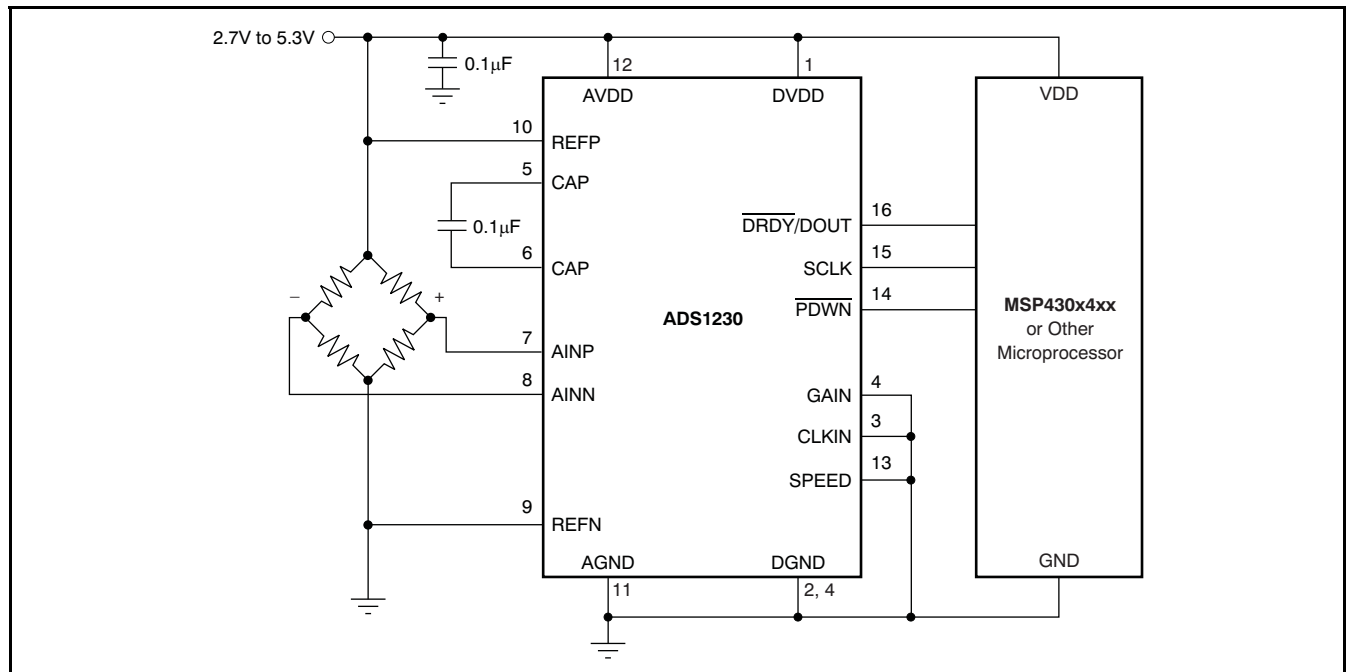


Figure 31. Weigh Scale Application

SUMMARY OF SERIAL INTERFACE WAVEFORMS

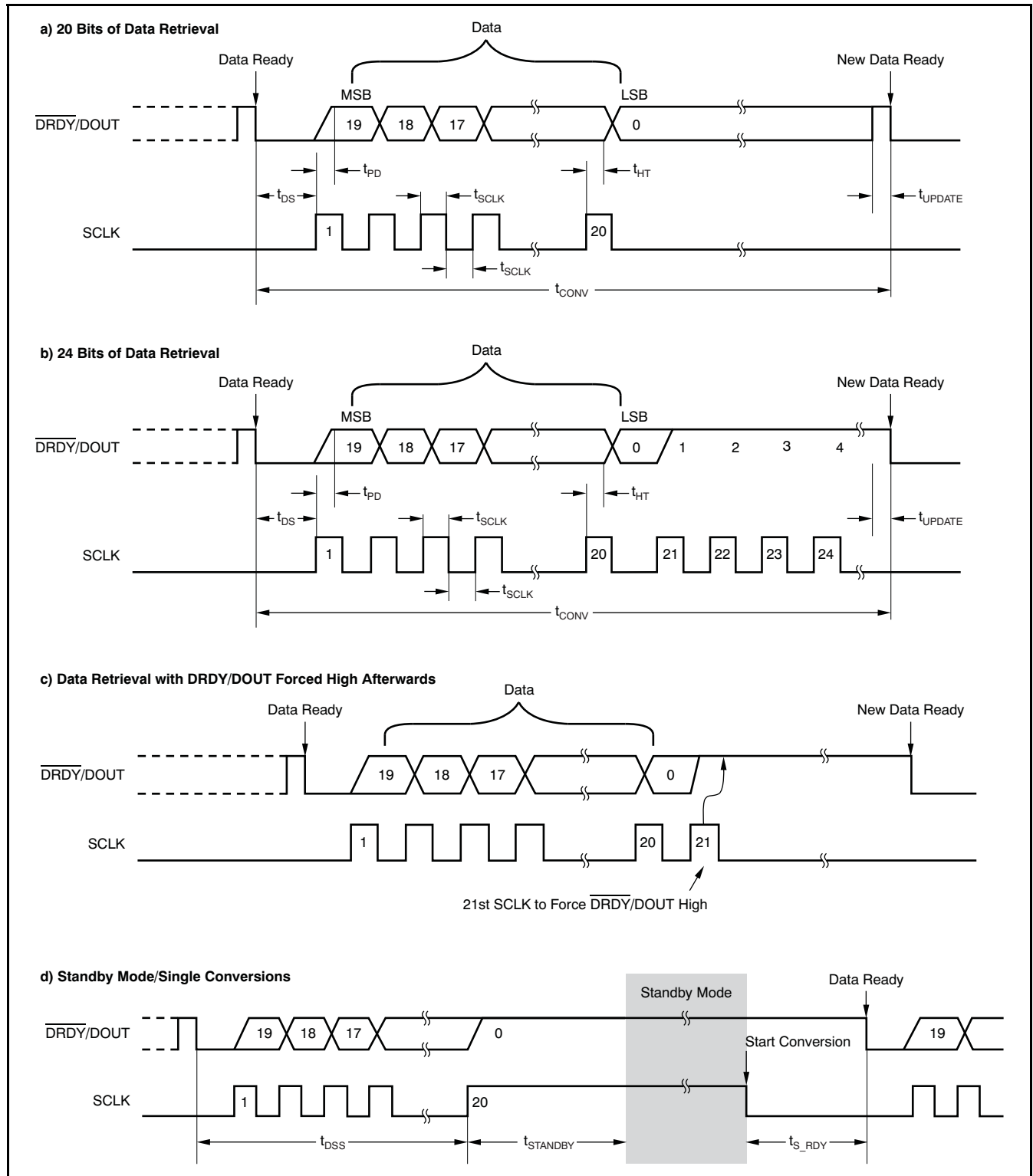


Figure 32. Summary of Data Retrieval Waveforms

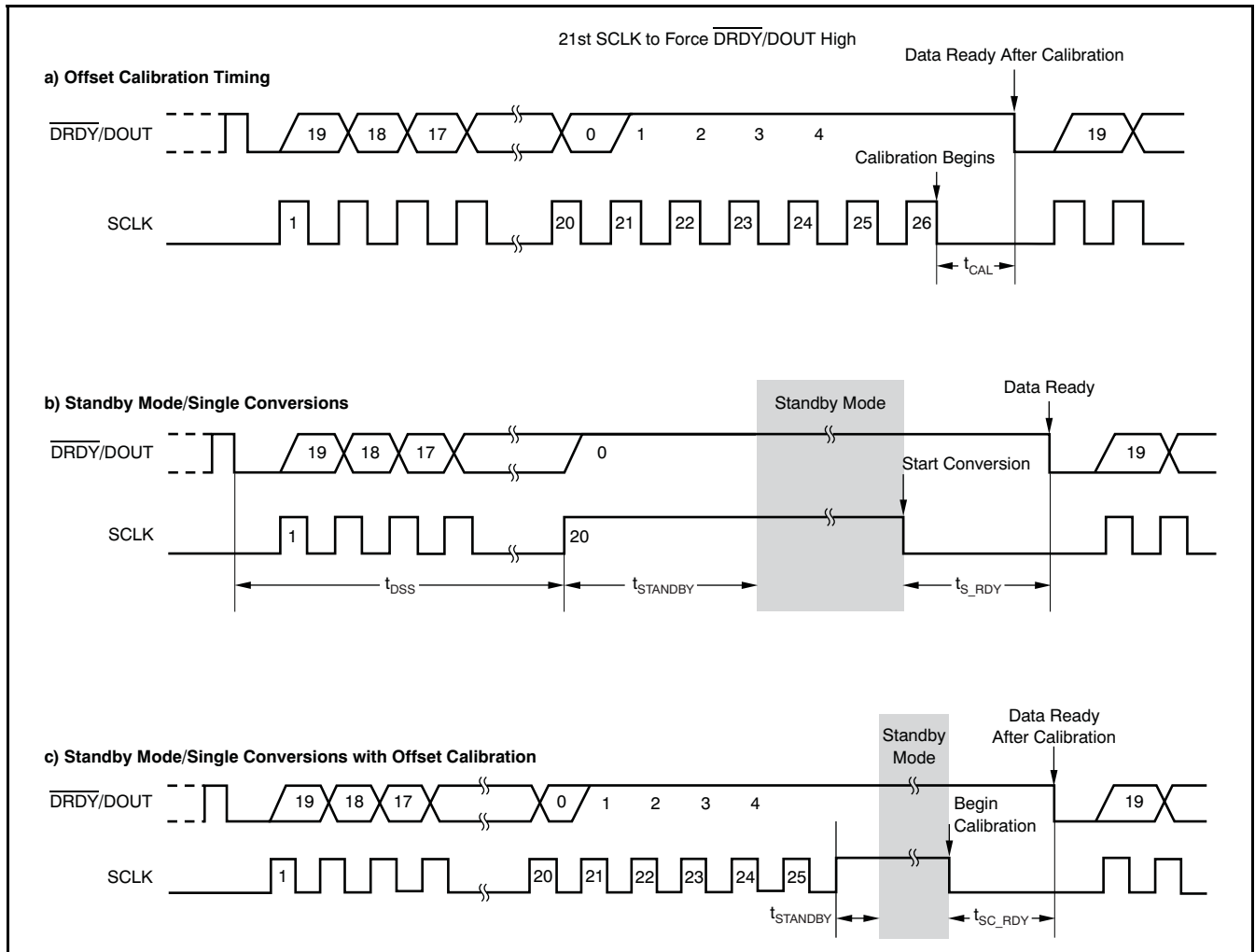


Figure 33. Summary of Standby Mode and Calibration Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ADS1230IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1230IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265