# ADS1235-Q1 Automotive Precision, 3-Channel, Differential-Input, 7200-SPS, 24-Bit Delta-Sigma ADC for Bridge Sensors

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, $T_A$
- 24-bit, high-precision ADC:
  - 120,000 noise-free counts (10-mV input, 10 SPS)
  - Offset drift: 1 nV/°C
  - Gain drift: 0.5 ppm/°C
- Three differential or five single-ended inputs
- Two reference inputs
- Wide input voltage range: ±7 mV to ±5 V
- Low-noise PGA, gain: 1, 64, and 128
- Data rate: 2.5 SPS to 7200 SPS
- AC- or DC-bridge excitation option
- Chop mode for zero-drift operation
- Simultaneous 50-Hz and 60-Hz rejection mode
- Single-cycle settling mode
- Missing reference input monitor
- Signal overrange monitor
- Temperature sensor
- Cyclic redundancy check (CRC)
- 5-V or ±2.5-V power supply

## 2 Applications

- On-board weighing systems (OBW)
- Weigh scales and strain-gauge digitizers
- Dynamic weigh systems
- Pressure measurement

## 3 Description

The ADS1235-Q1 is a precision, 7200-SPS, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with an integrated programmable gain amplifier (PGA). This device also includes diagnostic features such as PGA overrange and reference monitors. The ADC provides high-accuracy, zero-drift conversion data for high-precision equipment, including weigh scales, strain gauges, and resistive pressure sensors.

The ADC has signal and reference multiplexers that support three differential signal inputs and two reference inputs. The ADC also includes a low-noise PGA that provides gains of 1, 64, and 128. The ADC also has a 24-bit ΔΣ modulator and programmable digital filter.

The high-impedance inputs (1 GΩ) of the PGA reduce measurement error that is caused by sensor loading.

The ADC supports ac-bridge excitation to remove the drift errors from the sensor wiring. The ADC provides the clock control signals for the ac-excitation operation.

The flexible digital filter is programmable for single-cycle settled conversions, and provides 50-Hz and 60-Hz line cycle rejection at the same time.

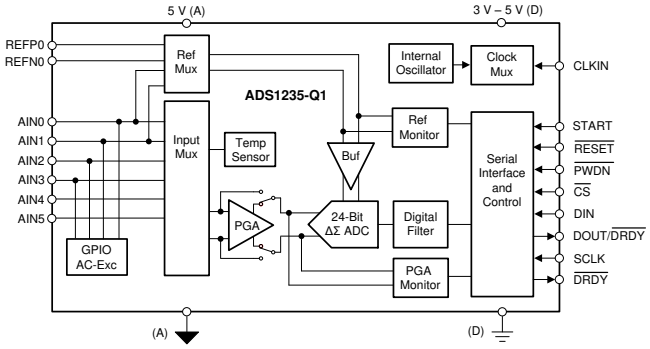
The ADS1235-Q1 is available in a 5-mm × 5-mm VQFN package, and is specified across the –40°C to +125°C temperature range.

**Device Information**(1)

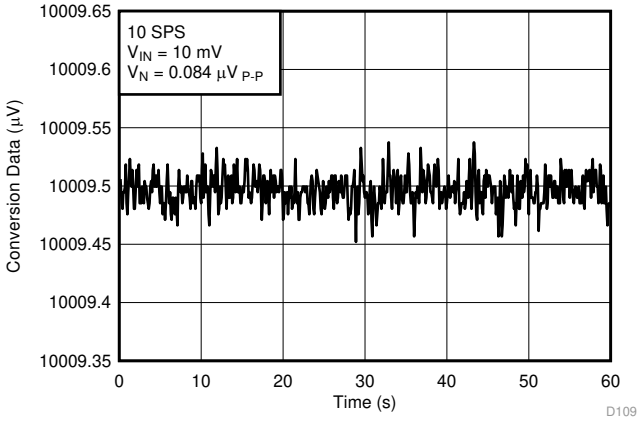
| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|---|---|---|
| ADS1235-Q1 | VQFN (32) | 5.0 mm × 5.0 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

**Block Diagram**




**ADC Conversion Noise**



# Table of Contents



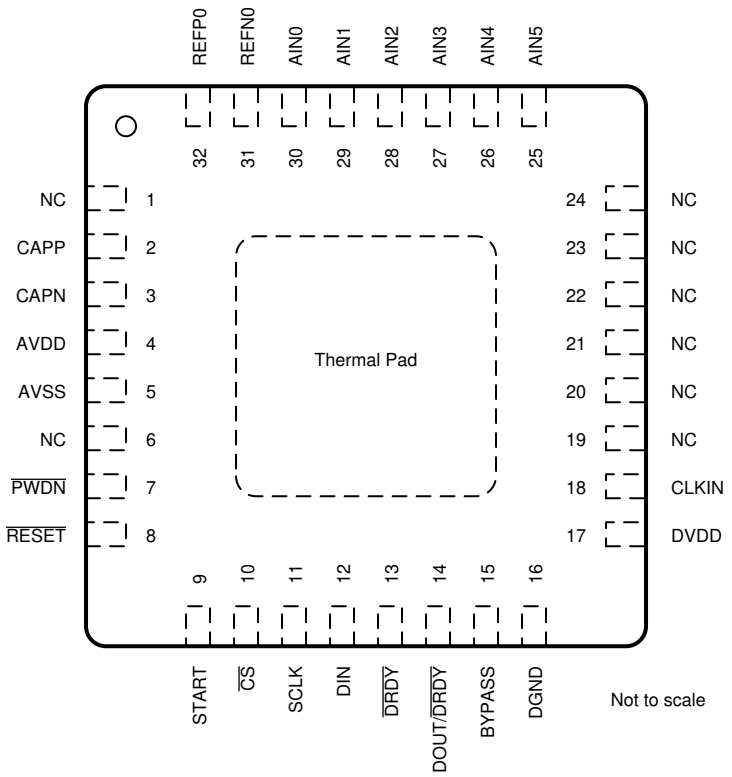
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| October 2019 | * | Initial release. |

# 5 Pin Configuration and Functions

**RHM Package**
**VQFN-32**
**Top View**




**Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | NC | — | No connection; float or connect to AVSS |
| 2 | CAPP | Analog output | PGA output P; connect a 4.7-nF C0G dielectric capacitor across CAPP and CAPN |
| 3 | CAPN | Analog output | PGA output N; connect a 4.7-nF C0G dielectric capacitor across CAPP and CAPN |
| 4 | AVDD | Analog | Positive analog power supply |
| 5 | AVSS | Analog | Negative analog power supply |
| 6 | NC | — | No connection - solder the pin for mechanical support, float or connect to DGND |
| 7 | $\overline{\text{PWDN}}$ | Digital input | Power down, active low |
| 8 | $\overline{\text{RESET}}$ | Digital input | Reset, active low |
| 9 | START | Digital input | Start conversion control, active high |
| 10 | $\overline{\text{CS}}$ | Digital input | Serial interface chip select, active low |
| 11 | SCLK | Digital Input | Serial interface shift clock |
| 12 | DIN | Digital Input | Serial interface data input |
| 13 | $\overline{\text{DRDY}}$ | Digital output | Data ready indicator, active low |
| 14 | DOUT/$\overline{\text{DRDY}}$ | Digital output | Dual function serial interface data output and active-low data ready indicator |
| 15 | BYPASS | Analog output | Internal subregulator bypass; connect a 1-µF capacitor to DGND |
| 16 | DGND | Digital | Digital ground |
| 17 | DVDD | Digital | Digital power supply |
| 18 | CLKIN | Digital input | 1) Internal oscillator: connect to DGND, 2) External clock: connect clock input |
| 19-24 | NC | — | No connection - solder the pin for mechanical support, float or connect to DGND |

**Pin Functions (continued)**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 25 | AIN5 | Analog input | Analog input 5 |
| 26 | AIN4 | Analog input | Analog input 4 |
| 27 | AIN3 | Analog input/output | Analog input 3, GPIO3, ACX2 |
| 28 | AIN2 | Analog input/output | Analog input 2, GPIO2, ACX1 |
| 29 | AIN1 | Analog input/output | Analog input 1, GPIO1, $\overline{\text{ACX2}}$, Reference input 1 negative |
| 30 | AIN0 | Analog input/output | Analog input 0, GPIO0, $\overline{\text{ACX1}}$, Reference input 1 positive |
| 31 | REFN0 | Analog input/output | Reference input 0 negative |
| 32 | REFP0 | Analog input/output | Reference input 0 positive |
| — | Thermal Pad | — | Exposed thermal pad - solder the pad for mechanical support; connect to AVSS. |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

see (1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Power supply voltage | AVDD to AVSS | –0.3 | 7 | V |
| | AVSS to DGND | –3 | 0.3 | |
| | DVDD to DGND | –0.3 | 7 | |
| Analog input voltage | AINx, REFP0, REFN0 | AVSS – 0.3 | AVDD + 0.3 | V |
| Digital input voltage | $\overline{\text{CS}}$, SCLK, DIN, DOUT/$\overline{\text{DRDY}}$, $\overline{\text{DRDY}}$, START, $\overline{\text{RESET}}$, $\overline{\text{PWDN}}$, CLKIN | DGND – 0.3 | DVDD + 0.3 | V |
| Input Current | Continuous, all pins except power-supply pins (2) | –10 | 10 | mA |
| Temperature | Junction, $T_J$ | | 150 | °C |
| | Storage, $T_{stg}$ | –60 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input and output pins are diode-clamped to the internal power supplies. Limit the input current to 10 mA in the event the analog input voltage exceeds AVDD + 0.3 V or AVSS – 0.3 V, or if the digital input voltage exceeds DVDD + 0.3 V or DGND – 0.3 V.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 (1)<br>HBM ESD classification level 2 | | ±2000 | V |
| | | Charged-device model (CDM), per AEC Q100-011<br>CDM ESD classification level C4B | Corner pins | ±750 | |
| | | | All other non-corner pins | ±500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | |
| | Analog power supply | AVDD to AVSS | 4.75 | 5 | 5.25 | V |
| | | AVSS to DGND | –2.6 | | 0 | |
| | Digital power supply | DVDD to DGND | 2.7 | | 5.25 | V |
| **ANALOG INPUTS** | | | | | | |
| $V_{(AINx)}$ | Absolute input voltage | PGA mode | See Equation 3 | | | V |
| | | PGA bypassed | AVSS – 0.1 | | AVDD + 0.1 | |
| $V_{IN}$ | Differential input voltage | $V_{IN} = V_{AINP} – V_{AINN}$ | | $\pm V_{REF}$ / Gain | See (1) | V |
| **VOLTAGE REFERENCE INPUTS** | | | | | | |
| $V_{REF}$ | Differential reference voltage | $V_{REF} = V_{(REFPx)} – V_{(REFNx)}$ | 0.9 | | AVDD – AVSS | V |
| $V_{(REFNx)}$ | Negative reference voltage | | AVSS – 0.05 | | $V_{(REFPx)}$ – 0.9 | V |
| $V_{(REFPx)}$ | Positive reference voltage | | $V_{(REFNx)}$ + 0.9 | | AVDD + 0.05 | V |
| **EXTERNAL CLOCK** | | | | | | |
| $f_{CLK}$ | Frequency | | 1 | 7.3728 | 8 | MHz |
| | Duty cycle | | 40% | | 60% | |
| **GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)** | | | | | | |
| | Input voltage | | AVSS | | AVDD | V |
| **DIGITAL INPUTS (other than GPIOs)** | | | | | | |
| | Input voltage | | DGND | | DVDD | V |
| **TEMPERATURE** | | | | | | |
| $T_A$ | Operating ambient temperature | | –40 | | 125 | °C |

(1) In PGA mode, the maximum differential input voltage is ±(AVDD – AVSS – 0.6 V) / Gain, when operating with $V_{REF} \geq$ AVDD – AVSS – 0.6 V

## 6.4 Thermal Information

| THERMAL METRIC (1) | | ADS1235-Q1 RHM (VQFN) 32 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 29.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 17.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 9.8 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.2 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 9.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.1 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

minimum and maximum specifications apply from $T_A$ = –40°C to +125°C; typical specifications are at $T_A$ = 25°C; all specifications at AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, $f_{CLK}$ = 7.3728 MHz, PGA mode, gain = 1, and data rate = 20 SPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ANALOG INPUTS** | | | | | | |
| | Absolute input current | PGA mode, $V_{(AINx)}$ = 2.5 V | | 4 | 12 | nA |
| | | PGA bypass | | 200 | | |
| | Absolute input current drift | | | 0.01 | | nA/°C |
| | Differential input current | PGA mode, $V_{IN}$ = 39 mV | | ±0.1 | | nA |
| | | PGA mode, $V_{IN}$ = 2.5 V | –8 | ±1 | 8 | |
| | | PGA and chop modes, $V_{IN}$ = 2.5 V(1) | | ±5 | | |
| | | PGA bypass, $V_{IN}$ = 2.5 V | | ±40 | | |
| | Differential input current drift | | | 0.05 | | nA/°C |
| | Differential input impedance | PGA mode | | 1 | | GΩ |
| | | PGA bypass | | 50 | | MΩ |
| | Crosstalk | | | 0.1 | | µV/V |
| **PGA** | | | | | | |
| | Gain settings | | | 1, 64, 128 | | V/V |
| | Antialias filter frequency | $C_{CAPP, CAPN}$ = 4.7 nF | | 60 | | kHz |
| | Output voltage monitor | Low threshold | | AVSS + 0.2 | | V |
| | | High threshold | | AVDD – 0.2 | | |
| **PERFORMANCE** | | | | | | |
| | Resolution | No missing codes | 24 | | | Bits |
| | Equivalent input noise density | Gain = 64 and 128 | | 8 | | nV/√Hz |
| DR | Data rate | | 2.5 | | 7200 | SPS |
| | Noise performance | | | See Table 1 | | |
| INL | Integral non-linearity | Gain = 1, 64 and 128 | –10 | ±2 | 10 | $ppm_{FSR}$ |
| $V_{OS}$ | Offset voltage | $T_A$ = 25°C, gain = 1 | –355 | ±50 | 355 | µV |
| | | $T_A$ = 25°C, gain = 64 and 128 | –10 | ±1.5 | 10 | |
| | | $T_A$ = 25°C, gain = 1, chop mode | –0.6 | ±0.2 | 0.6 | |
| | | $T_A$ = 25°C, gain = 64 and 128, chop mode | –0.06 | ±0.005 | 0.06 | |
| | | After calibration | | On the level of noise | | |
| | Offset voltage drift | Gain = 1 | | 150 | 350 | nV/°C |
| | | Gain = 64 and 128 | | 15 | 75 | |
| | | Gain = 1, 64, and 128, chop mode | | 1 | 5 | |
| GE | Gain error | $T_A$ = 25°C | –0.6% | ±0.05% | 0.6% | |
| | | After calibration | | on the level of noise | | |
| | Gain drift | | | 0.5 | 4 | ppm/°C |
| NMRR | Normal-mode rejection ratio(2) | | | See Table 5 | | |
| CMRR | Common-mode rejection ratio(3) | Data rate = 20 SPS | | 130 | | dB |
| | | Data rate = 400 SPS | 105 | 115 | | |
| PSRR | Power-supply rejection ratio(4) | AVDD and AVSS | 85 | 100 | | dB |
| | | DVDD | 95 | 120 | | |
| **INTERNAL OSCILLATOR** | | | | | | |
| $f_{CLK}$ | Frequency | | | 7.3728 | | MHz |
| | Accuracy | | –2% | ±0.5% | 2% | |

(1) Chop-mode input current scales with data rate. See Figure 27 for chop mode input current at 20 SPS and 1200 SPS.
(2) Normal-mode rejection ratio performance depends on the digital filter configuration.
(3) Common-mode rejection ratio is specified at $f_{IN}$ = 60 Hz.
(4) Power-supply rejection ratio specified at dc.

## Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A$ = –40°C to +125°C; typical specifications are at $T_A$ = 25°C; all specifications at AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, $f_{CLK}$ = 7.3728 MHz, PGA mode, gain = 1, and data rate = 20 SPS (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **VOLTAGE REFERENCE INPUTS** | | | | | | |
| | Reference input current | | | 500 | | nA |
| | Input current vs voltage | | | 100 | | nA/V |
| | Input current drift | | | 0.1 | | nA/V/°C |
| | Input impedance | Differential | | 5 | | MΩ |
| | Low voltage monitor | Threshold low | | 0.4 | 0.6 | V |
| **TEMPERATURE SENSOR** | | | | | | |
| | Sensor voltage | $T_A$ = 25°C | | 122.4 | | mV |
| | Temperature coefficient | | | 420 | | µV/°C |
| **GENERAL-PURPOSE INPUTS/OUTPUTS (GPIOs)**(5) | | | | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = –1 mA | | | 0.2 · AVDD | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 1 mA | 0.8 · AVDD | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.3 · AVDD | V |
| $V_{IH}$ | High-level input voltage | | 0.7 · AVDD | | | V |
| | Input hysteresis | | | 0.5 | | V |
| **DIGITAL INPUTS/OUTPUTS (Other Than GPIOs)** | | | | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = –1 mA | | | 0.2 · DVDD | V |
| | | $I_{OL}$ = –8 mA | | 0.2 · DVDD | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 1 mA | 0.8 · DVDD | | | V |
| | | $I_{OH}$ = 8 mA | | 0.75 · DVDD | | |
| $V_{IL}$ | Low-level input voltage | | | | 0.3 · DVDD | V |
| $V_{IH}$ | High-level input voltage | | 0.7 · DVDD | | | V |
| | Input hysteresis | | | 0.1 | | V |
| | Input leakage | $V_{IH}$ or $V_{IL}$ | –10 | | 10 | µA |
| **POWER SUPPLY** | | | | | | |
| $I_{AVDD}$ $I_{AVSS}$ | Analog supply current | PGA bypass | | 2.7 | 4.5 | mA |
| | | PGA mode, gain = 64 and 128 | | 4.3 | 6.5 | |
| | | Power-down mode | | 2 | 8 | µA |
| $I_{DVDD}$ | Digital supply current | | | 0.4 | 0.7 | mA |
| | | Power-down mode(6) | | 30 | 75 | µA |
| $P_D$ | Power dissipation | PGA mode, gain = 64 and 128 | | 23 | 35 | mW |
| | | Power-down mode | | 0.1 | 0.3 | |

(5) GPIO voltage with respect to AVSS.
(6) CLKIN input stopped.

## 6.6 Timing Requirements

over operating ambient temperature range, DVDD = 2.7 V to 5.25 V, and DOUT/$\overline{\text{DRDY}}$ load: 20 pF || 100 kΩ to DGND (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| **SERIAL INTERFACE** | | | | |
| $t_{d(CSSC)}$ | Delay time, first SCLK rising edge after $\overline{\text{CS}}$ falling edge (1) | 50 | | ns |
| $t_{su(DI)}$ | Setup time, DIN valid before SCLK falling edge | 25 | | ns |
| $t_{h(DI)}$ | Hold time, DIN valid after SCLK falling edge | 25 | | ns |
| $t_{c(SC)}$ | SCLK period (2) | 97 | $10^6$ | ns |
| $t_{w(SCH)}$, $t_{w(SCL)}$ | Pulse duration, SCLK high or low | 40 | | ns |
| $t_{d(SCCS)}$ | Delay time, last SCLK falling edge before $\overline{\text{CS}}$ rising edge | 50 | | ns |
| $t_{w(CSH)}$ | Pulse duration, $\overline{\text{CS}}$ high to reset interface | 25 | | ns |
| $t_{d(SCIR)}$ | Delay time, SCLK high or low to force interface auto-reset | | 65540 | $1/f_{CLK}$ |
| **RESET** | | | | |
| $t_{w(RSTL)}$ | Pulse duration, $\overline{\text{RESET}}$ low | 4 | | $1/f_{CLK}$ |
| **CONVERSION CONTROL** | | | | |
| $t_{w(STH)}$ | Pulse duration, START high | 4 | | $1/f_{CLK}$ |
| $t_{w(STL)}$ | Pulse duration, START low | 4 | | $1/f_{CLK}$ |
| $t_{su(DRST)}$ | Setup time, START low or STOP command after $\overline{\text{DRDY}}$ low to stop next conversion (Continuous-conversion mode) | | 100 | $1/f_{CLK}$ |
| $t_{h(DRSP)}$ | Hold time, START low or STOP command after $\overline{\text{DRDY}}$ low to continue next conversion (Continuous-conversion mode) | 150 | | $1/f_{CLK}$ |

(1) $\overline{\text{CS}}$ can be tied low.
(2) Serial interface time-out mode: minimum SCLK frequency = 1 kHz. Otherwise, no minimum SCLK frequency.

## 6.7 Switching Characteristics

over operating ambient temperature range, DVDD = 2.7 V to 5.25 V, and DOUT/$\overline{\text{DRDY}}$ load: 20 pF || 100 kΩ to DGND (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **SERIAL INTERFACE** | | | | | |
| $t_{w(DRH)}$ | Pulse duration, $\overline{\text{DRDY}}$ high | 16 | | | $1/f_{CLK}$ |
| $t_{p(CSDO)}$ | Propagation delay time, $\overline{\text{CS}}$ falling edge to DOUT/$\overline{\text{DRDY}}$ driven | 0 | | 50 | ns |
| $t_{p(SCDO1)}$ | Propagation delay time, SCLK rising edge to valid DOUT/$\overline{\text{DRDY}}$ | | | 40 | ns |
| $t_{h(SCDO1)}$ | Hold time, SCLK rising edge to invalid data on DOUT/$\overline{\text{DRDY}}$ | 0 | | | ns |
| $t_{h(SCDO2)}$ | Hold time, last SCLK falling edge of operation to invalid data on DOUT/$\overline{\text{DRDY}}$ | 15 | | | ns |
| $t_{p(SCDO2)}$ | Propagation delay time, last SCLK falling edge to valid data ready function on DOUT/$\overline{\text{DRDY}}$ | | | 110 | ns |
| $t_{p(CSDOZ)}$ | Propagation delay time, $\overline{\text{CS}}$ rising edge to DOUT/$\overline{\text{DRDY}}$ high impedance | | | 50 | ns |
| **RESET** | | | | | |
| $t_{p(RSCN)}$ | Propagation delay time, $\overline{\text{RESET}}$ rising edge or RESET command to start of conversion | 512 | | | $1/f_{CLK}$ |
| $t_{p(PRCM)}$ | Propagation delay time, power-on threshold voltage to ADC communication | | $2^{16}$ | | $1/f_{CLK}$ |
| $t_{p(CMCN)}$ | Propagation delay time, ADC communication to conversion start | 512 | | | $1/f_{CLK}$ |
| **AC EXCITATION** | | | | | |
| $t_{d(ACX)}$ | Delay time, phase-to-phase blanking period | | 8 | | $1/f_{CLK}$ |
| $t_{c(ACX)}$ | ACX period | 2 | | | $t_{STDR}$ |
| **CONVERSION CONTROL** | | | | | |
| $t_{p(STDR)}$ | Propagation delay time, START high or START command to $\overline{\text{DRDY}}$ high | | | 2 | $1/f_{CLK}$ |

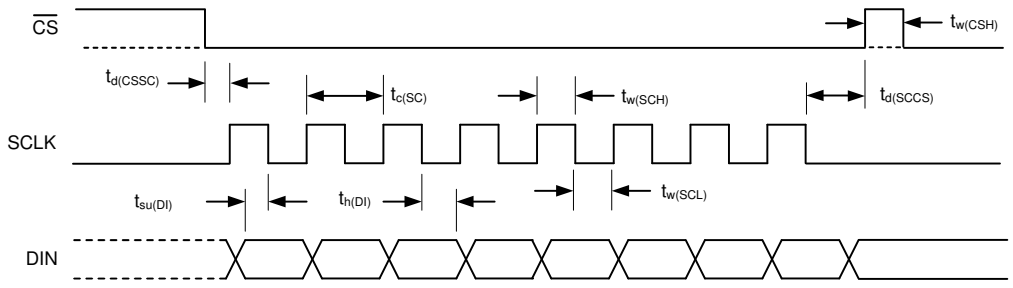
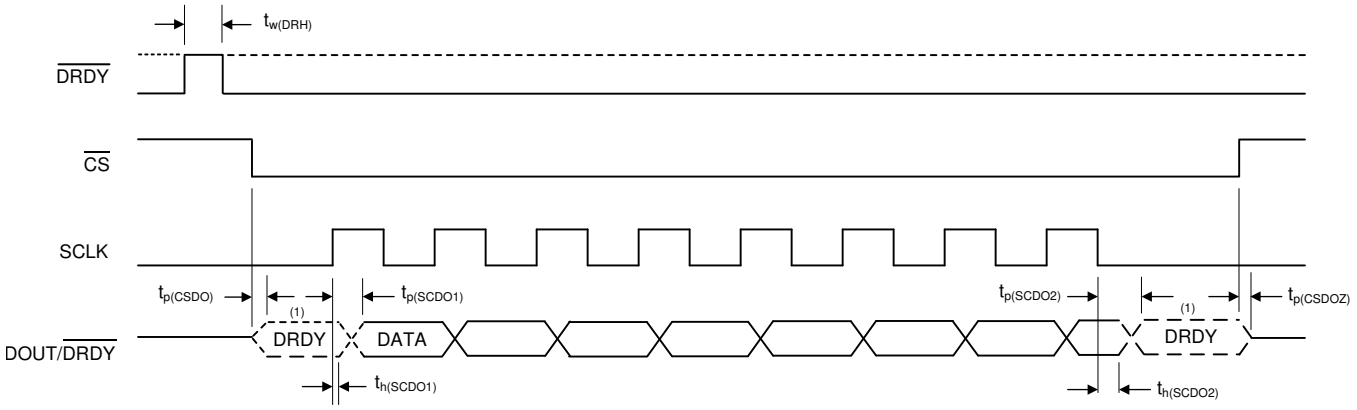



**Figure 1. Serial Interface Timing Requirements**




(1) Before the first SCLK rising edge and after the last SCLK falling edge of a command, the function of DOUT/$\overline{\text{DRDY}}$ is data ready.

**Figure 2. Serial Interface Switching Characteristics**

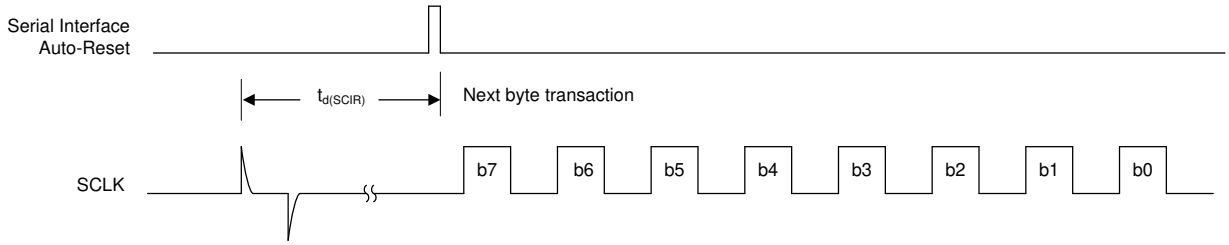



**Figure 3. Serial Interface Auto-Reset Characteristics**

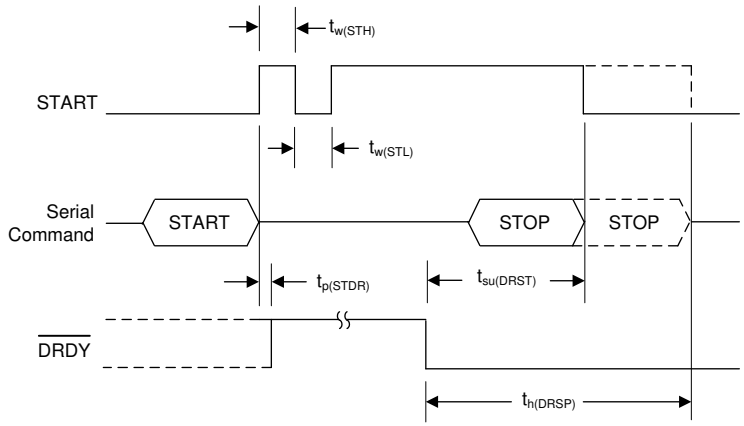



**Figure 4. Conversion Control Timing Requirements**

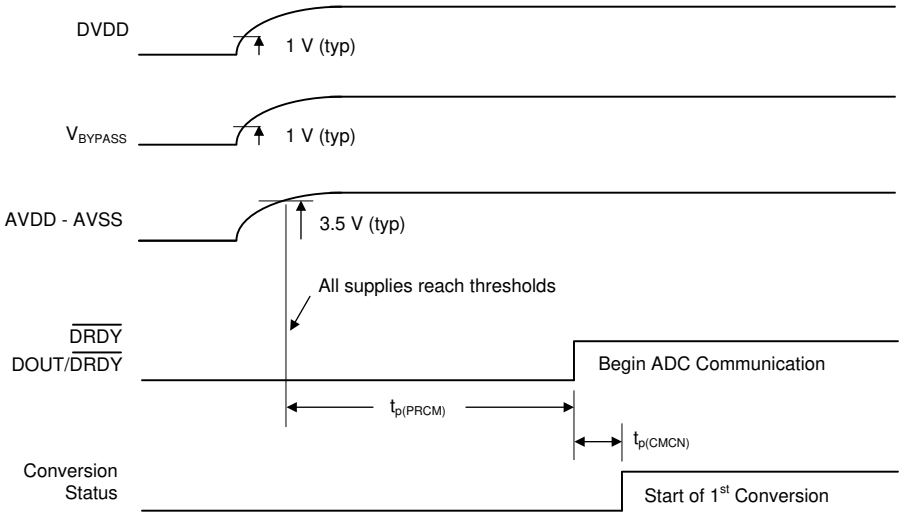



**Figure 5. Power-Up Characteristics**

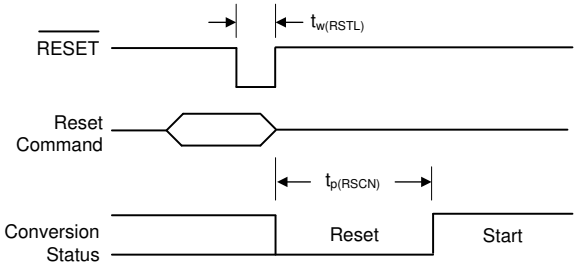



**Figure 6. $\overline{RESET}$ pin and RESET Command Timing Requirements**

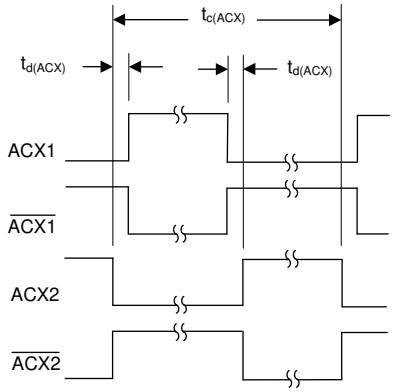



**Figure 7. AC-Excitation Switching Characteristics**

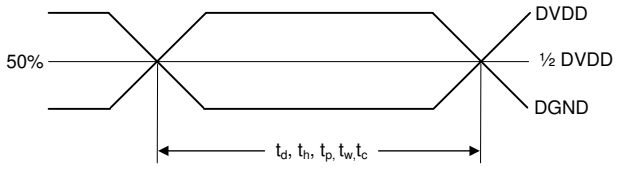
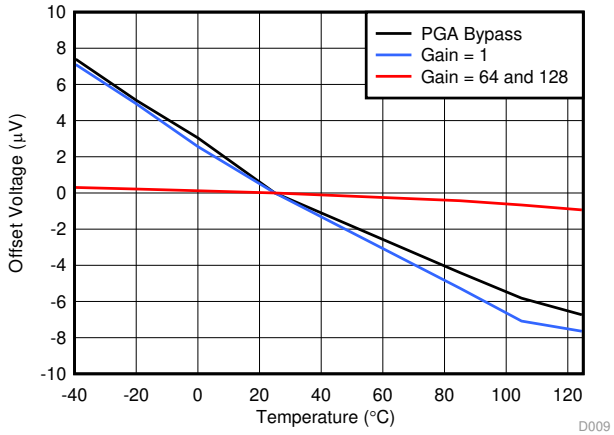



**Figure 8. Timing Voltage-Level Reference**

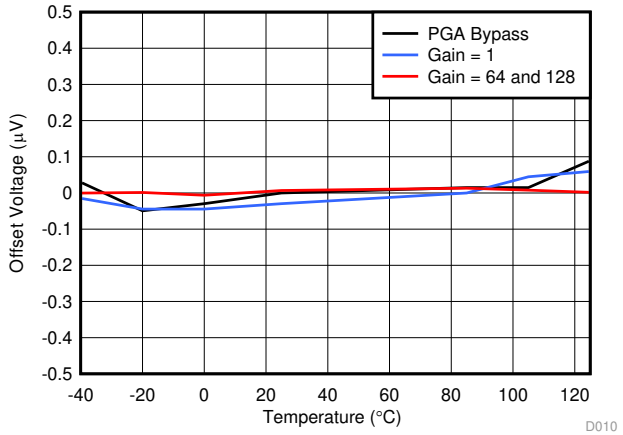
## 6.8 Typical Characteristics

at $T_A$ = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, data rate = 20 SPS, $f_{CLK}$ = 7.3728 MHz and gain = 128 (unless otherwise noted)



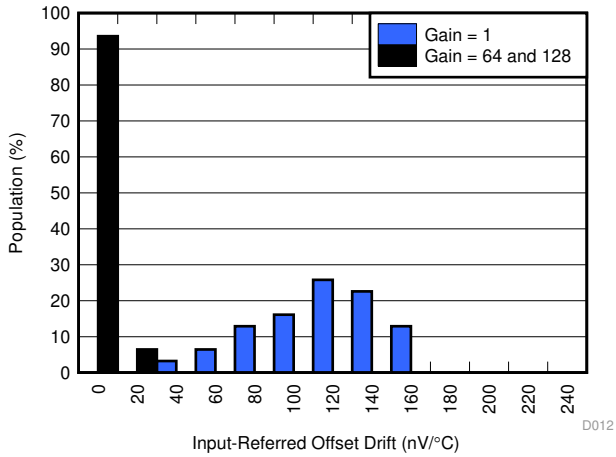

After calibration, shorted input

**Figure 9. Offset Voltage vs Temperature**



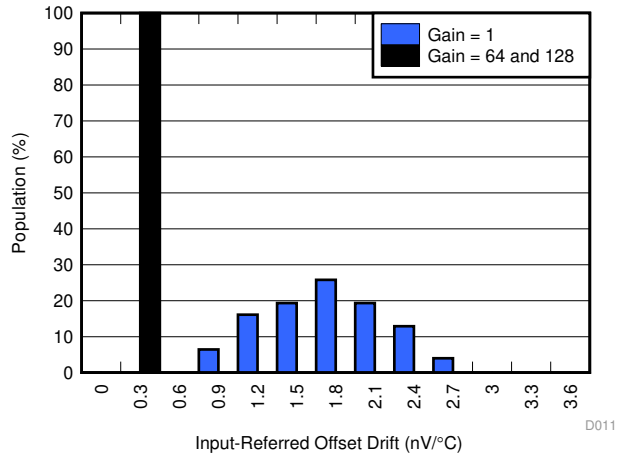

Chop mode, after calibration, shorted input

**Figure 10. Offset Voltage vs Temperature**



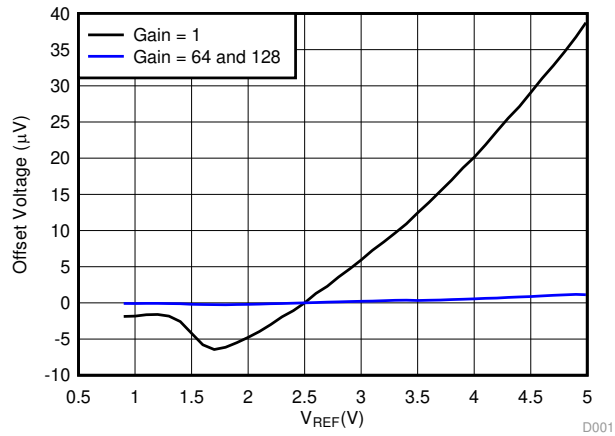

Shorted input, 30 units

**Figure 11. Offset Voltage Drift Distribution**



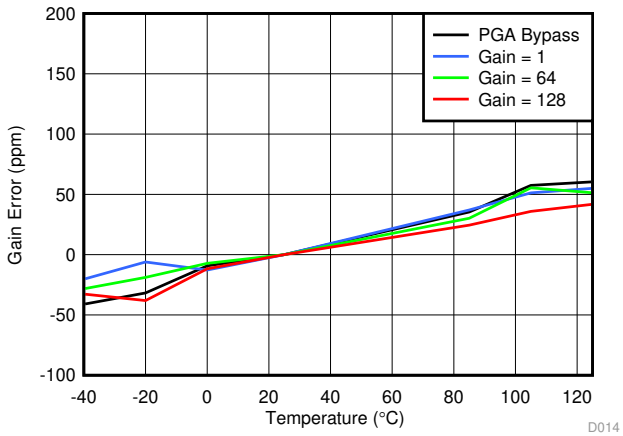

Chop mode, shorted input, 30 units

**Figure 12. Offset Voltage Drift Distribution**




After calibration

**Figure 13. Offset Voltage vs Reference Voltage**

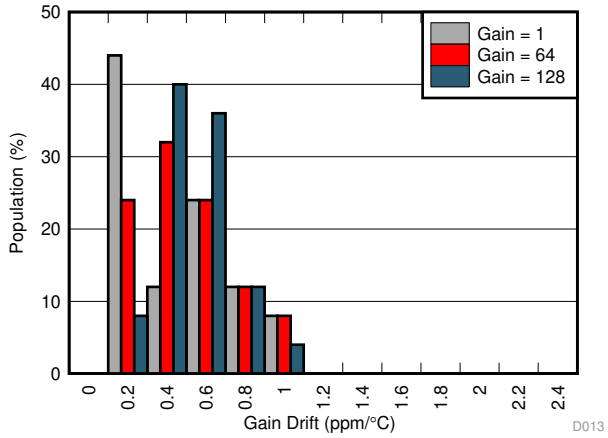



After calibration

**Figure 14. Gain Error vs Temperature**

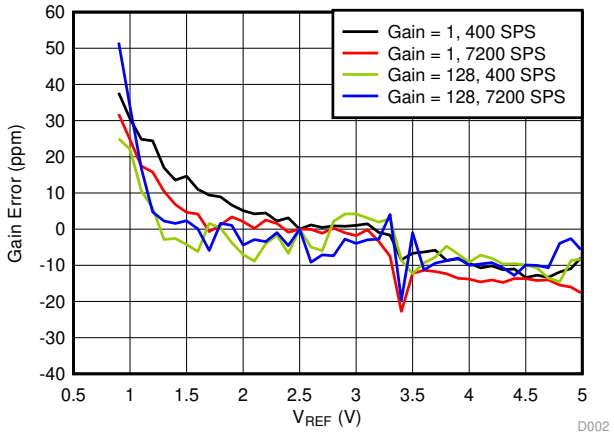
## Typical Characteristics (continued)

at $T_A$ = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, data rate = 20 SPS, $f_{CLK}$ = 7.3728 MHz and gain = 128 (unless otherwise noted)



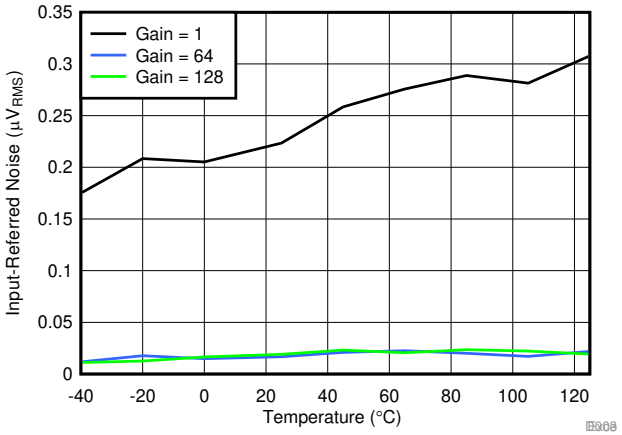

30 units

**Figure 15. Gain Drift Distribution**



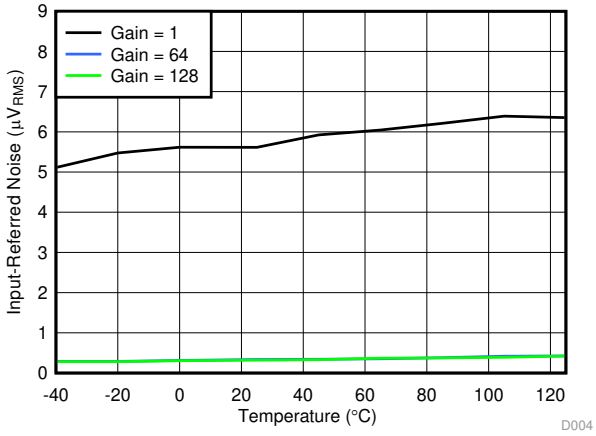

After calibration

**Figure 16. Gain vs Reference Voltage**




20 SPS, Sinc4 mode

**Figure 17. Noise vs Temperature**




7200 SPS, Sinc1 mode

**Figure 18. Noise vs Temperature**

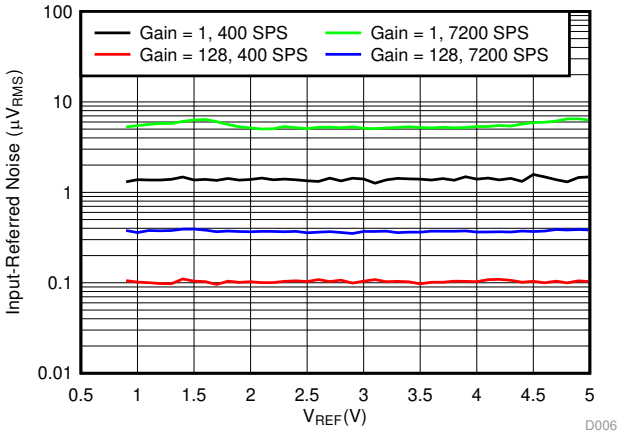
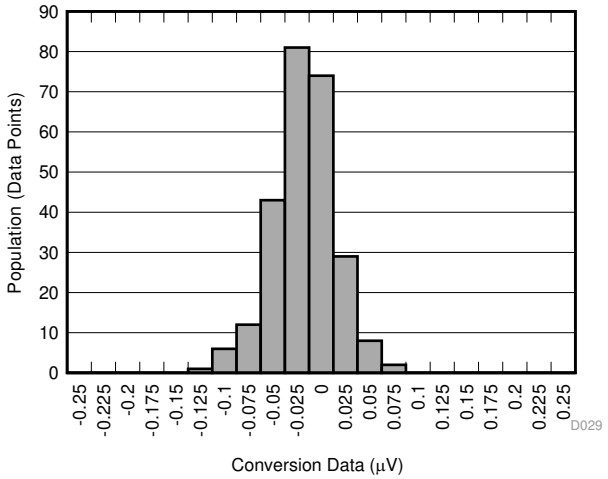



**Figure 19. Noise vs Reference Voltage**

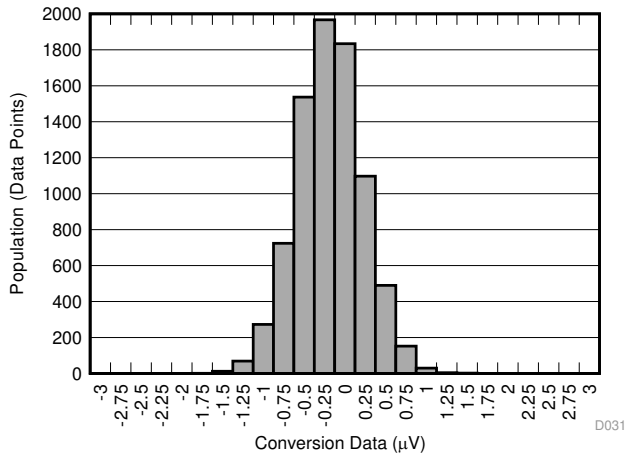



20 SPS, Gain = 128, 256 data points, shorted inputs

**Figure 20. Conversion Data Histogram**

## Typical Characteristics (continued)

at $T_A$ = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, data rate = 20 SPS, $f_{CLK}$ = 7.3728 MHz and gain = 128 (unless otherwise noted)




7200 SPS, Gain = 128, 8192 data points, shorted inputs

**Figure 21. Conversion Data Histogram**

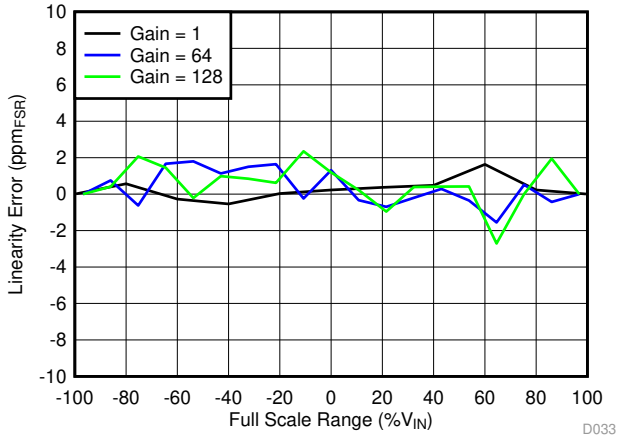



**Figure 22. Integral Non-Linearity vs $V_{IN}$**

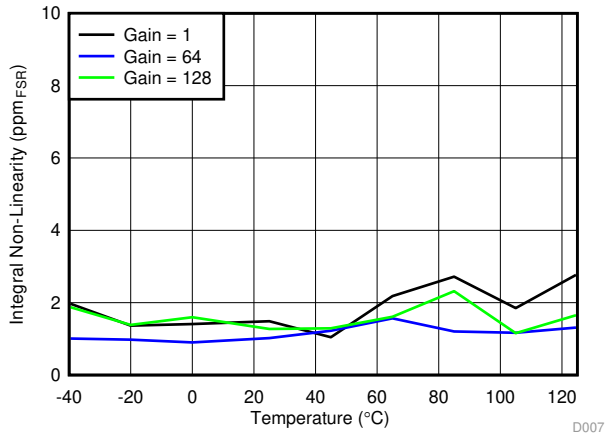



**Figure 23. Integral Non-Linearity vs Temperature**

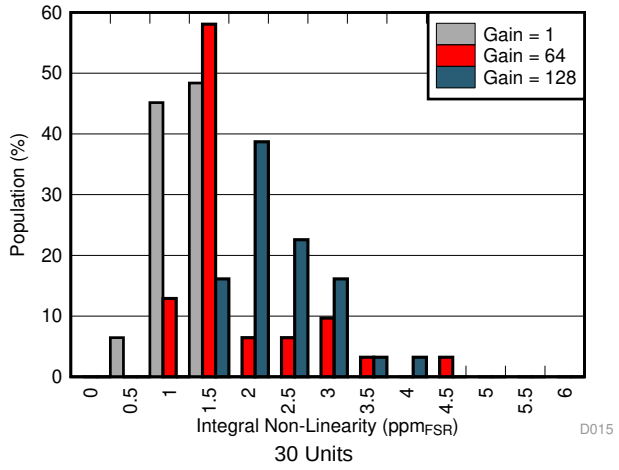



**Figure 24. Integral Non-Linearity Distribution**

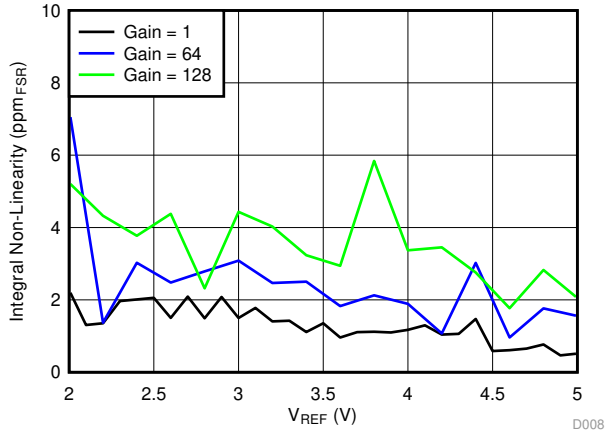
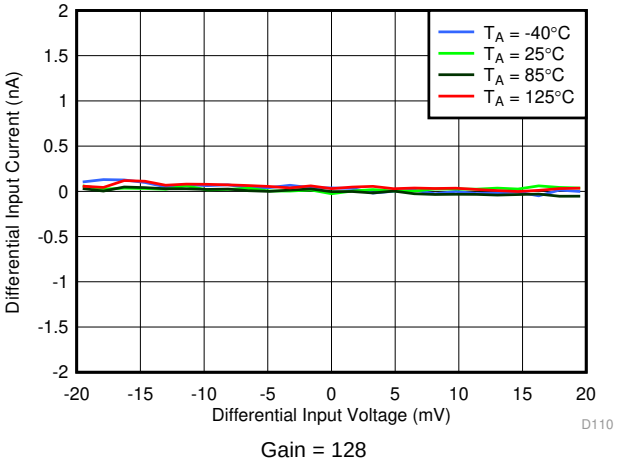



**Figure 25. Integral Non-Linearity vs Reference Voltage**

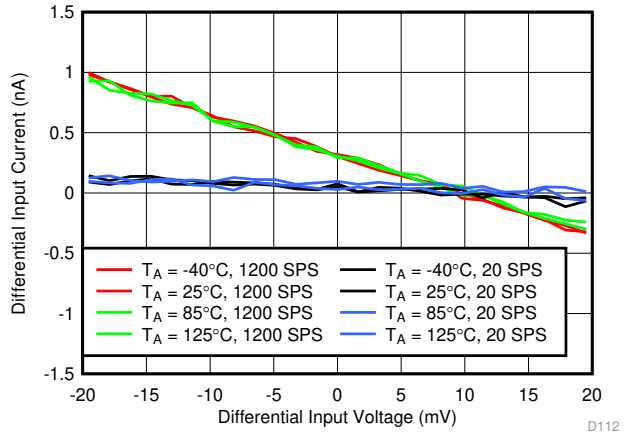



Gain = 128

**Figure 26. Differential Input Current**

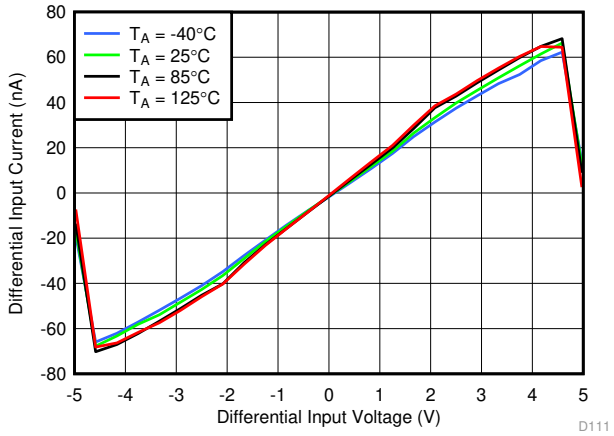
## Typical Characteristics (continued)

at $T_A$ = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, data rate = 20 SPS, $f_{CLK}$ = 7.3728 MHz and gain = 128 (unless otherwise noted)



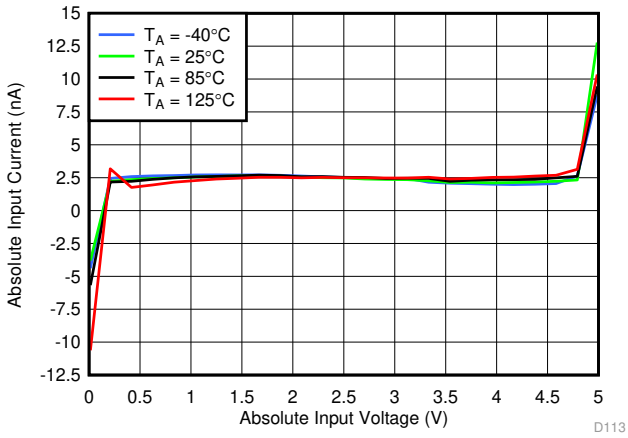

Chop Mode, Gain = 128

**Figure 27. Differential Input Current**



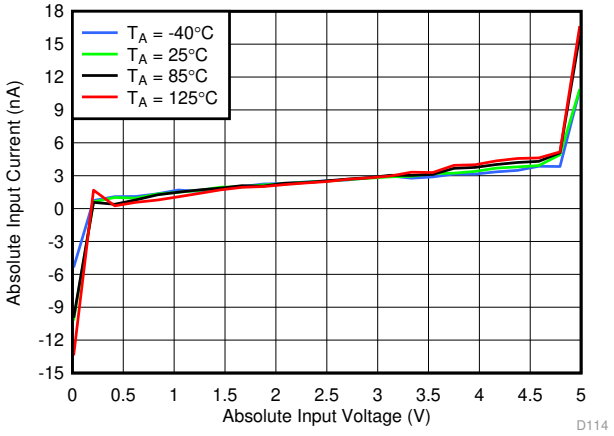

PGA Bypass (gain = 1)

**Figure 28. Differential Input Current**



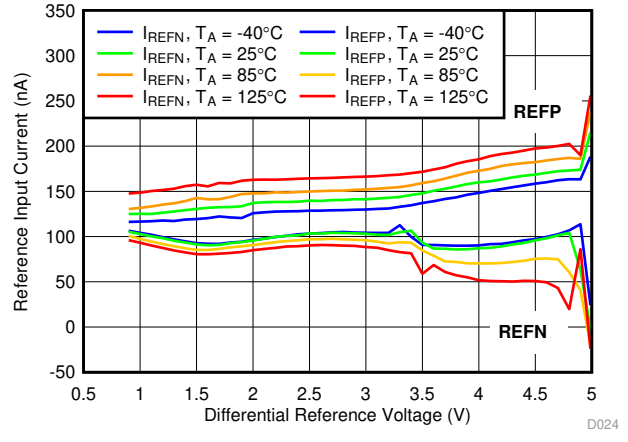

Gain = 128

**Figure 29. Absolute Input Current**



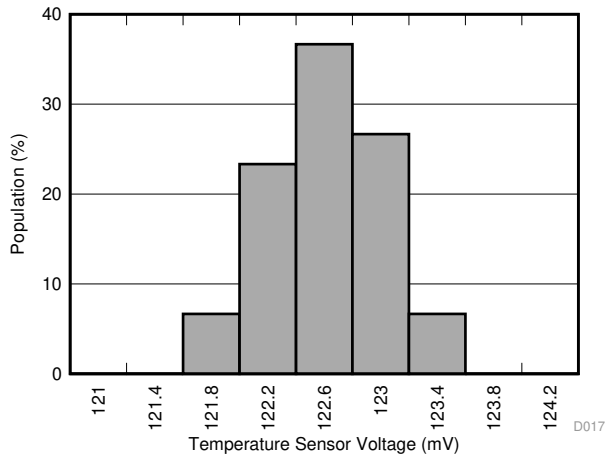

Chop Mode, Gain = 128

**Figure 30. Absolute Input Current**




$V_{REFN}$ = AVSS

**Figure 31. Reference Input Current vs Reference Voltage**




30 units

**Figure 32. Temperature Sensor Voltage Histogram**

## Typical Characteristics (continued)

at $T_A$ = 25°C, AVDD = 5 V, AVSS = 0 V, DVDD = 3.3 V, $V_{REF}$ = 5 V, data rate = 20 SPS, $f_{CLK}$ = 7.3728 MHz and gain = 128 (unless otherwise noted)

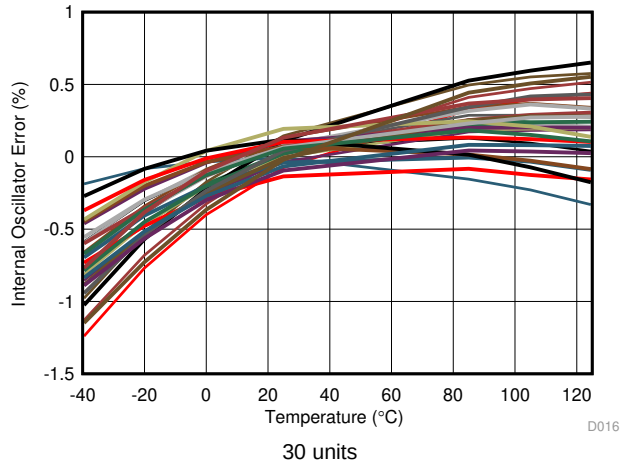



**Figure 33. Internal Oscillator Frequency vs Temperature**

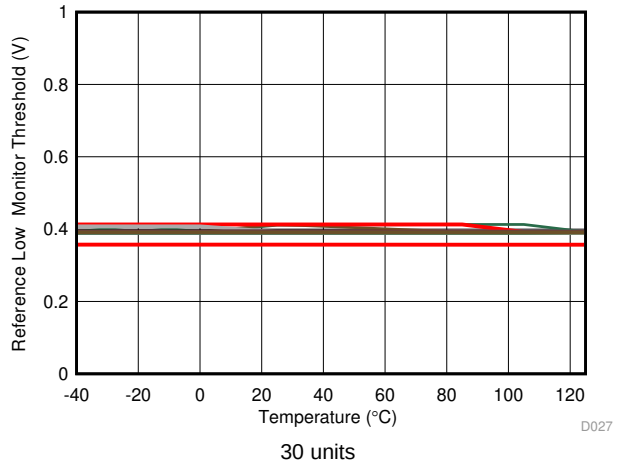



**Figure 34. Reference Low Monitor Threshold vs Temperature**

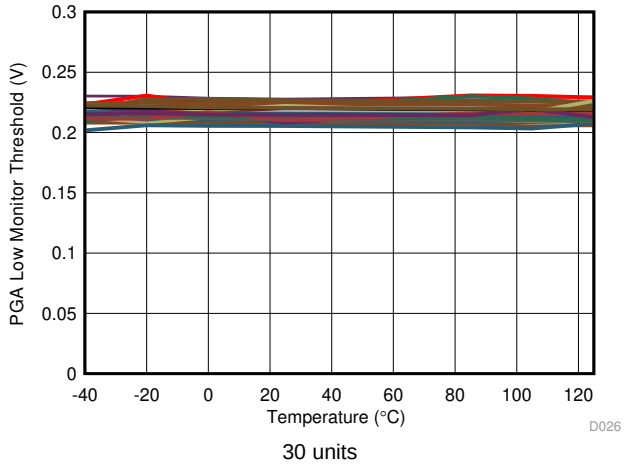



**Figure 35. PGA Low Monitor Threshold vs Temperature**

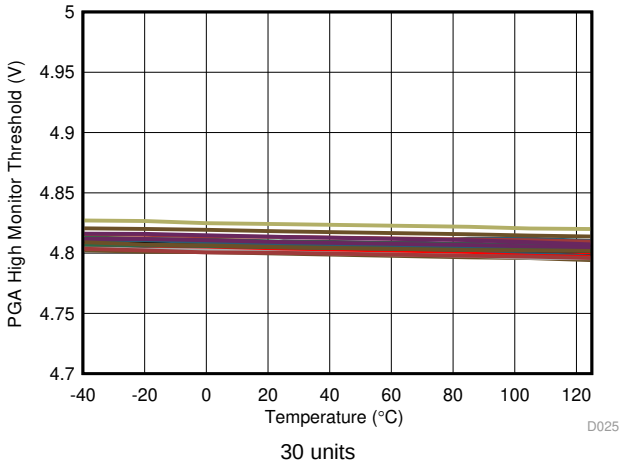



**Figure 36. PGA High Monitor Threshold vs Temperature**

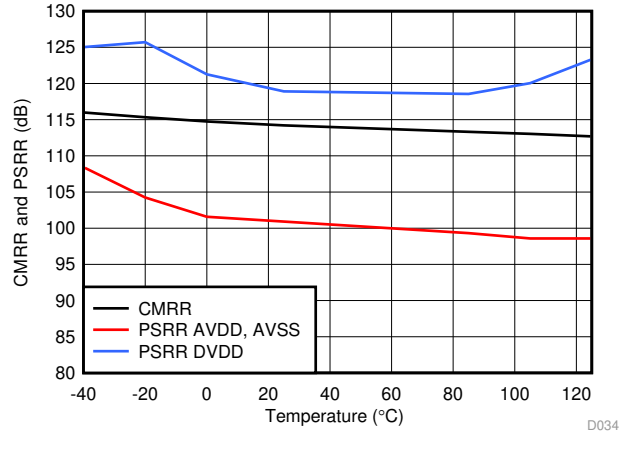



**Figure 37. CMRR and PSRR vs Temperature**

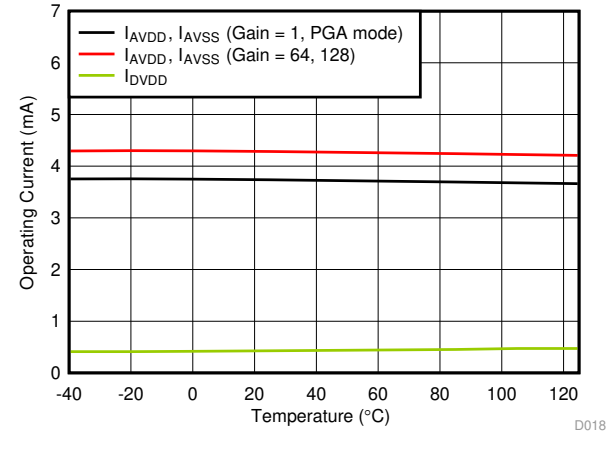



**Figure 38. Operating Current vs Temperature**

# 7 Parameter Measurement Information

## 7.1 Noise Performance

The ADS1235-Q1 noise performance depends on the ADC configuration: data rate, PGA gain, digital filter configuration, and chop mode. The combination of the parameters affect noise performance. Two significant factors affecting noise performance are data rate and PGA gain. Since the profile of noise is predominantly white (flat vs frequency), decreasing the data rate proportionally decreases bandwidth and therefore, decreases total noise. Since the noise of the PGA is lower than that of the modulator, increasing the gain decreases overall conversion noise when treated as an input-referred quantity. Noise performance also depends on the digital filter and chop mode. As the order of the digital filter increases, the noise bandwidth correspondingly decreases resulting in decreased noise. Further, as a result of two-point data averaging performed in chop mode, noise decreases by √2 compared to normal operation.

Table 1 shows noise performance in units of $\mu V_{RMS}$ (RMS = root mean square) and in units of effective resolution (bits) under the conditions listed. The values in parenthesis are peak-to-peak values (μV) and noise free resolution (bits). Noise-free resolution is the resolution of the ADC with no code flicker. The noise-free resolution data are calculated based on the peak-to-peak noise data.

The effective resolution data listed in the tables are calculated using Equation 1:

$$\text{Effective Resolution or Noise-Free Resolution} = \ln (FSR / e_n) / \ln (2) \quad (1)$$

where

- FSR = full scale range = $2 \cdot V_{REF}$ / Gain (See *Recommended Operating Conditions* for limitations of FSR)
- $e_n$ = Input referred voltage noise (RMS value to calculate effective resolution, p-p value to calculate noise-free resolution)

The data shown in the noise performance table represent typical ADC performance at $T_A$ = 25°C. The noise-performance data are the standard deviation and peak-to-peak computations of the ADC data. The noise data are acquired with inputs shorted, based on consecutive ADC readings for a period of ten seconds or 8192 data points, whichever occurs first. Because of the statistical nature of noise, repeated noise measurements may yield higher or lower noise performance results.

**Table 1. Noise in $\mu V_{RMS}$ ($\mu V_{PP}$) and Effective Resolution (Noise-Free Resolution) at $T_A$ = 25°C and $V_{REF}$ = 5 V**

| DATA RATE | FILTER | NOISE, $\mu V_{RMS}$ ($\mu V_{PP}$) | | | EFFECTIVE RESOLUTION (Bits), [NOISE-FREE RESOLUTION (Bits)] | | |
|---|---|---|---|---|---|---|---|
| | | GAIN = 1 | GAIN = 64 | GAIN = 128 | GAIN = 1 | GAIN = 64 | GAIN = 128 |
| 2.5 SPS | FIR | 0.21 (0.6) | 0.008 (0.028) | 0.011 (0.042) | 24 (23.8) | 24 (22.4) | 22.7 (20.8) |
| 2.5 SPS | Sinc1 | 0.12 (0.3) | 0.009 (0.037) | 0.008 (0.033) | 24 (24) | 24 (22) | 23.2 (21.2) |
| 2.5 SPS | Sinc2 | 0.15 (0.3) | 0.007 (0.023) | 0.006 (0.021) | 24 (24) | 24 (22.7) | 23.7 (21.8) |
| 2.5 SPS | Sinc3 | 0.15 (0.3) | 0.007 (0.023) | 0.005 (0.014) | 24 (24) | 24 (22.7) | 24 (22.4) |
| 2.5 SPS | Sinc4 | 0.15 (0.3) | 0.005 (0.019) | 0.006 (0.019) | 24 (24) | 24 (23) | 23.7 (22) |
| 5 SPS | FIR | 0.29 (0.89) | 0.013 (0.051) | 0.013 (0.051) | 24 (23.2) | 23.6 (21.5) | 22.5 (20.5) |
| 5 SPS | Sinc1 | 0.15 (0.3) | 0.015 (0.051) | 0.01 (0.044) | 24 (24) | 23.4 (21.5) | 22.9 (20.8) |
| 5 SPS | Sinc2 | 0.17 (0.6) | 0.012 (0.047) | 0.009 (0.035) | 24 (23.8) | 23.7 (21.7) | 23 (21.1) |
| 5 SPS | Sinc3 | 0.12 (0.6) | 0.011 (0.047) | 0.008 (0.037) | 24 (23.8) | 23.7 (21.7) | 23.1 (21) |
| 5 SPS | Sinc4 | 0.088 (0.3) | 0.007 (0.028) | 0.007 (0.03) | 24 (24) | 24 (22.4) | 23.3 (21.3) |
| 10 SPS | FIR | 0.36 (1.5) | 0.022 (0.11) | 0.02 (0.096) | 24 (22.5) | 22.8 (20.5) | 21.9 (19.6) |
| 10 SPS | Sinc1 | 0.28 (0.89) | 0.015 (0.065) | 0.016 (0.082) | 24 (23.2) | 23.3 (21.2) | 22.2 (19.9) |
| 10 SPS | Sinc2 | 0.26 (0.89) | 0.015 (0.061) | 0.013 (0.065) | 24 (23.2) | 23.3 (21.3) | 22.5 (20.2) |
| 10 SPS | Sinc3 | 0.26 (0.6) | 0.014 (0.065) | 0.011 (0.047) | 24 (23.8) | 23.4 (21.2) | 22.7 (20.7) |
| 10 SPS | Sinc4 | 0.24 (0.6) | 0.013 (0.056) | 0.01 (0.042) | 24 (23.8) | 23.6 (21.4) | 22.9 (20.8) |
| 16.6 SPS | Sinc1 | 0.41 (1.8) | 0.025 (0.12) | 0.022 (0.12) | 24 (22.2) | 22.6 (20.3) | 21.8 (19.4) |
| 16.6 SPS | Sinc2 | 0.32 (1.5) | 0.018 (0.089) | 0.018 (0.096) | 24 (22.5) | 23 (20.8) | 22 (19.6) |
| 16.6 SPS | Sinc3 | 0.3 (1.2) | 0.017 (0.079) | 0.018 (0.091) | 24 (22.8) | 23.1 (20.9) | 22.1 (19.7) |
| 16.6 SPS | Sinc4 | 0.23 (1.2) | 0.015 (0.084) | 0.014 (0.072) | 24 (22.8) | 23.3 (20.8) | 22.4 (20) |

## Noise Performance (continued)

**Table 1. Noise in $\mu V_{RMS}$ ($\mu V_{PP}$) and Effective Resolution (Noise-Free Resolution) at $T_A$ = 25°C and $V_{REF}$ = 5 V (continued)**

| DATA RATE | FILTER | NOISE, $\mu V_{RMS}$ ($\mu V_{PP}$) | | | EFFECTIVE RESOLUTION (Bits), [NOISE-FREE RESOLUTION (Bits)] | | |
|---|---|---|---|---|---|---|---|
| | | GAIN = 1 | GAIN = 64 | GAIN = 128 | GAIN = 1 | GAIN = 64 | GAIN = 128 |
| 20 SPS | FIR | 0.51 (2.1) | 0.032 (0.16) | 0.029 (0.16) | 24 (22) | 22.2 (19.9) | 21.3 (18.9) |
| 20 SPS | Sinc1 | 0.44 (2.1) | 0.025 (0.13) | 0.026 (0.13) | 24 (22) | 22.6 (20.2) | 21.5 (19.2) |
| 20 SPS | Sinc2 | 0.36 (1.2) | 0.02 (0.12) | 0.02 (0.1) | 24 (22.8) | 22.9 (20.4) | 21.9 (19.5) |
| 20 SPS | Sinc3 | 0.32 (1.5) | 0.017 (0.089) | 0.018 (0.096) | 24 (22.5) | 23.1 (20.8) | 22 (19.6) |
| 20 SPS | Sinc4 | 0.3 (1.2) | 0.017 (0.084) | 0.018 (0.1) | 24 (22.8) | 23.1 (20.8) | 22.1 (19.6) |
| 50 SPS | Sinc1 | 0.63 (3.6) | 0.04 (0.25) | 0.038 (0.23) | 23.7 (21.2) | 21.9 (19.2) | 21 (18.4) |
| 50 SPS | Sinc2 | 0.57 (3) | 0.033 (0.21) | 0.032 (0.18) | 23.9 (21.5) | 22.2 (19.5) | 21.2 (18.7) |
| 50 SPS | Sinc3 | 0.53 (2.4) | 0.03 (0.19) | 0.03 (0.17) | 24 (21.8) | 22.3 (19.7) | 21.3 (18.8) |
| 50 SPS | Sinc4 | 0.49 (2.4) | 0.028 (0.15) | 0.026 (0.16) | 24 (21.8) | 22.4 (20) | 21.5 (18.9) |
| 60 SPS | Sinc1 | 0.71 (3.9) | 0.043 (0.27) | 0.042 (0.26) | 23.6 (21.1) | 21.8 (19.1) | 20.8 (18.2) |
| 60 SPS | Sinc2 | 0.6 (3.3) | 0.036 (0.24) | 0.034 (0.21) | 23.8 (21.4) | 22.1 (19.3) | 21.1 (18.5) |
| 60 SPS | Sinc3 | 0.56 (3) | 0.032 (0.19) | 0.03 (0.17) | 23.9 (21.5) | 22.2 (19.6) | 21.3 (18.8) |
| 60 SPS | Sinc4 | 0.53 (2.7) | 0.031 (0.19) | 0.03 (0.18) | 24 (21.6) | 22.3 (19.7) | 21.3 (18.7) |
| 100 SPS | Sinc1 | 0.8 (4.8) | 0.056 (0.34) | 0.054 (0.35) | 23.4 (20.8) | 21.4 (18.8) | 20.5 (17.8) |
| 100 SPS | Sinc2 | 0.68 (4.2) | 0.047 (0.29) | 0.043 (0.3) | 23.6 (21) | 21.7 (19) | 20.8 (18) |
| 100 SPS | Sinc3 | 0.67 (4.2) | 0.042 (0.28) | 0.041 (0.27) | 23.6 (21) | 21.8 (19.1) | 20.9 (18.1) |
| 100 SPS | Sinc4 | 0.62 (3.6) | 0.039 (0.24) | 0.039 (0.27) | 23.8 (21.2) | 21.9 (19.3) | 20.9 (18.2) |
| 400 SPS | Sinc1 | 1.4 (11) | 0.11 (0.81) | 0.11 (0.75) | 22.6 (19.6) | 20.4 (17.5) | 19.5 (16.7) |
| 400 SPS | Sinc2 | 1.2 (8.3) | 0.09 (0.64) | 0.086 (0.6) | 22.8 (20) | 20.7 (17.9) | 19.8 (17) |
| 400 SPS | Sinc3 | 1.1 (7.7) | 0.082 (0.61) | 0.078 (0.56) | 22.9 (20.1) | 20.9 (18) | 19.9 (17.1) |
| 400 SPS | Sinc4 | 1 (7.7) | 0.076 (0.59) | 0.072 (0.53) | 23 (20.1) | 21 (18) | 20 (17.2) |
| 1200 SPS | Sinc1 | 2.3 (17) | 0.18 (1.3) | 0.18 (1.4) | 21.9 (19) | 19.7 (16.9) | 18.8 (15.7) |
| 1200 SPS | Sinc2 | 2 (14) | 0.15 (1.2) | 0.15 (1.1) | 22.1 (19.3) | 20 (17) | 19 (16.1) |
| 1200 SPS | Sinc3 | 1.8 (13) | 0.14 (1) | 0.13 (1) | 22.2 (19.4) | 20.1 (17.2) | 19.2 (16.2) |
| 1200 SPS | Sinc4 | 1.7 (13) | 0.13 (1) | 0.13 (0.94) | 22.3 (19.4) | 20.2 (17.2) | 19.2 (16.3) |
| 2400 SPS | Sinc1 | 3.2 (26) | 0.25 (2) | 0.24 (1.8) | 21.4 (18.4) | 19.2 (16.2) | 18.3 (15.4) |
| 2400 SPS | Sinc2 | 2.7 (20) | 0.22 (1.7) | 0.21 (1.5) | 21.6 (18.7) | 19.5 (16.5) | 18.5 (15.6) |
| 2400 SPS | Sinc3 | 2.5 (18) | 0.2 (1.4) | 0.19 (1.4) | 21.7 (18.9) | 19.6 (16.7) | 18.6 (15.8) |
| 2400 SPS | Sinc4 | 2.3 (18) | 0.18 (1.5) | 0.18 (1.4) | 21.8 (18.9) | 19.7 (16.7) | 18.8 (15.8) |
| 4800 SPS | Sinc1 | 4.4 (35) | 0.34 (2.5) | 0.32 (2.4) | 20.9 (17.9) | 18.8 (15.9) | 17.9 (15) |
| 4800 SPS | Sinc2 | 3.9 (30) | 0.3 (2.3) | 0.29 (2.4) | 21.1 (18.1) | 19 (16.1) | 18 (15) |
| 4800 SPS | Sinc3 | 3.6 (27) | 0.28 (2) | 0.26 (2) | 21.2 (18.3) | 19.1 (16.3) | 18.2 (15.2) |
| 4800 SPS | Sinc4 | 3.4 (27) | 0.26 (1.9) | 0.25 (1.9) | 21.3 (18.3) | 19.2 (16.3) | 18.2 (15.3) |
| 7200 SPS | Sinc1 | 5.2 (42) | 0.38 (2.9) | 0.37 (3) | 20.7 (17.7) | 18.6 (15.7) | 17.7 (14.7) |
| 7200 SPS | Sinc2 | 4.7 (37) | 0.36 (2.8) | 0.34 (2.5) | 20.8 (17.9) | 18.7 (15.8) | 17.8 (14.9) |
| 7200 SPS | Sinc3 | 4.5 (35) | 0.34 (2.5) | 0.32 (2.4) | 20.9 (18) | 18.8 (15.9) | 17.9 (15) |
| 7200 SPS | Sinc4 | 4.2 (36) | 0.32 (2.5) | 0.31 (2.3) | 21 (17.9) | 18.9 (16) | 18 (15.1) |

# 8 Detailed Description

## 8.1 Overview

The ADS1235-Q1 is a three differential-input, precision 24-bit, ΔΣ ADC with a low-noise PGA and programmable digital filter. The low-noise, low-drift architecture of the PGA makes the ADC suitable for precision measurement of low signal level sensors, such as strain-gauge bridges and resistive pressure transducers. The ADC provides optional chop and ac-bridge excitation modes to eliminate offset drift error.

Key features of the ADC are:

- 1-GΩ input impedance, low-noise PGA
- High-resolution 24-bit ΔΣ ADC
- Four GPIO with ac-bridge excitation control output
- Internal oscillator
- Voltage reference monitor
- Signal overrange monitor
- Temperature sensor
- CRC communication error detection

The analog inputs (AINx) connect to the input multiplexer (MUX). The ADC supports three differential or five single-ended input measurement configurations. A second voltage reference input and AC-bridge excitation drive outputs (GPIO) are multiplexed with the analog input pins.

The programmable gain amplifier (PGA) follows the input multiplexer. The gain is programmable to 1, 64 or 128. The PGA bypass option connects the analog inputs directly to the precharge buffered modulator, extending the input voltage range to the voltage of the power supplies. The PGA output connects to pins CAPP and CAPN. The ADC antialias filter is provided at the PGA output with an external capacitor. A monitor is used for detection of PGA overrange conditions.

The delta-sigma modulator measures the differential input voltage relative to the reference voltage to produce the 24-bit conversion result. The differential input range of the ADC is $\pm V_{REF}$ / Gain.

The digital filter averages and decimates the modulator output data to yield the final, down-sampled conversion result. The sinc filter is programmable (sinc1 through sinc4) allowing optimization of conversion time, conversion noise and line-cycle rejection. The finite impulse response (FIR) filter mode provides single-cycle settled data with simultaneous rejection of 50-Hz and 60-Hz at data rates of 20 SPS or less.

Two reference voltage input pairs are provided. The primary reference input pair (REFP0/REFN0) is available as standalone input pins. A second reference input pair (REFP1/REFN1) is multiplexed with analog inputs AIN0 and AIN1. A monitor is used for detection of low or missing reference voltage.

The ADC provides four GPIO control lines. The GPIOs are used for input and output of general-purpose logic signals, as well as providing output drive signals for ac-excited bridges. The GPIOs and ac-bridge excitation drive outputs are multiplexed to the analog inputs.

The internal temperature sensor voltage is read by the ADC through the analog input multiplexer.

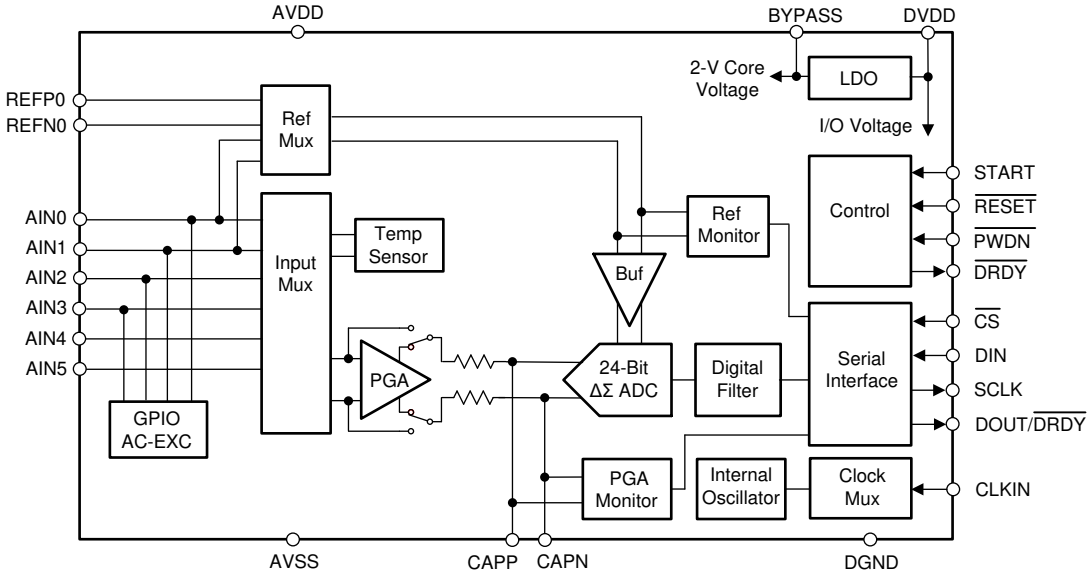
The SPI-compatible serial interface is used to read the conversion data and also to configure and control the ADC. Data communication errors are detected by CRC. The serial interface consists of four signals: $\overline{CS}$, SCLK, DIN and DOUT/$\overline{DRDY}$. The dual function DOUT/$\overline{DRDY}$ provides data output and also the data ready signal. The ADC serial interface can be implemented with as little as three pins by tying $\overline{CS}$ low.

The ADC clock is either internal or external. The ADC detects the mode of clock operation automatically. The clock frequency is 7.3728 MHz.

Data conversions are controlled by the START pin or by the START command. The ADC is programmable for continuous or one-shot conversions. The $\overline{DRDY}$ or DOUT/$\overline{DRDY}$ pin provides the conversion-data ready signal. When taken low, the $\overline{RESET}$ pin resets the ADC. The ADC is powered down by the $\overline{PWDN}$ pin or is powered down in software mode.

The ADC operates in either bipolar analog supply configuration (±2.5 V), or in single 5-V supply configuration. The digital power supply range is 2.7 V to 5 V. The BYPASS pin is the internal subregulator output used for the ADC digital core.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

The following sections describe the functional blocks of the ADC.

### 8.3.1 Analog Inputs

Figure 39 shows the analog input circuit consisting of ESD-protection diodes, the input multiplexer and the PGA. The ADS1235-Q1 has six analog inputs to support three differential-input measurement channels. In addition, there are two internal (system) measurements, and an option to disconnect all inputs.

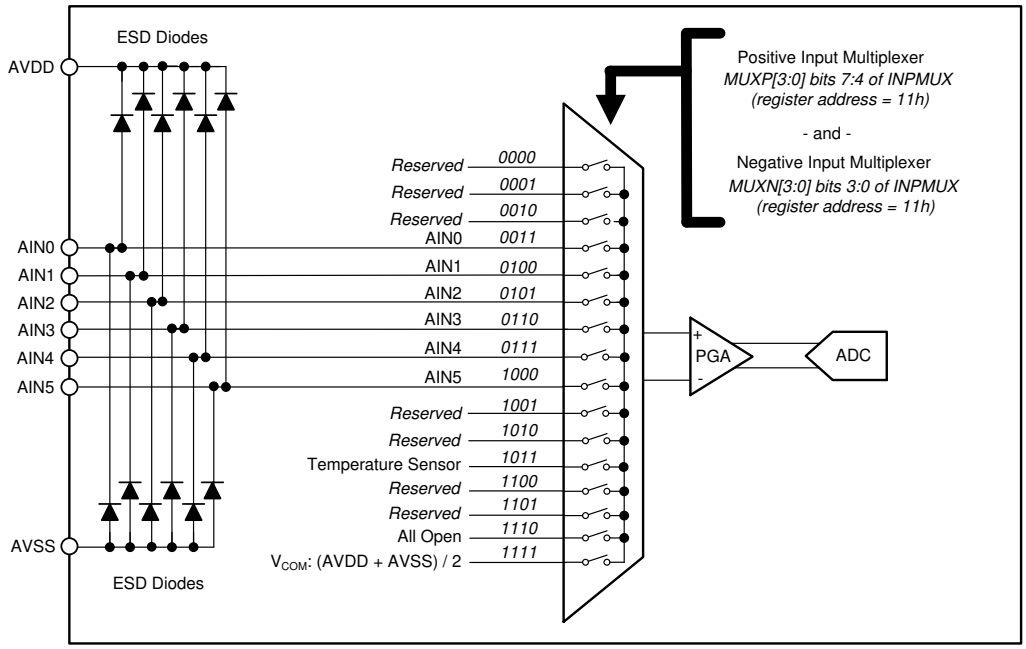



**Figure 39. Analog Input Block Diagram**

#### 8.3.1.1 ESD Diodes

ESD diodes are incorporated to protect the ADC inputs from possible ESD events occurring during the manufacturing process and during PCB assembly when manufactured in an ESD-controlled environment. For system-level ESD protection, consider the use of external ESD protection devices for pins that are exposed to ESD, including the analog inputs.

If either input is driven below AVSS – 0.3 V, or above AVDD + 0.3 V, the internal protection diodes may conduct. If these conditions are possible, use external clamp diodes, series resistors, or both to limit the input current to the specified maximum value.

#### 8.3.1.2 Input Multiplexer

The input multiplexer selects the signal for measurement. The multiplexer consists of independently programmable positive and negative sections. See Figure 39 for multiplexer register settings. The multiplexers select any input as positive and any input as negative for connection to the PGA. For example, to select AIN5 and AIN4 as a differential input with (+) and (-) polarity, program the INPMUX register to the value of 87h.

When the multiplexer is changed, a break-before-make sequence is performed in order to reduce charge injection into the next measurement channel. Be aware that over-driving unused channels beyond the power supplies can effect conversions taking place on active channels. See the Input Overload section for more information.

## Feature Description (continued)

### 8.3.1.3 Temperature Sensor

The ADC has an internal temperature sensor. The temperature sensor is comprised of two internal diodes with one diode having 80 times the current density of the other. The difference in current density of the diodes yields a differential output voltage that is proportional to absolute temperature. The temperature sensor reading is converted by the ADC. See Figure 39 for register settings to select the temperature sensor for measurement.

Equation 2 shows how to convert the temperature sensor reading to degrees Celsius (˚C):

$$\text{Temperature (°C)} = [(\text{Temperature Reading (µV)} - 122{,}400) / 420\ \text{µV/°C}] + 25°C \quad (2)$$

Measure the temperature sensor with PGA on, gain = 1 and ac-bridge excitation mode disabled. As a result of the low package-to-PCB thermal resistance, the internal temperature closely tracks the PCB temperature.

### 8.3.1.4 Inputs Open

This configuration opens the inputs to the PGA. Use this configuration to disconnect the PGA from the sensor. With all inputs disconnected, the conversion data are invalid due to the floating input condition. See Figure 39 for the register setting value to open all inputs.

### 8.3.1.5 Internal $V_{COM}$ Connection

This configuration connects the PGA inputs to the internal $V_{COM}$ voltage as defined: (AVDD + AVSS) / 2. Use this connection to short the inputs to measure the ADC noise performance and offset voltage, or to short the inputs for offset calibration. See Figure 39 for register settings for the internal $V_{COM}$ connection.

### 8.3.1.6 Alternate Functions

The analog input pins have multiplexed alternate functions. The alternate functions are the second reference input and GPIO to provide the ac-bridge excitation drive signals. The functions are enabled by programming the associated function registers. The analog inputs retain measurement capability if the alternate functions are programmed. Table 2 summarizes the alternate functions multiplexed to the analog input pins.

**Table 2. Analog Input Alternate Functions**

| ANALOG INPUTS | REFERENCE INPUTS | GPIO/AC-BRIDGE EXCITATION (2-wire mode) | GPIO/AC-BRIDGE EXCITATION (4-wire mode) |
|---|---|---|---|
| AIN0 | REFP1 | GPIO0/$\overline{\text{ACX1}}$ | GPIO0/$\overline{\text{ACX1}}$ |
| AIN1 | REFN1 | GPIO1/$\overline{\text{ACX2}}$ | GPIO1/$\overline{\text{ACX2}}$ |
| AIN2 | | | GPIO2/ACX1 |
| AIN3 | | | GPIO3/ACX2 |
| AIN4 | | | |
| AIN5 | | | |

### 8.3.2 PGA

The PGA is a low-noise, CMOS differential-input, differential-output amplifier. The PGA extends the dynamic range of the ADC, important when used with low-level output sensors. Gain is controlled by the GAIN[2:0] register bits as shown in Figure 40. In PGA bypass mode, the input voltage range extends to the analog supplies. The PGA is powered down in bypass mode.

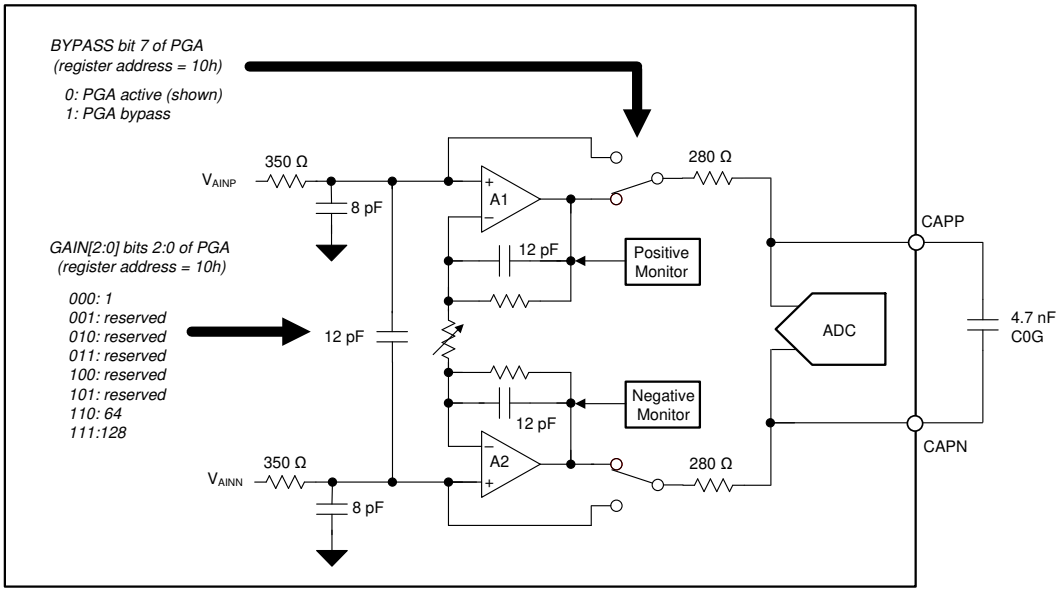



**Figure 40. PGA Block Diagram**

The PGA consists of two chopper-stabilized amplifiers (A1 and A2), and a resistor network that determines the PGA gain. The resistor network is precision-matched, providing low drift performance. The PGA has internal noise filters to reduce sensitivity to electromagnetic-interference (EMI). The PGA output is monitored to provide indication of a possible PGA overload condition.

Pins CAPP and CAPN are the PGA positive and negative outputs, respectively. Connect an external 4.7-nF capacitor (type C0G) as shown in Figure 40. The capacitor filters the sample pulses caused by the modulator, and with the internal resistors the antialias filter is provided. Place the capacitor as close as possible to the pins using short, direct traces. Avoid running clock traces or other digital traces close to these pins.

#### *8.3.2.1 Input Voltage Range*

The input voltage range is determined by the magnitude of the reference voltage and ADC gain. As shown in Figure 19, conversion voltage noise is constant over the specified reference voltage range. Table 3 shows the differential input voltage range verses gain for $V_{REF}$ = 5 V.

**Table 3. Input Voltage Range**

| GAIN[2:0] BITS | GAIN | FULL-SCALE DIFFERENTIAL INPUT VOLTAGE RANGE(1) |
|---|---|---|
| 000 | 1 | ±5.000 V |
| 110 | 64 | ±0.078 V |
| 111 | 128 | ±0.039 V |

(1) $V_{REF}$ = 5 V. Input voltage range scales with $V_{REF}$. For gain = 1 and PGA mode, the input voltage range is limited by evaluation of Equation 3.

As with many amplifiers, the PGA has an input voltage range specification that must not be exceeded in order to maintain linear operation. The input range is specified as an absolute voltage (signal plus common mode voltage) at both positive and negative inputs. As specified in Equation 3, the maximum and minimum absolute input voltage depends on gain, the expected maximum differential voltage, and the minimum value of the analog power supply voltage.

$$AVSS + 0.3\ V + V_{IN} \cdot (Gain - 1) / 2 \cdot < V_{AINP} \text{ and } V_{AINN} < AVDD - 0.3\ V - V_{IN} \cdot (Gain - 1) / 2$$

where

- $V_{AINP}$, $V_{AINN}$ = absolute input voltage
- $V_{IN} = V_{AINP} - V_{AINN}$, maximum differential input voltage
- Gain (for gains = 64 and 128, use 32 for calculation)
- AVDD = minimum AVDD voltage
- AVSS = maximum AVSS voltage (3)

The relationship of the PGA input to the PGA output is shown graphically in Figure 41. The PGA output voltages ($V_{OUTP}$, $V_{OUTN}$) depend on the respective absolute input voltage, the differential input voltage, and the PGA gain. To maintain the PGA within the linear operating range, the PGA output voltages must be restricted within AVDD – 0.3 V and AVSS + 0.3 V. The diagram depicts a positive differential input voltage that results in a positive differential output voltage.

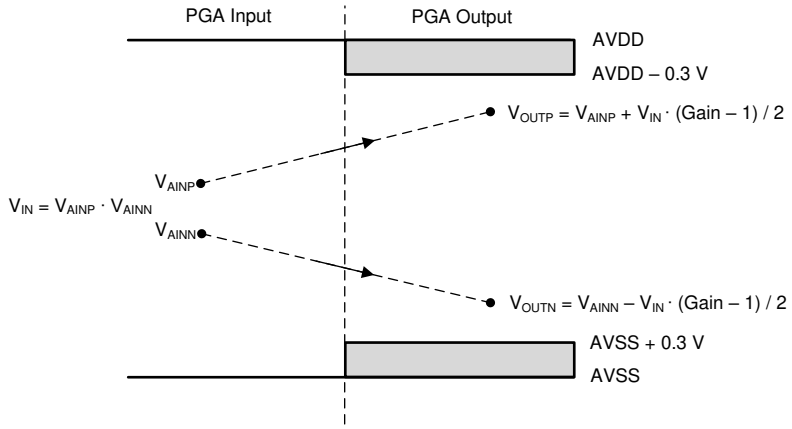



**Figure 41. PGA Input/Output Range**

### *8.3.2.2 PGA Bypass Mode*

Bypass the PGA to extend the input voltage range to the analog power supply voltages. In bypass mode, the PGA is bypassed and the analog inputs are connected directly to the precharge buffers of the modulator, thereby extending the input voltage range. Be aware of the increased input current in bypass mode. See the *Electrical Characteristics* for the input current specification.

### 8.3.3 PGA Voltage Monitor

The PGA has internal monitors to alarm of possible overrange conditions. Overrange conditions are possible if the signal voltage is over-driven, the common-mode voltage is out of range or if too much gain is used for the normal range of input signal. When overranged, the PGA output nodes are in saturation resulting in invalid conversion data. The high alarm bit asserts high (PGAH_ALM) If *either* the positive or negative PGA output is greater than AVDD – 0.2 V. Similarly, the low alarm bit asserts high (PGAL_ALM) if *either* positive or negative PGA output is less than AVSS + 0.2 V. The status of the alarm bits are read in the STATUS byte. The alarm bits are read-only and automatically reset at the start of the next conversion cycle after the overrange condition is cleared. The PGA voltage monitor diagram and threshold values are shown in Figure 42 and Figure 43.

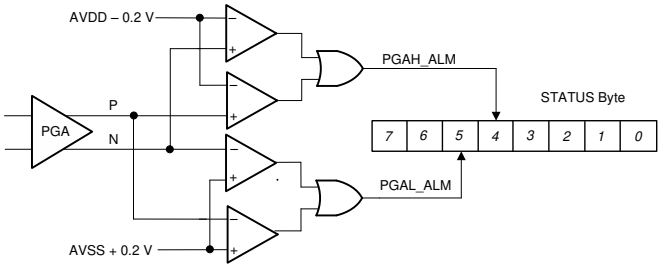



**Figure 42. PGA Voltage Monitor Diagram**

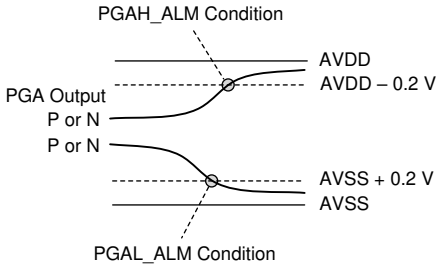



**Figure 43. PGA Monitor Thresholds**

The PGA voltage monitors are fast-responding voltage comparators. Comparator operation is disabled during multiplexer changes to minimize triggering of false alarms. However, it is possible the alarms can trigger on other transient overload conditions that may occur after gain changes, sensor connection changes, and so on.

### 8.3.4 Reference Voltage

The ADC requires a reference voltage for operation. The ADC allows two external inputs and the internal analog power supply as reference options. The reference voltage is selected by independent positive and negative multiplexers. The default reference is the 5-V analog power supply (AVDD – AVSS). Figure 44 shows the block diagram of the reference multiplexer.

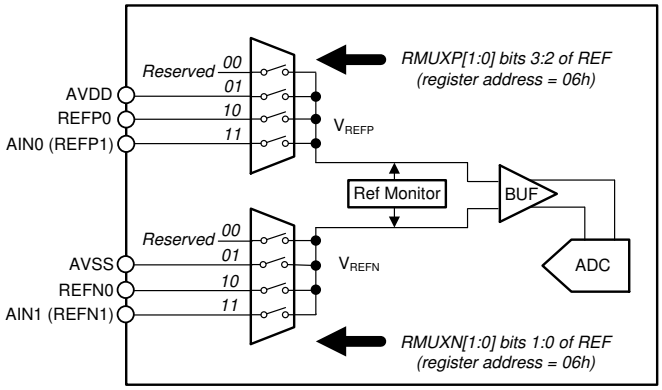



**Figure 44. Reference Input Block Diagram**

Program the RMUXP[1:0] and RMUXN[1:0] bits of the REF register to select the positive and negative reference voltages, respectively. The positive reference selections are AVDD, REFP0 and AIN0 (REFP1). The negative reference input selections are internal AVSS, REFN0, AIN1 (REFN1). The reference low-voltage monitor is located after the reference multiplexer. See the *Reference Monitor* section for more information.

#### *8.3.4.1 External Reference*

Use the external reference by applying the reference voltage to the designated reference input pins. The reference input pins are differential with positive and negative inputs. Program the reference multiplexer bits RMUXP[1:0] and RMUXN[1:0] to select the respective reference voltage for operation. For example, to select REFP0 and REFN0 as the reference voltage, program the REF register to the value of 0Ah. Follow the specified absolute and differential reference voltage operating conditions, as specified in the *Recommended Operating Conditions*.

Be aware of the reference input current when reference impedances are present, such as by the use of a resistor divider. Consider the effect of the resistance to system accuracy. Connect a capacitor across the reference input pins to filter noise. When R-C filters are used, match the time constants of the input signal filter to the reference voltage filter to maintain constant conversion noise over the signal operating range.

#### 8.3.4.2 AVDD – AVSS Reference (Default)

A third reference option is the 5-V analog power supply (AVDD – AVSS). Select this reference option by programming the REF register to 05h. For 6-wire strain-gauge bridge applications that use excitation-sense connections, or for ac-bridge excitation operation, connect the excitation sense lines to the reference input pins and program the ADC for external reference operation.

#### 8.3.4.3 Reference Monitor

The ADC incorporates an internal low-voltage monitor of the reference voltage. As shown in Figure 45 and Figure 46, the REFL_ALM bit of the STATUS byte asserts if the reference voltage ($V_{REF} = V_{REFP} – V_{REFN}$) falls below 0.4 V. The alarm is read-only and resets at the next conversion after the low reference condition is no longer present.

Use the reference monitor to detect a missing or failed reference voltage. To implement detection of a missing reference, use a 100-kΩ resistor across the reference inputs. If either reference input is disconnected, the resistor biases the differential reference input toward 0 V so that the reference monitor detects the disconnected reference.

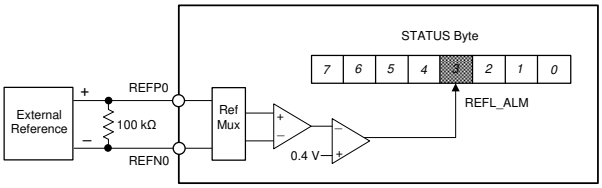



**Figure 45. Reference Monitor**

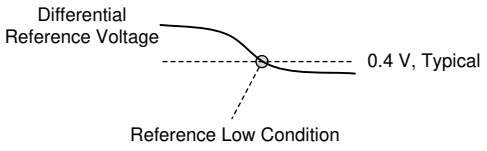



**Figure 46. Reference Monitor Threshold**

### 8.3.5 General-Purpose Input/Outputs (GPIOs)

The ADC includes four GPIO pins, GPIO0 through GPIO3. The GPIOs are digital inputs/outputs that are referenced to analog AVDD and AVSS. The GPIOs are read and written by the GPIO_DAT bits of the MODE3 register. The GPIOs are multiplexed with analog inputs AIN0 to AIN3. As shown in Figure 47, the GPIOs are configured through a series of programming registers. Bits GPIO_CON[3:0] connect the GPIOs to the associated pin (1 = connect). Bits GPIO_DIR program the direction of the GPIOs; (0 = output, 1 = input). The input voltage threshold is the voltage value between AVDD and AVSS. Bits GPIO_DAT[3:0] are the data values for the GPIOs. Observe that if a GPIO pin is programmed as an output, the value read is the value previously written to the register data, not the actual voltage at the pin.

The GPIOs also provide the ac-bridge excitation drive signals. AC-bridge excitation mode overrides the GPIO register data values. See the *AC-Bridge Excitation Mode* section for details.

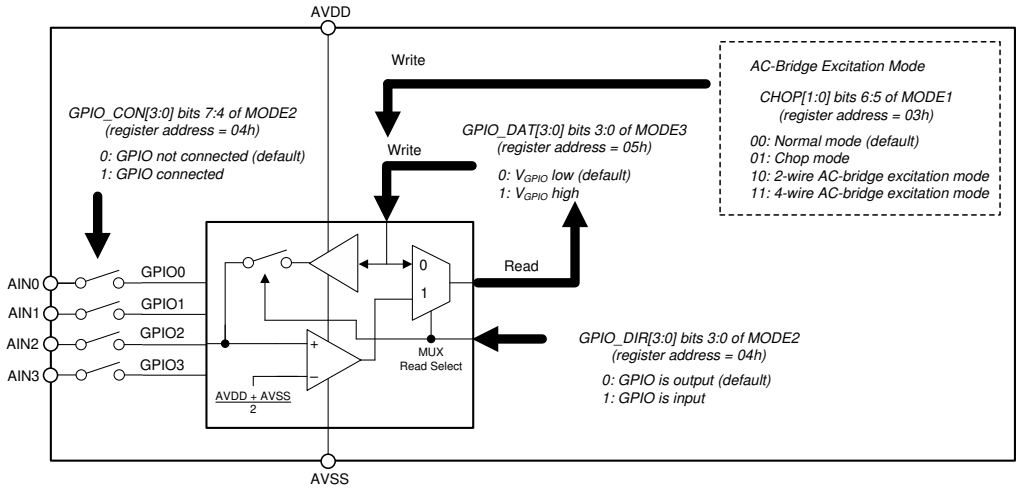



**Figure 47. GPIO Block Diagram**

### 8.3.6 Modulator

The modulator is an inherently stable, fourth-order, 2 + 2 pipelined ΔΣ modulator. The modulator samples the analog input voltage at a high sample rate ($f_{MOD} = f_{CLK} / 8$) and converts the analog input to a ones-density bit-stream with the density given by the ratio of the input signal to the reference voltage. The modulator shapes the noise of the converter to high frequency, where the noise is removed by the digital filter.

### 8.3.7 Digital Filter

The ADC operates on the principle of oversampling. Oversampling is defined as the ratio of the sample rate of the modulator to that of the ADC output data rate. Oversampling improves ADC noise by digital bandwidth limiting (low-pass filtering) of the data.

The digital filter receives the modulator output data and produces a high-resolution conversion result. The digital filter low-pass filters and decimates the modulator data (data rate reduction), yielding the final data output. By adjusting the type of filtering, tradeoffs are made between resolution, data throughput and line-cycle rejection.

The digital filter has two selectable modes: sin (x) / x (sinc) mode and finite impulse response (FIR) mode (see Figure 48). The sinc mode provides data rates of 2.5 SPS through 7200 SPS with variable sinc orders of 1 through 4. The FIR filter provides simultaneous rejection of 50-Hz and 60-Hz frequencies with data rates of 2.5 SPS through 20 SPS while providing single-cycle settled conversions.

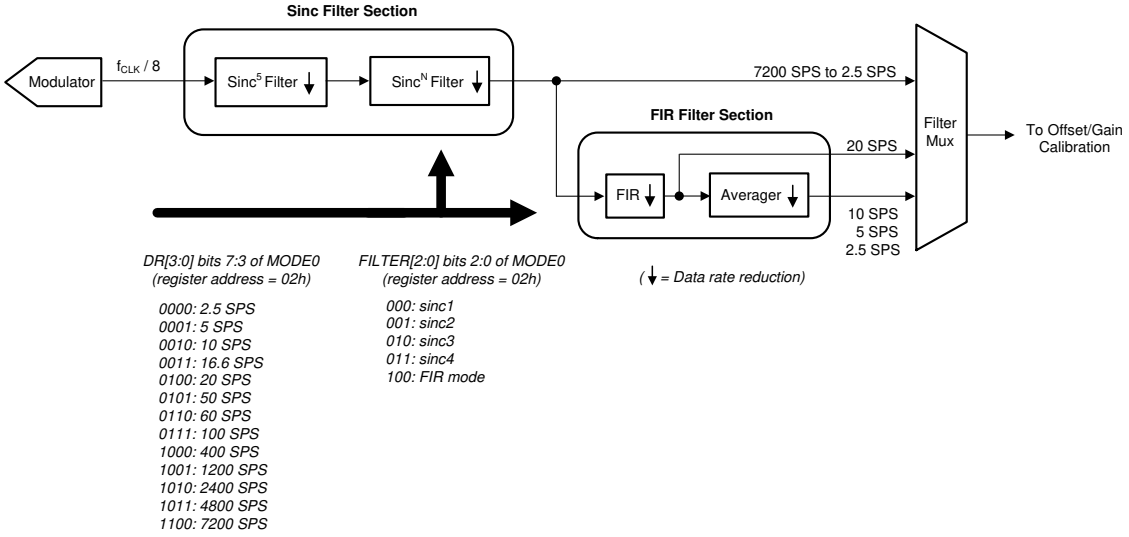



**Figure 48. Digital Filter Block Diagram**

#### *8.3.7.1 Sinc Filter*

The sinc filter is comprised of two stages: a fixed-decimation sinc5 filter, followed by a variable-decimation, variable-order sinc filter. The first stage filters and down-samples the input data from the modulator to produce an intermediate data rate of 14400 SPS. The second stage receives the intermediate data to provide final output data rates of 7200 SPS through 2.5 SPS. The second stage has programmable orders of sinc.

The data rate is programmed by the DR[3:0] bits of the MODE0 register. The filter mode is programmed by the FILTER[2:0] bits of the MODE0 register (see Figure 48).

#### 8.3.7.1.1 Sinc Filter Frequency Response

The overall frequency response of the sinc filter is low pass. The filter reduces signal and noise beginning at the -3-dB bandwidth. Changing the data rate and filter order changes the filter bandwidth together with the rate of frequency roll-off. See the *Filter Bandwidth* section for the bandwidth of the filter settings.

Figure 49 shows the frequency response of the sinc filter at 2400 SPS for various orders of the sinc filter. The peaks and nulls are characteristic of the sinc filter response. The frequency response nulls occur at f (Hz) = N · $f_{DATA}$, where N = 1, 2, 3 and so on. At the null frequencies, the filter has zero gain. The response nulls are superimposed with the larger nulls beginning at 14400 Hz. The larger nulls are produced by the first stage. The frequency response is similar to that of data rates 2.5 SPS through 7200 SPS. Figure 50 shows the frequency response nulls for 10 SPS.

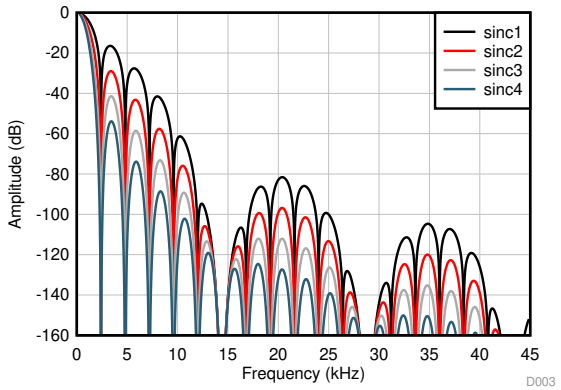



**Figure 49. Sinc Frequency Response (2400 SPS)**

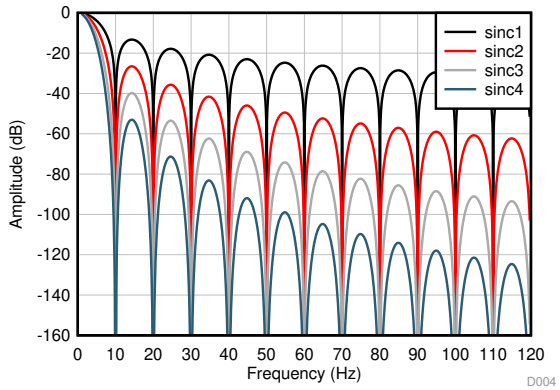



**Figure 50. Sinc Frequency Response (10 SPS)**

Figure 51 and Figure 52 show the frequency response of data rates 50 SPS and 60 SPS, respectively. Increase the attenuation at 50 Hz or 60 Hz and harmonics by increasing the order of the sinc filter, as shown in the figures.

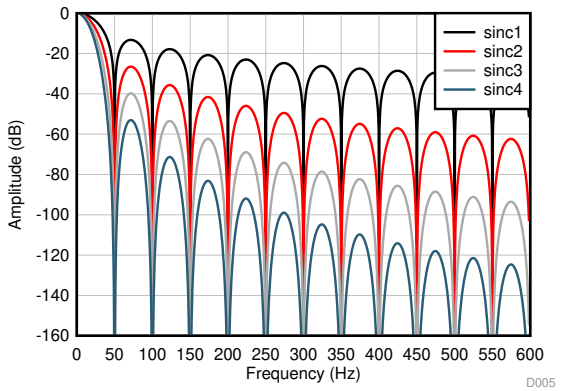



**Figure 51. Sinc Frequency Response (50 SPS)**

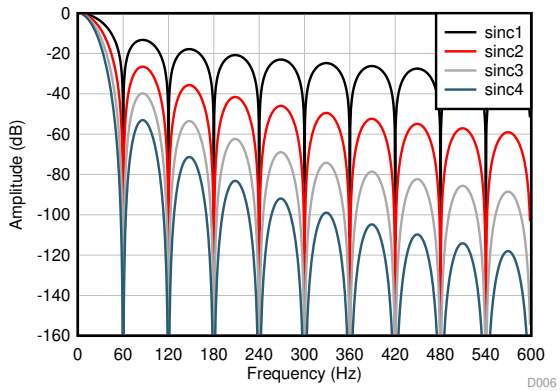



**Figure 52. Sinc Frequency Response (60 SPS)**

Figure 53 and Figure 54 show the detailed frequency response at 50 SPS and 60 SPS, respectively.

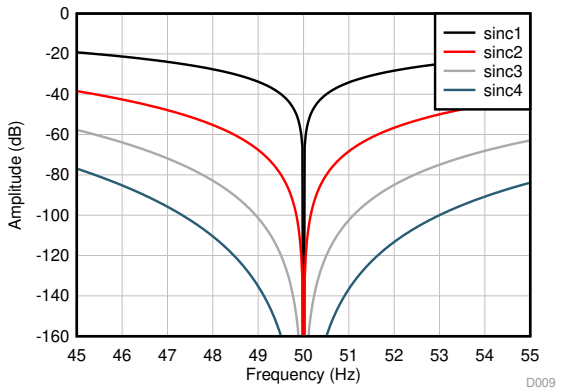



**Figure 53. Detail Sinc Frequency Response (50 SPS)**

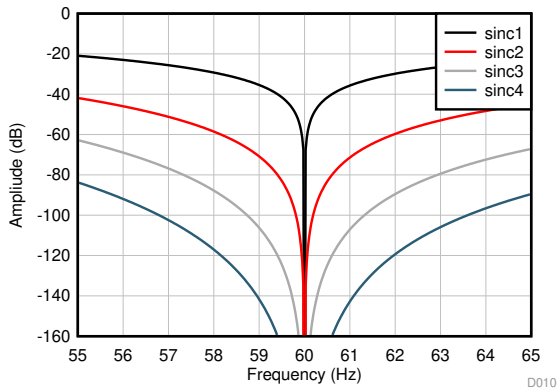



**Figure 54. Detail Sinc Frequency Response (60 SPS)**

### *8.3.7.2 FIR Filter*

The finite impulse response (FIR) filter is a coefficient based filter that provides an overall low-pass filter response. The filter provides simultaneous attenuation of 50 Hz and 60 Hz and harmonics at data rates of 2.5 SPS through 20 SPS. The conversion latency time of the FIR filter data rates is single-cycle. As shown in Figure 48, the FIR filter receives pre-filtered data from the sinc filter. The FIR filter decimates the data to yield the output data rates of 20 SPS. A variable averager (sinc1) provides data rates of 10 SPS, 5 SPS, and 2.5 SPS. Table 4 lists the bandwidth of the data rates in FIR filter mode.

#### 8.3.7.2.1 FIR Filter Frequency Response

Figure 55 and Figure 56 show the FIR filter attenuation at 50 Hz and 60 Hz provided by a series of response nulls placed close to these frequencies. The response nulls are repeated at harmonics of 50 Hz and 60 Hz.

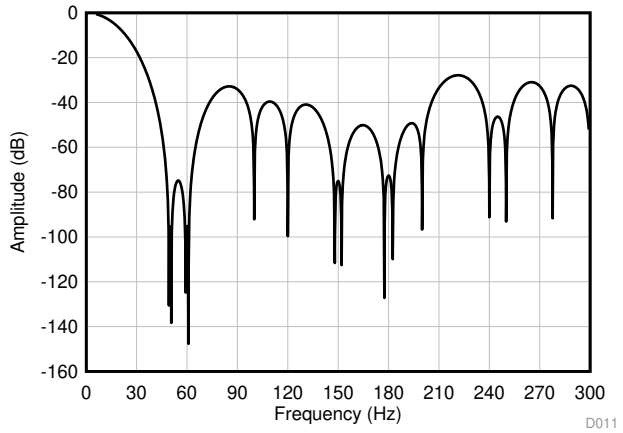



**Figure 55. FIR Frequency Response (20 SPS)**

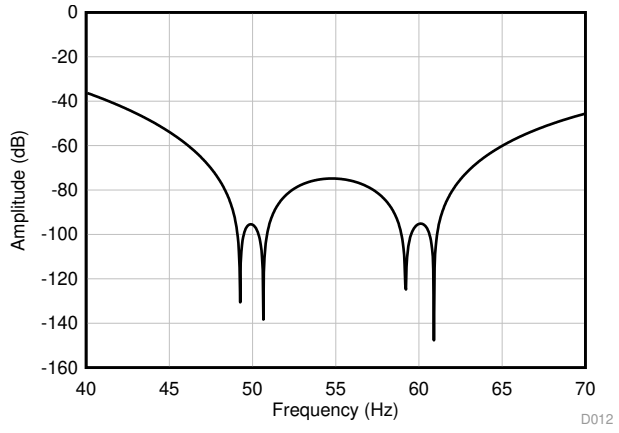



**Figure 56. FIR Frequency Response Detail (20 SPS)**

Figure 57 is the FIR filter response at 10 SPS. As a result of the variable averager used to produce rates of 10 SPS and lower, new frequency nulls are superimposed to the response. The first null appears at the data rate. At 10 SPS, additional nulls occur at frequencies folded around multiples of 20 Hz.

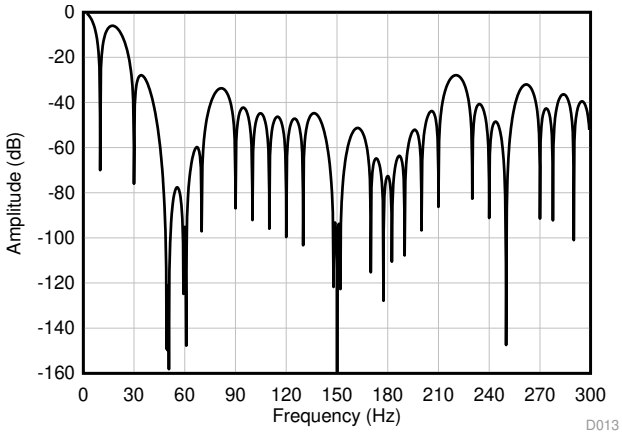



**Figure 57. FIR Frequency Response (10 SPS)**

### *8.3.7.3 Filter Bandwidth*

The bandwidth of the digital filter depends on the data rate, filter type and order. Be aware that the bandwidth of the entire system is the combined response of the digital filter, the antialias filter and the use of external analog filters. Table 4 lists the bandwidth of the digital filter versus data rate and filter mode.

**Table 4. Filter Bandwidth**

| DATA RATE (SPS) | -3-dB BANDWIDTH (Hz) | | | | |
|---|---|---|---|---|---|
| | FIR | SINC1 | SINC2 | SINC3 | SINC4 |
| 2.5 | 1.2 | 1.10 | 0.80 | 0.65 | 0.58 |
| 5 | 2.4 | 2.23 | 1.60 | 1.33 | 1.15 |
| 10 | 4.7 | 4.43 | 3.20 | 2.62 | 2.28 |
| 16.6 | — | 7.38 | 5.33 | 4.37 | 3.80 |
| 20 | 13 | 8.85 | 6.38 | 5.25 | 4.63 |
| 50 | — | 22.1 | 16.0 | 13.1 | 11.4 |
| 60 | — | 26.6 | 19.1 | 15.7 | 13.7 |
| 100 | — | 44.3 | 31.9 | 26.2 | 22.8 |
| 400 | — | 177 | 128 | 105 | 91.0 |
| 1200 | — | 525 | 381 | 314 | 273 |
| 2400 | — | 1015 | 751 | 623 | 544 |
| 4800 | — | 1798 | 1421 | 1214 | 1077 |
| 7200 | — | 2310 | 1972 | 1750 | 1590 |

### 8.3.7.4 50-Hz and 60-Hz Normal Mode Rejection

To reduce 50-Hz and 60-Hz noise interference, configure the data rate and filter to reject noise at 50 Hz and 60 Hz. Table 5 summarizes the 50-Hz and 60-Hz noise rejection versus data rate and filter mode. The table values are based on 2% and 6% tolerance of signal frequency to ADC clock frequency. For the sinc filter, increase noise rejection by increasing the order of the filter. Common-mode noise is also rejected at these frequencies.

**Table 5. 50-Hz and 60-Hz Normal Mode Rejection**

| DATA RATE (SPS) | FILTER TYPE | DIGITAL FILTER RESPONSE (dB) | | | |
|---|---|---|---|---|---|
| | | 50 Hz ±2% | 60 Hz ±2% | 50 Hz ±6% | 60 Hz ±6% |
| 2.5 | FIR | –113 | –99 | –88 | –80 |
| 2.5 | Sinc1 | –36 | –37 | –40 | –37 |
| 2.5 | Sinc2 | –72 | –74 | –80 | –74 |
| 2.5 | Sinc3 | –108 | –111 | –120 | –111 |
| 2.5 | Sinc4 | –144 | –148 | –160 | –148 |
| 5 | FIR | –111 | –95 | –77 | –76 |
| 5 | Sinc1 | –34 | –34 | –30 | –30 |
| 5 | Sinc2 | –68 | –68 | –60 | –60 |
| 5 | Sinc3 | –102 | –102 | –90 | –90 |
| 5 | Sinc4 | –136 | –136 | –120 | –120 |
| 10 | FIR | –111 | –94 | –73 | –68 |
| 10 | Sinc1 | –34 | –34 | –25 | –25 |
| 10 | Sinc2 | –68 | –68 | –50 | –50 |
| 10 | Sinc3 | –102 | –102 | –75 | –75 |
| 10 | Sinc4 | –136 | –136 | –100 | –100 |
| 16.6 | Sinc1 | –34 | –21 | –24 | –21 |
| 16.6 | Sinc2 | –68 | –42 | –48 | –42 |
| 16.6 | Sinc3 | –102 | –63 | –72 | –63 |
| 16.6 | Sinc4 | –136 | –84 | –96 | –84 |
| 20 | FIR | –95 | –94 | –66 | –66 |
| 20 | Sinc1 | –18 | –34 | –18 | –24 |
| 20 | Sinc2 | –36 | –68 | –36 | –48 |
| 20 | Sinc3 | –54 | –102 | –54 | –72 |
| 20 | Sinc4 | –72 | –136 | –72 | –96 |
| 50 | Sinc1 | –34 | –15 | –24 | –15 |
| 50 | Sinc2 | –68 | –30 | –48 | –30 |
| 50 | Sinc3 | –102 | –45 | –72 | –45 |
| 50 | Sinc4 | –136 | –60 | –96 | –60 |
| 60 | Sinc1 | –13 | –34 | –12 | –24 |
| 60 | Sinc2 | –27 | –68 | –24 | –48 |
| 60 | Sinc3 | –40 | –102 | –36 | –72 |
| 60 | Sinc4 | –53 | –136 | –48 | –96 |

## 8.4 Device Functional Modes

### 8.4.1 Conversion Control

Conversions are controlled by either the START pin or by the START command. If using commands to control conversions, keep the START pin low to avoid contentions between pin and commands. Commands take affect on the 16th falling SCLK edge (CRC mode disabled) or on the 32nd falling SCLK edge (CRC mode enabled). See Figure 4 for conversion-control timing details.

The ADC provides two conversion modes: continuous and pulse. The continuous-conversion mode performs conversions indefinitely until stopped by the user. Pulse-conversion mode performs one conversion and then stops. The conversion mode is programmed by the CONVRT bit (bit 4 of register MODE0).

#### *8.4.1.1 Continuous-Conversion Mode*

This conversion mode performs continuous conversions until stopped by the user. To start conversions, take the START pin high or send the START command. $\overline{\text{DRDY}}$ is driven high at the time the conversion is initiated. $\overline{\text{DRDY}}$ is driven low when the conversion data are ready. Conversion data are available to read at that time. Conversions are stopped by taking the START pin low or by sending the STOP command. When conversions are stopped, the conversion in progress runs to completion. To restart a conversion that is in progress, toggle the START pin low-then-high or send a new START command.

#### *8.4.1.2 Pulse-Conversion Mode*

In pulse-conversion mode, the ADC performs one conversion when START is taken high or when the START command is sent. When the conversion completes, further conversions stop. The $\overline{\text{DRDY}}$ output is driven high to indicate the conversion is in progress, and is driven low when the conversion data are ready. Conversion data are available to read at that time. To restart a conversion in progress, toggle the START pin low-then-high or send a new START command. Driving START low or sending the STOP command does not interrupt the current conversion.

#### *8.4.1.3 Conversion Latency*

The digital filter averages data from the modulator in order to produce the conversion result. The stages of the digital filter must have settled data in order to provide fully-settled output data. The order and the decimation ratio of the digital filter determine the amount of data averaged, and in turn, affect the latency of the conversion data. The FIR and sinc1 filter modes are zero latency because the ADC provides the conversion result in one conversion cycle. Latency time is an important consideration for the data throughput rate in multiplexed applications.

Table 6 lists the conversion latency values of the ADC. Conversion latency is defined as the time from the start of the first conversion, by taking the START pin high or sending the START command, to the time when fully settled conversion data are ready. If the input signal is settled, then the ADC provides fully settled data. The conversion latency values listed in the table are with the start-conversion delay parameter = 50 µs, and include the overhead time needed to process the data. After the first conversion completes (in continuous conversion mode), the period of the following conversions are equal to $1/f_{DATA}$. The first conversion latency in chop and ac-excitation modes are twice the values listed in the table. Also when operating in these modes, the period of following conversions are equal to the values listed in the table.

## Device Functional Modes (continued)

**Table 6. Conversion Latency**

| DATA RATE (SPS) | CONVERSION LATENCY - $t_{(STDR)}$ (1) (ms) | | | | |
|---|---|---|---|---|---|
| | FIR | SINC1 | SINC2 | SINC3 | SINC4 |
| 2.5 | 402.2 | 400.4 | 800.4 | 1,200 | 1,600 |
| 5 | 202.2 | 200.4 | 400.4 | 600.4 | 800.4 |
| 10 | 102.2 | 100.4 | 200.4 | 300.4 | 400.4 |
| 16.6 | — | 60.43 | 120.4 | 180.4 | 240.4 |
| 20 | 52.23 | 50.43 | 100.4 | 150.4 | 200.4 |
| 50 | — | 20.43 | 40.43 | 60.43 | 80.43 |
| 60 | — | 17.09 | 33.76 | 50.43 | 67.09 |
| 100 | — | 10.43 | 20.43 | 30.43 | 40.43 |
| 400 | — | 2.925 | 5.425 | 7.925 | 10.43 |
| 1200 | — | 1.258 | 2.091 | 2.925 | 3.758 |
| 2400 | — | 0.841 | 1.258 | 1.675 | 2.091 |
| 4800 | — | 0.633 | 0.841 | 1.050 | 1.258 |
| 7200 | — | 0.564 | 0.702 | 0.841 | 0.980 |

(1) Chop mode off, conversion-start delay = 50 µs (DELAY[3:0] = 0001)

If the input signal changes while free-running conversions, the conversion data are a mix of old and new data, as shown in Figure 58. After an input change, the number of conversion periods required for fully settled data are determined by dividing the conversion latency by the period of the data rate, plus add one conversion period to the result. In chop and ac-bridge excitation modes, use twice the latency values listed in the table.

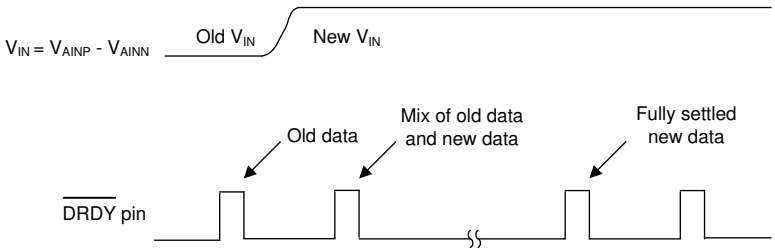



**Figure 58. Input Change During Conversions**

### *8.4.1.4 Start-Conversion Delay*

Some applications require a delay at the start of a conversion in order to allow settling time for the PGA antialias filter or to allow time after input and configuration changes. The ADC provides a user programmable delay time that delays the start of a new conversion. The default value is 50 µs. 50 µs allows for settling of the antialiasing filter placed at the PGA output. Use additional delay time as needed to provide settling time for external components. The delay time increases the conversion latency values listed in Table 6. As an alternative to the programmable start-conversion delay, manually delay the start of conversion after input and configuration changes.

Start-conversion delay is an important consideration for operation in ac-bridge excitation mode. In this mode, the reference inputs to the bridge, and therefore, the bridge output signals are reversed for each conversion. As a result, time delay is required to allow for settling of external filter components after the bridge voltage is reversed. As a general guideline, set the start-conversion delay parameter to a minimum of 15 times the R-C time constant of the signal input and reference input filters.

### 8.4.2 Chop Mode

The PGA and modulator are chopper-stabilized at high frequency in order to reduce offset voltage, offset voltage drift and 1/f noise. The offset and noise artifacts are modulated to a high frequency by the chop operation, which are removed by the digital filter. Although chopper stabilization is designed to remove all offset, a small offset voltage may remain. The optional *global* chop mode removes the remaining offset errors, providing near zero offset voltage drift performance.

Chop mode alternates the signal polarity between consecutive conversions in order to remove offset. The ADC subtracts consecutive, alternate-polarity conversions to yield the final conversion data. The result of subtraction removes the offset.

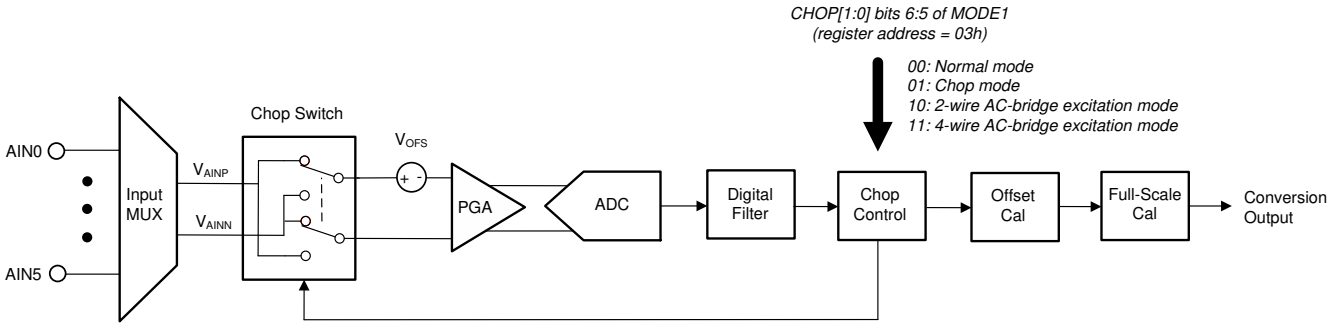



**Figure 59. ADC Chop Mode**

As shown in Figure 59, the internal chop switch reverses the signal after the input multiplexer. $V_{OFS}$ models the internal offset voltage. The operational sequence of chop mode is as follows:

**Conversion C1**: $V_{AINP} – V_{AINN} – V_{OFS} \rightarrow$ First conversion withheld after start

**Conversion C2**: $V_{AINN} – V_{AINP} – V_{OFS} \rightarrow$ Output 1 = (C1 – C2) / 2 = $V_{AINP} – V_{AINN}$

**Conversion C3:** $V_{AINP} – V_{AINN} – V_{OFS} \rightarrow$ Output 2 =-(C3 – C2) / 2 = $V_{AINP} – V_{AINN}$

The sequence repeats for all conversions. Because of the required settling time to alternate the internal polarity, the effective data rate in chop mode operation is reduced. The chop mode data rate is proportional to the order of the sinc filter. Referring to Table 6, the new data rate is equal to 1 / latency values; and be aware the chop mode first conversion latency is 2 × latency values. As a consequence of the internal data subtraction, two data points are effectively averaged together. Averaging of data reduces noise by $\sqrt{2}$. Divide the noise data values shown in Table 1 by $\sqrt{2}$ to derive the chop mode noise performance data. The null frequencies of the digital filter are not changed in chop-mode operation. However, new null frequencies appear at multiples of $f_{DATA}$ / 2 as a result of averaging.

### 8.4.3 AC-Bridge Excitation Mode

Resistive bridge sensors are excited by dc or ac voltages; or by dc or ac currents. DC voltage excitation is the most common type of excitation. AC excitation reverses the polarity of the excitation voltage by the use of external switching components. Similar in concept to chop mode, the result of the voltage reversal removes offset voltage in the connections leading from the bridge to the ADC inputs. This also includes the offset voltage of the ADC itself. The ADC provides the signals necessary to drive the external switching components in order to reverse the bridge voltage.

The timing of the drive signals is synchronized to the ADC conversion phase. During one conversion phase, the voltage polarity is normal. For the alternate conversion phase, the voltage polarity is reversed. The ADC compensates the reversed polarity conversion by internal reversing the reference voltage. The ADC subtracts the data corresponding to the normal and reverse phases in order to remove offset voltage from the input.

The ADC output drive signals are non-overlapping in order to avoid bridge cross-conduction that can otherwise occur during excitation voltage reversal. The switch rate of the ac-excitation drive signals are performed at the data rate to avoid unnecessary fast switching. See Figure 7 for output drive timing.

Table 7 shows the ac-bridge excitation drive signals and the associated GPIO pins. Program the ac-bridge excitation mode using the CHOP[1:0] bits in register MODE1. AC-bridge excitation can be programmed for two-wire or four-wire drive mode. For two-wire operation, two drive signals are provided on the GPIOs. If needed, use two external inverters to derive four signals to drive discrete transistors. The GPIO drive levels are referred to the 5-V analog supply. Be aware that the ac-bridge excitation mode changes the nominal data rate, depending on the order of the sinc filter. See the *Chop Mode* section for details of the effective data rate.

**Table 7. AC-Bridge Excitation Drive Pins**

| DEVICE PIN | GPIO | 2-WIRE MODE (CHOP[1:0] = 10) | 4-WIRE MODE (CHOP[1:0] = 11) |
|---|---|---|---|
| AIN0 | GPIO0 | $\overline{\text{ACX1}}$ | $\overline{\text{ACX1}}$ |
| AIN1 | GPIO1 | $\overline{\text{ACX2}}$ | $\overline{\text{ACX2}}$ |
| AIN2 | GPIO2 | — | ACX1 |
| AIN3 | GPIO3 | — | ACX2 |

### 8.4.4 ADC Clock Mode

Operate the ADC with an external clock or with the internal oscillator. The clock frequency is 7.3728 MHz. For external clock operation, apply the clock signal to CLKIN. For internal-clock operation, connect CLKIN to DGND. The internal oscillator begins operation immediately at power-up. The ADC automatically selects the clock mode of operation. Read the clock mode bit in the STATUS register to determine the clock mode.

### 8.4.5 Power-Down Mode

The ADC has two power-down modes: hardware and software. In both power-down modes, the digital outputs remain driven. The digital inputs must be maintained at $V_{IH}$ or $V_{IL}$ levels (do not float the digital inputs). The internal low-dropout regulator remains on, drawing 25 µA (typical) from DVDD.

#### *8.4.5.1 Hardware Power-Down*

Take the $\overline{\text{PWDN}}$ pin low to engage hardware power-down mode. Except for the internal LDO, all ADC functions are disabled. To exit hardware power-down mode (wake-up) take the $\overline{\text{PWDN}}$ pin high. The register values are not reset at wake-up.

#### *8.4.5.2 Software Power-Down*

Set the PWDN bit (bit 7 of register MODE3) to engage software power-down mode. Similar to the operation of hardware power-down mode, software mode powers down the internal functions except in this case the serial interface. Exit the software power-down mode by clearing the PWDN bit. The register values are not reset.

### 8.4.6 Reset

The ADC is reset in three ways: at power-on, by the $\overline{\text{RESET}}$ pin, and by the RESET command. When reset, the serial interface, conversion-control logic, digital filter, and register values are reset. The RESET bit of the STATUS byte is set to indicate a device reset has occurred by any of the three reset methods. Clear the bit to detect the next device reset. If the START pin is high after reset, the ADC begins conversions.

#### *8.4.6.1 Power-on Reset*

At power-on, after the supply voltages cross the reset-voltage thresholds, the ADC is reset and $2^{16}$ $f_{CLK}$ cycles later the ADC is ready for communication. Until this time, $\overline{\text{DRDY}}$ is held low. $\overline{\text{DRDY}}$ is driven high to indicate when the ADC is ready for communication. If the START pin is high, the conversion cycle starts 512 / $f_{CLK}$ cycles after $\overline{\text{DRDY}}$ asserts high. Figure 5 shows the power-on reset behavior.

#### *8.4.6.2 Reset by Pin*

Reset the ADC by taking the $\overline{\text{RESET}}$ pin low and then returning the pin high. After reset, the conversion starts 512 / $f_{CLK}$ cycles later. See Figure 6 for RESET timing.

#### 8.4.6.3 Reset by Command

Reset the ADC by the RESET command. Toggle $\overline{CS}$ high to make sure the serial interface resets before sending the command. For applications that tie $\overline{CS}$ low, see the *Serial Interface Auto-Reset* section for information on how to reset the serial interface. After reset, the conversion starts 512 / $f_{CLK}$ cycles later. See Figure 6 for timing details.

### 8.4.7 Calibration

The ADC incorporates calibration registers and associated commands to calibrate offset and full-scale errors. Calibrate by using calibration commands, or calibrate by writing to the calibration registers directly (user calibration). To calibrate by command, send the offset or full-scale calibration commands. To user calibrate, write values to the calibration registers based on calculations of the conversion data. Perform offset calibration before full-scale calibration.

#### 8.4.7.1 Offset and Full-Scale Calibration

Use the offset and full-scale (gain) registers to correct offset or full-scale errors, respectively. As shown in Figure 60, the offset calibration register is subtracted from the output data before multiplication by the full-scale register, which is divided by 400000h. After the calibration operation, the final output data are clipped to 24 bits.

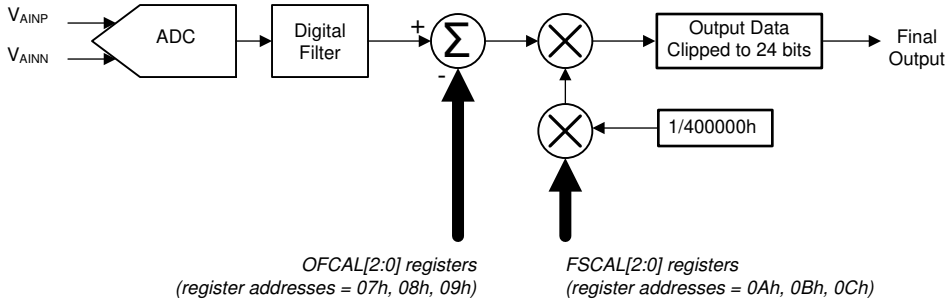



**Figure 60. Calibration Block Diagram**

Equation 4 shows the internal calibration.

$$\text{Final Output Data} = (\text{Filter Output} - \text{OFCAL}[2:0]) \cdot \text{FSCAL}[2:0] / 400000\text{h} \quad (4)$$

##### 8.4.7.1.1 Offset Calibration Registers

The offset calibration word is 24 bits, consisting of three 8-bit registers, as listed in Table 8. The offset value is subtracted from the conversion result. The offset value is in two's complement format with a maximum positive value equal to 7FFFFFh, and a maximum negative value equal to 800000h. A register value equal to 000000h has no offset correction. Although the offset calibration register provides a wide range of possible offset values, the input signal after calibration cannot exceed ±106% of the pre-calibrated range; otherwise, the ADC is overranged. Table 9 lists example values of the offset register.

**Table 8. Offset Calibration Registers**

| REGISTER | BYTE ORDER | ADDRESS | BIT ORDER | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| OFCAL0 | LSB | 07h | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 (LSB) |
| OFCAL1 | MID | 08h | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
| OFCAL2 | MSB | 09h | B23 (MSB) | B22 | B21 | B20 | B19 | B18 | B17 | B16 |

**Table 9. Offset Calibration Register Values**

| OFCAL[2:0] REGISTER VALUE | IDEAL OUTPUT VALUE(1) |
|---|---|
| 000001h | FFFFFFh |
| 000000h | 000000h |
| FFFFFFh | 000001h |

(1) Output value with no offset error

#### 8.4.7.1.2 Full-Scale Calibration Registers

The full-scale calibration word is 24 bits consisting of three 8-bit registers, as listed in Table 10. The full-scale calibration value is in straight-binary format, normalized to a unity-gain factor at a value of 400000h. Table 11 lists register values for selected gain factors. Gain errors greater than unity are corrected by using full-scale values less than 400000h. Although the full-scale register provides a wide range of possible values, the input signal after calibration must not exceed ±106% of the precalibrated input range; otherwise, the ADC is overranged.

**Table 10. Full-Scale Calibration Registers**

| REGISTER | BYTE ORDER | ADDRESS | BIT ORDER | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| FSCAL0 | LSB | 0Ah | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 (LSB) |
| FSCAL1 | MID | 0Bh | B15 | B14 | B13 | B12 | B11 | B10 | B9 | B8 |
| FSCAL2 | MSB | 0Ch | B23 (MSB) | B22 | B21 | B20 | B19 | B18 | B17 | B16 |

**Table 11. Full-Scale Calibration Register Values**

| FSCAL[2:0] REGISTER VALUE | GAIN FACTOR |
|---|---|
| 433333h | 1.05 |
| 400000h | 1.00 |
| 3CCCCCh | 0.95 |

### *8.4.7.2 Offset Self-Calibration (SFOCAL)*

The offset self-calibration command corrects offset errors internal to the ADC. When the offset self-calibration command is sent, the ADC disconnects the external inputs, shorts the inputs to the PGA, and then averages 16 conversion results to compute the calibration value. Averaging the data reduces conversion noise to improve calibration accuracy. When calibration is complete, the ADC restores the user input and performs one conversion using the new calibration value.

### *8.4.7.3 Offset System-Calibration (SYOCAL)*

The offset system-calibration command corrects system offset errors. For this type of calibration, the user shorts the inputs to either the ADC or to the system. When the command is sent, the ADC averages 16 conversion results to compute the calibration value. Averaging the data reduces conversion noise to improve calibration accuracy. When calibration is complete, the ADC performs one conversion using the new calibration value.

### *8.4.7.4 Full-Scale Calibration (GANCAL)*

The full-scale calibration command corrects gain error. To calibrate, apply a positive full-scale calibration voltage to the ADC, wait for the signal to settle, and then send the calibration command. The ADC averages 16 conversion results to compute the calibration value. Averaging the data reduces conversion noise to improve calibration accuracy. The ADC computes the full-scale calibration value so that the calibration voltage is scaled to positive full scale output code. When calibration is complete, the ADC performs one new conversion using the new calibration value.

#### 8.4.7.5 Calibration Command Procedure

Use the following procedure to calibrate using commands. The register-lock mode must be UNLOCK for all calibration commands. After power-on, make sure the reference voltage has stabilized before calibrating. Perform offset calibration before full-scale calibration.

1. Configure the ADC as required.
2. Apply the appropriate calibration signal (zero or full-scale)
3. Take the START pin high or send the START command to start conversions. $\overline{\text{DRDY}}$ is driven high.
4. Before the conversion cycle completes, send the calibration command. Keep $\overline{\text{CS}}$ low otherwise the command is cancelled. Send no other commands during the calibration period.
5. Calibration time depends on the data rate and digital filter mode. See Table 12. $\overline{\text{DRDY}}$ asserts low when calibration is complete. The offset or full-scale calibration registers are updated with new values. At calibration completion, new conversion data are ready using the new calibration value.

**Table 12. Calibration Time (ms)**

| DATA RATE (SPS) | FILTER MODE (1) | | | | |
|---|---|---|---|---|---|
| | FIR | SINC1 | SINC2 | SINC3 | SINC4 |
| 2.5 | 6805 | 6801 | 7601 | 8401 | 9201 |
| 5 | 3405 | 3401 | 3801 | 4201 | 4601 |
| 10 | 1705 | 1701 | 1901 | 2101 | 2301 |
| 16.6 | — | 1021 | 1141 | 1261 | 1381 |
| 20 | 854.5 | 850.9 | 951.0 | 1051 | 1151 |
| 50 | — | 340.9 | 380.9 | 420.9 | 460.9 |
| 60 | — | 284.2 | 317.5 | 350.9 | 384.2 |
| 100 | — | 170.9 | 190.9 | 210.9 | 230.9 |
| 400 | — | 43.36 | 48.36 | 53.36 | 58.36 |
| 1200 | — | 15.02 | 16.69 | 18.36 | 20.02 |
| 2400 | — | 7.938 | 8.772 | 9.605 | 10.44 |
| 4800 | — | 4.397 | 4.813 | 5.230 | 5.647 |
| 7200 | — | 3.216 | 3.494 | 3.772 | 4.050 |

(1) Nominal clock frequency. Chop and AC-Excitation modes disabled.

#### 8.4.7.6 User Calibration Procedure

To user calibrate, apply the calibration voltage, acquire conversion data, and compute the calibration value. The computed value is written to the corresponding calibration registers. Before starting calibration, preset the offset and full-scale registers to 000000h and 400000h, respectively.

To offset calibrate, short the ADC inputs (or inputs to the system) and average n number of the conversion results. Averaging conversion data reduces noise to improve calibration accuracy. Write the averaged value of the conversion data to the offset registers.

To gain calibrate using a full scale calibration voltage, temporarily reduce the full scale register 95% to avoid output clipped codes (set FSCAL[2:0] to 3CCCCCh). Acquire n number of conversions and average the conversions to reduce noise to improve calibration accuracy. Compute the full-scale calibration value as shown in Equation 5:

$$\text{Full-Scale Calibration Value} = \text{Expected Code} / \text{Actual Code} \cdot 400000\text{h} \quad (5)$$

where

- Expected code = 799998h using full scale calibration signal and 95% scale factor

## 8.5 Programming

### 8.5.1 Serial Interface

The serial interface is SPI-compatible and is used to read conversion data, configure registers, and control the ADC. The serial interface consists of four control lines: $\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$. Most microcontroller SPI peripherals can operate with the ADC. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated or changed on SCLK rising edges; data are latched or read on SCLK falling edges. Timing details of the SPI protocol are found in Figure 1 and Figure 2.

#### *8.5.1.1 Chip Select ($\overline{CS}$)*

$\overline{CS}$ is an active-low input that selects the serial interface for communication. $\overline{CS}$ must be low during the entire data transaction. When $\overline{CS}$ is taken high, the serial interface resets, SCLK input activity is ignored (blocking commands), and DOUT/$\overline{DRDY}$ enters the high-impedance state. The operation of $\overline{DRDY}$ is not effected by $\overline{CS}$. If the ADC is a single device connected to the serial bus, $\overline{CS}$ can be tied low in order to reduce the serial interface to three lines.

#### *8.5.1.2 Serial Clock (SCLK)*

SCLK is the serial clock input that shifts data into and out of the ADC. Output data are updated on the rising edge of SCLK and input data are latched on the falling edge of SCLK. Return SCLK low after the data operation is completed. SCLK is a Schmidt-triggered input designed to improve noise immunity. Even though SCLK is noise resistant, keep SCLK as noise-free as possible to avoid unintentional SCLK transitions. Avoid ringing and overshoot on the SCLK input. Place a series termination resistor close to the SCLK drive pin to reduce ringing.

#### *8.5.1.3 Data Input (DIN)*

DIN is the serial data input to the ADC. DIN is used to input commands and register data to the ADC. Data are latched on the falling edge of SCLK.

#### *8.5.1.4 Data Output/Data Ready (DOUT/$\overline{DRDY}$)*

The DOUT/$\overline{DRDY}$ pin is a dual-function output. The functions of this pin are data output and data ready. The functionality changes automatically based on whether a read data operation is in progress. During a read data operation, the functionality is data output. After the read operation is complete, the functionality changes to data ready.

In data output mode, data are updated on the SCLK rising edge, therefore the host latches the data on the falling edge of SCLK. In data-ready mode, the pin functions the same as $\overline{DRDY}$ (if $\overline{CS}$ is low) by asserting low when data are ready. Therefore, monitor either DOUT/$\overline{DRDY}$ or $\overline{DRDY}$ to determine when data are ready. When $\overline{CS}$ is high, the DOUT/$\overline{DRDY}$ pin is in the high-impedance mode (tri-state).

#### *8.5.1.5 Serial Interface Auto-Reset*

The serial interface is reset by taking $\overline{CS}$ high. Applications that tie $\overline{CS}$ low do not have the ability to reset the serial interface by $\overline{CS}$. If a false SCLK occurs (for example, caused by a noise pulse or clocking glitch), the serial interface may inadvertently advance one or more bit positions, resulting in loss of synchronization to the host. If loss of synchronization occurs, the ADC interface does not respond correctly until the interface is reset.

For applications that tie $\overline{CS}$ low, the serial interface auto-reset feature recovers the interface in the event that an unintentional SCLK glitch occurs. When the first SCLK low-to-high transition occurs (either caused by a glitch or by normal SCLK activity), seven SCLK transitions must occur within 65536 $f_{CLK}$ cycles (8.9 ms) to complete the byte transaction, otherwise the serial interface resets. After reset, the interface is ready to begin the next byte transaction. If the byte transaction is completed within the 65536 $f_{CLK}$ cycles, the serial interface does not reset. The cycle of SCLK detection re-starts at the next rising edge of SCLK. The serial interface is reset by holding SCLK low for a minimum 65536 $f_{CLK}$ cycles.

The auto-reset function is enabled by the SPITIM bit (default is off). See Figure 3 for timing details.

## Programming (continued)

### 8.5.2 Data Ready ($\overline{\text{DRDY}}$)

$\overline{\text{DRDY}}$ is an output that asserts low when conversion data are ready. After power-up, $\overline{\text{DRDY}}$ also indicates when the ADC is ready for communication. The operation of $\overline{\text{DRDY}}$ depends on the conversion mode (continuous or pulse) and whether the conversion data are retrieved or not. Figure 61 shows $\overline{\text{DRDY}}$ operation with and without data retrieval in the two modes of conversion.

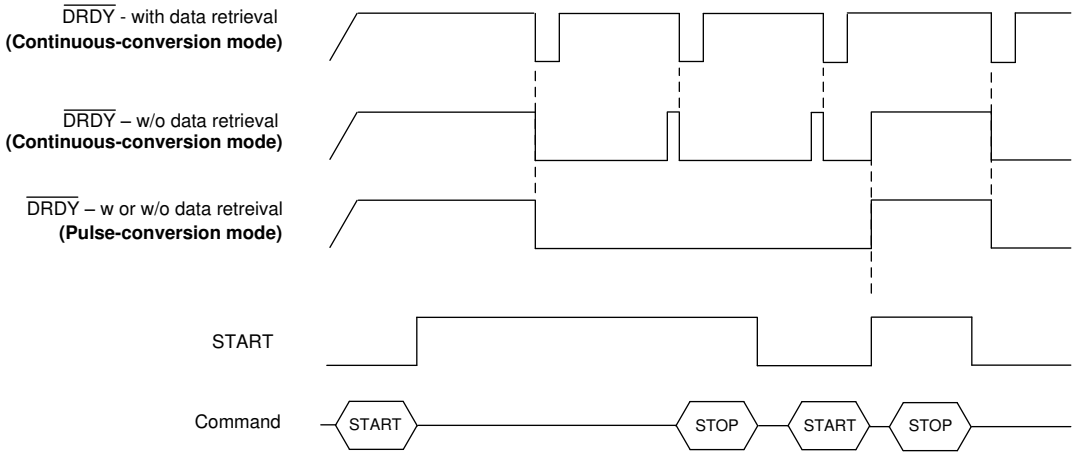



**Figure 61. $\overline{\text{DRDY}}$ Operation**

#### *8.5.2.1 $\overline{\text{DRDY}}$ in Continuous-Conversion Mode*

In continuous-conversion mode, $\overline{\text{DRDY}}$ is driven high when conversions are started and is driven low when conversion data are ready. During data readback, $\overline{\text{DRDY}}$ returns high at the end of the read operation. If the conversion data are not read, $\overline{\text{DRDY}}$ pulses high 16 $f_{CLK}$ cycles prior to the next falling edge.

To read conversion data before the next conversion is ready, send the complete read-data command 16 $f_{CLK}$ cycles before the next $\overline{\text{DRDY}}$ falling edge. If the readback command is sent less than 16 $f_{CLK}$ cycles before the $\overline{\text{DRDY}}$ falling edge, either old or new conversion data are provided, depending on the timing of when the command is sent. In the case that old conversion data are provided, $\overline{\text{DRDY}}$ driven low is delayed until after the read data operation is completed. In this case, the DRDY bit of the STATUS byte is cleared to indicate the same data have been read. If new conversion data are provided, $\overline{\text{DRDY}}$ transitions low at the normal period of the data rate. In this case, the DRDY bit of the STATUS byte is set to indicate that new data have been read. To make sure new data are read back, wait until $\overline{\text{DRDY}}$ asserts low before starting the data read operation.

#### *8.5.2.2 $\overline{\text{DRDY}}$ in Pulse-Conversion Mode*

$\overline{\text{DRDY}}$ is driven high at conversion start and is driven low when the conversion data are ready. During the data read operation $\overline{\text{DRDY}}$ remains low until a new conversion is started.

#### *8.5.2.3 Data Ready by Software Polling*

Use software polling of data ready in lieu of hardware polling of $\overline{\text{DRDY}}$ or DOUT/$\overline{\text{DRDY}}$. To software poll, read the STATUS register and poll the DRDY bit. In order to not skip conversion data in continuous conversion mode, poll the bit at least as often as the period of the data rate. If the DRDY bit is set, then conversion data are new since the previous data read operation. If the bit is cleared, conversion data are not new since the previous data read operation. In this case, the previous conversion data are returned.

### 8.5.3 Conversion Data

Conversion data are read by the RDATA command. To read data, take $\overline{\text{CS}}$ low and issue the read data command. The data field response consists of the optional STATUS byte, three data bytes, and the optional CRC byte. The CRC is computed over the combination of status byte and conversion data bytes. See the RDATA Command for details to read conversion data.

## Programming (continued)

### 8.5.3.1 Status byte (STATUS)

The status byte contains information on the operating state of the ADC. The STATUS byte is included with the conversion data by enabling bit STATENB of register MODE3. Optionally, read the STATUS register to directly determine status information without the need to read conversion data. See Figure 67 for details.

### 8.5.3.2 Conversion Data Format

The conversion data are 24 bits, in two's-complement format to represent positive and negative values. The data output begins with the most significant bit (sign bit) first. The data are scaled so that $V_{IN}$ = 0 V results in an uncalibrated code value of 000000h; positive full scale equals 7FFFFFh and negative full scale equals 800000h; see Table 13 for the uncalibrated code values. The data are clipped to 7FFFFFh (positive full scale) and 800000h (negative full scale) during positive and negative signal overdrive, respectively.

**Table 13. ADC Conversion Data Codes**

| DESCRIPTION | INPUT SIGNAL (V) | 24-BIT CONVERSION DATA (1) |
|---|---|---|
| Positive Full Scale | ≥ $V_{REF}$ / Gain · ($2^{23}$ - 1) / $2^{23}$ | 7FFFFFh |
| 1 LSB | $V_{REF}$ / (Gain · $2^{23}$ ) | 000001h |
| Zero scale | 0 | 000000h |
| -1 LSB | –$V_{REF}$ / (Gain · $2^{23}$ ) | FFFFFFh |
| Negative Full Scale | ≤ –$V_{REF}$ / Gain | 800000h |

(1) Ideal (calibrated) conversion data

### 8.5.4 CRC

Cyclic redundancy check (CRC) is an error checking code that detects communication errors to and from the host. CRC is the division remainder of the data payload bytes by a fixed polynomial. The data payload is 1, 2, 3 or 4 bytes depending on the data operation. The CRC mode is optional and is enabled by the CRCENB bit. See Table 33 to program the CRC mode.

The user computes the CRC corresponding to the two command bytes and appends the CRC to the command string (3rd byte). A 4th, zero-value byte completes the command field. The ADC repeats the CRC calculation and compares the calculation to the received CRC. If the user and repeated CRC values match, the command executes and the ADC responds by transmitting the repeated CRC during the 4th byte of the command. If the operation is conversion data or register data read, the ADC responds with a 2nd CRC that is computed over the requested data payload bytes. The response data payload is 1, 3, or 4 bytes depending on the data operation.

If the user and repeated CRC values do not match, the command does not execute and the ADC responds with an inverted CRC for the actual received command bytes. The inverted CRC is intended to signal the host of the failed operation. The user terminates transmission of the command bytes to match the action of ADC termination. The CRCERR bit is set in the STATUS register when a CRC error is detected. The ADC is ready to accept the next command after a CRC error occurs at the end of the 4th byte.

The CRC data byte is the 8-bit remainder of the bitwise exclusive-OR (XOR) operation of the argument by a CRC polynomial. The CRC polynomial is based on the CRC-8-ATM (HEC): $X^8 + X^2 + X^1 + 1$. The nine binary polynomial coefficients are: 100000111. The CRC calculation is preset with "1" data values.

The CRC mnemonics apply to the following command sections.

- CRC-2: Input CRC of command bytes 1 and 2. Except for WREG command, the value of byte 2 is arbitrary
- Out CRC-1: Output CRC of one register data byte
- Out CRC-2: Output CRC of two command bytes, inverted value if input CRC error detected
- Out CRC-3: Output CRC of three conversion data bytes
- Out CRC-4: Output CRC of three conversion data bytes plus STATUS byte
- Echo Byte 1: Echo of received input byte 1
- Echo Byte 2: Echo of received input byte 2

### 8.5.5 Commands

Commands read conversion data, control the ADC, and read and write register data. See Table 14 for the list of commands. Send only the commands that are listed in Table 14. The ADC executes commands at completion of the 2nd byte (no CRC verification) or at completion of the 4th byte (with CRC verification). Follow the two byte or four byte format according to the CRC mode. Except for register write commands, the value of the second command byte is arbitrary but the value is included in the CRC calculation (total of two-byte CRC). If a CRC error is detected, the ADC does not execute the command. Taking $\overline{CS}$ high before the command is completed results in termination of the command. When $\overline{CS}$ is taken low, the communication frame is reset to begin a new command.

**Table 14. Command Byte Summary**

| MNEMONIC | DESCRIPTION | BYTE 1 | BYTE 2 | BYTE 3 (CRC Mode Only) | BYTE 4 (CRC Mode only) |
|---|---|---|---|---|---|
| **Control Commands** | | | | | |
| NOP | No operation | 00h | Arbitrary | CRC-2 | 00h |
| RESET | Reset | 06h | Arbitrary | CRC-2 | 00h |
| START | Start conversion | 08h | Arbitrary | CRC-2 | 00h |
| STOP | Stop conversion | 0Ah | Arbitrary | CRC-2 | 00h |
| **Read Data Command** | | | | | |
| RDATA | Read conversion data | 12h | Arbitrary | CRC-2 | 00h |
| **Calibration Commands** | | | | | |
| SYOCAL | System offset calibration | 16h | Arbitrary | CRC-2 | 00h |
| GANCAL | Gain calibration | 17h | Arbitrary | CRC-2 | 00h |
| SFOCAL | Self offset calibration | 19h | Arbitrary | CRC-2 | 00h |
| **Register Commands** | | | | | |
| RREG | Read register data | 20h + rrh(1) | Arbitrary | CRC-2 | 00h |
| WREG | Write register data | 40h + rrh(1) | Register data | CRC-2 | 00h |
| **Protection Commands** | | | | | |
| LOCK | Register lock | F2h | Arbitrary | CRC-2 | 00h |
| UNLOCK | Register unlock | F5h | Arbitrary | CRC-2 | 00h |

(1) rrh = 5-bit register address.

#### *8.5.5.1 NOP Command*

This command is no operation. Use the NOP command to validate the CRC response byte and error detection without affecting normal operation. Table 15 shows the NOP command byte sequence.

**Table 15. NOP Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 00h | Arbitrary | | |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 00h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 |

#### 8.5.5.2 RESET Command

The RESET command resets ADC operation and resets the registers to default values. See the *Reset by Command* section for details. Table 16 shows the RESET command byte sequence.

**Table 16. RESET Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 06h | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 06h | Arbitrary | CRC-2 | 00H |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 |

#### 8.5.5.3 START Command

This command starts conversions. See the *Conversion Control* section for details. Table 17 shows the START command byte sequence.

**Table 17. START Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 08h | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 08h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 |

#### 8.5.5.4 STOP Command

This command stops conversions. See the *Conversion Control* section for details. Table 18 shows the STOP command byte sequence.

**Table 18. STOP Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 0Ah | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 0Ah | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 |

#### 8.5.5.5 RDATA Command

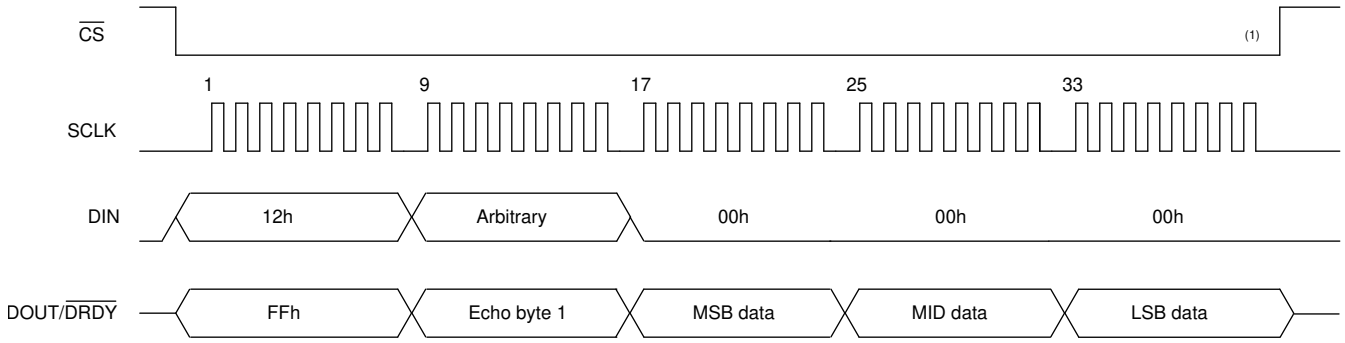
This command reads conversion data. Because the data are buffered, the data can be read at any time during the conversion phase. If data are read near the completion of the next conversion, old or new conversion data are returned. See the *Data Ready ($\overline{\text{DRDY}}$)* section for details.

The response of conversion data varies in length from 3 to 5 bytes depending if the STATUS byte and CRC bytes are included. See the *Conversion Data Format* section for the numeric data format. See Table 19, Figure 62 (minimum configuration) and Figure 63 (maximum configuration) for operation of the RDATA command.

**Table 19. RDATA Command**

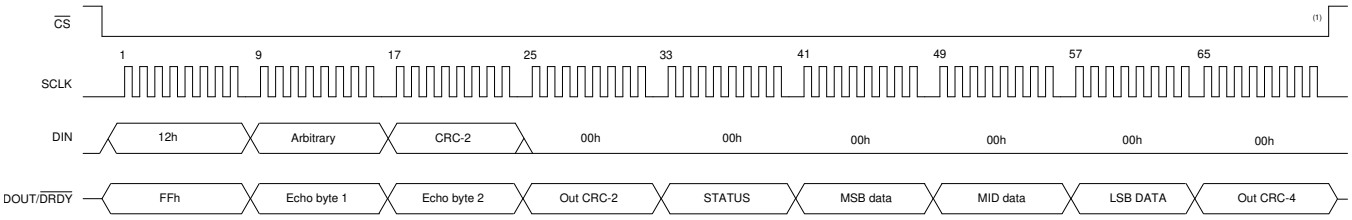
| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 | BYTE 7 | BYTE 8 | BYTE 9 |
|---|---|---|---|---|---|---|---|---|---|
| **No CRC mode** | | | | | | | | | |
| DIN | 12h | Arbitrary | 00h | 00h | 00h | 00h | | | |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | STATUS (1) | MSB data | MID data | LSB data | | | |
| **CRC mode** | | | | | | | | | |
| DIN | 12h | Arbitrary | CRC-2 | 00h | 00h | 00h | 00h | 00h | 00h |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 | STATUS (1) | MSB data | MID data | LSB data | Out CRC-3 or Out CRC-4 |

(1) Optional STATUS byte




(1) $\overline{CS}$ can be tied low

**Figure 62. Conversion Data Read Operation (STATUS Byte and CRC Mode Disabled)**




A. $\overline{CS}$ can be tied low

**Figure 63. Conversion Data Read Operation (STATUS Byte and CRC Mode Enabled)**

### *8.5.5.6 SYOCAL Command*

This command is used for *system* offset calibration. See the *Offset System-Calibration (SYOCAL)* section for details. Table 20 shows the SYOCAL command byte sequence.

**Table 20. SYOCAL Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 16h | Arbitrary | | |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 16h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | Echo Byte 2 | Out CRC-2 |

#### 8.5.5.7 GANCAL Command

This command is for gain calibration. See the *Calibration* section for details. Full-Scale Calibration (GANCAL) shows the GANCAL command byte sequence.

**Table 21. GANCAL Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 17h | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 17h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo Byte 2 | Out CRC-2 |

#### 8.5.5.8 SFOCAL Command

This command is used for *self* offset calibration. See the *Offset Self-Calibration (SFOCAL)* section for details. Table 22 shows the SFOCAL command byte sequence.

**Table 22. SFOCAL Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 19h | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 19h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo Byte 2 | Out CRC-2 |

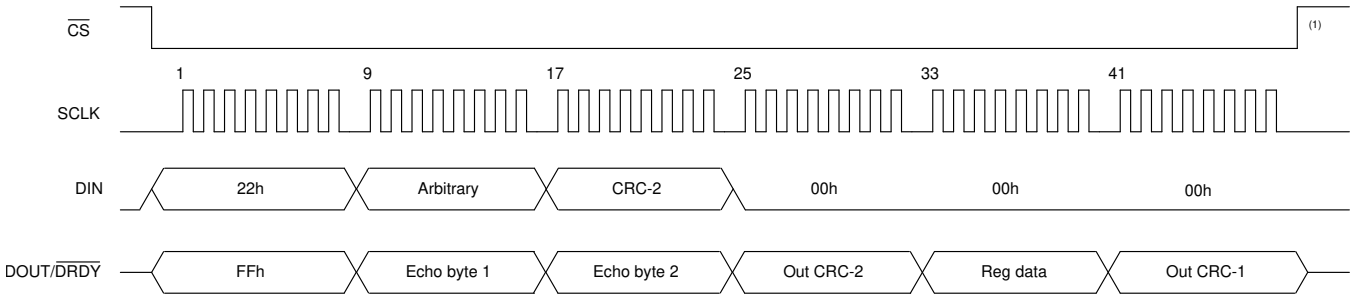
#### 8.5.5.9 RREG Command

Use the RREG command to read register data. The register data are read one byte at a time by issuing the RREG command for each operation. Add the register address (rrh) to the base opcode (20h) to construct the command byte (20h + rrh). Table 23 shows the command byte sequence. The ADC responds with the register data byte, most significant bit first. The response to registers outside the valid address range is 00h. Figure 64 shows an example of the register read operation. The Out CRC-1 byte is the CRC calculated for the register data byte.

**Table 23. RREG Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 | BYTE 5 | BYTE 6 |
|---|---|---|---|---|---|---|
| **No CRC mode** | | | | | | |
| DIN | 20h + rrh(1) | Arbitrary | 00h | | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Register data | | | |
| **CRC mode** | | | | | | |
| DIN | 20h + rrh | Arbitrary | CRC-2 | 00h | 00h | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 | Register data | Out CRC-1 |

(1) rrh = 5-bit register address




(1) $\overline{CS}$ can be tied low

**Figure 64. Register Read Operation (address = 02h, CRC Mode Enabled)**

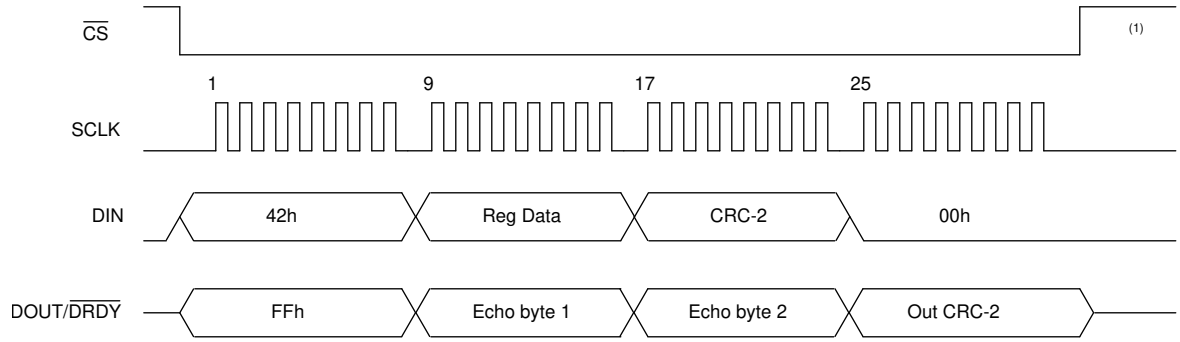
### *8.5.5.10 WREG Command*

Use the WREG command to write register data. The register data are written one byte at a time by issuing the WREG command for each operation. Add the register address (rrh) to the base opcode (40h) to construct the command byte (40h + rrh). Table 24 shows the command byte sequence. Figure 65 shows an example of the WREG operation. Be aware that writing to certain registers results in conversion restart. Table 27 lists the registers that restart an ongoing conversion when written to. Do not write to registers outside the address range.

**Table 24. WREG Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | 40h + rrh(1) | Register data | | |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | 40h + rrh | Register data | CRC-2 | 00h |
| DOUT/$\overline{DRDY}$ | FFh | Echo byte 1 | Echo byte 2 | Out CRC-2 |

(1) rrh = 5-bit register address.




A. $\overline{CS}$ can be tied low

**Figure 65. Register Write Operation (address = 02h, CRC Mode Enabled)**

#### 8.5.5.11 LOCK Command

The LOCK command locks-out write access to the registers including the calibration registers that are changed by calibration commands. The default mode is UNLOCK. Read access is allowed in LOCK mode. Table 25 shows the LOCK command byte sequence.

**Table 25. LOCK Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | F2h | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | F2h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo Byte2 | out CRC-2 |

#### 8.5.5.12 UNLOCK Command

The UNLOCK command allows register write access, including access to the contents of the calibration registers that can be changed by the calibration commands. Table 26 shows the UNLOCK command byte sequence.

**Table 26. UNLOCK Command**

| DIRECTION | BYTE 1 | BYTE 2 | BYTE 3 | BYTE 4 |
|---|---|---|---|---|
| **No CRC mode** | | | | |
| DIN | F5h | Arbitrary | | |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | | |
| **CRC mode** | | | | |
| DIN | F5h | Arbitrary | CRC-2 | 00h |
| DOUT/$\overline{\text{DRDY}}$ | FFh | Echo byte 1 | Echo Byte2 | Out CRC-2 |

## 8.6 Register Map

The register map consists of 18, one-byte registers. Collectively, the registers are used to configure the ADC to the desired operating mode. Access the registers by using the RREG and WREG (read-register and write-register) commands. Register data are accessed one register byte at a time for each command operation. At power-on or device reset, the registers are reset to the default values, as shown in the *Default* column of Table 27. Writing new data to certain registers causes the ADC conversion in progress to restart. The affected registers are listed in the *Restart* column in Table 27.

Register-write access is enabled or disabled by the UNLOCK and LOCK commands, respectively. The default mode is register UNLOCK. See the *LOCK Command* section for more details.

**Table 27. Register Map Summary**

| (rrh) | REGISTER | DEFAULT | RESTART | BIT 7 | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 00h | ID | Cxh | | DEV_ID[3:0] | | | | REV_ID[3:0] | | | |
| 01h | STATUS | 01h | | LOCK | CRCERR | PGAL_ALM | PGAH_ALM | REFL_ALM | DRDY | CLOCK | RESET |
| 02h | MODE0 | 24h | Yes | 0 | DR[3:0] | | | | FILTER[2:0] | | |
| 03h | MODE1 | 01h | Yes | 0 | CHOP[1:0] | | CONVRT | DELAY[3:0] | | | |
| 04h | MODE2 | 00h | | GPIO_CON[3:0] | | | | GPIO_DIR[3:0] | | | |
| 05h | MODE3 | 00h | | PWDN | STATENB | CRCENB | SPITIM | GPIO_DAT[3:0] | | | |
| 06h | REF | 05h | Yes | 0 | 0 | 0 | 0 | RMUXP[1:0] | | RMUXN[1:0] | |
| 07h | OFCAL0 | 00h | | OFC[7:0] | | | | | | | |
| 08h | OFCAL1 | 00h | | OFC[15:8] | | | | | | | |
| 09h | OFCAL2 | 00h | | OFC[23:16] | | | | | | | |
| 0Ah | FSCAL0 | 00h | | FSC[7:0] | | | | | | | |
| 0Bh | FSCAL1 | 00h | | FSC[15:8] | | | | | | | |
| 0Ch | FSCAL2 | 40h | | FSC[23:16] | | | | | | | |
| 0Dh | RESERVED | FFh | | FFh | | | | | | | |
| 0Eh | RESERVED | 00h | | 00h | | | | | | | |
| 0Fh | RESERVED | 00h | | 00h | | | | | | | |
| 10h | PGA | 00h | Yes | BYPASS | 0 | 0 | 0 | 0 | GAIN[2:0] | | |
| 11h | INPMUX | FFh | Yes | MUXP[3:0] | | | | MUXN[3:0] | | | |

### 8.6.1 Device Identification (ID) Register (address = 00h) [reset = Cxh]

**Figure 66. ID Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DEV_ID[3:0] | | | | REV_ID[3:0] | | | |
| NOTE: Reset values are device dependent | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 28. ID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | DEV_ID[3:0] | R | Ch | **Device ID**<br>1100 |
| 3:0 | REV_ID[3:0] | R | xh | **Revision ID**<br>*Note: Revision ID can change without notification* |

### 8.6.2 Device Status (STATUS) Register (address = 01h) [reset = 01h]

**Figure 67. STATUS Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| LOCK | CRCERR | PGAL_ALM | PGAH_ALM | REFL_ALM | DRDY | CLOCK | RESET |
| R-0h | R/W-0h | R-0h | R-0h | R-0h | R-0h | R-xh | R/W-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 29. STATUS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | LOCK | R | 0h | **Register Lock Status**<br>Indicates register lock status. Register writes are locked by the LOCK command and unlocked by the UNLOCK command.<br>0: Register write not locked (default)<br>1: Register write locked |
| 6 | CRCERR | R/W | 0h | **CRC Error**<br>Indicates that a CRC error is detected by the ADC. The CRC error bit remains set until cleared by the user.<br>0: No CRC error<br>1: CRC error |
| 5 | PGAL_ALM | R | 0h | **PGA Low Alarm**<br>Indicates PGA output voltage is below the low limit. The alarm resets at the start of conversion cycles.<br>0: No Alarm<br>1: Alarm |
| 4 | PGAH_ALM | R | 0h | **PGA High Alarm**<br>Indicates PGA output voltage is above the high limit. The alarm resets at the start of conversion cycles.<br>0: No Alarm<br>1: Alarm |
| 3 | REFL_ALM | R | 0h | **Reference Low Alarm**<br>Indicates reference voltage is below the low limit. The alarm resets at the start of conversion cycles.<br>0: No Alarm<br>1: Alarm |
| 2 | DRDY | R | 0h | **Data Ready**<br>Indicates conversion data ready.<br>0: Conversion data **not new** since the previous read operation<br>1: Conversion data **new** since the previous read operation |
| 1 | CLOCK | R | xh | **Clock**<br>Indicates internal or external clock mode. The ADC automatically selects the clock source.<br>0: ADC clock is internal<br>1: ADC clock is external |
| 0 | RESET | R/W | 1h | **Reset**<br>Indicates ADC reset. Clear the bit to detect next device reset.<br>0: No reset<br>1: Reset (default) |

### 8.6.3 Mode 0 (MODE0) Register (address = 02h) [reset = 24h]

**Figure 68. MODE0 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DR[3:0] | | | | FILTER[2:0] | | |
| R/W-0h | R/W-4h | | | | R/W-4h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 30. MODE0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0h | **Reserved**<br>Always write 0 |
| 6:3 | DR[3:0] | R/W | 4h | **Data Rate**<br>Select the ADC data rate.<br>0000: 2.5 SPS<br>0001: 5 SPS<br>0010: 10 SPS<br>0011: 16.$\overline{6}$ SPS<br>0100: 20 SPS (default)<br>0101: 50 SPS<br>0110: 60 SPS<br>0111: 100 SPS<br>1000: 400 SPS<br>1001: 1200 SPS<br>1010: 2400 SPS<br>1011: 4800 SPS<br>1100: 7200 SPS<br>1101 - 1111: Reserved |
| 2:0 | FILTER[2:0] | R/W | 4h | **Digital Filter**<br>Select the digital filter mode.<br>000: sinc1<br>001: sinc2<br>010: sinc3<br>011: sinc4<br>100: FIR (default)<br>101 - 111: Reserved |

### 8.6.4 Mode 1 (MODE1) Register (address = 03h) [reset = 01h]

**Figure 69. MODE1 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | CHOP[1:0] | | CONVRT | DELAY[3:0] | | | |
| R/W-0h | R/W-0h | | R/W-0h | R/W-1h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 31. MODE1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0h | **Reserved**<br>Always write 0 |
| 6:5 | CHOP[1:0] | R/W | 0h | **Chop and AC-Bridge Excitation Modes**<br>Select the Chop and ac-bridge excitation modes.<br>00: Normal mode (default)<br>01: Chop mode<br>10: 2-wire ac-bridge excitation mode<br>11: 4-wire ac-bridge excitation mode |
| 4 | CONVRT | R/W | 0h | **ADC Conversion Mode**<br>Select the ADC conversion mode.<br>0: Continuous conversions (default)<br>1: Pulse (one shot) conversion |
| 3:0 | DELAY[3:0] | R/W | 1h | **Conversion Start Delay**<br>Program the time delay at conversion start. Delay values are with $f_{CLK}$ = 7.3728 MHz.<br>0000: 0 µs<br>0001: 50 µs (default)<br>0010: 59 µs<br>0011: 67 µs<br>0100: 85 µs<br>0101: 119 µs<br>0110: 189 µs<br>0111: 328 µs<br>1000: 605 µs<br>1001: 1.16 ms<br>1010: 2.27 ms<br>1011: 4.49 ms<br>1100: 8.93 ms<br>1101: 17.8 ms<br>1110, 1111: Reserved |

### 8.6.5 Mode 2 (MODE2) Register (address = 04h) [reset = 00h]

**Figure 70. MODE2 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| GPIO_CON[3:0] | | | | GPIO_DIR[3:0] | | | |
| R/W-0h | | | | R/W-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 32. MODE2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | GPIO_CON[3] | R/W | 0h | **GPIO3 Pin Connection**<br>Connect GPIO3 to analog input AIN3.<br>0: GPIO3 not connected to AIN3 (default)<br>1: GPIO3 connected to AIN3 |
| 6 | GPIO_CON[2] | R/W | 0h | **GPIO2 Pin Connection**<br>Connect GPIO2 to analog input AIN2.<br>0: GPIO2 not connected to AIN2 (default)<br>1: GPIO2 connected to AIN2 |
| 5 | GPIO_CON[1] | R/W | 0h | **GPIO1 Pin Connection**<br>Connect GPIO1 to analog input AIN1.<br>0: GPIO1 not connected to AIN1 (default)<br>1: GPIO1 connected to AIN1 |
| 4 | GPIO_CON[0] | R/W | 0h | **GPIO0 Pin Connection**<br>Connect GPIO0 to analog input AIN0<br>0: GPIO0 not connected to AIN0 (default)<br>1: GPIO0 connected to AIN0 |
| 3 | GPIO_DIR[3] | R/W | 0h | **GPIO3 Pin Direction**<br>Configure GPIO3 as a GPIO input or GPIO output on AIN3.<br>0: GPIO3 is an output (default)<br>1: GPIO3 is an input |
| 2 | GPIO_DIR[2] | R/W | 0h | **GPIO2 Pin Direction**<br>Configure GPIO2 as a GPIO input or GPIO output on AIN2.<br>0: GPIO2 is an output (default)<br>1: GPIO2 is an input |
| 1 | GPIO_DIR[1] | R/W | 0h | **GPIO1 Pin Direction**<br>Configure GPIO1 as a GPIO input or GPIO output on AIN1.<br>0: GPIO1 is an output (default)<br>1: GPIO1 is an input |
| 0 | GPIO_DIR[0] | R/W | 0h | **GPIO0 Pin Direction**<br>Configure GPIO0 as a GPIO input or GPIO output on AIN0.<br>0: GPIO0 is an output (default)<br>1: GPIO0 is an input |

### 8.6.6 Mode 3 (MODE3) Register (address = 05h) [reset = 00h]

**Figure 71. MODE3 Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PWDN | STATENB | CRCENB | SPITIM | GPIO_DAT[3:0] | | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 33. MODE3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PWDN | R/W | 0h | **Software Power-down Mode**<br>Enable the software power-down mode.<br>0: Normal mode (default)<br>1: Software power-down mode |
| 6 | STATENB | R/W | 0h | **STATUS Byte**<br>Enable the Status byte in the conversion data read operation.<br>0: No Status byte (default)<br>1: Status byte enabled |
| 5 | CRCENB | R/W | 0h | **CRC Data Verification**<br>Enable the CRC data verification.<br>0: No CRC (default)<br>1: CRC enabled |
| 4 | SPITIM | R/W | 0h | **SPI Auto-Reset Function**<br>Enable the SPI auto-reset function.<br>0: SPI auto-reset disabled (default)<br>1: SPI auto-reset enabled |
| 3 | GPIO_DAT[3] | R/W | 0h | **GPIO3 Data**<br>Read or write the GPIO3 data on AIN3.<br>0: GPIO3 is low (default)<br>1: GPIO3 is high |
| 2 | GPIO_DAT[2] | R/W | 0h | **GPIO2 Data**<br>Read or write the GPIO2 data on AIN2.<br>0: GPIO2 is low (default)<br>1: GPIO2 is high |
| 1 | GPIO_DAT[1] | R/W | 0h | **GPIO1 Data**<br>Read or write the GPIO1 data on AIN1.<br>0: GPIO1 is low (default)<br>1: GPIO1 is high |
| 0 | GPIO_DAT[0] | R/W | 0h | **GPIO0 Data**<br>Read or write the GPIO1 data on AIN0.<br>0: GPIO0 is low (default)<br>1: GPIO0 is high |

### 8.6.7 Reference Configuration (REF) Register (address = 06h) [reset = 05h]

**Figure 72. REF Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | RMUXP[1:0] | | RMUXN[1:0] | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-1h | | R/W-1h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 34. REF Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | 0 | R/W | 0h | **Reserved**<br>Always write 0h |
| 3:2 | RMUXP[1:0] | R/W | 1h | **Reference Positive Input**<br>Select the positive reference input.<br>00: Reserved<br>01: AVDD (default)<br>10: REFP0<br>11: AIN0 (REFP1) |
| 1:0 | RMUXN[1:0] | R/W | 1h | **Reference Negative Input**<br>Select the negative reference input.<br>00: Reserved<br>01: AVSS (default)<br>10: REFN0<br>11: AIN1 (REFN1) |

### 8.6.8 Offset Calibration (OFCALx) Registers (address = 07h, 08h, 09h) [reset = 00h, 00h, 00h]

**Figure 73. OFCAL0, OFCAL1, OFCAL2 Registers**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| OFC[7:0] | | | | | | | |
| R/W-00h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| OFC[15:8] | | | | | | | |
| R/W-00h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| OFC[23:16] | | | | | | | |
| R/W-00h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 35. OFCAL0, OFCAL1, OFCAL2 Registers Field Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23:0 | OFC[23:0] | R/W | 000000h | **Offset Calibration**<br>These three registers are the 24-bit offset calibration word. The offset calibration is two's complement format. The ADC subtracts the offset value from the conversion result before the full-scale operation. |

### 8.6.9 Full-Scale Calibration (FSCALx) Registers (address = 0Ah, 0Bh, 0Ch) [reset = 00h, 00h, 40h]

**Figure 74. FSCAL0, FSCAL1, FSCAL2 Registers**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| FSC[7:0] | | | | | | | |
| R/W-00h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| FSC[15:8] | | | | | | | |
| R/W-00h | | | | | | | |
| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| FSC[23:16] | | | | | | | |
| R/W-40h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 36. FSCAL0, FSCAL1, FSCAL2 Registers Field Description**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23:0 | FSC[23:0] | R/W | 400000h | **Full-Scale Calibration**<br>These three registers are the 24-bit full scale calibration word. The full-scale calibration is straight binary format. The ADC divides the register value by 400000h then multiplies the result with the conversion data. The scaling operation occurs after the offset operation. |

### 8.6.10 Reserved (RESERVED) Register (address = 0Dh) [reset = FFh]

**Figure 75. RESERVED Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 37. RESERVED Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | 0 | R | FFh | **Reserved**<br>These bits are read only and always return 0 |

### 8.6.11 Reserved (RESERVED) Register (address = 0Eh) [reset = 00h]

**Figure 76. RESERVED Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 38. RESERVED Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | 0 | R | 0h | **Reserved**<br>These bits are read only and always return 0 |

### 8.6.12 Reserved (RESERVED) Register (address = 0Fh) [reset = 00h]

**Figure 77. RESERVED Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 39. RESERVED Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | 0 | R | 0h | **Reserved**<br>These bits are read only and always return 0 |

### 8.6.13 PGA Configuration (PGA) Register (address = 10h) [reset = 00h]

**Figure 78. PGA Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| BYPASS | 0 | 0 | 0 | 0 | GAIN[2:0] | | |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 40. PGA Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | BYPASS | R/W | 0h | **PGA Bypass Mode**<br>Select the PGA mode.<br>0: PGA mode (default)<br>1: PGA bypass |
| 6:3 | 0 | R/W | 0h | **Reserved**<br>Always write 0 |
| 2:0 | GAIN[2:0] | R/W | 0h | **Gain**<br>Select the gain.<br>000: 1 (default)<br>001 - 101: Reserved<br>110: 64<br>111: 128 |

### 8.6.14 Input Multiplexer (INPMUX) Register (address = 11h) [reset = FFh]

**Figure 79. INPMUX Register**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| MUXP[3:0] | | | | MUXN[3:0] | | | |
| R/W-Fh | | | | R/W-Fh | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 41. INPMUX Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:4 | MUXP[3:0] | R/W | Fh | **Positive Input Multiplexer**<br>Select the positive multiplexer input.<br>0000 - 0010: Reserved<br>0011: AIN0<br>0100: AIN1<br>0101: AIN2<br>0110: AIN3<br>0111: AIN4<br>1000: AIN5<br>1001, 1010: Reserved<br>1011: Internal temperature sensor positive<br>1100, 1101: Reserved<br>1110: PGA P input open<br>1111: Internal connection to $V_{COM}$ (default) |
| 3:0 | MUXN[3:0] | R/W | Fh | **Negative Input Multiplexer**<br>Select the negative multiplexer input.<br>0000 - 0010: Reserved<br>0011: AIN0<br>0100: AIN1<br>0101: AIN2<br>0110: AIN3<br>0111: AIN4<br>1000: AIN5<br>1001, 1010: Reserved<br>1011: Internal temperature sensor negative<br>1100, 1101: Reserved<br>1110: PGA N Input open<br>1111: Internal connection to $V_{COM}$ (default) |

# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Input Range

The input voltage must be maintained within the specified input range for linear ADC operation otherwise the conversion data is invalid. Use Equation 3 to verify the input voltage of the PGA is within specification. The input requirement can also be verified by measuring the PGA output voltages (pins CAPP and CAPN) with a voltmeter under the conditions of maximum expected input signal, ADC gain, and worst case (low) power-supply voltage. Check that voltages measured on the pins are within the range: AVSS + 0.3 V < $V_{(CAPP)}$ and $V_{(CAPN)}$ < AVDD – 0.3 V.

### 9.1.2 Input Overload

Observe the input overvoltage precautions as outlined in the ESD Diodes section. If an overvoltage condition occurs on an unused channel, the overvoltage channel may crosstalk to the measurement channel. One solution is to externally clamp the inputs with low-forward voltage diodes as shown in Figure 80. The external diodes divert the overvoltage current around the ADC inputs to the power supply and ground. Be aware of the reverse leakage current of the Schottky diodes that may lead to measurement errors.

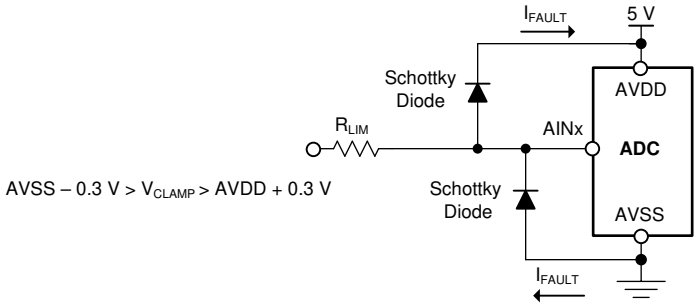



**Figure 80. External Diode Clamps**

## Application Information (continued)

### 9.1.3 Unused Inputs and Outputs

- Analog Inputs

  To minimize input leakage of the measurement channel, tie unused inputs to mid-supply voltage (AVDD + AVSS) / 2 or to AVDD.
- Digital I/O

  Not all the digital I/Os may be needed to operate the ADC. Be sure not to float both used and unused digital inputs, including during power-down mode. The following is a summary of the optional digital I/Os connection:
  - $\overline{CS}$: Tie $\overline{CS}$ low to permanently enable the serial interface.
  - CLKIN: Tie CLKIN to DGND to permanently operate the ADC with the internal oscillator.
  - START: Tie START to DGND to control conversions by command. Tie START to DVDD to permanently free-run conversions (Continuous-conversion mode only)
  - $\overline{RESET}$: Tie $\overline{RESET}$ to DVDD if not using hardware reset. The ADC is reset at power-on. The ADC is also reset by the RESET command.
  - $\overline{PWDN}$: Tie $\overline{PWDN}$ to DVDD if not using the hardware power-down mode. The ADC can be powered down by software.
  - $\overline{DRDY}$: The functionality of the $\overline{DRDY}$ output is also provided by the dual-mode DOUT/$\overline{DRDY}$ pin. The DOUT/$\overline{DRDY}$ output is active when $\overline{CS}$ is low. Data ready is also determined by software polling. Because the conversion data are buffered, data can be read at any time without the need to synchronize to data ready.

### 9.1.4 Multiplexed 2-Bridge Input Example

Figure 81 shows an example of a multiplexed, two-bridge system. The figure is a simplified diagram and excludes input filter components. The bridges are connected with independent excitation sense lines leading from each bridge to the ADC for accurate reference voltage tracking. Adjust the time delay parameter of the ADC as necessary to provide delay for settling time that is required after changing the ADC input multiplexer for each bridge measurement.

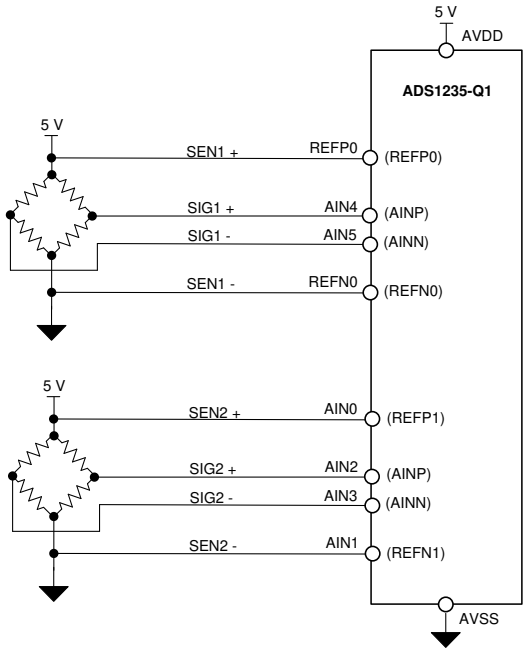



**Figure 81. Multiplexed 2-Bridge Application**

## Application Information (continued)

### 9.1.5 AC-Bridge Excitation Example

Figure 82 shows an ac-excited bridge measurement system in the 4-wire, GPIO-control mode. Signal and reference-input filter components are omitted for clarity. The transistors switch the polarity of the excitation voltage provided to the bridge by the drive signals from the ADC GPIO drivers via the spare analog input pins. The timing of the drive signals are synchronized to the ADC conversions. The drive signals are non-overlapping in order to avoid commutation errors that can occur during the switching phase. The resistors located at the gates of each transistor maintain the transistors off at power-on, while the ADC drive signals are initialized by the host after system power up. See Figure 7 for timing of the drive signals.

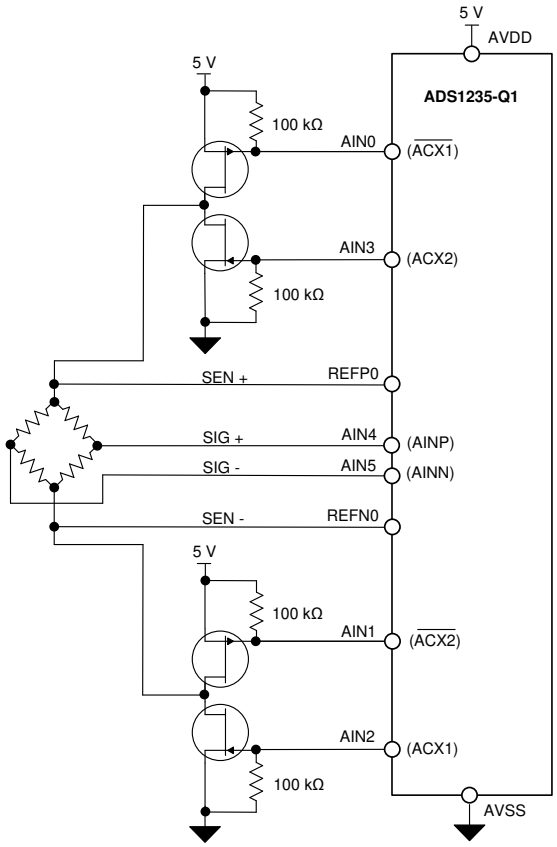



**Figure 82. AC-Bridge Excitation Application**

The recommended configuration sequence for ac-bridge excitation mode follows:

1. Stop conversions by taking the START pin low, or by control of conversions in software mode; send the STOP command
2. Program the signal and reference input multiplexers, gain, data rata, filter mode and other configurations as needed
3. Program the 2-wire or 4-wire ac-bridge excitation mode. 2-wire mode requires complementary output switching devices
4. Program the GPIO internal connection to the analog input pins
5. Program the GPIO as outputs to enable drive signals at the analog input pins. The bridge output drive signals appear on the GPIO pins.

Start the conversions. Adjust the time delay parameter as necessary to provide sufficient bridge switch delay. The delay is based on the time constant of the input and reference filters.

## Application Information (continued)

### 9.1.6 Serial Interface and Digital Connections

Figure 83 shows an example of the digital connections between the host µC and ADC. Not all I/O connections are necessary for basic ADC operation; see the Unused Inputs and Outputs section. Impedance-matching resistors in series with the I/O PCB traces help reduce overshoot and ringing, and are particularly helpful over long trace runs.

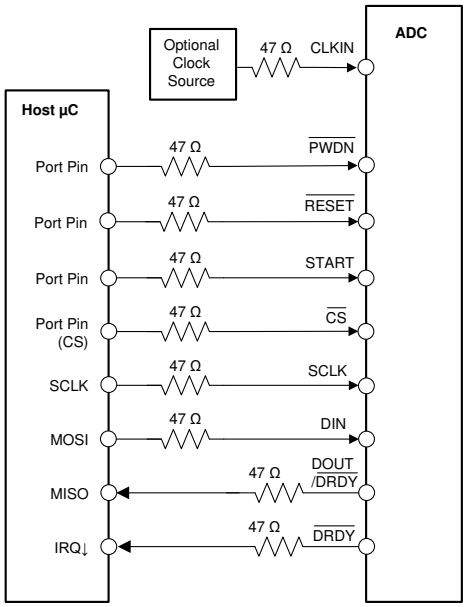



**Figure 83. Serial Interface and Digital I/O Connections**

## 9.2 Typical Application

Figure 84 shows an application of the ADS1235-Q1 with a bridge circuit. The excitation voltage provided to the bridge is the ADC power supply voltage (5 V). Due to the low input-referred noise of the ADS1235-Q1, in many applications there is no need for an additional gain amplifier. The excitation voltage sense lines are connected to the reference inputs of the ADC with a noise filter. This configuration provides ratiometric operation that cancels noise and drift of the excitation voltage.

The input signal and reference voltage paths are filtered with equal-value components to remove high frequency noise from affecting the measurement.

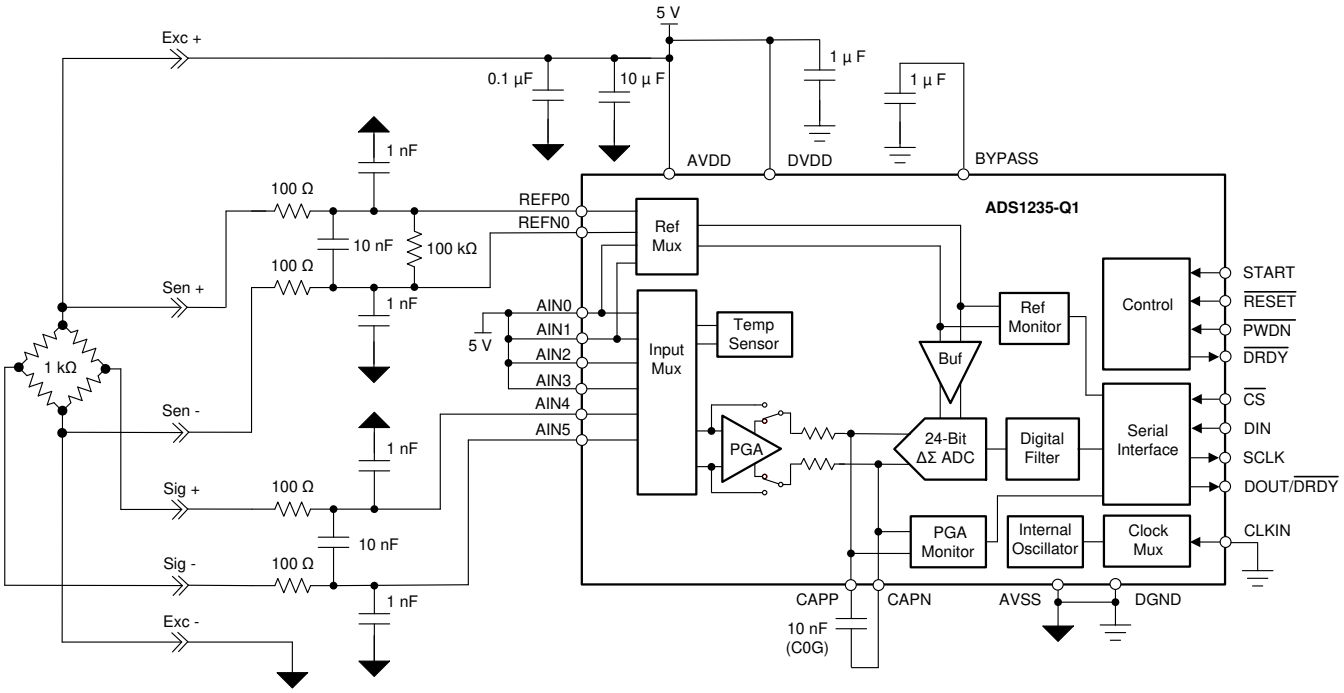



**Figure 84. Bridge Input Application**

### 9.2.1 Design Requirements

The ADC can be configured to provide tradeoffs between conversion noise, sample rate and conversion settling time. Table 42 summarizes the design performance goals. Table 43 summarizes the design parameters.

1 kΩ fixed-value precision resistors simulate the bridge circuit. One of the four resistor values is unbalanced (1.008 kΩ) in order to generate a 10 mV output signal to simulate a full scale output with 2 mV/V bridge gauge factor when used with 5 V excitation.

**Table 42. Design Goals**

| DESIGN GOAL | VALUE |
|---|---|
| Noise free resolution (counts) | > 100,000 counts |
| Sample rate | 10 SPS |
| Settling time | 200 ms |

**Table 43. Design Parameters**

| DESIGN PARAMETER | DESIGN VALUE |
|---|---|
| Bridge resistance | 1 kΩ |
| Bridge excitation voltage | 5 V |
| Bridge gauge factor | 2 mV/V |
| Bridge full scale signal | 10 mV |

### 9.2.2 Detailed Design Procedure

A key consideration in the design of a bridge transducer for weigh applications is noise-free resolution. Noise-free resolution is defined by the ratio of full scale signal to the conversion noise of the ADC. Other considerations are data throughput rate and input signal settling time.

Table 1 shows the ADC conversion noise expressed as an input-referred quantity. The table shows various tradeoffs among gain, sample rate and sinc filter in order to optimize noise for a given design. For this example, the configuration of the ADC that yields the lowest noise while achieving the sample rate and settling time requirement is gain = 128, 10 SPS, filter order = sinc 1 and by using the chop mode. Use of the chop mode has the additional advantage of eliminating offset drift from the ADC.

Configuring the ADC for 10 SPS, the sinc4 filter order and disabling chop mode yields approximately the same noise performance compared to the target configuration (shown above) but do not satisfy the settling time requirement of 200 ms. The sinc4 filter order settles in four conversion periods, or 400 ms.

Noise-free counts are improved by increasing the signal output from the bridge. Increasing the signal output is possible by the use of a bridge with a higher gauge-factor, or by increasing the excitation voltage. Operation with an excitation voltage above 5 V requires voltage division of the bridge sense voltage before it is input to the ADC reference pins.

External filter components filter the signal and reference inputs of the ADC. The filters remove both differential and common-mode high-frequency noise. Component value mismatch in the common-mode filter converts common-mode noise into differential noise. To minimize the effect of the mismatch, the differential filter capacitor values (10 nF) are 10x higher value than the common-mode capacitors (1 nF). Increase the capacitor values to provides additional noise filtering. Maintain the resistors at low values to minimize thermal noise. For consistent noise performance, match the corner frequencies of the input and reference filters. More information is found in the *RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248 Family of Devices Application Report*.

### 9.2.3 Application Curves

Figure 85 and Figure 86 show the conversion data that was acquired over a 60 second interval. 60 seconds of data provides evaluation of noise performance under actual conditions. The acquired conversion data is taken with a full-scale signal (10 mV) to show the noise cancelling effects of the ADC provided by ratiometric operation. Figure 85 and Figure 86 show conversion data in normal mode and in chop mode operation, respectively. In normal mode, the approximate noise free resolution is 100,000 counts. In chop mode, approximate noise free resolution is 120,000 counts. Chop mode provides the additional advantage of zero offset drift, but requires an additional conversion period for fully settled data after an input step change occurs (200 ms total).

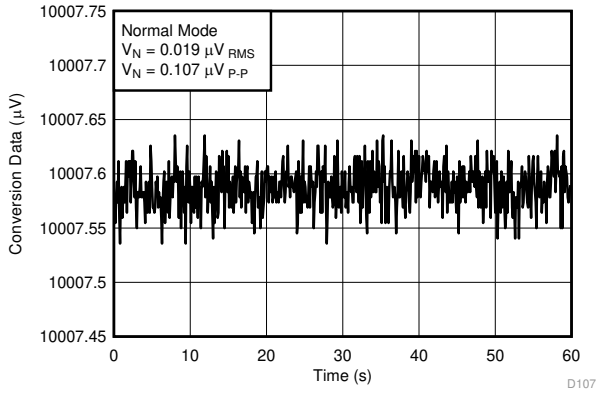



**Figure 85. Conversion Data (Normal Mode)**

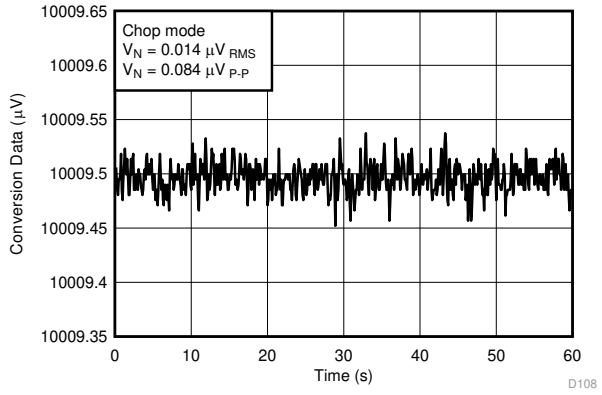



**Figure 86. Conversion Data (Chop Mode)**

## 9.3 Initialization Setup

Figure 87 shows a general configuration and measurement procedure.

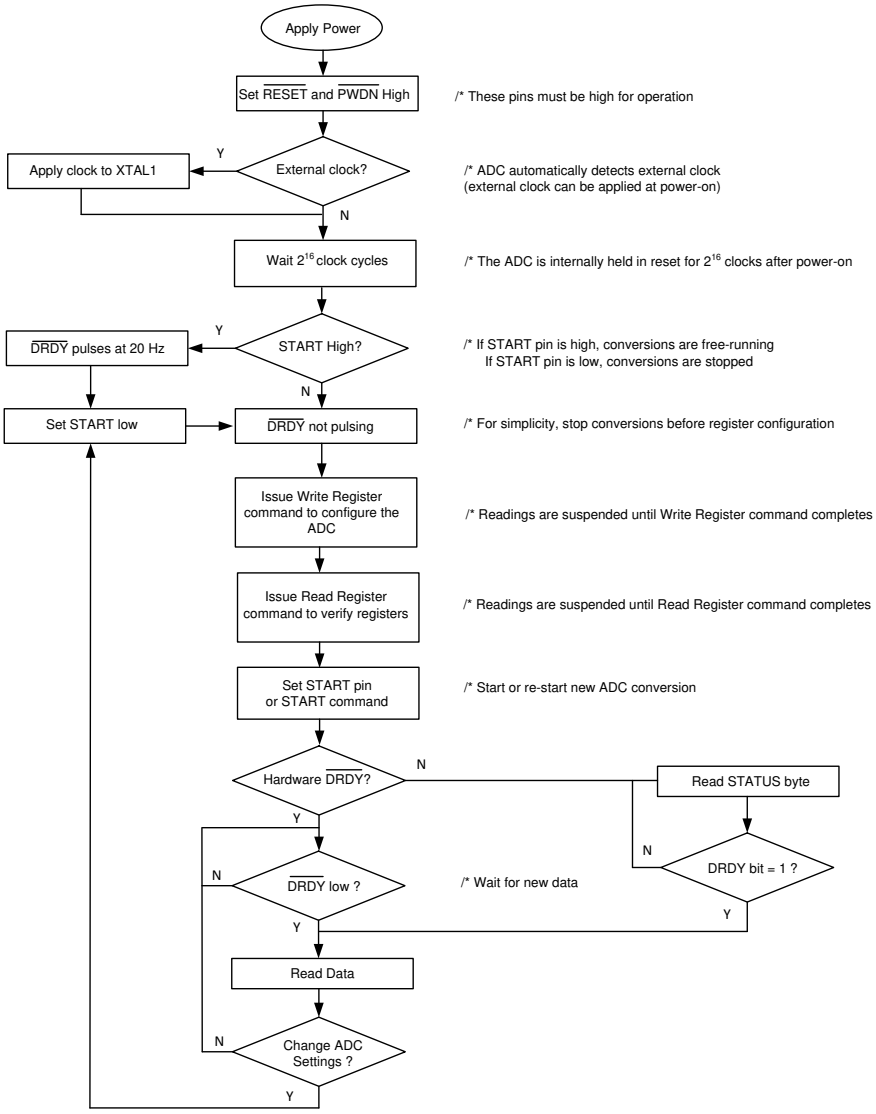



**Figure 87. ADC Configuration and Measurement Procedure**

# 10 Power Supply Recommendations

The ADC requires an analog power supply (AVDD, AVSS) and digital power supply (DVDD). The analog power supply can be bipolar (AVDD = +2.5 V and AVSS = –2.5 V) or unipolar (AVDD = 5 V and AVSS = DGND). The digital supply range is 2.7 V to 5.25 V. DVDD powers the ADC core by use of an internal regulator. DVDD also sets the digital I/O voltage. Keep in mind that the GPIO I/O voltages are AVDD and AVSS. Voltage ripple produced by switch-mode power supplies may interfere with the ADC conversions. Use low-dropout regulators (LDOs) to reduce voltage ripple caused by switch-mode power supplies.

## 10.1 Power-Supply Decoupling

Good power-supply decoupling is important in order to achieve rated performance. Power supplies must be decoupled close to the power supply pins using short, direct connections to ground. For the analog supply, place 0.1-µF and 10-µF capacitors between AVDD and AVSS. Connect a 1-µF capacitor from DVDD to the ground plane. Connect a 1-µF capacitor from BYPASS to the ground plane.

## 10.2 Analog Power-Supply Clamp

It is important to evaluate circumstances when an input signal is present with the ADC, both powered and unpowered. When the input signal exceeds the power-supply voltage, it is possible to *backdrive* the analog power-supply voltage with the input signal through a conduction path of the internal ESD diodes. Backdriving the ADC power supply can also occur when the power-supply is on. The backdriven current path is illustrated in Figure 88. Depending on how the power supply responds during a backdriven condition, it is possible to exceed the maximum rated ADC supply voltage. The ADC voltage must not be exceeded at all times. One solution is to clamp the analog supply to safe voltage using an external zener diode.

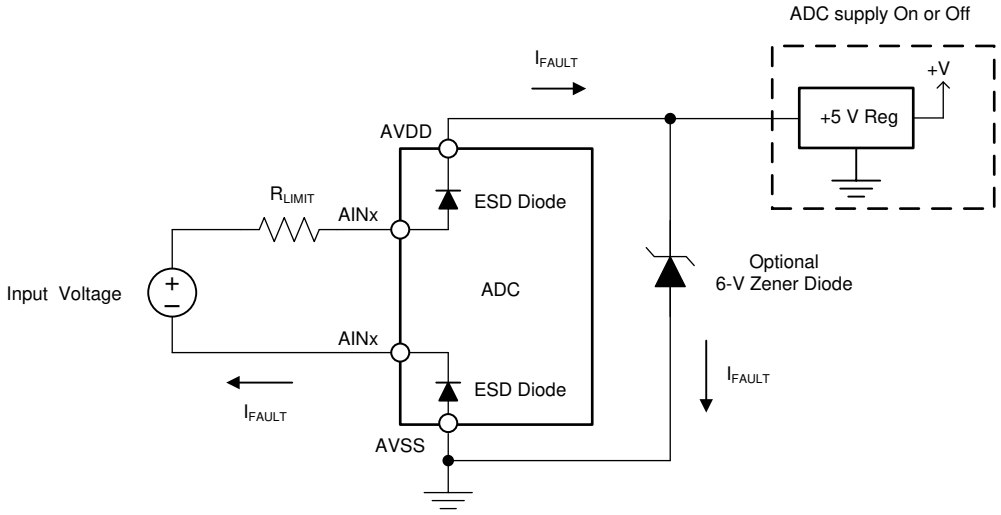



**Figure 88. Analog Power-Supply Clamp**

## 10.3 Power-Supply Sequencing

The power supplies can be sequenced in any order, but do not allow the analog or digital inputs to exceed the respective analog or digital power-supply voltage without external limits of the possible input fault currents.

# 11 Layout

Good layout practices are crucial to realize the full-performance of the ADC. Poor grounding can quickly degrade the noise performance. The following layout guidelines help provide the best results.

## 11.1 Layout Guidelines

For best performance, dedicate an entire PCB layer to a ground plane and do not route any other signal traces on this layer. However, depending on restrictions imposed by specific end equipment, a dedicated ground plane may not be practical. If ground plane separation is necessary, make a direct connection of the planes at the ADC. Do not connect individual ground planes at multiple locations because this configuration creates ground loops.

Route digital traces away from the CAPP and CAPN pins and away from all analog inputs and associated components in order to minimize interference.

Avoid long traces on DOUT/$\overline{\text{DRDY}}$, because high capacitance on this pin can lead to increased ADC noise levels. Use a series resistor or a buffer if long traces are used.

C0G capacitors are preferred for the analog input filters. Evaluate other types of capacitors carefully for input filtering use. Use a C0G-type capacitor for the CAPP to CAPN capacitor. Use X7R-type capacitors for the power supply decoupling capacitors. High-K type capacitors (Y5V) are not recommended. Place the capacitors as close as possible to the device pins using short, direct traces. For optimum performance, use low-impedance connections on the ground-side connections of the bypass capacitors.

When applying an external clock, be sure the clock is free of overshoot and glitches. A source-termination resistor placed at the clock buffer helps control reflections and overshoot. Glitches present on the clock signal can lead to increased noise and possible mis-operation.

## 11.2 Layout Example

Figure 89 is an example layout of the ADS1235-Q1, requiring a minimum of three PCB layers. The example circuit is shown with single supply operation (AVSS = DGND). In this example, the inner layer is dedicated to the ground plane and the outer layers are used for signal and power traces. If a four-layer PCB is used, dedicate the additional inner layer as the power plane. In this example, the ADC is oriented in such a way to minimize crossover of the analog and digital signal traces.

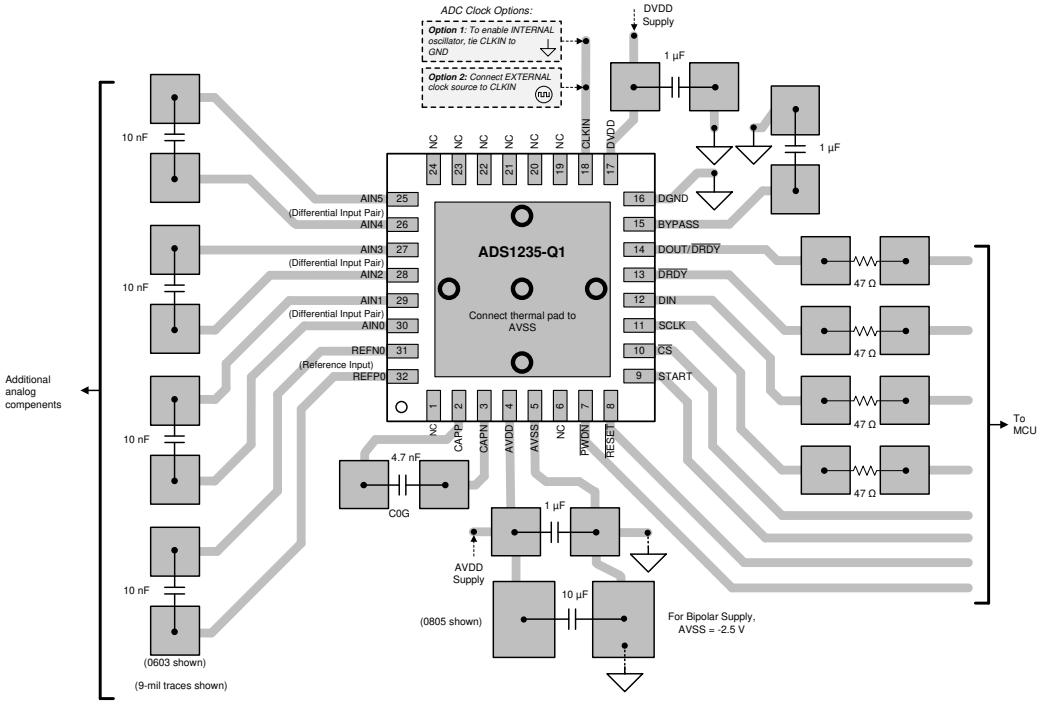



**Figure 89. ADS1235-Q1 Layout Example**

# 12 Device and Documentation Support

## 12.1 Documentation Support

### 12.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *ADS1261 and ADS1235 Evaluation Module* user's guide

## 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 12.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 12.4 Trademarks

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## 12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1235QWRHMRQ1 | ACTIVE | VQFN | RHM | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAUAG | Level-3-260C-168 HR | -40 to 125 | ADS 1235Q | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF ADS1235-Q1 :**

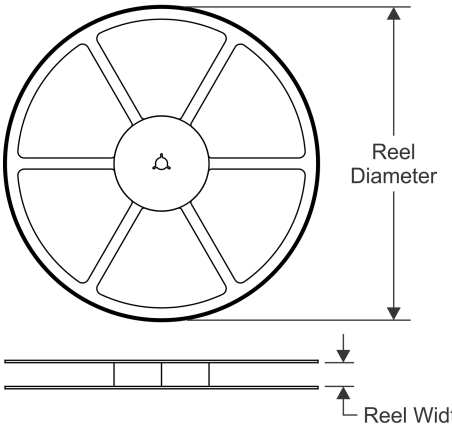
- Catalog: ADS1235

NOTE: Qualified Version Definitions:

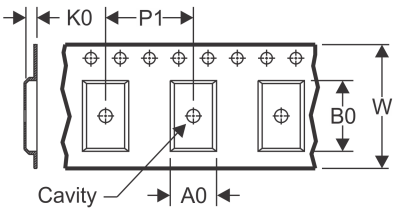
- Catalog - TI's standard catalog product

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

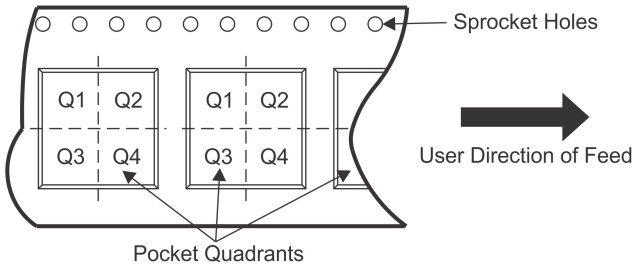



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

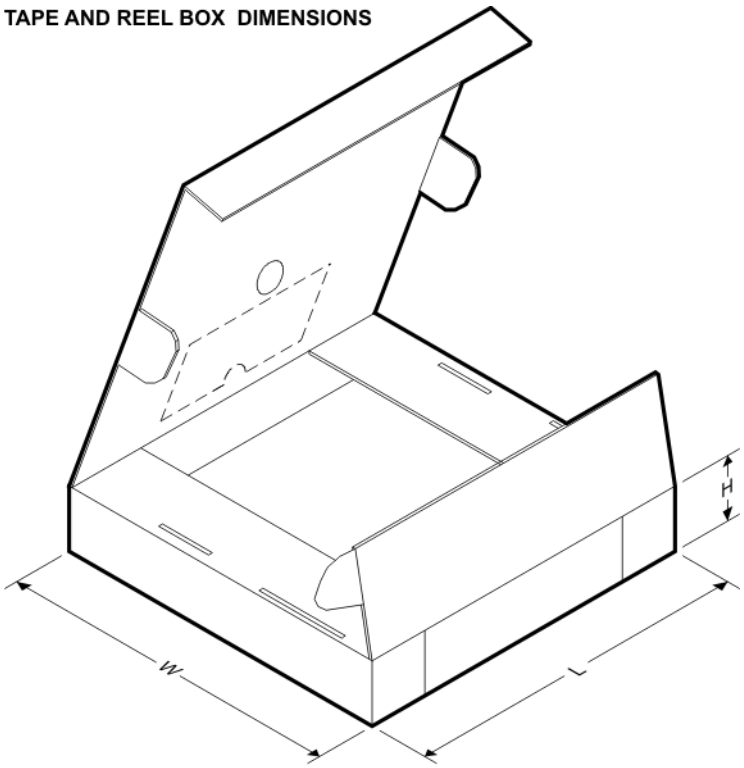
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADS1235QWRHMRQ1 | VQFN | RHM | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS



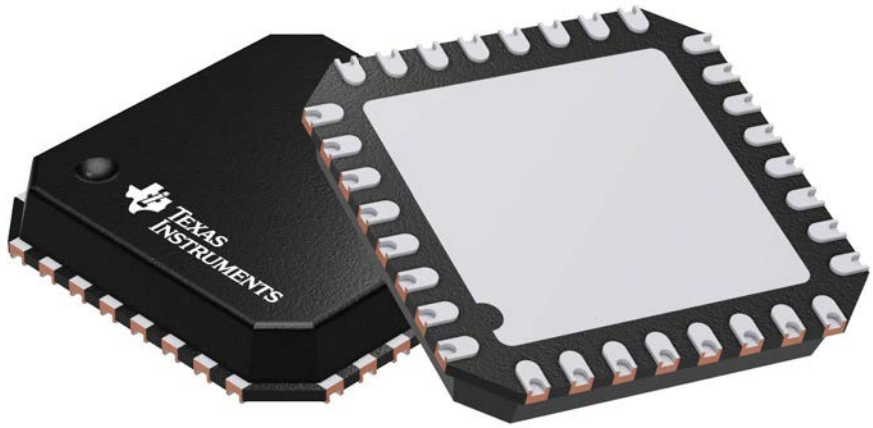

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| ADS1235QWRHMRQ1 | VQFN | RHM | 32 | 3000 | 367.0 | 367.0 | 35.0 |

# GENERIC PACKAGE VIEW

## RHM 32 VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD




Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

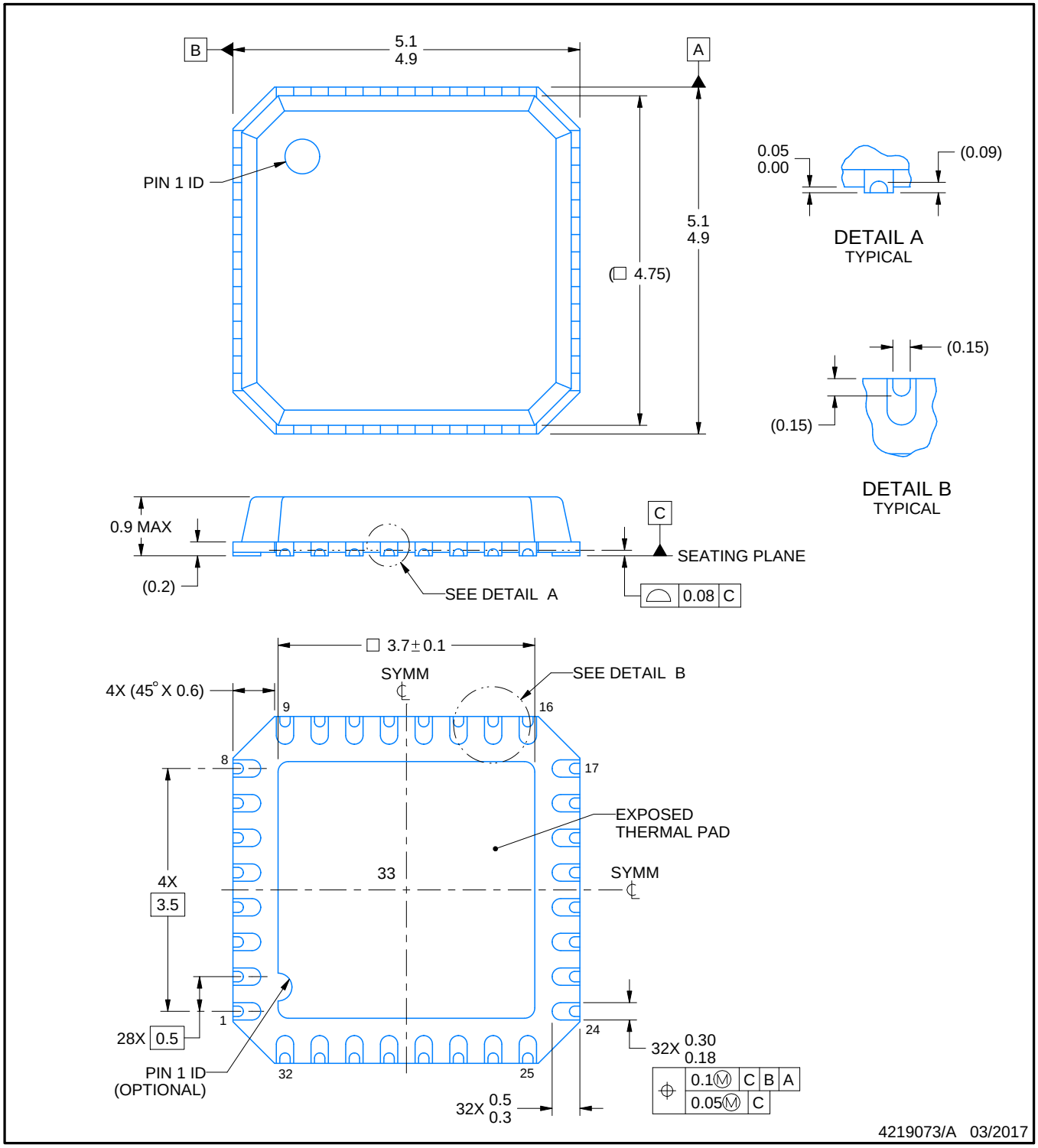
4205347/C

# PACKAGE OUTLINE

## RHM0032A

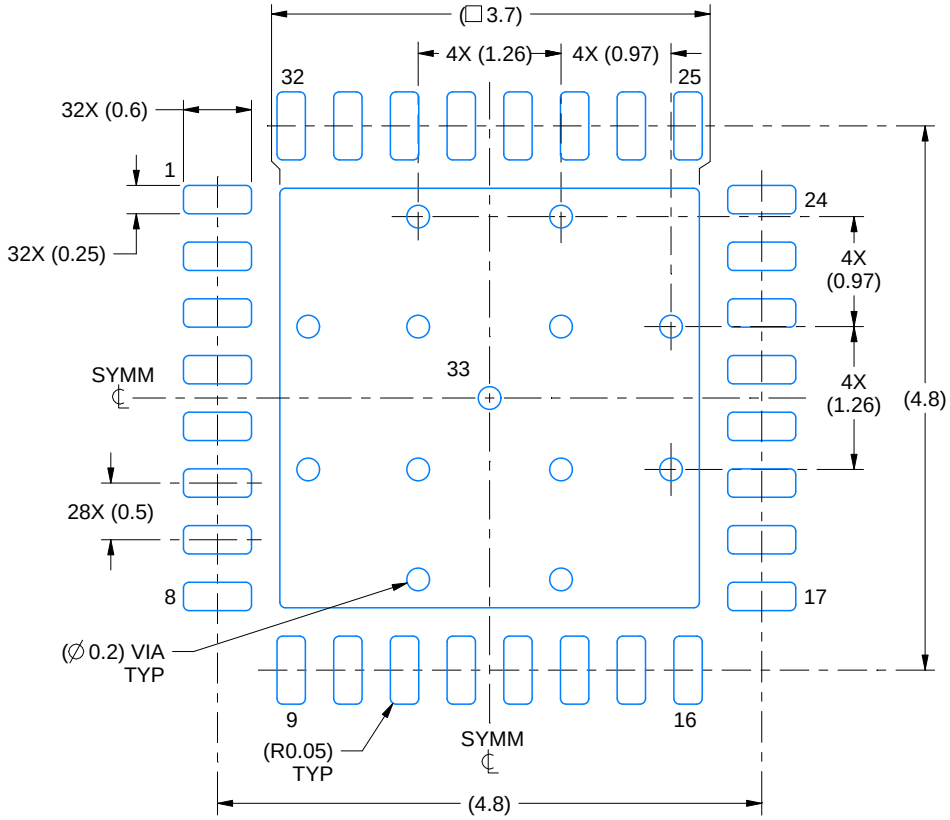
## VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

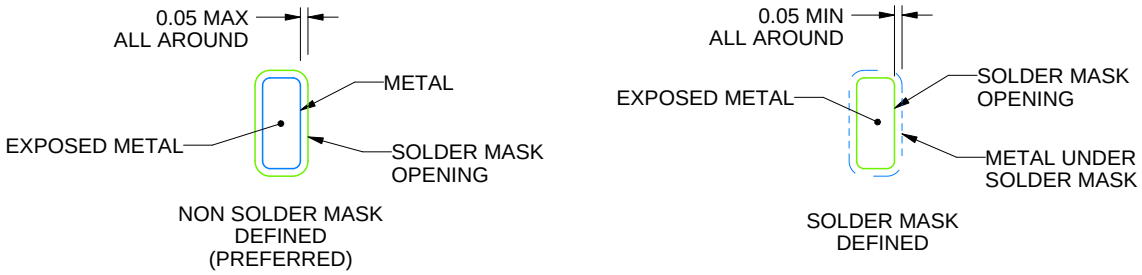



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

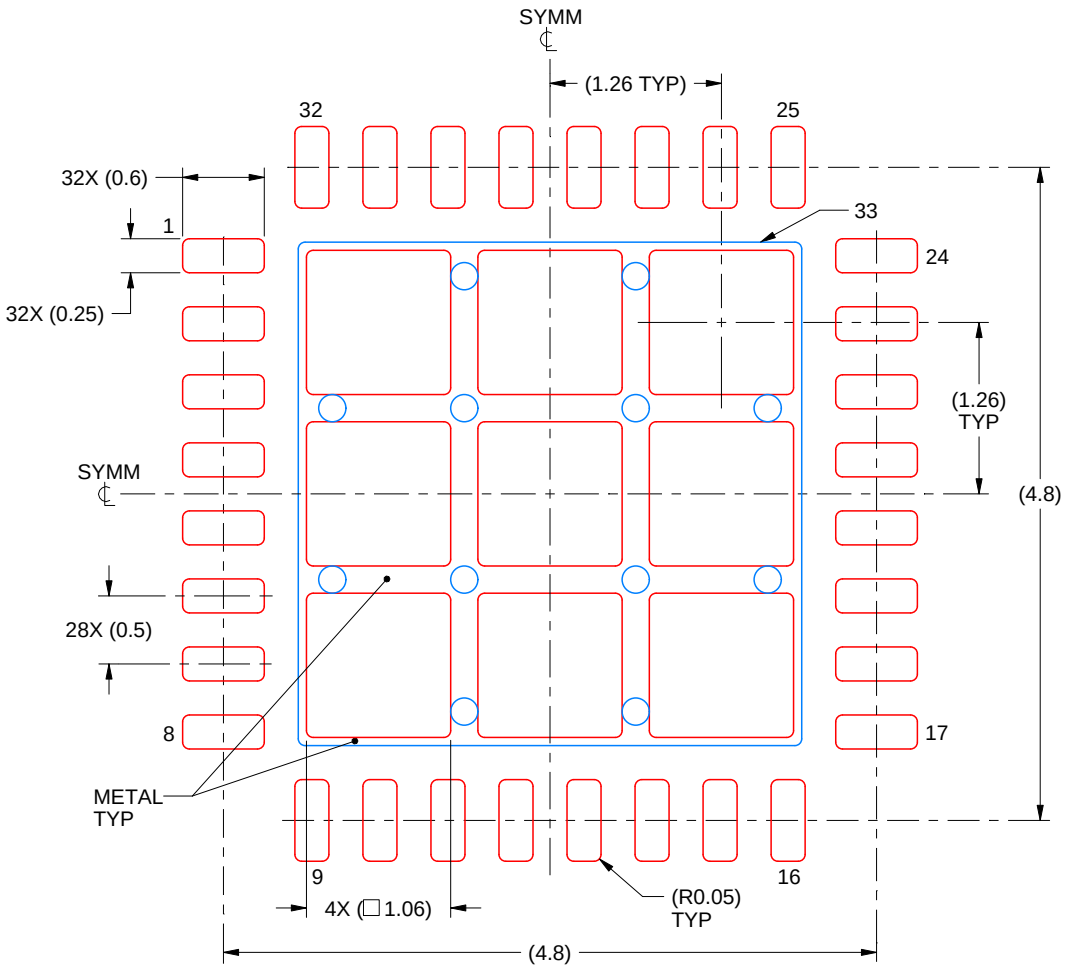



SOLDER MASK DETAILS

4219073/A 03/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
74% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:18X

4219073/A 03/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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