TEXAS INSTRUMENTS

ADS1257

SBAS656B –SEPTEMBER 2015–REVISED APRIL 2016

ADS1257 30-kSPS, 4-Channel, 24-Bit ADC with PGA in 5-mm × 5-mm VQFN Package

1 Features

- Up to 23-Bits Noise-Free Resolution
- Small 5-mm × 5-mm VQFN Package
- 4 Analog Inputs
  - 2 Differential or 3 Single-Ended Measurements
- Excellent DC Performance
  - Offset Drift: 4 nV/°C (Gain = 64)
  - Gain Drift: 0.8 ppm/°C
  - Nonlinearity: 3 ppm (Gain = 1)
- Programmable Data Rates: 2.5 SPS to 30 kSPS
- Single-Cycle Settled Conversions (≤ 1000 SPS)
- 50-Hz and 60-Hz Rejection
- High Impedance Input Buffer
- Differential-Input PGA
- Integrated Sensor Break Detection
- 2 General-Purpose Input/Outputs
- Power Supplies:
  - Analog: 5 V
  - Digital: 1.8 V to 3.6 V
- 5-V Tolerant SPI™-Compatible Serial Interface

2 Applications

- Factory Automation and Process Control
- Test and Measurement
- Medical Equipment
- Scientific Instrumentation

3 Description

The ADS1257 is a low-noise, 30-kSPS, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) with an integrated multiplexer (mux), input buffer, and programmable gain amplifier (PGA) in a small 20-pin, 5-mm × 5-mm VQFN package. The combination of integration, high conversion rate, and 24-bit resolution together in a small package makes the device ideally suited for space-constrained applications.

The input multiplexer accepts either two differential or three single-ended input measurements. The sensor-break detection circuit verifies the input connection continuity to the ADC. The selectable input buffer greatly increases the input impedance, and in many cases, eliminates the need for external buffers. The buffer input voltage range includes AGND. The low-noise PGA provides gains from 1 to 64 to accommodate a wide range of inputs signals. The programmable digital filter optimizes ADC resolution (up to 23 bits noise-free) and conversion rates (up to 30 kSPS). The digital filter provides single-cycle settled conversions, and rejection of 50-Hz and 60-Hz interference signals.
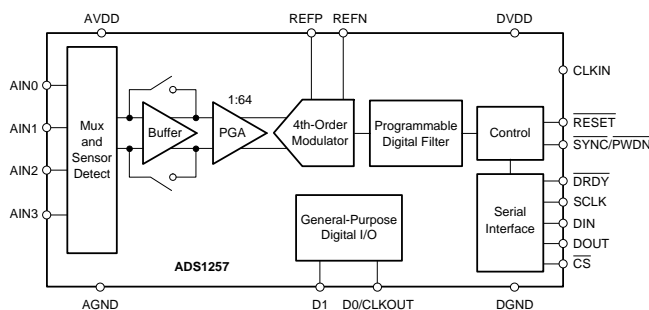
The SPI-compatible serial interface operates with as little as three wires, simplifying connections to external controllers. Integrated calibration features support both self and system correction of offset and gain errors for all PGA gain settings. Two bidirectional digital I/Os pins control external circuits.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADS1257	VQFN (20)	5.00 mm × 5.00 mm

(1) For all available packages, see the package option addendum at the end of the data sheet.

Block Diagram

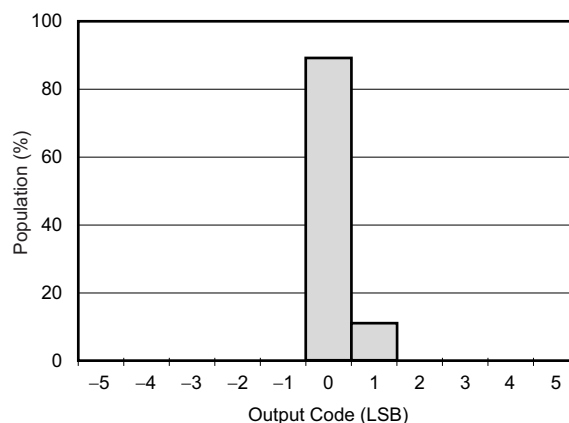**Output Data Histogram (256 Readings, 2.5 SPS, Gain = 1)**

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

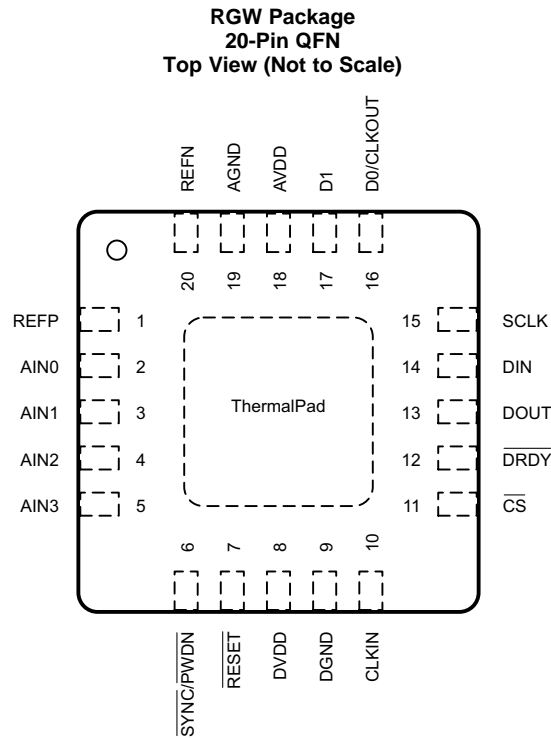# 5 Device Comparison Table

DEVICE	SINGLE-ENDED INPUTS	DIFFERENTIAL INPUTS	NUMBER OF GPIOS
ADS1255	2	1	2
ADS1256	8	4	4
ADS1257	3	2	2

6 Pin Configuration and Functions

**RGW Package
20-Pin QFN
Top View (Not to Scale)**

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	REFP	Analog input	Positive reference input
2	AIN0	Analog input	Analog input 0; Leave unconnected or connect to AVDD if not used[1]
3	AIN1	Analog input	Analog input 1; Leave unconnected or connect to AVDD if not used[1]
4	AIN2	Analog input	Analog input 2; Leave unconnected or connect to AVDD if not used[1]
5	AIN3	Analog input	Analog input 3; Leave unconnected or connect to AVDD if not used[1]
6	$\overline{\text{SYNC}}$/$\overline{\text{PWDN}}$	Digital input[2][3]	Synchronization or power-down input, active low; Connect to DVDD if not used[1]
7	$\overline{\text{RESET}}$	Digital input[2][3]	Reset input, active low; Connect to DVDD if not used[1]
8	DVDD	Digital	Digital power supply; Connect decoupling capacitor to DGND
9	DGND	Digital	Digital ground
10	CLKIN	Digital input[3]	External clock input
11	$\overline{\text{CS}}$	Digital input[2][3]	Chip select, active low; Connect to DGND if not used
12	$\overline{\text{DRDY}}$	Digital output	Data ready output; active low
13	DOUT	Digital output	Serial data output
14	DIN	Digital input[2][3]	Serial data input
15	SCLK	Digital input[2][3]	Serial clock input
16	D0/CLKOUT	Digital input/output[4]	General-purpose digital I/O 0 or clock output[1]
17	D1	Digital input/output[4]	General-purpose digital I/O 1[1]
18	AVDD	Analog	Analog power supply; Connect decoupling capacitor to AGND
19	AGND	Analog	Analog ground
20	REFN	Analog input	Negative reference input
	Thermal Pad	—	Thermal power pad; Connect to AGND

(1) See the *Unused Inputs and Outputs* section for additional details.
(2) Schmitt-trigger digital input.
(3) 5-V tolerant digital input.
(4) Schmitt-trigger digital input when the digital I/O is configured as an input.

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Product Folder Links: *ADS1257*

7 Specifications

7.1 Absolute Maximum Ratings[1]

		MIN	MAX	UNIT
Power-supply voltage	AVDD to AGND	−0.3	6.0	V
	DVDD to DGND	−0.3	3.6	
Analog input voltage	AINx, REFP, REFN	AGND − 0.3	AVDD + 0.3	V
Digital input voltage	DIN, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SYNC}/\overline{PWDN}$, CLKIN	DGND − 0.3	DGND + 6.0	V
	D0/CLKOUT, D1	DGND − 0.3	DVDD + 0.3	
Input current	Continuous, any pins except power-supply pins	−10	10	mA
Temperature	Operating ambient, T_A	−40	105	°C
	Junction, T_J	−40	150	
	Storage, T_{stg}	−60	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
	Analog power supply	AVDD to AGND	4.75	5	5.25	V
	Digital power supply	DVDD to DGND	1.8		3.6	V
	Analog-to-digital ground potential	AGND to DGND	−0.1	0	0.1	V
ANALOG INPUTS						
V_{IN}	Differential input voltage	$V_{IN} = V_{(AINP)} − V_{(AINN)}$	$−2\ V_{REF}$ / Gain		$2\ V_{REF}$ / Gain	V
$V_{(AINx)}$	Absolute input voltage	Buffer off	AGND − 0.1		AVDD + 0.1	V
		Buffer on	AGND		AVDD − 2.0	
VOLTAGE REFERENCE INPUTS						
V_{REF}	Differential reference input voltage	$V_{REF} = V_{(REFP)} − V_{(REFN)}$	0.5	2.5	2.6	V
$V_{(REFN)}$	Absolute negative reference input voltage	Buffer off	AGND − 0.1		$V_{(REFP)}$ − 0.5	V
		Buffer on[1]	AGND		$V_{(REFP)}$ − 0.5	
$V_{(REFP)}$	Absolute positive reference input voltage	Buffer off	$V_{(REFN)}$ + 0.5		AVDD + 0.1	V
		Buffer on[1]	$V_{(REFN)}$ + 0.5		AVDD − 2.0	
CLOCK SOURCE						
$f_{(CLKIN)}$	Clock frequency		0.1	7.68	10	MHz
	Duty cycle		40%	50%	60%	
DIGITAL INPUTS						
	Digital input voltage	DIN, SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SYNC}$/PWDN, CLKIN	DGND		DGND + 5.25	V
		D0/CLKOUT, D1	DGND		DVDD	
TEMPERATURE						
T_A	Operating ambient temperature		−40		85	°C

(1) The reference input range with buffer on is restricted only if self-calibration is used. If using system calibration or writing calibration values directly to the registers, the buffer off range can be used for the reference input range.

7.4 Thermal Information

THERMAL METRIC[1]		ADS1257	UNIT
		RGW (QFN)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Minimum and maximum specifications apply from T_A = −40°C to +85°C. Typical specifications are at T_A = 25°C.
All specifications at AVDD = 5 V, DVDD = 1.8 V, buffer on, $f_{(CLKIN)}$ = 7.68 MHz, gain = 1, and V_{REF} = 2.5 V (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
Gain	PGA gain			1, 2, 4, 8, 16, 32, 64		V/V
	Differential input impedance	Buffer off, gain = 1, 2, 4, 8, 16		150 / Gain		kΩ
		Buffer off, gain = 32, 64		4.7		
		Buffer on, DR ≤ 50 SPS[1]		80		MΩ
SYSTEM PERFORMANCE						
	Resolution	All data rates and PGA gain settings		24		Bit
DR	Data rate		2.5		30,000	SPS
INL	Integral nonlinearity	Differential input, gain = 1, buffer off		3	10	ppm
		Differential input, gain = 64, buffer off		7		
V_{IO}	Input offset voltage	After calibration		On the level of the noise		
	Offset drift	Gain = 1		100		nV/°C
		Gain = 64		4		
	Gain error	After calibration, gain = 1, buffer on		±0.005%		
		After calibration, gain = 64, buffer on		±0.03%		
	Gain drift	Gain = 1		0.8		ppm/°C
		Gain = 64		0.8		
CMRR	Common-mode rejection ratio	f_{CM} = 60 Hz, DR = 30 kSPS[2]	95	110		dB
PSRR	Power-supply rejection ratio	Analog, ±5% Δ in AVDD	60	70		dB
		Digital, ±10% Δ in DVDD		100		dB
VOLTAGE REFERENCE INPUTS						
	Reference input impedance			18.5		kΩ
SENSOR DETECT CURRENT SOURCES						
	Current settings			0.5, 2, 10		µA
DIGITAL INPUTS/OUTPUTS						
V_{IH}	High-level input voltage	DIN, SCLK, CLKIN, $\overline{SYNC}/\overline{PWDN}$, $\overline{CS}$, $\overline{RESET}$	0.8 DVDD		5.25	V
		D0/CLKOUT, D1	0.8 DVDD		DVDD	V
V_{IL}	Low-level input voltage		DGND		0.2 DVDD	
V_{OH}	High-level output voltage	I_{OH} = 4 mA	0.8 DVDD			V
V_{OL}	Low-level output voltage	I_{OL} = 4 mA			0.2 DVDD	V
	Input hysteresis			0.5		V
	Input leakage	0 < digital input voltage < DVDD	−10		10	µA
POWER SUPPLY						
I_{AVDD}	Analog supply current	Power-down mode			5	µA
		Standby mode		20		µA
		Normal mode, gain = 1, buffer off		7	10	mA
		Normal mode, gain = 64, buffer off		16	24	mA
		Normal mode, gain = 1, buffer on		13	19	mA
		Normal mode, gain = 64, buffer on		36	50	mA
I_{DVDD}	Digital supply current	Power-down mode			5	µA
		Standby mode, CLKOUT off, DVDD = 3.3 V		95		µA
		Normal mode, CLKOUT off, DVDD = 3.3 V		0.9	2	mA
P_D	Power dissipation	Normal mode, gain = 1, buffer off, DVDD = 3.3 V		38	57	mW
		Standby mode, DVDD = 3.3 V		0.4		

(1) See the *Analog Input Buffer* section for more information on input impedance.
(2) f_{CM} is the frequency of the common-mode input signal. Place a notch of the digital filter at 60 Hz by setting DR = 60 samples per second.(SPS), 30 SPS, 15 SPS, 10 SPS, 5 SPS, or 2.5 SPS to further improve the common-mode rejection of this frequency.

7.6 Serial Interface Timing Requirements

over recommended operating conditions (unless otherwise noted)

				MIN	MAX	UNIT
t_1	SCLK period			4		$t_{(CLKIN)}$ [1]
					10	$t_{(DATA)}$ [2]
t_{2H}	Pulse duration, SCLK high			200		ns
					9	$t_{(DATA)}$
t_{2L}	Pulse duration, SCLK low			200		ns
t_3	Delay time, $\overline{CS}$ falling edge to first SCLK rising edge [3]			50		ns
t_4	Setup time, DIN valid before SCLK falling edge			50		ns
t_5	Hold time, DIN valid after SCLK falling edge			50		ns
t_6	Delay time, last SCLK falling edge for DIN to first SCLK rising edge for DOUT: RDATA, RDATAC, RREG Commands			50		$t_{(CLKIN)}$
t_{10}	Delay time, final SCLK falling edge to $\overline{CS}$ rising edge			8		$t_{(CLKIN)}$
t_{11}	Delay time, final SCLK falling edge of command to first SCLK rising edge of next command	RREG, WREG, RDATA		4		$t_{(CLKIN)}$
		RDATAC, SDATAC, SYNC		24		$t_{(CLKIN)}$
t_{11B}	Pulse duration, $\overline{CS}$ high			4		$t_{(CLKIN)}$

(1) Master clock period: $t_{(CLKIN)} = 1 / f_{(CLKIN)}$.
(2) Output data period: $t_{(DATA)} = 1 / DR$.
(3) $\overline{CS}$ can be tied low.

7.7 Serial Interface Switching Characteristics

over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_7	Propagation delay time, SCLK rising edge to valid new DOUT	DOUT load = 20 pF || 100 kΩ to DGND			50	ns
t_8	Propagation delay time, SCLK rising edge to DOUT invalid		0			ns
t_9	Propagation delay time, last SCLK falling edge to DOUT high impedance		6		10	$t_{(CLKIN)}$
t_{11C}	Propagation delay time, $\overline{CS}$ rising edge to DOUT high impedance		0		50	ns
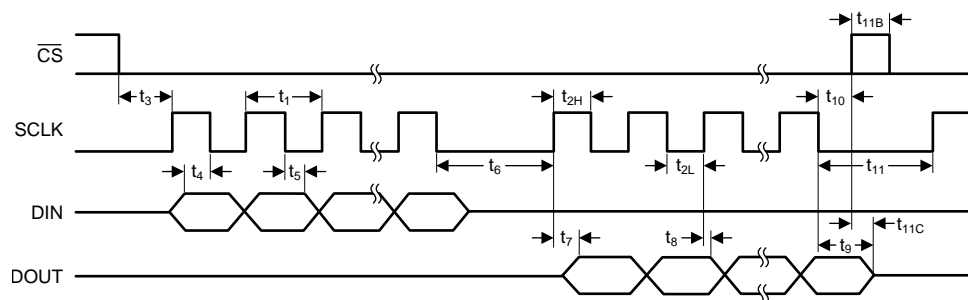
Figure 1. Serial Interface Timing

Product Folder Links: *ADS1257*

7.8 $\overline{\text{RESET}}$ and $\overline{\text{SYNC}}$/PWDN Timing Requirements

over recommended operating conditions (unless otherwise noted)

		MIN	MAX	UNIT
t_{16}	Pulse duration, $\overline{\text{RESET}}$, $\overline{\text{SYNC}}$/PWDN low	4		$t_{(CLKIN)}$ [(1)]
t_{16B}	Delay time, $\overline{\text{SYNC}}$/PWDN rising edge to CLKIN rising edge	−25	25	ns

(1) Master clock period: $t_{(CLKIN)} = 1 / f_{(CLKIN)}$

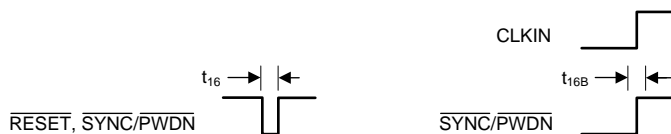**Figure 2. $\overline{\text{RESET}}$ and $\overline{\text{SYNC}}$/PWDN Timing**

7.9 SCLK Reset Timing Requirements

over recommended operating conditions (unless otherwise noted)

		MIN	MAX	UNIT
t_{12}	Pulse duration, first high pulse	300	500	$t_{(CLKIN)}$ [(1)]
t_{13}	Pulse duration, low pulse	5		$t_{(CLKIN)}$
t_{14}	Pulse duration, second high pulse	550	750	$t_{(CLKIN)}$
t_{15}	Pulse duration, third high pulse	1050	1250	$t_{(CLKIN)}$

(1) Master clock period: $t_{(CLKIN)} = 1 / f_{(CLKIN)}$
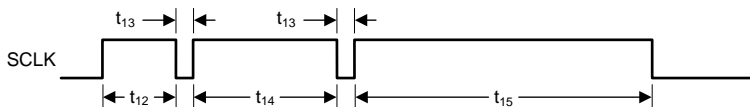
Figure 3. SCLK Reset Timing

7.10 $\overline{\text{DRDY}}$ Update Timing Characteristics

over recommended operating conditions (unless otherwise noted)

		MIN	MAX	UNIT
t_{17}	Pulse duration, conversion data invalid while updating	16		$t_{(CLKIN)}$ [(1)]

(1) Master clock period: $t_{(CLKIN)} = 1 / f_{(CLKIN)}$

NOTE: $\overline{\text{DRDY}}$ shown with no data retrieval.

Figure 4. $\overline{\text{DRDY}}$ Update Timing

7.11 Typical Characteristics

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, $f_{(CLKIN)}$ = 7.68 MHz, and V_{REF} = 2.5 V (unless otherwise noted)
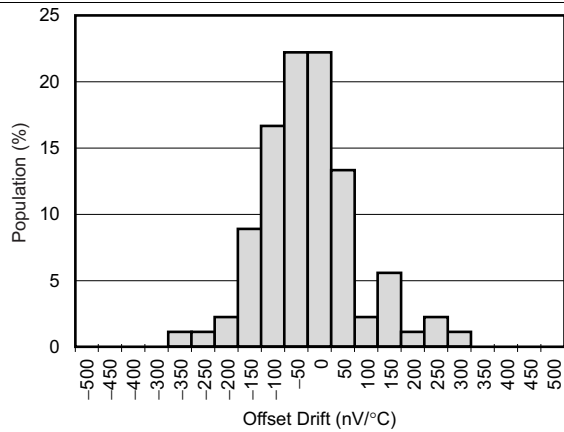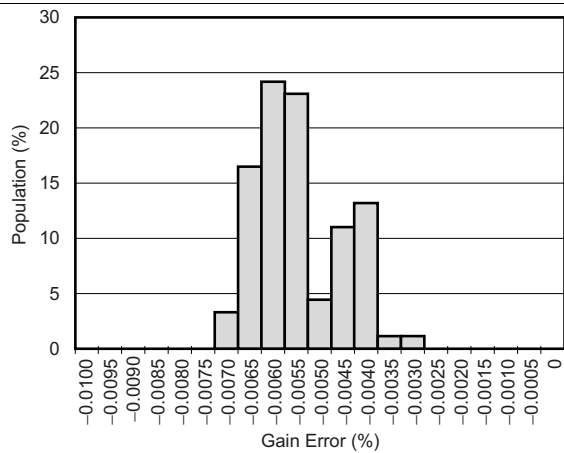

Gain = 1, 90 units from three production lots

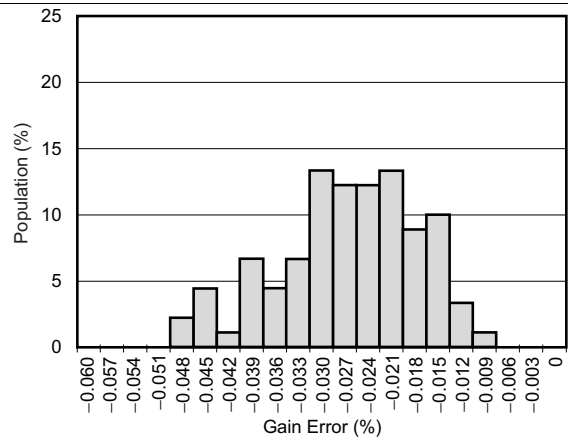**Figure 5. Offset Drift Histogram**
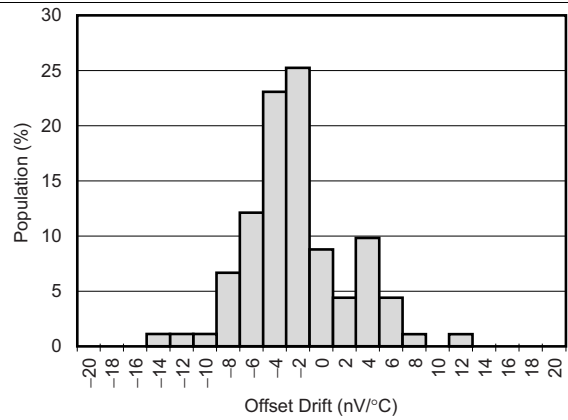
Gain = 64, 90 units from three production lots

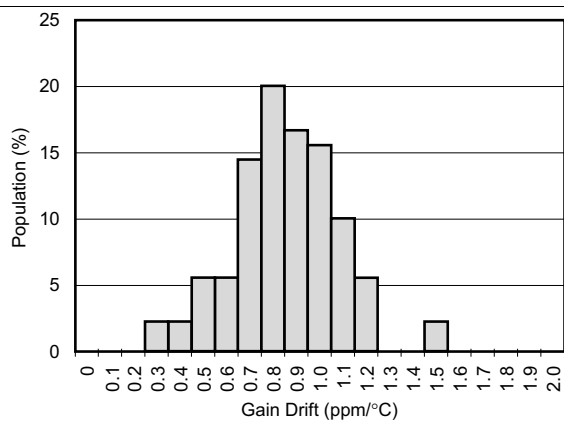**Figure 6. Offset Drift Histogram**

Gain = 1, 90 units from three production lots
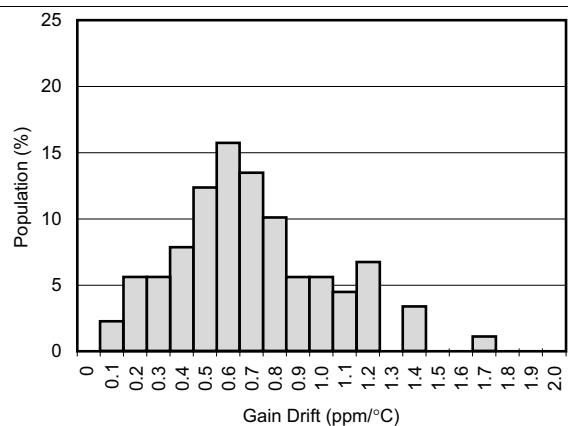
Figure 7. Gain Error Histogram

Gain = 64, 90 units from three production lots

Figure 8. Gain Error Histogram

Gain = 1, 90 units from three production lots

Figure 9. Gain Drift Histogram

Gain = 64, 90 units from three production lots

Figure 10. Gain Drift Histogram

Product Folder Links: *ADS1257*

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, $f_{(CLKIN)}$ = 7.68 MHz, and V_{REF} = 2.5 V (unless otherwise noted)

Gain = 1, data rate = 2.5 SPS, buffer = off, 256 readings

Figure 11. Noise Histogram
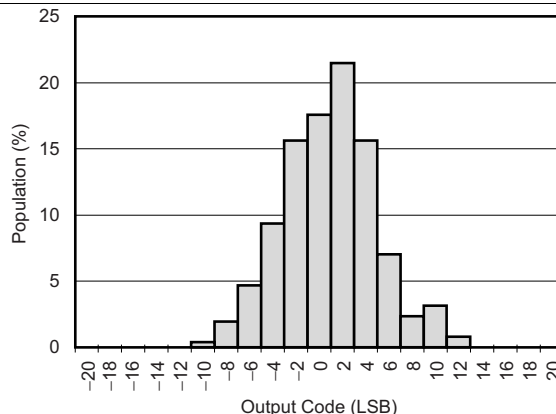
Gain = 64, data rate = 2.5 SPS, buffer = off, 256 readings

Figure 12. Noise Histogram
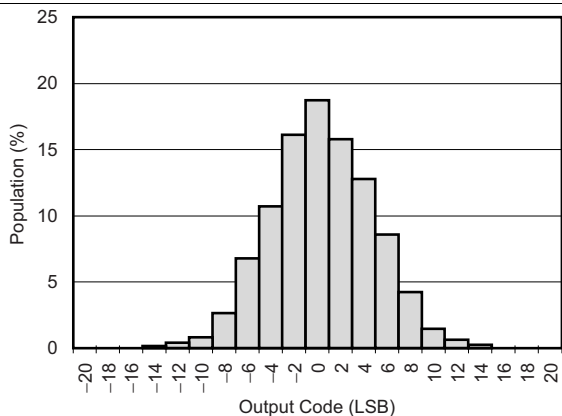
Gain = 1, data rate = 1 kSPS, buffer = off, 4096 readings

Figure 13. Noise Histogram
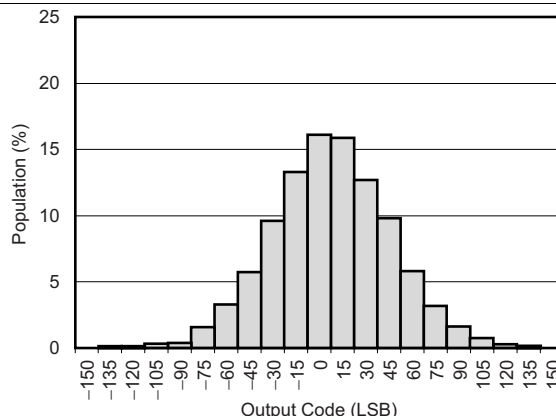
Gain = 64, data rate = 1 kSPS, buffer = off, 4096 readings

Figure 14. Noise Histogram
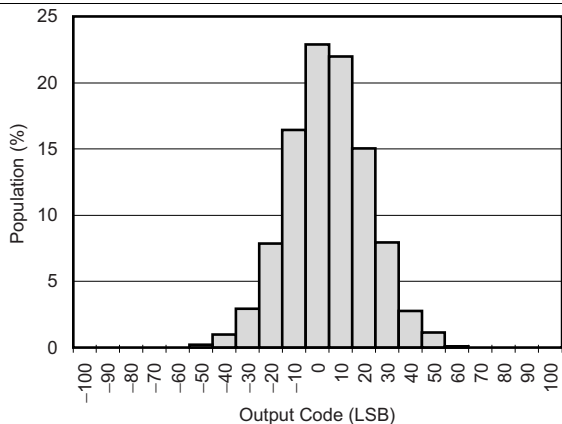
Gain = 1, data rate = 30 kSPS, buffer = off, 4096 readings

Figure 15. Noise Histogram
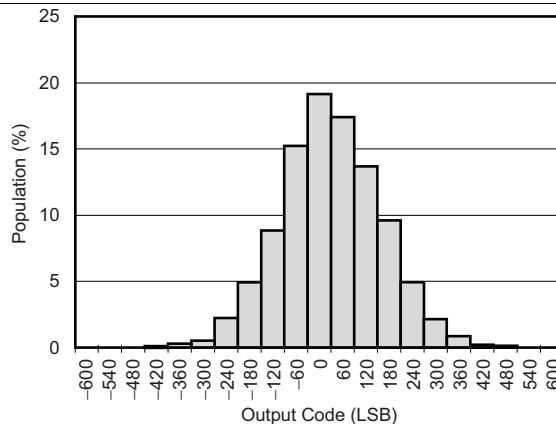
Gain = 64, data rate = 30 kSPS, buffer = off, 4096 readings

Figure 16. Noise Histogram

Typical Characteristics (continued)

at T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, $f_{(CLKIN)}$ = 7.68 MHz, and V_{REF} = 2.5 V (unless otherwise noted)

Gain = 1
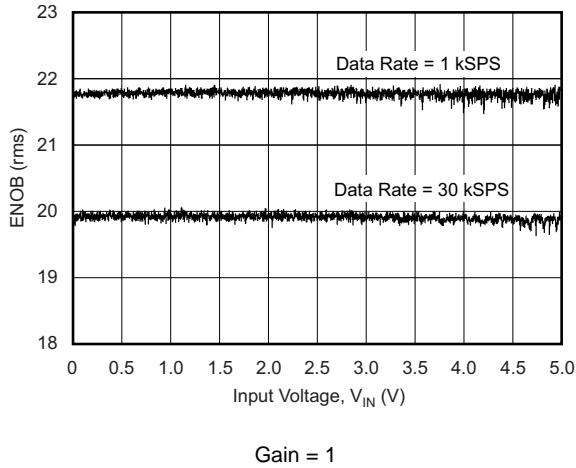
Figure 17. Effective Number of Bits vs Input Voltage

Gain = 1
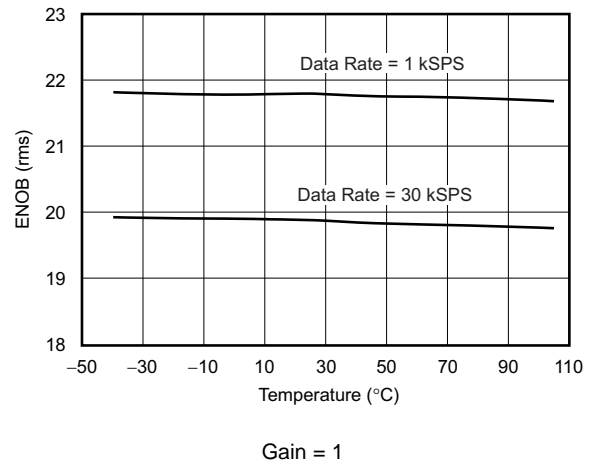
Figure 18. Effective Number of Bits vs Temperature

Gain = 1
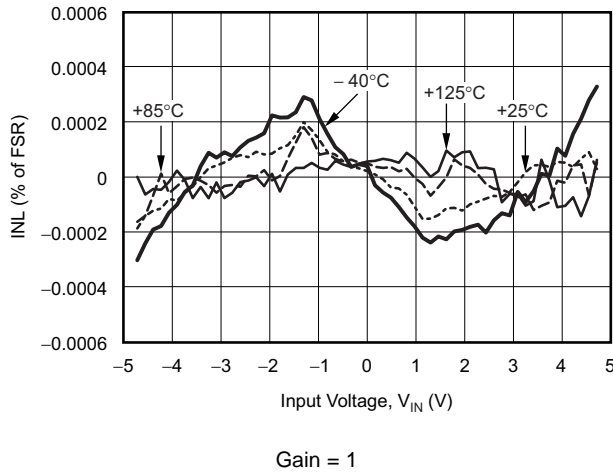
Figure 19. Integral Nonlinearity vs Input Signal
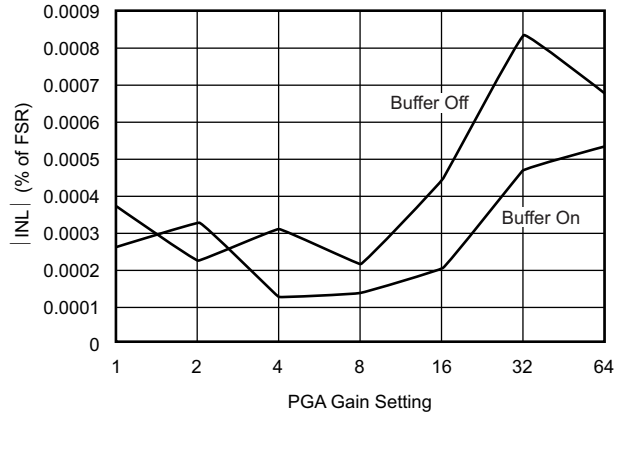
Figure 20. Integral Nonlinearity vs PGA Gain
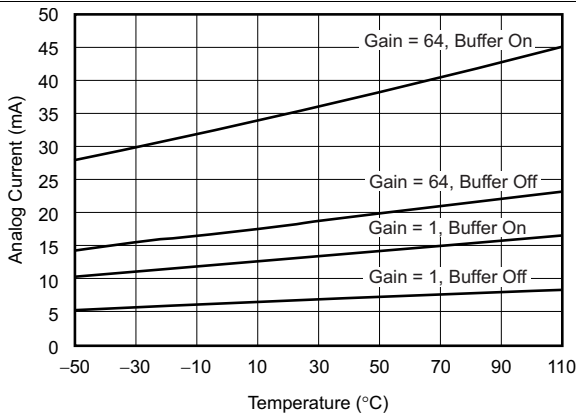
Figure 21. Analog Supply Current vs Temperature
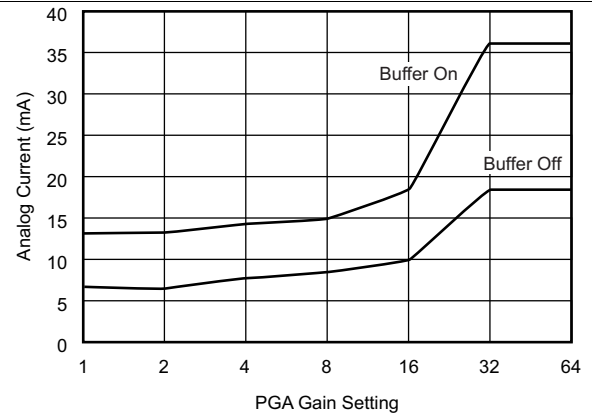
Figure 22. Analog Supply Current vs PGA Gain

Product Folder Links: *ADS1257*

8 Parameter Measurement Information

8.1 Noise Performance

The ADS1257 offers outstanding noise performance that can be optimized by adjusting the data rate or PGA gain setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. The PGA reduces the input-referred noise when measuring lower level signals. Table 1 through Table 4 summarize the typical noise performance with the inputs shorted externally.

In all four tables, the following conditions apply: T_A = 25°C, AVDD = 5 V, DVDD = 1.8 V, V_{REF} = 2.5 V, and $f_{(CLKIN)}$ = 7.68 MHz.

Table 1 and Table 3 show the root-mean-square (RMS) value of the input-referred noise. Table 2 and Table 4 show the effective number of bits of resolution (ENOB), using the noise data from Table 1 and Table 3 respectively. ENOB is defined as shown in Equation 1:

$$\text{ENOB} = \frac{\ln\left(\text{FSR}\,/\,\text{RMS Noise}\right)}{\ln(2)}$$

where FSR is the full-scale range: FSR = 4 · V_{REF} / Gain　　　　　　　　　　　　　　　　(1)

Table 2 and Table 4 also show the noise-free bits of resolution in parenthesis. Noise-free bits are calculated with the same formula as ENOB except the peak-to-peak noise values are used instead of RMS noise.

Table 1. Input-Referred Noise (μV_{RMS}) With Buffer On

DATA RATE (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
2.5	0.247	0.156	0.080	0.056	0.043	0.037	0.033
5	0.301	0.175	0.102	0.076	0.061	0.045	0.044
10	0.339	0.214	0.138	0.106	0.082	0.061	0.061
15	0.401	0.264	0.169	0.126	0.107	0.085	0.073
25	0.494	0.305	0.224	0.149	0.134	0.102	0.093
30	0.533	0.335	0.245	0.176	0.138	0.104	0.106
50	0.629	0.393	0.292	0.216	0.168	0.136	0.122
60	0.692	0.438	0.321	0.233	0.184	0.146	0.131
100	0.875	0.589	0.409	0.305	0.229	0.170	0.169
500	1.946	1.250	0.630	0.648	0.497	0.390	0.367
1000	2.931	1.891	1.325	1.070	0.689	0.512	0.486
2000	4.173	2.589	1.827	1.492	0.943	0.692	0.654
3750	5.394	3.460	2.376	1.865	1.224	0.912	0.906
7500	7.249	4.593	3.149	2.436	1.691	1.234	1.187
15,000	9.074	5.921	3.961	2.984	2.125	1.517	1.515
30,000	10.728	6.705	4.446	3.280	2.416	1.785	1.742

Table 2. Effective Number of Bits (Noise-Free Resolution) With Buffer On

DATA RATE (SPS)	PGA GAIN						
	1[1]	2	4	8	16	32	64
2.5	24.5 (22.3)	24.9 (22.6)	24.9 (22.1)	24.4 (21.7)	23.8 (21.3)	23.0 (20.8)	22.2 (19.7)
5	24.2 (21.6)	24.8 (22.4)	24.5 (21.9)	24.0 (21.3)	23.3 (20.7)	22.7 (20.3)	21.8 (19.3)
10	24.1 (21.6)	24.5 (22.0)	24.1 (21.6)	23.5 (21.0)	22.9 (20.4)	22.3 (19.9)	21.3 (18.9)
15	23.8 (21.3)	24.2 (21.7)	23.8 (21.3)	23.2 (20.7)	22.5 (20.1)	21.8 (19.3)	21.0 (18.7)
25	23.5 (21.0)	24.0 (21.4)	23.4 (21.1)	23.0 (20.5)	22.2 (19.7)	21.5 (19.2)	20.7 (18.5)
30	23.4 (21.1)	23.8 (21.3)	23.3 (20.8)	22.8 (20.4)	22.1 (19.8)	21.5 (19.0)	20.5 (18.1)
50	23.2 (20.6)	23.6 (21.1)	23.0 (20.4)	22.5 (19.9)	21.8 (19.4)	21.1 (18.8)	20.3 (17.9)
60	23.0 (20.6)	23.4 (20.9)	22.9 (20.5)	22.4 (19.8)	21.7 (19.3)	21.0 (18.8)	20.2 (17.8)
100	22.7 (20.2)	23.0 (20.7)	22.5 (20.2)	22.0 (19.6)	21.4 (19.1)	20.8 (18.5)	19.8 (17.4)
500	21.6 (19.4)	21.9 (19.6)	21.5 (19.1)	20.9 (18.6)	20.3 (18.0)	19.6 (17.3)	18.7 (16.3)
1000	21.0 (18.3)	21.3 (18.6)	20.8 (18.1)	20.2 (17.5)	19.8 (17.2)	19.2 (16.5)	18.3 (15.6)
2000	20.5 (17.8)	20.9 (18.1)	20.4 (17.8)	19.7 (17.0)	19.3 (16.6)	18.8 (16.1)	17.9 (15.3)
3750	20.1 (17.4)	20.5 (17.8)	20.0 (17.3)	19.4 (16.6)	19.0 (16.2)	18.4 (15.7)	17.4 (14.7)
7500	19.7 (17.0)	20.1 (17.3)	19.6 (16.9)	19.0 (16.2)	18.5 (15.8)	17.9 (15.3)	17.0 (14.4)
15,000	19.3 (16.6)	19.7 (17.0)	19.3 (16.5)	18.7 (15.9)	18.2 (15.5)	17.7 (14.9)	16.7 (13.9)
30,000	19.1 (16.4)	19.5 (16.7)	19.1 (16.4)	18.5 (15.9)	18.0 (15.4)	17.4 (14.6)	16.5 (13.8)

(1) The full FSR cannot be used when V_{REF} = 2.5 V, gain = 1 V/V, and buffer enabled because of the limited absolute input voltage. Therefore, the values in this column are calculated using a maximum FSR = 6 V.

Table 3. Input-Referred Noise (μV_{RMS}) With Buffer Off

DATA RATE (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
2.5	0.247	0.149	0.097	0.058	0.036	0.031	0.027
5	0.275	0.176	0.109	0.07	0.046	0.039	0.038
10	0.338	0.201	0.129	0.084	0.063	0.048	0.047
15	0.401	0.221	0.15	0.109	0.07	0.063	0.057
25	0.485	0.279	0.177	0.136	0.093	0.076	0.076
30	0.559	0.315	0.202	0.142	0.107	0.093	0.082
50	0.644	0.39	0.238	0.187	0.129	0.108	0.103
60	0.688	0.417	0.281	0.204	0.134	0.109	0.111
100	0.815	0.53	0.36	0.233	0.169	0.123	0.122
500	1.957	1.148	0.772	0.531	0.375	0.276	0.259
1000	2.803	1.797	1.191	0.94	0.518	0.392	0.365
2000	4.025	2.444	1.615	1.31	0.7	0.526	0.461
3750	5.413	3.25	2.061	1.578	0.914	0.693	0.625
7500	7.017	4.143	2.722	1.998	1.241	0.914	0.857
15,000	8.862	5.432	3.378	2.411	1.569	1.149	1.051
30,000	10.341	6.137	3.873	2.775	1.805	1.313	1.211

Table 4. Effective Number of Bits (Noise-Free Resolution) With Buffer Off

| DATA RATE (SPS)	PGA GAIN						
	1	2	4	8	16	32	64
2.5	25.3 (23.0)	25.0 (22.4)	24.6 (22.0)	24.4 (21.9)	24.0 (21.3)	23.2 (21.1)	22.5 (20.0)
5	25.1 (22.4)	24.8 (22.1)	24.5 (21.9)	24.1 (21.5)	23.7 (21.2)	22.9 (20.4)	22.0 (19.4)
10	24.8 (22.3)	24.6 (22.1)	24.2 (21.7)	23.8 (21.5)	23.2 (20.8)	22.6 (20.3)	21.7 (19.2)
15	24.6 (22.0)	24.4 (21.8)	24.0 (21.4)	23.4 (20.8)	23.1 (20.6)	22.2 (19.9)	21.4 (19.0)
25	24.3 (21.8)	24.1 (21.7)	23.8 (21.1)	23.1 (20.7)	22.7 (20.3)	22.0 (19.5)	21.0 (18.6)
30	24.1 (21.6)	23.9 (21.4)	23.6 (21.1)	23.1 (20.4)	22.5 (20.0)	21.7 (16.4)	20.9 (18.5)
50	23.9 (21.3)	23.6 (21.3)	23.3 (20.7)	22.7 (20.1)	22.2 (19.8)	21.5 (19.1)	20.5 (18.2)
60	23.8 (21.2)	23.5 (21.0)	23.1 (20.6)	22.5 (20.0)	22.1 (19.8)	21.5 (19.1)	20.4 (18.1)
100	23.5 (21.1)	23.2 (20.5)	22.7 (20.3)	22.4 (19.9)	21.8 (19.5)	21.3 (19.0)	20.3 (17.9)
500	22.3 (20.0)	22.1 (19.7)	21.6 (19.3)	21.2 (18.9)	20.7 (18.3)	20.1 (17.8)	19.2 (16.9)
1000	21.8 (19.0)	21.4 (18.7)	21.0 (18.4)	20.3 (17.7)	20.2 (17.5)	19.6 (16.9)	18.7 (15.9)
2000	21.2 (18.5)	21.0 (18.3)	20.6 (17.9)	19.9 (17.4)	19.8 (17.0)	19.2 (16.4)	18.4 (15.6)
3750	20.8 (18.1)	20.6 (17.8)	20.2 (17.5)	19.6 (17.0)	19.4 (16.7)	18.8 (16.1)	17.9 (15.2)
7500	20.4 (17.7)	20.2 (17.6)	19.8 (17.0)	19.3 (16.6)	18.9 (16.2)	18.4 (15.7)	17.5 (14.8)
15,000	20.1 (17.4)	19.8 (17.1)	19.5 (16.8)	19.0 (16.3)	18.6 (15.9)	18.1 (15.3)	17.2 (14.4)
30,000	19.9 (17.1)	19.6 (17.0)	19.3 (16.6)	18.8 (16.0)	18.4 (15.6)	17.9 (15.0)	17.0 (14.3)

9 Detailed Description

9.1 Overview

The ADS1257 is a very low-noise ADC that supports four analog inputs and offers two general-purpose digital I/Os. The *Functional Block Diagram* shows a block diagram of the ADS1257. The input multiplexer selects the ADC input pin connection. Selectable current sources within the input multiplexer check for open- or short-circuit conditions on the external sensor. A selectable input buffer greatly reduces the input circuitry loading by providing up to 80 MΩ of impedance. A low-noise PGA provides gains of 1 V/V, 2 V/V, 4 V/V, 8 V/V, 16 V/V, 32 V/V, or 64 V/V. The ADS1257 is comprised of a fourth-order, delta-sigma modulator followed by a programmable digital filter.

The modulator measures the amplified differential input signal, $V_{IN} \cdot Gain = (V_{(AINP)} - V_{(AINN)}) \cdot Gain$, against the differential reference, $V_{REF} = V_{(REFP)} - V_{(REFN)}$. The ADC requires an external reference voltage to operate. The differential reference is scaled internally by a factor of two so that the full-scale input range is $\pm 2 \cdot V_{REF} / Gain$.

The digital filter receives the modulator signal and provides a low-noise digital output. The data rate of the filter is programmable from 2.5 SPS to 30 kSPS, and allows tradeoffs between resolution and speed.

Communication is over an SPI-compatible serial interface with a set of commands providing control of the ADS1257. The configuration registers store the various settings for the input multiplexer, sensor-detect current sources, input buffer enable, PGA gain setting, output data rate, and more. The ADC requires an external clock source to operate. General-purpose digital I/Os provide static read and write control of up to two pins. The D0 pin is also used to supply a programmable clock output.

9.2 Functional Block Diagram
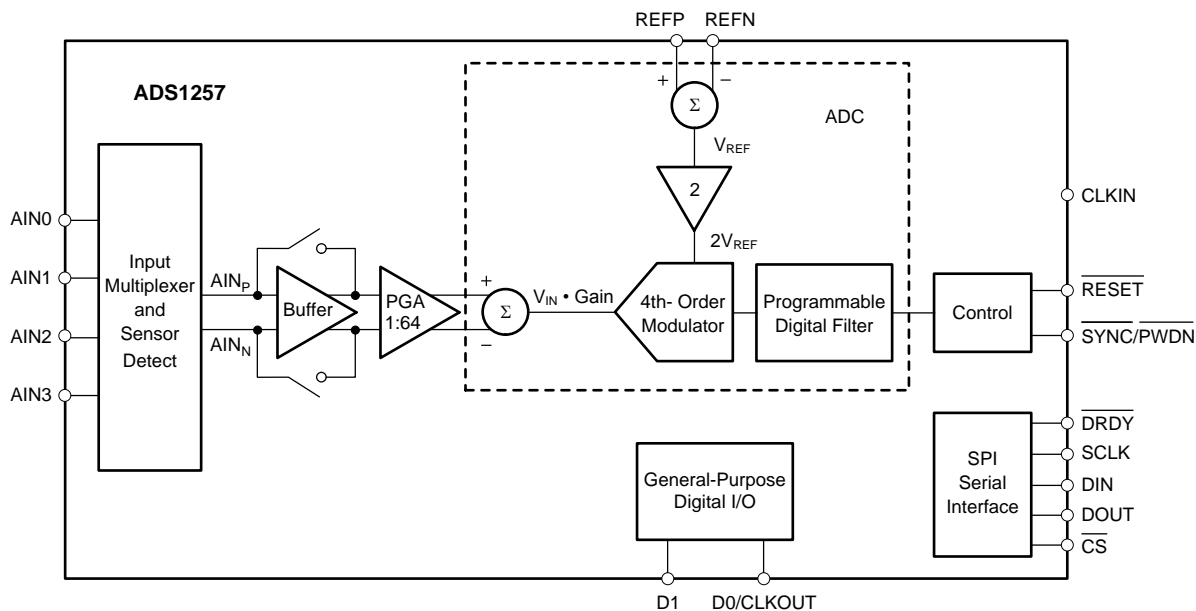
9.3 Feature Description

9.3.1 Input Multiplexer

Figure 23 shows a simplified diagram of the input multiplexer. Select any pin as the positive input (AIN$_P$) and any pin as the negative input (AIN$_N$). Pin selection is controlled by the MUX register.
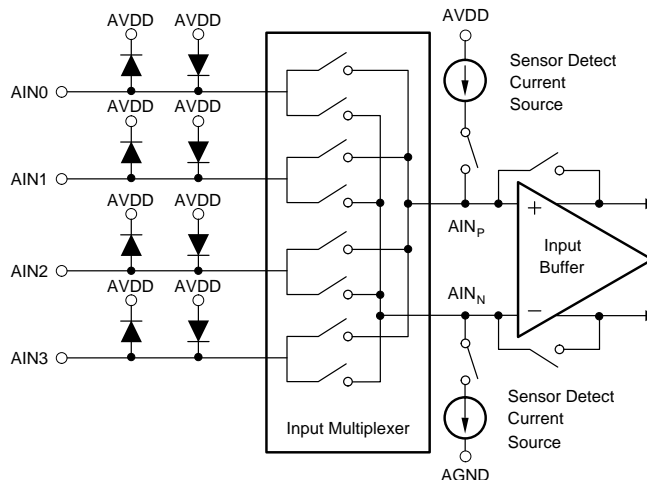
Figure 23. Simplified Diagram of the Input Multiplexer

The ADS1257 offers four analog inputs that can be configured as two independent differential inputs, three single-ended inputs, or a combination of differential and single-ended inputs.

In general, there are no restrictions on input-pin selection. However, follow these recommendations for optimal performance:

1. Preferably, use adjacent inputs for differential measurements. For example, use AIN0 and AIN1.
2. Leave any unused analog inputs floating, or connect them to AVDD in order to minimize the input-pin leakage current.

ESD diodes protect the analog inputs. To keep these diodes from turning on, voltages on the input pins must not go below AGND by more than 100 mV, and likewise, must not exceed AVDD by more than 100 mV: −100 mV < (V$_{(AINx)}$) < AVDD + 100 mV.

Feature Description (continued)

9.3.2 Analog Input Buffer

To increase the input impedance presented by the ADS1257, enable the low-drift, chopper-stabilized buffer using the BUFEN bit in the STATUS register. As shown in Figure 24, the input impedance with the buffer enabled is modeled by a resistor. Table 5 lists the values of Zeff for the different data-rate settings. The input impedance scales inversely with the frequency of CLKIN. For example, if $f_{(CLKIN)}$ is reduced by half to 3.84 MHz, Zeff for a data-rate setting of 50 SPS (actual data rate of 25 SPS) doubles from 80 MΩ to 160 MΩ.s
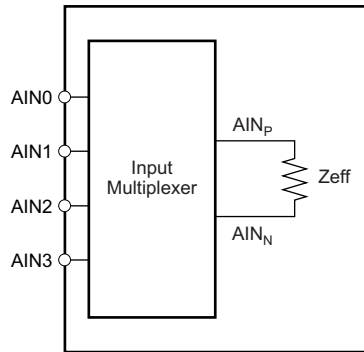
Figure 24. Effective Impedance with Buffer On

Table 5. Input Impedance with Buffer On[1]

DATA RATE (SPS)	Zeff (MΩ)
≤ 50	80
60	40
100	40
500	40
1,000	20
2,000	10
3,750	10
7,500	10
15,000	10
30,000	10

(1) $f_{(CLKIN)}$ = 7.68 MHz

NOTE

With the buffer enabled, the voltage on the analog inputs with respect to ground (listed in the *Recommended Operating Conditions* as *Absolute Input Voltage*) must remain between AGND and AVDD − 2.0 V. Exceeding this range reduces performance; in particular, the linearity of the ADS1257. This same voltage range, AGND to AVDD − 2.0 V, applies to the reference inputs when performing a self-gain calibration with the buffer enabled.

Product Folder Links: *ADS1257*

9.3.3 Programmable Gain Amplifier (PGA)

The ADS1257 is a very high resolution converter. To further complement converter performance, the low-noise PGA increases the ADC resolution when measuring smaller input signals. For the best resolution, set the PGA to the highest possible gain setting. The gain setting depends on the largest input signal to be measured. The ADS1257 full-scale input voltage equals $\pm 2 \cdot V_{REF}$ / Gain. Table 6 shows the full-scale input voltage for the different PGA gain settings for V_{REF} = 2.5 V. For example, if the largest signal to be measured is 1.0 V, the optimum PGA gain setting is 4 V/V, producing a full-scale input voltage of 4 V with no ADC overrange.

Table 6. Full-Scale Input Voltage vs PGA Setting

PGA GAIN SETTING	FULL-SCALE INPUT VOLTAGE V_{IN} [1] (V_{REF} = 2.5 V)
1	±5 V
2	±2.5 V
4	±1.25 V
8	±0.625 V
16	±312.5 mV
32	±156.25 mV
64	±78.125 mV

[1] The input voltage (V_{IN}) is the difference between the positive and negative input voltage. Make sure that neither input violates the absolute input voltage with respect to ground, as listed in the *Recommended Operating Conditions*.

The PGA is controlled by the ADCON register. Recalibrate the ADC after changing the PGA gain setting. The time required for self-calibration depends on the PGA gain setting; see the Calibration section for more details. The analog current and input impedance (when the buffer is disabled) vary as a function of the PGA gain setting.

Product Folder Links: *ADS1257*

9.3.4 Modulator Input Circuitry

The ADS1257 modulator measures the input signal using internal capacitors that are continuously charged and discharged. Figure 25 shows a simplified schematic of the ADS1257 input circuitry with the input buffer disabled. The on and off timing of the S1 and S2 switches are shown in Figure 26. The S1 switch closes during the input sampling phase. With S1 closed, C_{A1} charges to $V_{(AINP)}$, C_{A2} charges to $V_{(AINN)}$, and C_B charges to $(V_{(AINP)} - V_{(AINN)})$. For the discharge phase, S1 opens first and then S2 closes. C_{A1} and C_{A2} discharge to approximately AVDD / 2 and C_B discharges to 0 V. This two-phase sample and discharge cycle repeats with a period of t_{SAMPLE}. This time is a function of the PGA gain setting as shown in Table 7 along with the values of capacitors $C_{A1} = C_{A2} = C_A$ and C_B.
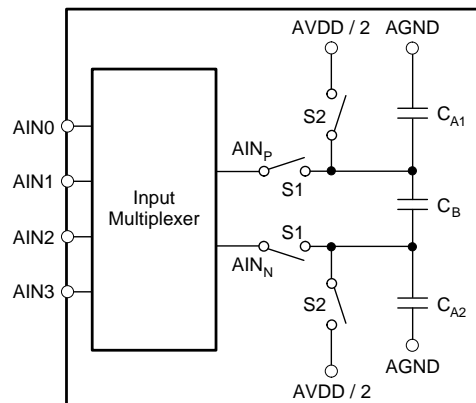
Figure 25. Simplified Input Structure with Buffer Off
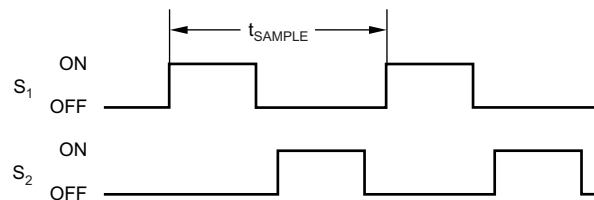
Figure 26. S1 and S2 Switch Timing for Figure 25

Table 7. Input Sampling Time (t_{SAMPLE}), C_A, and C_B vs PGA Gain

PGA GAIN SETTING	t_{SAMPLE}[1]	C_A	C_B
1	$f_{(CLKIN)}$ / 4 (521 ns)	2.1 pF	2.4 pF
2	$f_{(CLKIN)}$ / 4 (521 ns)	4.2 pF	4.9 pF
4	$f_{(CLKIN)}$ / 4 (521 ns)	8.3 pF	9.7 pF
8	$f_{(CLKIN)}$ / 4 (521 ns)	17 pF	19 pF
16	$f_{(CLKIN)}$ / 4 (521 ns)	33 pF	39 pF
32	$f_{(CLKIN)}$ / 2 (260 ns)	33 pF	39 pF
64	$f_{(CLKIN)}$ / 2 (260 ns)	33 pF	39 pF

(1) t_{SAMPLE} for $f_{(CLKIN)}$ = 7.68 MHz given in parenthesis.

Product Folder Links: *ADS1257*

The charging of the input capacitors draws a transient current from the sensor driving the ADS1257 inputs. The average value of this current is used to calculate an effective impedance Zeff, where $Zeff = V_{IN} / I_{AVERAGE}$. Figure 27 shows the input circuitry with the capacitors and switches of Figure 25 replaced by their effective impedances. These impedances scale inversely with the CLKIN frequency. For example, if $f_{(CLKIN)}$ is reduced by a factor of two, the impedances double. The impedance also changes with the PGA gain setting. Table 8 lists the effective impedances with the buffer off for $f_{(CLKIN)}$ = 7.68 MHz.

Figure 27. Analog Input Effective Impedances with Buffer Off

Table 8. Analog Input Impedances with Buffer Off[1]

PGA GAIN SETTING	Zeff$_A$ (kΩ)	Zeff$_B$ (kΩ)
1	260	220
2	130	110
4	65	55
8	33	28
16	16	14
32	8	7
64	8	7

(1) $f_{(CLKIN)}$ = 7.68 MHz.

9.3.5 Voltage Reference Inputs (REFP, REFN)

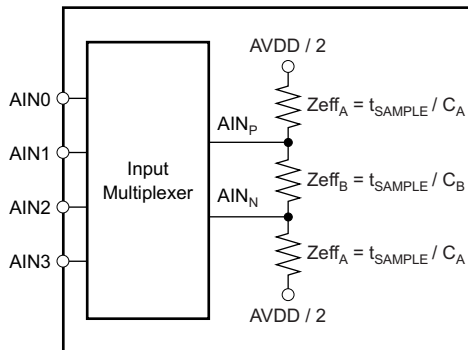The ADC requires a reference voltage for operation. The reference voltage for the ADS1257 is the differential voltage between REFP and REFN: $V_{REF} = V_{(REFP)} - V_{(REFN)}$. The reference inputs use a structure similar to that of the analog inputs with the circuitry on the reference inputs of Figure 28. The load presented by the switched capacitor is modeled with an effective impedance (Zeff) of 18.5 kΩ for $f_{(CLKIN)} = 7.68$ MHz. The temperature coefficient of the effective impedance of the voltage reference inputs is approximately 35 ppm/°C.
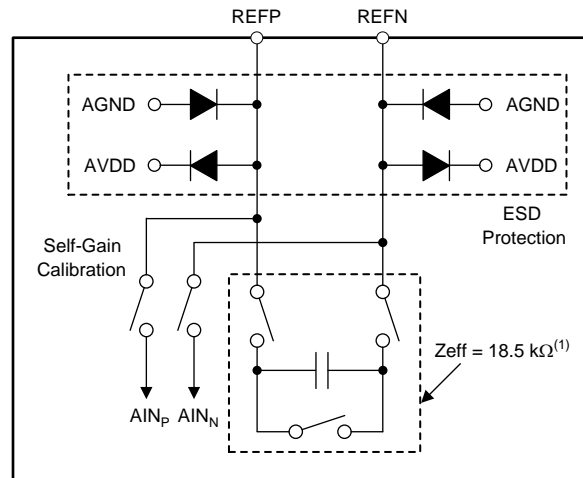
(1) $f_{(CLKIN)} = 7.68$ MHz

Figure 28. Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To keep these diodes from turning on, the voltages on the reference pins must not go below AGND by more than 100 mV, and must not exceed AVDD by 100 mV:

AGND − 100 mV < ($V_{(REFP)}$ or $V_{(REFN)}$) < AVDD + 100 mV

During self gain calibration, all the switches in the input multiplexer are opened, REFN is internally connected to AIN_N, and REFP is connected to AIN_P. The input buffer can be disabled or enabled during calibration. When the buffer is disabled, the reference pins drive the circuitry shown in Figure 25 during self gain calibration, resulting in increased loading. To prevent this additional loading from introducing gain errors, the circuitry driving the reference pins must have adequate drive capability. When the buffer is enabled, the loading on the reference pins is much less. However, the buffer limits the allowable voltage range on REFP and REFN during self- or self gain calibration because the reference pins must remain within the specified input range of the buffer in order to establish proper gain calibration.

A high-quality reference voltage capable of driving the switched capacitor load presented by the ADS1257 is essential for achieving the best performance. Noise and drift on the reference degrade overall system performance. Take special care with the circuitry generating the reference voltages and their layout when operating with low-noise settings (that is, with low data rates) in order to prevent the voltage reference from limiting performance.

See the *External Reference* section for more details.

9.3.6 Clock Input (CLKIN)

The master clock for the ADS1257 must be applied to the CLKIN pin. Keep the external clock signal clean and free of overshoot. Overshoot and glitches on the clock degrade overall performance. See the *Recommended Operating Conditions* section for the recommended master clock frequency range. Some of the timing requirements, as well as the output data rate, scale directly with the CLKIN frequency.

9.3.7 Clock Output (D0/CLKOUT)

Use the clock output pin (D0/CLKOUT) to clock another device, such as another ADS1257 or a microcontroller. This clock operates at frequencies of $f_{(CLKIN)}$, $f_{(CLKIN)}$ / 2, or $f_{(CLKIN)}$ / 4 and is configured by setting the CLK[1:0] bits in the ADCON register. If the output clock is enabled while driving an external load, the digital power consumption increases. Standby mode does not affect the clock output status. That is, if standby is enabled, the clock output continues to run during standby mode. If not needed, disable the clock output function by writing to the CLK bits in the ADCON register after power-up or reset.

9.3.8 General-Purpose Digital I/O (D0, D1)

The ADS1257 offers two pins dedicated for general-purpose digital I/Os. All of the digital I/O pins can be individually configured as either inputs or outputs through the IO register. The DIR bits of the IO register define whether each pin is an input or output, and the DIO bits control the status of the pins. Reading back the DIO bits shows the state of the digital I/O pins; that is, if configured as inputs or outputs by the DIR bits. When digital I/O pins are configured as inputs, the DIO bits are used to read the state of these pins. When configured as outputs, writing to the DIO bits sets the output value.

During standby and power-down modes, the GPIOs remain active. If configured as outputs, the GPIOs continue to drive the pins. If configured as inputs, the GPIOs must be driven (not left floating) to prevent excess power dissipation.

After power-up or reset, the D1 pin defaults to an input and the D0/CLKOUT pin defaults to the clock output. The CLK[1:0] bits that control the clock output on D0/CLKOUT are only reset after power-up or $\overline{\text{RESET}}$ pin toggle. If the digital I/O pins are not used, either leave them as inputs tied to ground, or configure them as outputs and leave them floating to avoid excess power dissipation.

9.3.9 Open- and Short-Circuit Sensor Detection

The sensor detect current sources (SDCS) provide a means to verify the integrity of the external sensor connected to the ADS1257. When enabled, the SDCS supply a current (I_{SDC}) of approximately 0.5 µA, 2 µA, or 10 µA to the sensor through the input multiplexer. The SDCS bits in the ADCON register enable the SDCS and set the value of I_{SDC}.

When the SDCS are enabled, the ADS1257 automatically turns on the analog input buffer, regardless of the BUFEN bit setting, in order to prevent the input circuitry from loading the SDCS. AIN_P must stay below 3 V to be within the absolute input range of the buffer. To help meet this condition, a 3-V clamp starts sinking current from AIN_P to AGND if AIN_P exceeds 3 V. Note that this clamp is activated only when the SDCS are enabled.

Figure 29 shows a simplified diagram of the ADS1257 input structure with the external sensor modeled as resistance R_{SENS} between two input pins. When enabled, the SDCS source I_{SDC} to the input pin connected to AIN_P, and sink I_{SDC} from the input pin connected to AIN_N. The two 25-Ω series resistors, R_{MUX}, model the ADS1257 internal multiplexer switch on-resistances. The signal measured with the SDCS enabled equals the total IR drop: $I_{SDC} \times (2R_{MUX} + R_{SENS})$. When the sensor is a direct short (that is, $R_{SENS} = 0\ \Omega$), there is still a small signal measured by the ADS1257 when the SDCS are enabled: $I_{SDC} \cdot 2R_{MUX}$.
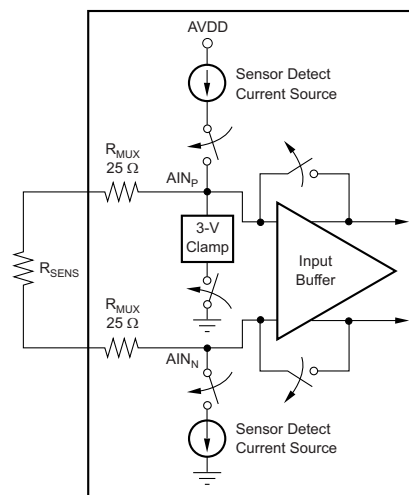
NOTE: Arrows indicate switch positions when the SDCS are enabled.

Figure 29. Sensor Detect Circuitry

9.3.10 Digital Filter

The programmable low-pass digital filter receives the modulator output and produces a high-resolution digital output. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, or filter less for higher data rate. The filter is comprised of two sections, a fixed filter followed by a programmable filter. Figure 30 shows the block diagram of the analog modulator and digital filter. Data are supplied to the filter from the analog modulator at a rate of $f_{(MOD)} = f_{(CLKIN)}$ / 4. The fixed filter is a fifth-order sinc filter with a decimation value of 64 that outputs data at a rate of $f_{(CLKIN)}$ / 256. The second stage of the filter is a programmable averager (first-order sinc filter) with the number of averages set by the DRATE register. The data rate is a function of the number of averages (Num_Ave) and is given by Equation 2.

$$\text{Data Rate} = \left(\frac{f_{(CLKIN)}}{256} \right)\left(\frac{1}{\text{Num\_Ave}} \right)$$

(2)
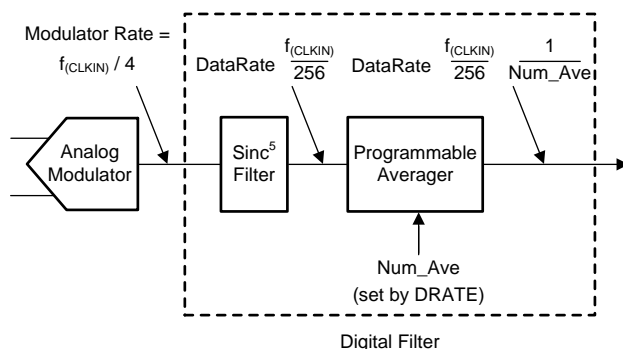
Figure 30. Block Diagram of the Analog Modulator and Digital Filter

Table 9 shows the averaging and corresponding data rate for each of the 16 valid DRATE register settings when $f_{(CLKIN)}$ = 7.68 MHz. The data rate scales directly with the CLKIN frequency. For example, reducing $f_{(CLKIN)}$ from 7.68 MHz to 3.84 MHz reduces the data rate for DR[7:0] = 1111 0000 from 30,000 SPS to 15,000 SPS.

**Table 9. Number of Averages and Data Rate for
Each Valid DRATE Register Setting**

DRATE[7:0]	NUMBER OF AVERAGES FOR PROGRAMMABLE FILTER (Num_Ave)	DATA RATE[1] (SPS)
0000 0011 (03h)	12,000	2.5
0001 0011 (13h)	6000	5
0010 0011 (23h)	3000	10
0011 0011 (33h)	2000	15
0100 0011 (43h)	1200	25
0101 0011 (53h)	1000	30
0110 0011 (63h)	600	50
0111 0010 (72h)	500	60
1000 0010 (82h)	300	100
1001 0010 (92h)	60	500
1010 0001 (A1h)	30	1000
1011 0000 (B0h)	15	2000
1100 0000 (C0h)	8	3750
1101 0000 (D0h)	4	7500
1110 0000 (E0h)	2	15,000
1111 0000 (F0h)	1 (averager bypassed)	30,000

(1)   For $f_{(CLKIN)}$ = 7.68 MHz.

Product Folder Links: *ADS1257*

9.3.10.1 Frequency Response

The low-pass digital filter sets the overall frequency response for the ADS1257. The filter response is the product of the responses of the fixed and programmable filter sections, and is given by Equation 3:

$$\left|H(f)\right| = \left|H_{\sin c}5(f)\right| \times \left|H_{\text{Averager}}(f)\right| = \left|\frac{\sin\left(\dfrac{256\pi \times f}{f_{(\text{CLKIN})}}\right)}{64 \times \sin\left(\dfrac{4\pi \times f}{f_{(\text{CLKIN})}}\right)}\right|^5 \times \left|\frac{\sin\left(\dfrac{256\pi \times \text{Num\_Ave} \times f}{f_{(\text{CLKIN})}}\right)}{\text{Num\_Ave} \times \sin\left(\dfrac{256\pi \times f}{f_{(\text{CLKIN})}}\right)}\right| \tag{3}$$

The digital filter attenuates noise on the modulator output, including noise from within the ADS1257 and external noise present on the ADS1257 input signal. Adjusting the filtering by changing the number of averages used in the programmable filter changes the filter bandwidth. With a higher number of averages, bandwidth is reduced, and more noise is attenuated.

The low-pass filter has notches (or zeros) at the data output rate and multiples thereof. At these frequencies, the filter has zero gain. This feature is useful when trying to reject a particular interference signal. For example, to reduce 60-Hz (and harmonic) noise coupling, set the data rate equal to 2.5 SPS, 5 SPS, 10 SPS, 15 SPS, 30 SPS, or 60 SPS. To help illustrate the filter characteristics, Figure 31 and Figure 32 show the responses at the data-rate extremes of 30 kSPS and 2.5 SPS, respectively.

**Figure 31. Frequency Response for
Data Rate = 30 kSPS**

**Figure 32. Frequency Response for
Data Rate = 2.5 SPS**
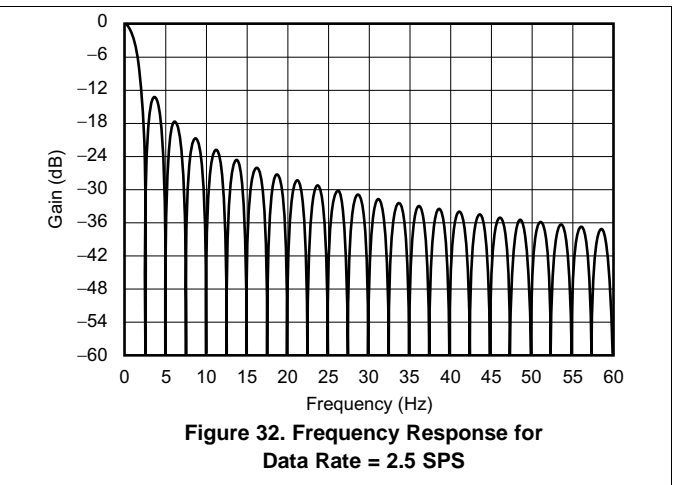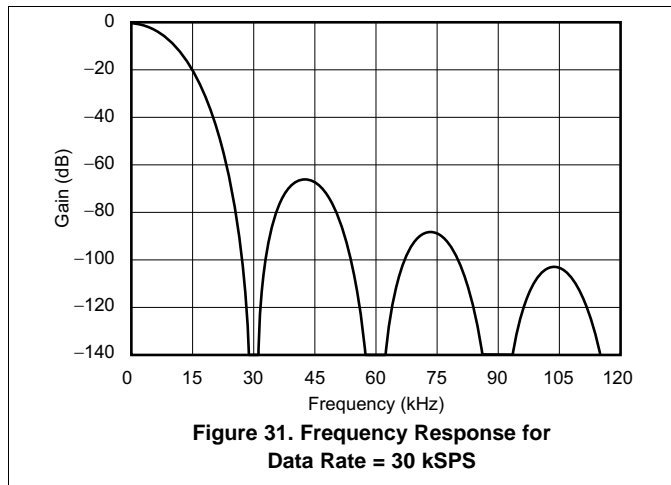
Table 10 summarizes the first-notch frequency and −3-dB bandwidth for the different data-rate settings.

**Table 10. First Notch Frequency and
-3-dB Filter Bandwidth[1]**

DATA RATE (SPS)	FIRST NOTCH (Hz)	-3 dB BANDWIDTH (Hz)
2.5	2.5	1.1
5	5	2.21
10	10	4.42
15	15	6.63
25	25	11.1
30	30	13.3
50	50	22.1
60	60	26.5
100	100	44.2
500	500	221
1000	1000	441
2000	2000	878
3750	3750	1615
7500	7500	3003
15,000	15,000	4807
30,000	30,000	6106

(1) $f_{(CLKIN)}$ = 7.68 MHz.

The digital filter low-pass characteristic repeats at multiples of the modulator rate of $f_{(MOD)} = f_{(CLKIN)}$ / 4. Figure 33 and Figure 34 show the responses plotted out to 7.68 MHz at the data-rate extremes of 30 kSPS and 2.5 SPS. Notice how the responses near dc, 1.92 MHz, 3.84 MHz, 5.76 MHz, and 7.68 MHz are the same. The digital filter attenuates high-frequency noise on the ADS1257 inputs, except for frequencies where the filter response repeats. External filtering is required to remove high-frequency input noise near these pass-band regions. See the *Analog Input Filtering* section for more details.

**Figure 33. Frequency Response Out to 7.68 MHz
for Data Rate = 30 kSPS**

**Figure 34. Frequency Response Out to 7.68 MHz
for Data Rate = 2.5 SPS**
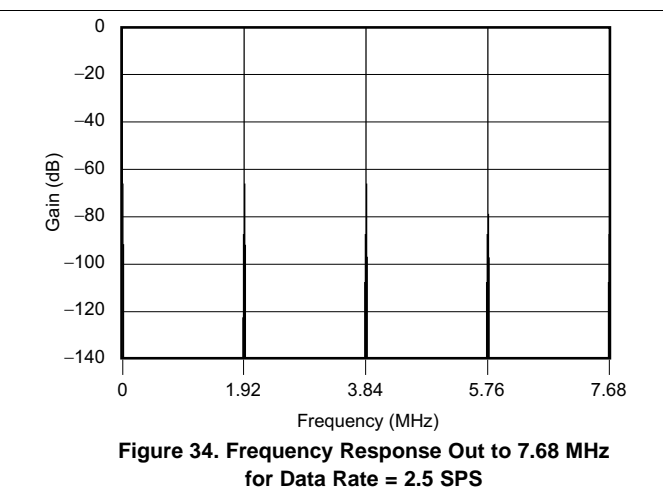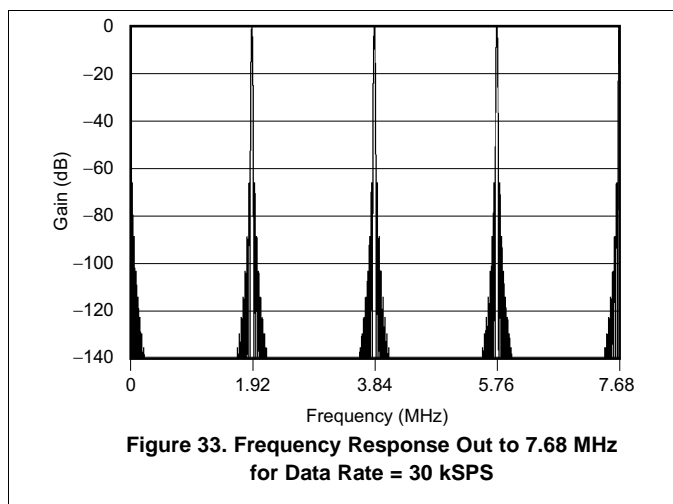
9.3.10.2 50-Hz and 60-Hz, Line Cycle Rejection

As a result of the proximity of the signal wires to industrial motors and conductors in some applications, coupling of 50-Hz and 60-Hz power-line frequencies can occur. Coupled noise can interfere with the signal voltage leading to inaccurate or unstable conversions. The digital filter rejects power-line interference for data rates of 60 SPS and less. Program the filter to tradeoff data rate and conversion latency versus the desired level of line-cycle rejection. Table 11 summarizes the 50-Hz and 60-Hz line-cycle rejection based on 2% tolerance of power-line frequency to ADC clock frequency.

Table 11. Minimum 50-Hz and 60-Hz, Line-Cycle Rejection

DATA RATE (SPS)	MINIMUM DIGITAL-FILTER MAGNITUDE (dB)	
	50 Hz ±2%	60 Hz ±2%
2.5	–36.2	–37.4
5	–34.4	–34.6
10	–33.9	–34.0
15	—	–33.9
25	–33.8	—
30	—	–33.8
50	–33.8	—
60	—	–33.8

9.3.10.3 Settling Time

The ADS1257 features a digital filter optimized for fast settling. The *Conversion Control and Synchronization* section describes the settling time of the ADS1257 for various modes of operation.

9.4 Device Functional Modes

9.4.1 Power-Up

All configuration registers are initialized to default states at power-up. Self-calibration is then performed automatically. For best performance, issue an additional self-calibration with the SELFCAL command or reset the device after the power supplies and voltage reference have settled to their final values.

NOTE

A reset is required after power-up to avoid invalid device operation.

9.4.2 Reset

Three methods are used to reset the ADS1257: the $\overline{\text{RESET}}$ pin, the RESET command, and a special SCLK reset pattern.

1. Take the $\overline{\text{RESET}}$ pin low to force a reset. Follow the minimum pulse-width timing specification (t_{16}) before taking the $\overline{\text{RESET}}$ pin high again (see Figure 2).
2. Issue the RESET command byte to force a reset (see the RESET section). The RESET command takes effect after all eight bits are shifted into DIN. Afterwards, the reset automatically releases.
3. Reset The ADS1257 using a special pattern on SCLK (see Figure 3). Reset occurs on the falling edge of the last SCLK edge in the pattern. $\overline{\text{CS}}$ must be low to perform the SCLK reset pattern. After performing the operation, the reset automatically releases.

After the device resets, the configuration registers are initialized to their default state, except for the CLK[1:0] bits in the ADCON register that control the D0/CLKOUT pin. The CLK[1:0] bits are only initialized to their default state when reset is performed using the $\overline{\text{RESET}}$ pin. Reset also exits from the read-data continuous mode.

After a reset, the device self-calibrates, regardless of the reset method or the state of the ACAL bit before the reset.

9.4.3 Standby Mode

Standby mode shuts down all of the analog circuitry and most of the digital features. To enter standby mode, issue the STANDBY command. To exit standby mode, issue the WAKEUP command. $\overline{\text{DRDY}}$ stays high after exiting standby mode until valid data are ready.

Use standby mode to perform single-shot conversions; see the *Settling Time Using Single-Shot Mode* section for more information.

If configured as a clock output, the clock signal on the D0/CLKOUT pin continues to run during standby mode.

9.4.4 Power-Down Mode

Hold the $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ pin low for 20 $\overline{\text{DRDY}}$ cycles to activate power-down mode. During power-down mode, all circuitry is disabled including the clock output.

To exit power-down mode, take the $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ pin high. After exiting from power-down mode, $8192 \cdot t_{(\text{CLKIN})}$ cycles are required before conversions begin.

Device Functional Modes (continued)

9.4.5 Conversion Control and Synchronization

Device synchronization is available to control the beginning of the analog-to-digital conversion with an external event, and also to improve settling time after a multiplexer change. Two methods are provided to perform synchronization, the SYNC/PWDN pin or the SYNC command:

- Method 1: Take the $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ pin low and then high, in accordance with timing specifications t_{16} and t_{16B}. Synchronization occurs when $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ is taken high. No communication is possible on the serial interface while $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ is low. If the $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ pin is held low for 20 $\overline{\text{DRDY}}$ periods, the ADS1257 enters power-down mode.
- Method 2: First, issue the SYNC command. The SYNC command stops the operation of the ADS1257. When ready to synchronize, issue the WAKEUP command. Synchronization occurs on the first rising edge of the master clock after the first SCLK used to shift in the WAKEUP command.

After a synchronization operation, either with the $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ pin or the SYNC command, $\overline{\text{DRDY}}$ stays high until valid data are ready.

The settling time (that is, the time required for a step change on the analog inputs to propagate through the filter) for the different data rates is shown in Table 12 and Figure 35. The following sections highlight the single-cycle settling ability of the filter, and show various ways to control the conversion process.

Table 12. Settling Time Versus Data Rate [1][2]

DATA RATE (SPS)	SETTLING TIME (t_{18}) (ms)
2.5	400.18
5	200.18
10	100.18
15	66.84
25	40.18
30	33.51
50	20.18
60	16.84
100	10.18
500	2.18
1000	1.18
2000	0.68
3750	0.44
7500	0.31
15,000	0.25
30,000	0.21

(1) $f_{(CLKIN)}$ = 7.68 MHz.
(2) Single-shot mode requires an additional delay of 256 · $t_{(CLKIN)}$ to power up the device from standby mode.

9.4.5.1 Settling Time Using Synchronization

The $\overline{SYNC}/\overline{PWDN}$ pin and SYNC command allow direct control of conversion timing. Issue a SYNC command or toggle the $\overline{SYNC}/\overline{PWDN}$ pin after changing the analog inputs to restart conversions (see the *Conversion Control and Synchronization* section for more information). The conversion begins when $\overline{SYNC}/\overline{PWDN}$ is taken high, thus stopping the current conversion, and restarting the digital filter. As soon as $\overline{SYNC}/\overline{PWDN}$ goes low, the $\overline{DRDY}$ output goes high and remains high during the conversion. $\overline{DRDY}$ goes low after the settling time (t_{18}, listed for each data rate in Table 12), indicating that data are available. There is no need to ignore or discard data after synchronization. Figure 35 shows the data retrieval sequence following synchronization.
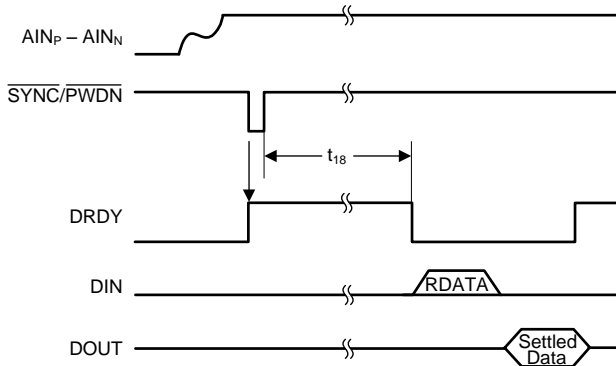
Figure 35. Data Retrieval After Synchronization

9.4.5.2 Settling Time Using Single-Shot Mode

To reduce power consumption in the ADS1257, perform single-shot conversions using the STANDBY command. The sequence for the STANDBY command is shown in Figure 36. Issue the WAKEUP command from standby mode to begin a single-shot conversion. When using single-shot mode, an additional delay is required for the modulator to power up and settle. This delay may require up to 64 modulator clocks ($64 \cdot 4 \cdot t_{(CKLIN)}$), or 33.3 µs for a 7.68-MHz master clock. Following the settling time ($t_{18} + 256 \cdot t_{(CLKIN)}$), $\overline{DRDY}$ goes low, indicating that the conversion is complete and data can be read using the RDATA command. The ADS1257 settles in a single cycle; there is no need to ignore or discard data. Following the data read cycle, issue another STANDBY command to reduce power consumption. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

Figure 36. Single-shot Conversions Using the STANDBY Command

9.4.5.3 Settling Time Using the Input Multiplexer

The most efficient way to cycle through the inputs is to change the multiplexer setting immediately after $\overline{\text{DRDY}}$ goes low. Changing the multiplexer before reading the data allows the ADS1257 to start sampling the new input channel sooner. Figure 37 demonstrates efficient input cycling. There is no need to ignore or discard data w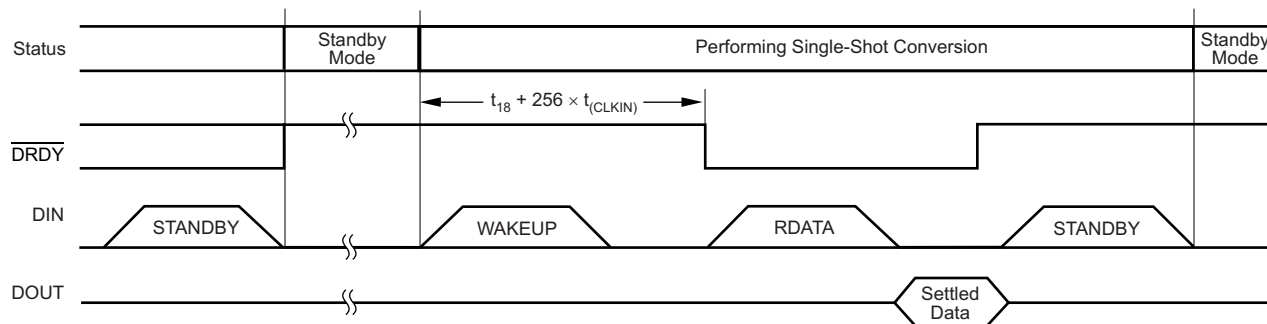hile cycling through the channels of the input multiplexer because the ADS1257 data are fully settled when $\overline{\text{DRDY}}$ goes low.
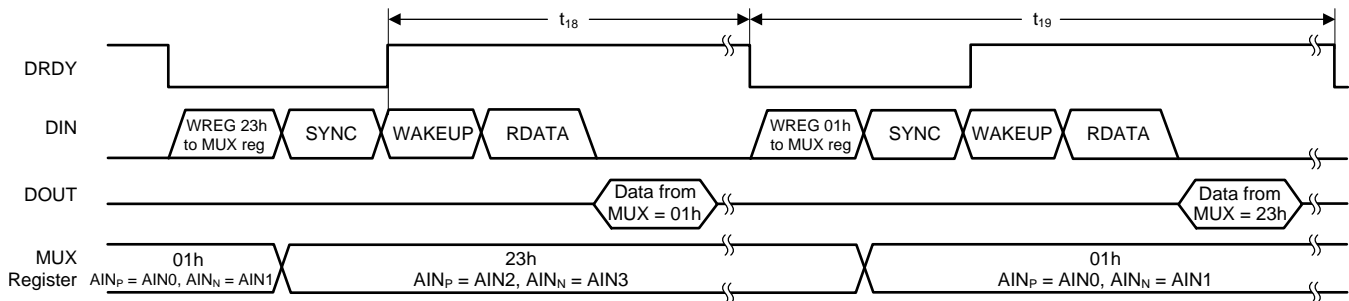
Figure 37. Cycling the ADS1257 Input Multiplexer

Step 1: When $\overline{\text{DRDY}}$ goes low (indicating that data are ready for retrieval), update the MUX register using the WREG command. For example, setting MUX to 23h selects AIN_P = AIN2, AIN_N = AIN3.

Step 2: Restart the conversion process by issuing a SYNC command followed by a WAKEUP command. Follow timing specification t_{11} between commands.

Step 3: Read the data from the previous conversion using the RDATA command. Repeat this process when $\overline{\text{DRDY}}$ goes low.

Table 13 gives the effective overall throughput (1 / t_{19}) when cycling the input multiplexer. The values for throughput (1 / t_{19}) assume the multiplexer is changed with a 3-byte WREG command and $f_{(SCLK)}$ = $f_{(CLKIN)}$ / 4.

Table 13. Multiplexer Cycling Throughput[1]

DATA RATE (SPS)	CYCLING THROUGHPUT (1 / t_{19}) (Hz)
2.5	2.5
5	5
10	10
15	15
25	25
30	30
50	50
60	59
100	98
500	456
1000	837
2000	1438
3750	2165
7500	3043
15,000	3817
30,000	4374

(1)　$f_{(CLKIN)}$ = 7.68 MHz.

9.4.5.4 Settling Time while Continuously Converting

After a synchronization, input multiplexer change, or wakeup from standby mode, the ADS1257 continuously converts the analog input. The conversions coincide with the falling edge of $\overline{DRDY}$. While continuously converting, the settling time is given by a number of $\overline{DRDY}$ periods, as shown in Table 14. The $\overline{DRDY}$ period equals the inverse of the selected data rate.

Table 14. Data Settling Delay Versus Data Rate

DATA RATE (SPS)	SETTLING TIME ($\overline{DRDY}$ PERIODS)
2.5	1
5	1
10	1
15	1
25	1
30	1
50	1
60	1
100	1
500	1
1000	1
2000	1
3750	1
7500	2
15,000	3
30,000	5

If there is a step change on the input signal while continuously converting, perform a synchronization operation to start a new conversion. Otherwise, the next data represent a combination of the previous and current input signal. Figure 38 shows an example of readback in this situation.
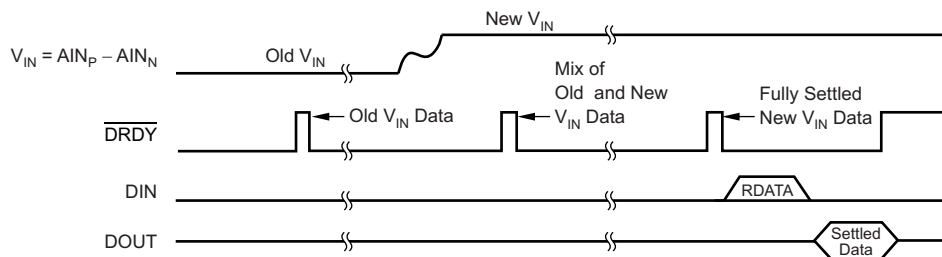

Figure 38. Step Change on V$_{IN}$ While Continuously Converting for Data Rates ≤ 3750 SPS

9.4.6 Calibration

Minimize offset and gain errors by using the ADS1257 internal calibration features. Figure 39 shows the calibration block diagram. Offset errors are corrected with the offset calibration registers (OFC2, OFC1, and OFC0). Full-scale errors are corrected with the full-scale calibration registers (FSC2, FSC1, and FSC2). Each of these registers are 8-bits with full read and write access. The OFC[2:0] registers and the FSC[2:0] registers both form 24-bit calibration words, referred to as OFC and FSC, respectively.
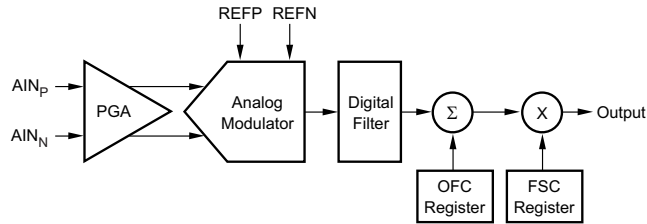

Figure 39. Calibration Block Diagram

The output of the ADS1257 after calibration is shown in Equation 4.

$$Output = \left(\frac{Gain \times V_{IN}}{2V_{REF}} - \frac{OFC}{\alpha} \right) FSC \times \beta$$

where

- α and β vary with data rate settings shown in Table 15 along with the ideal values (assumes perfect analog performance) for OFC and FSC.
- OFC is a binary twos complement number that can range from −8,388,608 to +8,388,607.
- FSC is unipolar ranging from 0 to 16,777,215. (4)

The ADS1257 supports both self-calibration and system calibration for any PGA gain setting using a set of five commands: SELFOCAL, SELFGCAL, SELFCAL, SYSOCAL, and SYSGCAL. Calibration can be performed at any time; however, in many applications, the ADS1257 drift performance is low enough that a single calibration is all that is needed. DRDY goes high when calibration begins and remains high until settled data are ready. There is no need to discard data after a calibration. For best performance, issue a self-calibration command after power-up when the reference voltage has stabilized. Additionally, performing a reset automatically performs self-calibration. Calibration must be performed whenever the data rate, buffer configuration, or PGA gain changes.

Table 15. Calibration Values for Different Data Rate Settings

DATA RATE (SPS)	α	β	IDEAL OFC	IDEAL FSC
2.5	5DC000h	2.7304	000000h	2EE14Ch
5	5DC000h	2.7304	000000h	2EE14Ch
10	5DC000h	2.7304	000000h	2EE14Ch
15	3E8000h	1.8202	000000h	4651F3h
25	4B0000h	2.1843	000000h	3A99A0h
30	3E8000h	1.8202	000000h	4651F3h
50	4B0000h	2.1843	000000h	3A99A0h
60	3E8000h	1.8202	000000h	4651F3h
100	4B0000h	2.1843	000000h	3A99A0h
500	3C0000h	1.7474	000000h	494008h
1000	3C0000h	1.7474	000000h	494008h
2000	3C0000h	1.7474	000000h	494008h
3750	400000h	1.8639	000000h	44AC08h
7500	400000h	1.8639	000000h	44AC08h
15,000	400000h	1.8639	000000h	44AC08h
30,000	400000h	1.8639	000000h	44AC08h

Product Folder Links: *ADS1257*

9.4.6.1 Self-Calibration

Self-calibration corrects internal offset and gain errors. During self-calibration, the appropriate calibration signals are applied internally to the analog inputs. There are three self-calibration commands: SELFOCAL, SELFGCAL, and SELFCAL. As with most of the ADS1257 timings, the calibration time scales directly with $f_{(CLKIN)}$.

9.4.6.1.1 SELFOCAL Command: Self-Offset Calibration

Issuing the SELFOCAL command performs a self-offset calibration. After the command is issued, the analog inputs AIN_P and AIN_N are disconnected from the signal source and connected to AVDD / 2. Table 16 lists the self-offset calibration time for the different data-rate settings. Self-offset calibration also updates the OFC register automatically.

Table 16. Self-Offset and System-Offset Calibration Timing[1]

DATA RATE (SPS)	SELF OFFSET CALIBRATION AND SYSTEM OFFSET CALIBRATION TIME
2.5	800.3 ms
5	400.3 ms
10	200.3 ms
15	133.7 ms
25	80.3 ms
30	67.0 ms
50	40.3 ms
60	33.7 ms
100	20.3 ms
500	4.3 ms
1000	2.3 ms
2000	1.3 ms
3750	853 µs
7500	587 µs
15,000	453 µs
30,000	387 µs

(1) For $f_{(CLKIN)}$ = 7.68 MHz.

9.4.6.1.2 SELFGCAL Command: Self-Gain Calibration

Issuing a SELFGCAL command performs a self-gain calibration. After issuing this command, the analog inputs AIN_P and AIN_N are disconnected from the signal source and AIN_P is connected internally to REFP, while AIN_N is connected to REFN. Self-gain calibration can be used with any PGA gain setting. The ADS1257 has low initial gain error and gain drift, even for the higher PGA gain settings, as shown in the *Typical Characteristics* section. Using the buffer limits the reference input voltage range during self-gain calibration because the reference is connected to the buffer inputs, and must be within the specified absolute input voltage range. When the voltage on REFP or REFN exceeds the buffer analog input range (AVDD – 2.0 V), the buffer must be turned off during self-gain calibration. Otherwise, use system gain calibration, or write the gain coefficients directly to the FSC register. Table 17 lists the self-gain calibration time for the different data-rate and PGA-gain settings. Self-gain calibration also updates the FSC register automatically.

Table 17. Self Gain Calibration Timing[1]

DATA RATE (SPS)	PGA GAIN SETTING				
	1	2	4	8	16, 32, 64
2.5	827.0 ms				
5	413.7 ms				
10	207.0 ms				
15	135.3 ms				
25	83.0 ms				
30	67.8 ms				
50	41.7 ms				
60	34.1 ms				
100	21.0 ms				
500	4.5 ms				
1000	2.4 ms				
2000	1.4 ms				
3750	884				
7500	617 µs	617 µs	617 µs	617 µs	751 µs
15,000	484 µs	484 µs	484 µs	551 µs	551 µs
30,000	417 µs	417 µs	451 µs	517 µs	651 µs

(1)   For $f_{(CLKIN)}$ = 7.68 MHz.

Product Folder Links: *ADS1257*

9.4.6.1.3 SELFCAL Command: Self-Offset and Self-Gain Calibration

Issuing the SELFCAL command first performs a self-offset calibration, and then a self-gain calibration. The analog inputs are disconnected from the signal source during self-calibration. When using the input buffer with self-calibration, observe the absolute voltage range of the reference inputs. Table 18 lists the self-calibration time for the different data-rate settings. Self-calibration also updates both the OFC and FSC registers automatically.

Table 18. Self-Calibration Timing[1]

DATA RATE (SPS)	PGA GAIN SETTING				
	1	2	4	8	16, 32, 64
2.5	1227.2 ms				
5	613.8 ms				
10	307.2 ms				
15	202.1 ms				
25	123.2 ms				
30	101.3 ms				
50	61.8 ms				
60	50.9 ms				
100	31.2 ms				
500	6.6 ms				
1000	3.6 ms				
2000	2.0 ms				
3750	1.3 ms				
7500	896 µs	896 µs	896 µs	896 µs	1029 µs
15,000	696 µs	696 µs	696 µs	762 µs	896 µs
30,000	596 µs	596 µs	692 µs	696 µs	892 µs

(1)   For $f_{(CLKIN)}$ = 7.68 MHz.

Product Folder Links: *ADS1257*

9.4.6.2 System Calibration

System calibration corrects both internal and external offset and gain errors using the SYSOCAL and SYSGCAL commands. During system calibration, apply the appropriate calibration signals directly to the inputs.

9.4.6.2.1 SYSOCAL Command: System-Offset Calibration

The SYSOCAL command performs a system-offset calibration. A zero-input differential signal must be supplied. The ADS1257 computes a value that nullifies the offset in the system, and then updates the OFC register.Table 16 shows the time required for system offset calibration for the different data-rate settings. This timing is the same as for the self-offset calibration.

9.4.6.2.2 SYSGCAL Command: System-Gain Calibration

The SYSGCAL command performs a system-gain calibration. A near full-scale input signal to the ADS1257 must be supplied. The ADS1257 computes a value to nullify the gain error in the system, and then automatically updates the FSC register. System-gain calibration corrects inputs that are greater than or equal to 80% of the full-scale input voltage. Do not exceed the full-scale input voltage when using system-gain calibration.

To calibrate with a signal less than full-scale (for example 95% full-scale), follow these steps:
1. Apply a *near* full-scale input signal and configure the registers settings for the appropriate mux inputs, data rate, PGA gain, and buffer state.
2. Perform system-gain calibration with the SYSGCAL command and wait for $\overline{DRDY}$ to go low.
3. Read back the calculated FSC value (24-bit word).
4. Multiply the FSC value by the ratio of the calibration signal to full-scale voltage (for example, 0.95 for an calibration signal of 95% full-scale).
5. Write the result of step 4 into the FSC[2:0] registers.

Table 19 shows the system gain calibration time for the different data-rate settings.

Table 19. System-Gain Calibration Timing[1]

DATA RATE (SPS)	SYSTEM GAIN CALIBRATION TIME
2.5	800.4 ms
5	400.4 ms
10	200.4 ms
15	133.7 ms
25	80.4 ms
30	67.0 ms
50	40.4 ms
60	33.7 ms
100	20.4 ms
500	4.4 ms
1000	2.4 ms
2000	1.4 ms
3750	884 µs
7500	617 µs
15,000	484 µs
30,000	417 µs

(1) For $f_{(CLKIN)}$ = 7.68 MHz.

9.4.6.3 Auto-Calibration

Enable auto-calibration (ACAL bit in STATUS register) in order for the ADS1257 to automatically initiate a self-calibration at the completion of a write command (WREG) that changes the data rate, PGA gain setting, or buffer state.

9.5 Programming

9.5.1 Serial Interface

The SPI-compatible serial interface consists of four signals ($\overline{CS}$, SCLK, DIN, and DOUT), and is used to read conversion data, read and write register data, and send ADC control commands. The programmable functions are controlled using a set of configuration registers. Data are written to and read from these registers through the serial interface. See the *Serial Interface Timing Requirements* section and Figure 1 for additional details on interfacing with the ADS1257.

9.5.1.1 Chip Select ($\overline{CS}$)

The chip select ($\overline{CS}$) input allows individual selection of a ADS1257 device when multiple devices share the same serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset and DOUT enters a high-impedance state. $\overline{CS}$ can be permanently tied to DGND if not used.

9.5.1.2 Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input, and is used to clock data on the DIN and DOUT pins into and out of (respectively) the ADS1257. Even though the input has hysteresis, keep the SCLK signal as clean as possible to prevent glitches from accidentally shifting data. If SCLK is held low for $32 \cdot \overline{DRDY}$ periods, the serial interface resets and the next SCLK pulse starts a new communication cycle. Use this timeout feature to recover communication when a serial interface transmission is interrupted. Apply a special pattern on SCLK to reset the ADC; see the *RESET* section for more details on this procedure. When the serial interface is idle, hold SCLK low.

9.5.1.3 Data Input (DIN) and Data Output (DOUT)

Use the data input pin (DIN) along with SCLK to send data to the ADS1257. Use the data output pin (DOUT) along with SCLK to read data from the ADS1257. Data on DIN are shifted into the device on the falling edge of SCLK, while data are shifted out on DOUT on the rising edge of SCLK. DOUT is high impedance when not in use in order to allow DIN and DOUT to be connected together, and then driven by a bidirectional driver. *Do not* issue the RDATAC command while DIN and DOUT are connected together.

9.5.1.4 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ output is a status signal that indicates when a conversion has completed and new data are available to read. $\overline{DRDY}$ goes low when new conversion data are available, and returns high after all 24 bits are read back using the read data (RDATA) or read data continuous (RDATAC) command. If data are not retrieved, $\overline{DRDY}$ returns high while new conversion data are updated, as shown in Figure 40 (see the *DRDY Update Timing Characteristics* section for more information). *Do not* retrieve data while data are updating; reading data during this period results in invalid data.
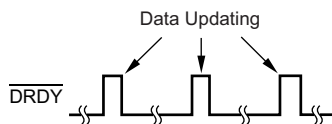
Figure 40. $\overline{DRDY}$ With No Data Retreival

After changing the PGA gain, data rate, buffer setting, sensor-detect current-source setting, or writing to the OFC or FSC registers, perform a synchronization operation to restart conversions and force $\overline{DRDY}$ high. $\overline{DRDY}$ stays high until valid data are ready. If auto-calibration is enabled (by setting the ACAL bit in the STATUS register), $\overline{DRDY}$ goes low after self-calibration is complete and new data are valid. Exiting standby or power-down mode, or performing a reset or SYNC command also forces $\overline{DRDY}$ high. $\overline{DRDY}$ goes low again when valid data are ready.

Programming (continued)

9.5.2 Data Format

The ADS1257 outputs 24 bits of data in binary twos complement format. The least significant bit (LSB) has a value of $(4 \cdot V_{REF} / gain) / 2^{24}$ V. A positive full-scale input produces an output code of 7FFFFFh, and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 20 summarizes the ideal output codes for different input signals.

Table 20. Ideal Output Code Versus Input Signal

INPUT SIGNAL $V_{IN} = V_{(AINP)} - V_{(AINN)}$	IDEAL OUTPUT CODE[1]
$+(2 \cdot V_{REF} / Gain) \cdot (2^{23} - 1) / 2^{23}$	7FFFFFh
$+(2 \cdot V_{REF} / Gain) / 2^{23}$	000001h
0	000000h
$-(2 \cdot V_{REF} / Gain) / 2^{23}$	FFFFFFh
$\leq -(2 \cdot V_{REF} / Gain)$	800000h

(1) Excludes effects of noise, INL, offset, and gain errors.

9.5.3 Command Definitions

The commands summarized in Table 21 control the operation of the ADS1257. All of the commands are stand-alone except for read data (RDATA) and the the register reads and writes (RREG, WREG) which require a second command byte plus data. Additional command and data bytes may be shifted in without delay after the first command byte. The ORDER bit in the STATUS register sets the order of the bits within the output data. CS must stay low during the entire command sequence.

Table 21. Command Defintions[1]

COMMAND	DESCRIPTION	1ST COMMAND BYTE	2ND COMMAND BYTE
WAKEUP/NOP	Completes SYNC, exits standby mode, and clocks out data	0000 0000 (00h)	
RDATA	Read data	0000 0001 (01h)	
RDATAC	Read data continuous	0000 0011 (03h)	
SDATAC	Stop read data continuous	0000 1111 (0Fh)	
RREG	Read from REG *rrrr*	0001 *rrrr* (1xh)	0000 *nnnn*
WREG	Write to REG *rrrr*	0101 *rrrr* (5xh)	0000 *nnnn*
SELFCAL	Offset and gain self-calibration	1111 0000 (F0h)	
SELFOCAL	Offset self-calibration	1111 0001 (F1h)	
SELFGCAL	Gain self-calibration	1111 0010 (F2h)	
SYSOCAL	System offset calibration	1111 0011 (F3h)	
SYSGCAL	System gain calibration	1111 0100 (F4h)	
SYNC	Synchronize the analog-to-digital conversion	1111 1100 (FCh)	
STANDBY	Enter standby mode	1111 1101 (FDh)	
RESET	Reset to default values	1111 1110 (FEh)	
WAKEUP/NOP	Completes SYNC, exits standby mode, and clocks out data	1111 1111 (FFh)	

(1) *nnnn* = number of registers to be read or written − 1. For example, to read or write three registers, set *nnnn* = 0010 (02h).
    rrrr = starting register address for read or write commands.

9.5.3.1 *WAKEUP/NOP: Complete Synchronization or Exit Standby Mode*

The WAKEUP and NOP commands are issued by holding DIN high or low, while sending eight SCLKs. The WAKEUP command is used in conjunction with the SYNC and STANDBY commands, and the NOP command is used to clock out data.

9.5.3.2 RDATA: Read Data

Issue the RDATA command after $\overline{DRDY}$ goes low to read a single conversion result. After all 24 bits are shifted out on DOUT, $\overline{DRDY}$ goes high. It is not necessary to read back all 24 bits, but $\overline{DRDY}$ does not return high until new data are updated. See the *Serial Interface Timing Requirements* for the required delay between the end of the RDATA command and the beginning of data shift on DOUT: t_6.
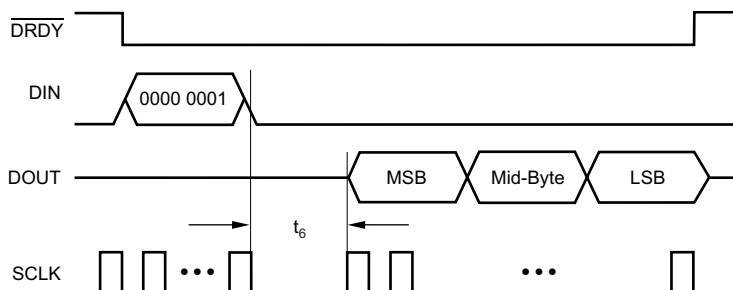

Figure 41. RDATA Command Sequence

9.5.3.3 RDATAC: Read Data Continuous

Issue the RDATAC command after $\overline{DRDY}$ goes low to enter the read-data-continuous mode. This mode enables the continuous output of new data on each $\overline{DRDY}$ without the need to issue subsequent read commands. After all 24 bits are read, $\overline{DRDY}$ goes high. It is not necessary to read back all 24 bits, but $\overline{DRDY}$ does not return high until new data are updated. This mode is terminated by the stop-read-data-continuous command (SDATAC). Terminate the read-data-continuous mode before reading and writing the device register settings. See the *Serial Interface Timing Requirements* section for the required t_6 delay between the end of the RDATAC command and the beginning of shifting data on DOUT.
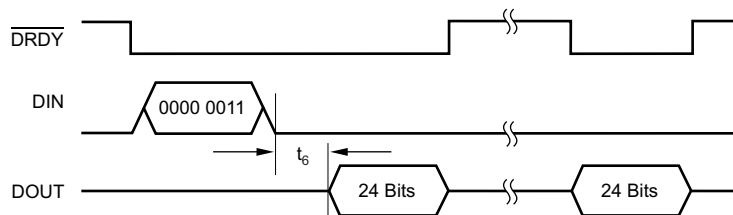
Figure 42. RDATAC Command Sequence

In read-data-continuous mode, shift out data by sending NOP commands. Three NOP commands are required to retrieve all 24 bits of data. The read data continuous mode terminates if input_data equals the SDATAC or RESET command in any of the three bytes on DIN.
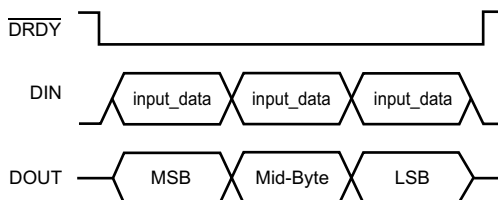
Figure 43. DIN and DOUT Command Sequence During Read Continuous Mode

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NOTE

Do not use read-data-continuous mode if DIN and DOUT are connected together, if $\overline{DRDY}$ is not used, or if reading data cannot be completed before the next $\overline{DRDY}$ falling edge.

Product Folder Links: *ADS1257*

9.5.3.4 SDATAC: Stop Read Data Continuous

The SDATAC command ends read-data-continuous mode and allows the device registers to be read or modified. The SDATAC command must be issued after DRDY goes low and completed before DRDY goes high.

DRDY

DIN   000 1111
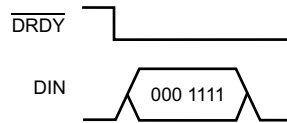
Figure 44. SDATAC Command Sequence

9.5.3.5 RREG: Read from Registers

Use the RREG command to output the data from up to 11 configuration registers starting at the register address specified as part of the command. The number of registers read is one plus the second byte of the command. If the count exceeds the remaining registers, the addresses wrap back to the beginning. Exit read-data-continuous mode (with the SDATAC command) before issuing a RREG command.

First command byte: 0001 *rrrr*, where *rrrr* is the address of the first register to read.

Second command byte: 0000 *nnnn*, where *nnnn* is the number of bytes to read – 1. See the *Serial Interface Timing Requirements* section for the required delay between the end of the RREG command and the beginning of shifting data on DOUT: t_6.

DIN   0001 0001   0000 0001

1st Command   2nd Command
Byte   Byte

t_6

DOUT   MUX   ADCON

Data   Data
Byte   Byte
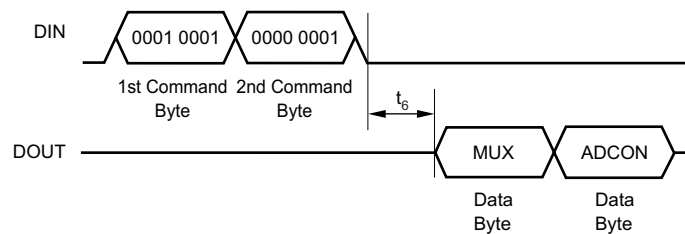
Figure 45. RREG Command Example: Read Two Registers Starting From Register 01h (MUX)

9.5.3.6 WREG: Write to Register

Use the WREG command to write to the configuration registers starting at the register address specified as part of the command. The number of registers that are written is one plus the value of the second byte in the command. If auto-calibration is enabled, writing to the PGA[2:0], DR [7:0] or BUFEN fields starts a self-calibration. Exit read-data-continuous mode (with the SDATAC command) before issuing a WREG command.

First command byte: 0101 *rrrr*, where *rrrr* is the address of the first register to be written.

Second command byte: 0000 *nnnn*, where *nnnn* is the number of bytes to be written – 1.

Data bytes: one or more data bytes to be written to the device registers.

DIN   0101 0011   0000 0001   DRATE Data   IO Data

1st Command   2nd Command   Data   Data
Byte   Byte   Byte   Byte

Figure 46. WREG Command Example: Write Two Registers Starting From 03h (DRATE)

Product Folder Links: *ADS1257*

9.5.3.7 SELFCAL: Self-Offset and Self-Gain Calibration

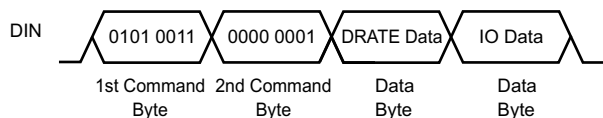This command performs both a self-offset and a self-gain calibration, as described in the *Self-Calibration* section. The offset calibration registers (OFC2, OFC1, and OFC0) and full-scale calibration registers (FSC2, FSC1, and FSC0) are updated after this operation. The SELFCAL command must be issued after $\overline{DRDY}$ goes low. $\overline{DRDY}$ goes high at the beginning of the calibration. Do not send any additional commands during calibration. $\overline{DRDY}$ goes low after the calibration completes and settled data are ready.

9.5.3.8 SELFOCAL: Self Offset Calibration

This command performs a self-offset calibration, as described in the *Self-Calibration* section. The offset calibration registers (OFC2, OFC1, and OFC0) are updated after this operation. The SELFOCAL command must be issued after $\overline{DRDY}$ goes low. $\overline{DRDY}$ goes high at the beginning of the calibration. Do not send any additional commands during calibration. $\overline{DRDY}$ goes low after the calibration completes and settled data are ready.

9.5.3.9 SELFGCAL: Self Gain Calibration

This command performs a self-gain calibration, as described in the *Self-Calibration* section. The full-scale calibration registers (FSC2, FSC1, and FSC0) are updated after this operation. The SELFGCAL command must be issued after $\overline{DRDY}$ goes low. $\overline{DRDY}$ goes high at the beginning of the calibration. Do not send any additional commands during calibration. $\overline{DRDY}$ goes low after the calibration completes and settled data are ready.

9.5.3.10 SYSOCAL: System Offset Calibration

This command performs a system-offset calibration, as described in the *System Calibration* section. The offset calibration registers (OFC2, OFC1, and OFC0) are updated after this operation. The SYSOCAL command must be issued after $\overline{DRDY}$ goes low. $\overline{DRDY}$ goes high at the beginning of the calibration. Do not send any additional commands during calibration. $\overline{DRDY}$ goes low after the calibration completes and settled data are ready.

9.5.3.11 SYSGCAL: System Gain Calibration

This command performs a system-gain calibration, as described in the *System Calibration* section. The full-scale calibration registers (FSC2, FSC1, and FSC0) are updated after this operation. The SYSGCAL command must be issued after $\overline{DRDY}$ goes low. $\overline{DRDY}$ goes high at the beginning of the calibration. Do not send any additional commands during calibration. $\overline{DRDY}$ goes low after the calibration completes and settled data are ready.

9.5.3.12 STANDBY: Standby Mode / Single-shot Mode

The STANDBY command puts the ADS1257 into a low-power standby mode. After issuing the STANDBY command, no more activity on SCLK may occur while $\overline{CS}$ is low, because SCLK activity interrupts standby mode. SCLK activity does not interrupt standby mode while $\overline{CS}$ is high. To exit standby mode, issue the WAKEUP command. This command can also be used to perform single conversions (see the *Settling Time Using Single-Shot Mode* section for more details). The STANDBY command must be issued after $\overline{DRDY}$ goes low.
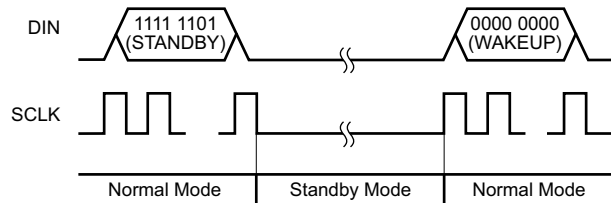
Figure 47. STANDBY Command Sequence

9.5.3.13 RESET: Reset Registers to Default Values

The RESET command returns all configuration registers to their default values, except for the CLK[1:0] bits in the ADCON register. This command also stops read-data-continuous mode. If operating in read-data-continuous mode, issue the RESET command after $\overline{DRDY}$ goes low.

9.5.3.14 SYNC: Synchronize the Analog-to-Digital Conversion

The SYNC command synchronizes the analog-to-digital conversion. To use the SYNC command, shift in the SYNC command followed by the WAKEUP command. Synchronization occurs on the first CLKIN rising edge after the first SCLK rising edge used to shift in the WAKEUP command. See the *Serial Interface Timing Requirements* section for the required delay between the end of the SYNC command and the beginning of the WAKEUP command: t_{11}.

Figure 48. SYNC Command Sequence

Product Folder Links: *ADS1257*

9.6 Register Map

The operation of the ADS1257 is controlled through a set of configuration registers. Collectively, the registers contain all the information needed to configure the part, such as data rate, multiplexer settings, PGA gain setting, calibration, and more, and are listed in Table 22.

Table 22. Register Map

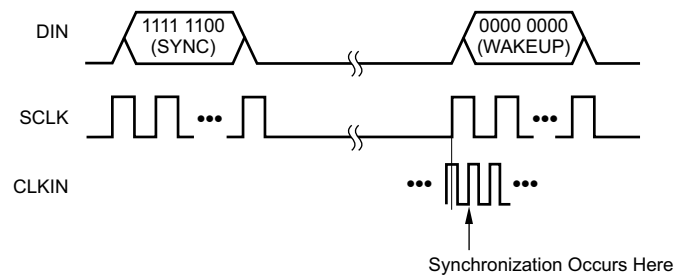| ADDRESS	REGISTER	RESET	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	STATUS	x1h	ID[3:0]				ORDER	ACAL	BUFEN	DRDY
01h	MUX	01h	0	0	PSEL[1:0]		0	0	NSEL[1:0]	
02h	ADCON	20h	0	CLK[1:0]		SDCS[1:0]		PGA[2:0]		
03h	DRATE	F0h	DR[7:0]							
04h	IO	E0h	1	1	DIR1	DIR0	0	0	DIO1	DIO0
05h	OFC0	xxh	OFC[7:0]							
06h	OFC1	xxh	OFC[15:8]							
07h	OFC2	xxh	OFC[23:16]							
08h	FSC0	xxh	FSC[7:0]							
09h	FSC1	xxh	FSC[15:8]							
0Ah	FSC2	xxh	FSC[23:16]							

9.6.1 STATUS: Status Register (address = 00h) [reset = x1h]

Figure 49. STATUS Register

7	6	5	4	3	2	1	0
ID[3:0]				ORDER	ACAL	BUFEN	DRDY
R-xh				R/W-0h	R/W-0h	R/W-0h	R-1h

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

Table 23. STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	ID[3:0]	R	xh	**Factory programmed identification bits** *NOTE: These bits can change without notice.*
3	ORDER	R/W	0h	**Data output bit order** Input data are always shifted in most significant bit first. Output data are always shifted out most significant byte first. The ORDER bit only controls the *bit order* of the output data within the byte. 0: Most significant bit first (default) 1: Least significant bit first
2	ACAL	R/W	0h	**Auto-calibration** When auto-calibration is enabled, self-calibration begins at the completion of the WREG command that changes the PGA[2:0], DR [7:0] or BUFEN values. 0: Auto-calibration disabled (default) 1: Auto-calibration enabled
1	BUFEN	R/W	0h	**Analog input buffer enable** Enables or disables the input buffer. The buffer is automatically enabled when the SDCS are enabled. 0: Buffer disabled (default) 1: Buffer enabled
0	DRDY	R	1h	**Data ready** This bit duplicates the state of the $\overline{DRDY}$ pin.

9.6.2 MUX : Input Multiplexer Control Register (address = 01h) [reset = 01h]

Figure 50. MUX Register

7	6	5	4	3	2	1	0
0	0	PSEL[1:0]		0	0	NSEL[1:0]	
R/W-0h	R/W-0h	R/W-0h		R/W-0h	R/W-0h	R/W-1h	

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

Table 24. MUX Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R/W	0h	**Reserved** Always write 0
6	0	R/W	0h	**Reserved** Always write 0
5:4	PSEL[1:0]	R/W	0h	**Positive input channel (AIN$_P$) selection** Selects the positive multiplexer input. 00: AIN0 (default) 01: AIN1 10: AIN2 11: AIN3
3	0	R/W	0h	**Reserved** Always write 0
2	0	R/W	0h	**Reserved** Always write 0
1:0	NSEL[1:0]	R/W	1h	**Negative input channel (AIN$_N$) selection** Selects the negative multiplexer input. 00: AIN0 01: AIN1 (default) 10: AIN2 11: AIN3

Product Folder Links: *ADS1257*

9.6.3 ADCON: ADC Control Register (address = 02h) [reset = 20h]

Figure 51. ADCON Register

7	6	5	4	3	2	1	0
0	CLK[1:0]		SDCS[1:0]		PGA[2:0]		
R-0h	R/W-1h		R/W-0h		R/W-0h		

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

Table 25. ADCON Register Field Descriptions

Bit	Field	Type	Reset	Description
7	0	R	0h	**Reserved** Always write 0
6:5	CLK[1:0]	R/W	1h	**D0/CLKOUT clock output rate setting** When CLKOUT is not used, turn CLKOUT off (00b). These bits can only be reset using the RESET pin. 00: Clock output off 01: $f_{(CLKOUT)} = f_{(CLKIN)}$ (default) 10: $f_{(CLKOUT)} = f_{(CLKIN)}$ / 2 11: $f_{(CLKOUT)} = f_{(CLKIN)}$ / 4
4:3	SDCS[1:0]	R/W	0h	**Sensor detect current source setting** The sensor detect current sources is activated to verify the integrity of an external sensor supplying a signal to the ADS1257. A shorted sensor produces a very small signal; an open-circuit sensor produces a very large signal. 00: Off (default) 01: 0.5 µA 10: 2 µA 11: 10 µA
2:0	PGA[2:0]	R/W	0h	**PGA gain setting** Selects the PGA gain 000: 1 V/V (default) 001: 2 V/V 010: 4 V/V 011: 8 V/V 100: 16 V/V 101: 32 V/V 110: 64 V/V 111: 64 V/V

9.6.4 DRATE: ADC Data Rate Register (address = 03h) [reset = F0h]

Figure 52. DRATE Register

7	6	5	4	3	2	1	0
			DR[7:0]				
			R/W-F0h				

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

Table 26. DRATE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DR[7:0]	R/W	F0h	**Data rate setting**[1]
				Selects the ADC data rate
				0000 0011 (03h): 2.5 SPS
				0001 0011 (13h): 5 SPS
				0010 0011 (23h): 10 SPS
				0011 0011 (33h): 15 SPS
				0100 0011 (43h): 25 SPS
				0101 0011 (53h): 30 SPS
				0110 0011 (63h): 50 SPS
				0111 0010 (72h): 60 SPS
				1000 0010 (82h): 100 SPS
				1001 0010 (92h): 500 SPS
				1010 0001 (A1h): 1,000 SPS
				1011 0000 (B0h): 2,000 SPS
				1100 0000 (C0h): 3,750 SPS
				1101 0000 (D0h): 7,500 SPS
				1110 0000 (E0h): 15,000 SPS
				1111 0000 (F0h): 30,000 SPS (default)

(1) For $f_{(CLKIN)}$ = 7.68 MHz. Data rates scale linearly with $f_{(CLKIN)}$.

9.6.5 IO: GPIO Control Register (address = 04h) [reset = E0h]

The states of these bits control the operation of the general-purpose digital I/O pins. The ADS1257 has two digital I/O pins: D0/CLKOUT and D1.

Figure 53. IO Register

7	6	5	4	3	2	1	0
1	1	DIR1	DIR0	0	0	DIO1	DIO0
R/W-1h	R/W-1h	R/W-1h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

Table 27. IO Register Field Descriptions

Bit	Field	Type	Reset	Description
7	1	R/W	1h	**Reserved** Always write 1
6	1	R/W	1h	**Reserved** Always write 1
5	DIR1	R/W	1h	**Digital I/O direction for D1 pin** Configures D1 as a GPIO input or GPIO output 0: D1 is an output 1: D1 is an input (default)
4	DIR0	R/W	0h	**Digital I/O direction for D0/CLKOUT pin** 0: D0/CLKOUT is a GPIO or clock output (default) 1: D0/CLKOUT is a GPIO input
3	0	R/W	0h	**Reserved** Always write 0
2	0	R/W	0h	**Reserved** Always write 0
1	DIO1	R/W	0h	**Status of digital I/O pin D1** Reading this bit shows the state of the D1 pin, regardless of the DIR1 bit configuration. When D1 is configured as an output by the DIR1 bit, writing to the this bit sets the output state of D1. When D1 is configured as an input by the DIR1 bit, writing to this bit has no effect.
0	DIO0	R/W	0h	**Status of digital I/O pin D0/CLKOUT** When D0/CLKOUT is configured as an input (DIR0 = 1), reading this bit shows the state of the D0/CLKOUT pin. When D0/CLKOUT is configured as an input (DIR0 = 1), writing to this bit has no effect. When D0/CLKOUT is configured as an output (DIR0 = 0) and CLKOUT is disabled (CLK[1:0] = 0), writing to this bit sets the output state of D0/CLKOUT. When D0/CLKOUT is configured as an output (DIR0 = 0) and CLKOUT is enabled (CLK[1:0] ≠ 0), writing to this bit has no effect.

9.6.6 OFC0: Offset Calibration Register 0 (address = 05h) [reset = depends on calibration results]

Figure 54. OFC0 Register

7	6	5	4	3	2	1	0
OFC[7:0]							
R/W-xxh							

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

9.6.7 OFC1: Offset Calibration Register 1 (address = 06h) [reset = depends on calibration results]

Figure 55. OFC1 Register

7	6	5	4	3	2	1	0
OFC[15:8]							
R/W-xxh							

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

9.6.8 OFC2: Offset Calibration Register 2 (address = 07h) [reset = depends on calibration results]

Figure 56. OFC2 Register

7	6	5	4	3	2	1	0
OFC[23:16]							
R/W-xxh							

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

9.6.9 FSC0: Full-Scale Calibration Register 0 (address = 08h) [reset = depends on calibration results]

Figure 57. FSC0 Register

7	6	5	4	3	2	1	0
FSC[7:0]							
R/W-xxh							

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

9.6.10 FSC1: Full-Scale Calibration Register 1 (address = 09h) [reset = depends on calibration results]

Figure 58. FSC1 Register

7	6	5	4	3	2	1	0
FSC[15:8]							
R/W-xxh							

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

9.6.11 FSC2: Full-Scale Calibration Register 2 (address = 0Ah) [reset = depends on calibration results]

Figure 59. FSC2 Register

7	6	5	4	3	2	1	0
FSC[23:16]							
R/W-xxh							

LEGEND: R/W = Read/Write; R = Read only; x = Variable; -n = value after reset

Product Folder Links: *ADS1257*

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The ADS1257 is a precision, 24-bit, ΔΣ ADC. Optimal performance is achieved with the ADS1257 by careful attention to the design of supporting circuitry and the printed circuit board (PCB) layout, as discussed in the following sections.

10.1.1 Basic Connections

Figure 60 shows the principle connections for the ADS1257.
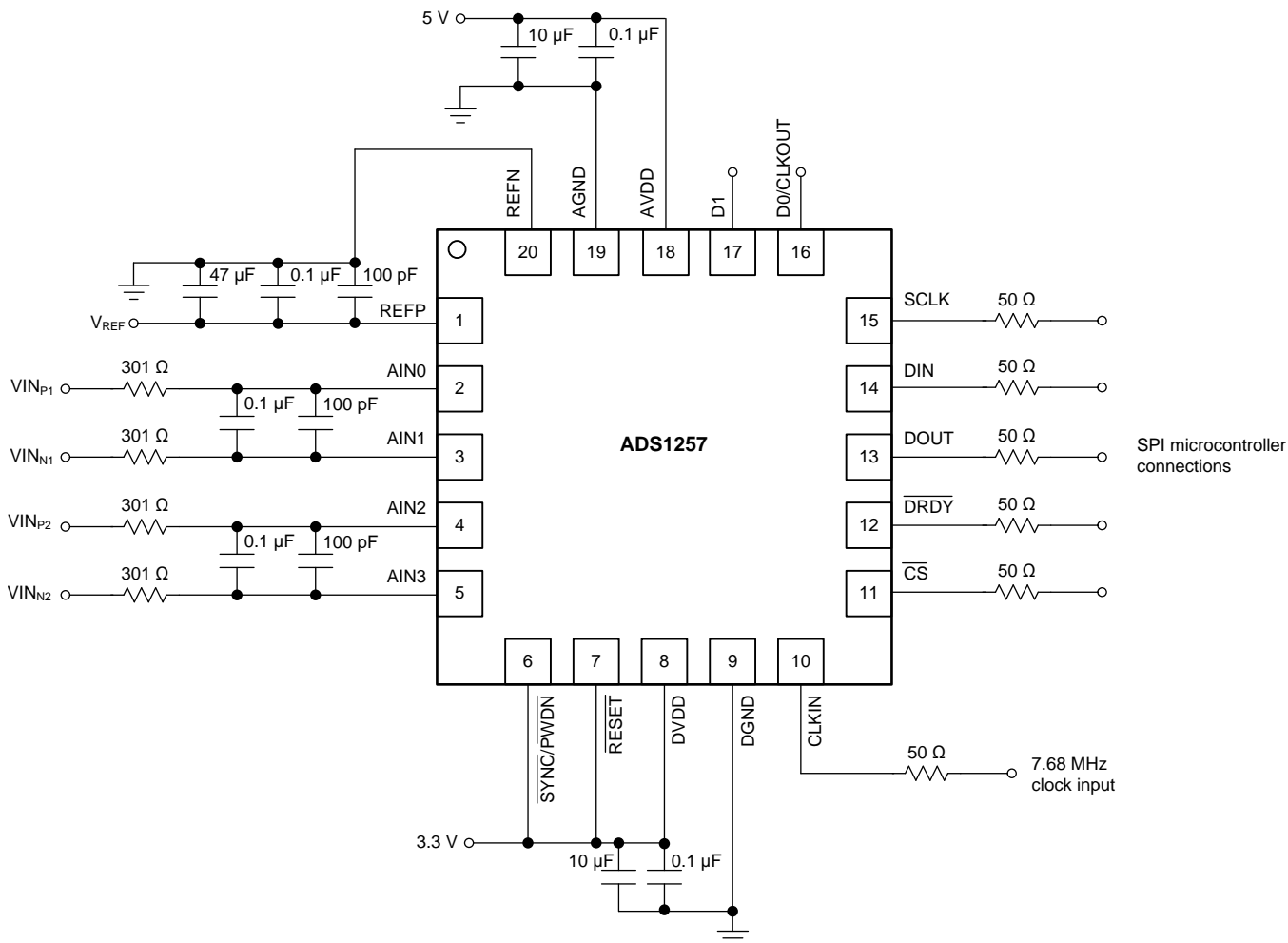
Figure 60. ADS1257 Basic Connections

Application Information (continued)

10.1.2 Digital Interface Connections

The ADS1257 5-V tolerant SPI-, QSPI™-, and Microwire™-compatible serial interface connects to a wide variety of microcontroller SPI peripherals. The interface operates in SPI mode 1, where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are updated only on SCLK rising edges; data are latched or read by the ADC and external controller on SCLK falling edges. See the *Serial Interface Timing Requirements* for details of the SPI communication protocol employed by the device.

Figure 61 shows how to connect to microcontrollers with a dedicated SPI, such as TI's MSP430 family of low-power microcontrollers. Additionally, the ADS1257 can connect to an 8xC51 UART in a two-wire configuration using serial mode 0, as shown in Figure 62. Avoid using read-data-continuous mode (RDATAC) when DIN and DOUT are connected together.

Place small series resistors on all digital signals to help smooth sharp transitions, suppress overshoot, and provide some overvoltage protection. Additional delays (due to the added resistance and bus capacitance) must still meet the SPI timing requirements.
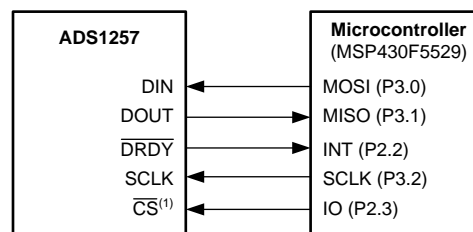
(1) $\overline{\text{CS}}$ may be tied low.

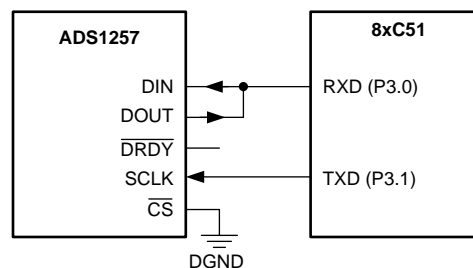**Figure 61. Connection to Microcontroller With an SPI**

Figure 62. Connection to 8xC51 Microcontroller UART With a 2-Wire Interface

10.1.3 Analog Input Filtering

Analog input filtering serves two purposes:

1. To limit the effect of aliasing during the sampling process.
2. To reduce the amount of external noise in the measurement.

As with any sampled system, aliasing can occur if proper antialias filtering is not in place. Aliasing occurs when frequency components are present in the input signal that are higher than half the sampling frequency of the ADC (also known as the Nyquist frequency). These frequency components are folded back into the frequency band of interest below half the sampling frequency. Inside a delta-sigma (ΔΣ) ADC, however, the input signal is sampled at the modulator frequency $f_{(MOD)}$ and not at the output data rate. The filter response of the digital filter repeats at multiples of the sampling frequency ($f_{(MOD)}$), as shown in Figure 63. Signals or noise up to frequencies near $f_{(MOD)}$ are attenuated to a certain amount by the digital filter. Any frequency components present in the input signal around the modulator frequency, or multiples thereof, are not attenuated and alias back into the band of interest unless attenuated by an external analog filter.
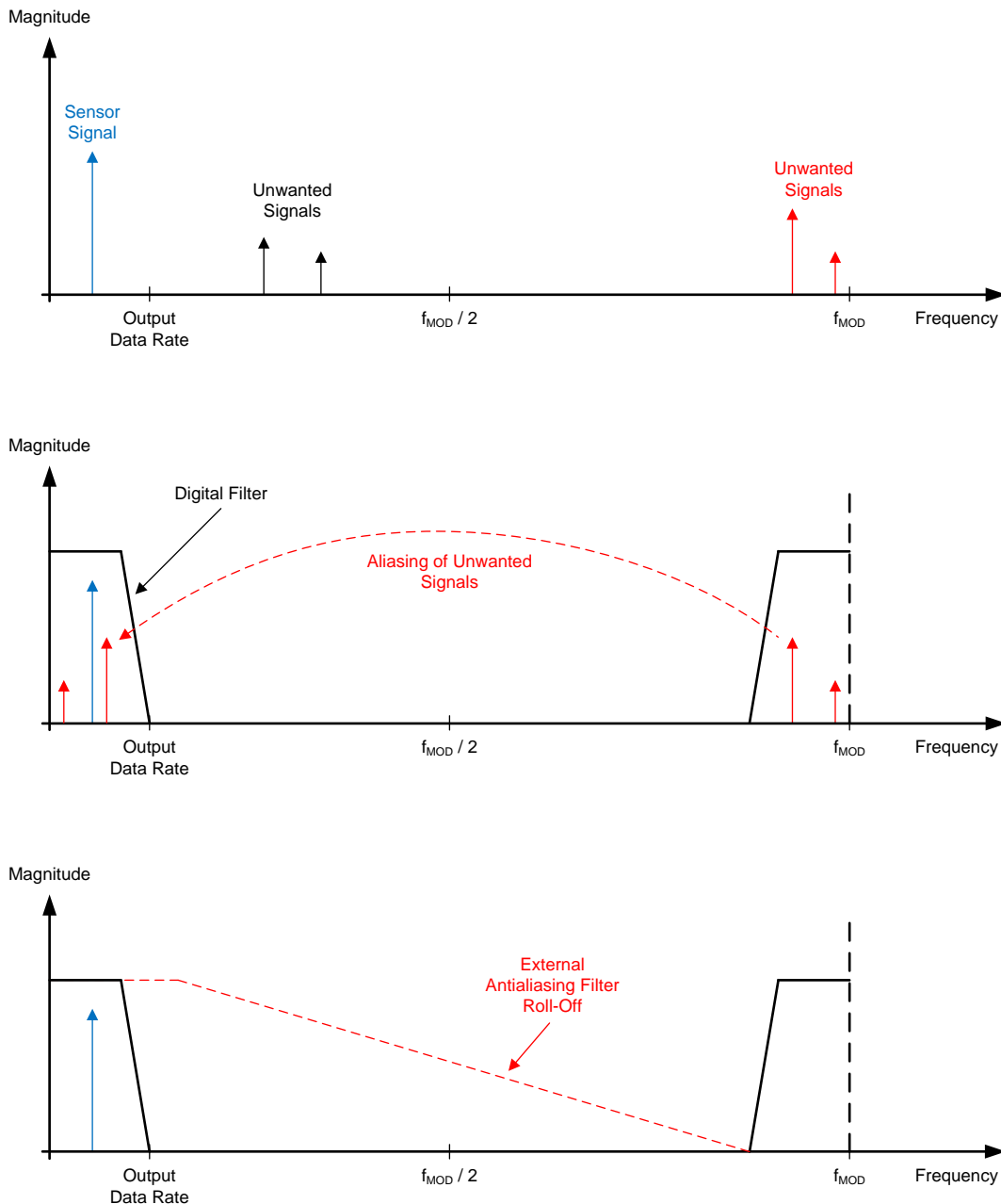
Product Folder Links: *ADS1257*

Figure 63. Alias Effect

Many sensor signals are inherently band-limited; for example, the output of a thermocouple has a limited rate of change. When band-limited, the sensor signal does not alias back into the pass band when using a ΔΣ ADC. However, any noise pick-up along the sensor wiring or the application circuitry can potentially alias into the pass-band. Power line-cycle frequency and harmonics are one common noise source example. External noise can also be generated from electromagnetic interference (EMI) or radio frequency interference (RFI) sources, such as nearby motors and cellular phones. Another noise source exists on the printed circuit board (PCB) itself in the form of clocks and other digital signals. Analog input filtering may help prevent such unwanted signals from affecting the measurement result.

Product Folder Links: *ADS1257*

A first-order resistor-capacitor (RC) filter is usually sufficient to either totally eliminate aliasing, or to reduce the effect of aliasing to a level within the noise floor of the sensor. Ideally, any signal beyond $f_{(MOD)}$ / 2 is attenuated to a level below the noise floor of the ADC. The digital filter of the ADS1257 attenuates signals to a certain degree, as illustrated in the filter response plots in the *Digital Filter* section. In addition, noise components are usually smaller in magnitude than the actual sensor signal. Therefore, using a first-order RC filter with a cutoff frequency set at the output data rate or higher is generally a good starting point for a system design. Avoid capacitors with low-grade dielectrics to minimize temperature variations and leakage.

10.1.4 External Reference

ADC measurement results are proportional to the ratio of the input and reference voltages; therefore, a stable and low-noise reference source is required for stable results. Select a reference source that is low noise, low drift, and low output impedance (such as the REF5025), which can drive the ADS1257 reference inputs directly. For voltage references not suited for driving the ADS1257 reference inputs directly (for example, high output impedance references or resistive voltage dividers), use the buffer circuit shown in Figure 64.
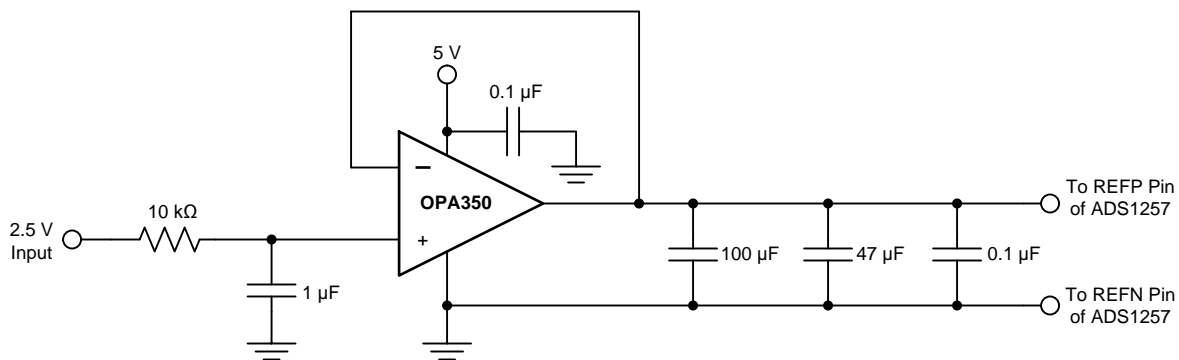

Figure 64. Voltage Reference Buffer Circuit

Always use low equivalent series resistance (ESR) capacitors to bypass the voltage reference signal near the ADS1257 reference input pins (REFP and REFN). Make these capacitors large in order to increase the filtering on the reference. Larger reference capacitors may take additional time to settle after power-up and when starting conversions.

The reference voltage (V_{REF}) must be between 0.5 V and 2.6 V.

10.1.5 Isolated (or Floating) Sensor Inputs

Isolated sensors (sensors that are not referenced to the ADC ground) must have an established common-mode voltage within the ADCs absolute input range, as specified by the *Recommended Operating Conditions*. Bias the ADCs input common-mode voltage by external resistors or by connecting to a dc voltage, such as the external reference voltage.

10.1.6 Unused Inputs and Outputs

To minimize leakage currents on the analog inputs, leave unused analog inputs floating, connect them to midsupply, or connect them to AVDD. Unused analog inputs can also be connected to AVSS, but may yield higher leakage currents than other connection options.

Tie all unused digital inputs to the appropriate levels (DVDD or DGND), including when in power-down mode. Do not float the digital inputs to the ADC; excessive power-supply leakage current can result. The D0/CLKOUT and D1 pins can be left floating if configured as outputs. If the DRDY output is not used, leave the DRDY pin unconnected or tie the pin to DVDD using a weak pull-up resistor.

10.1.7 Pseudo Code Example

The following list shows a sequence of steps for device set-up. The $\overline{\text{DRDY}}$ pin is used to indicate new conversion data. The register settings are configured for input buffer enabled, PGA gain = 16 V/V, and a data rate of 10 SPS.

```
Power-up the analog and digital supplies (allow time for power supplies to settle);

Set microcontroller GPIOs connected to the RESET and SYNC/PWDN pins low;
Configure the SPI of the microcontroller to SPI mode 1 (CPOL = 0, CPHA =1);
If the CS pin is not tied low permanently, configure microcontroller GPIO connected to CS as an output;
Configure microcontroller GPIO connected to the DRDY pin as a falling-edge triggered interrupt input;
Enable the external clock driving the CLKIN pin;
Enable the device by setting the RESET and SYNC/PWDN pins high;
Wait a minimum of 8192 clock cycles or for DRDY to transition low;

Set CS to the device low;
Delay for a minimum of t3;

Reset and Self-Calibration
{
    Send the RESET command (FEh) after power-up;
    Wait for DRDY to transition low (self-calibration has completed);
}

Send the SDATAC command (0Fh);
Delay for a minimum of t11;
Write the respective register configuration with the WREG command (50h, 03h, 02h, 01h, 24h and 23h);
Optional: As a sanity check, read back all configuration registers with the RREG command (10h);
Delay for a minimum of t11;

Send the RDATAC command (03h);
Delay for a minimum of t10;
Clear CS to high (resets the serial interface);

Loop
{
    Wait for DRDY to transition low;
    Take CS low;
    Delay for a minimum of t3;
    Send 24 SCLK rising edges to read out conversion data on DOUT;
    Delay for a minimum of t10;
    Clear CS to high;
}

Take SYNC/PWDN low for a minimum of 20 DRDY cycles to put the device in power-down mode;
```

Product Folder Links: *ADS1257*

10.2 Typical Application

Figure 65 shows an example of a programmable-logic controller (PLC) analog front-end circuit with ±10 V and 4-20 mA inputs, with 10% input over-range tolerance. A level-shifted resistor divider (R_1 and R_2) accepts input voltages from –11 V to +11 V, and a ground-referenced current-sense resistor (R_3) allows for current inputs ranging from 0 to 22 mA. The ADS1257 does not require any additional signal conditioning with its integrated multiplexer, buffer, PGA, and four analog input pins that accept single-ended, AGND-referenced voltages. The REF5025 provides the ADC reference voltage, and is capable of driving the ADC reference input pins without additional buffering. Resistor divider R_4 and R_5 and the buffer amplifier (OPA188) provide a 1.5-V level shift for the ±10-V input divider network. All three devices (the ADS1257, REF5025, and OPA188) are powered by a single 5-V supply.
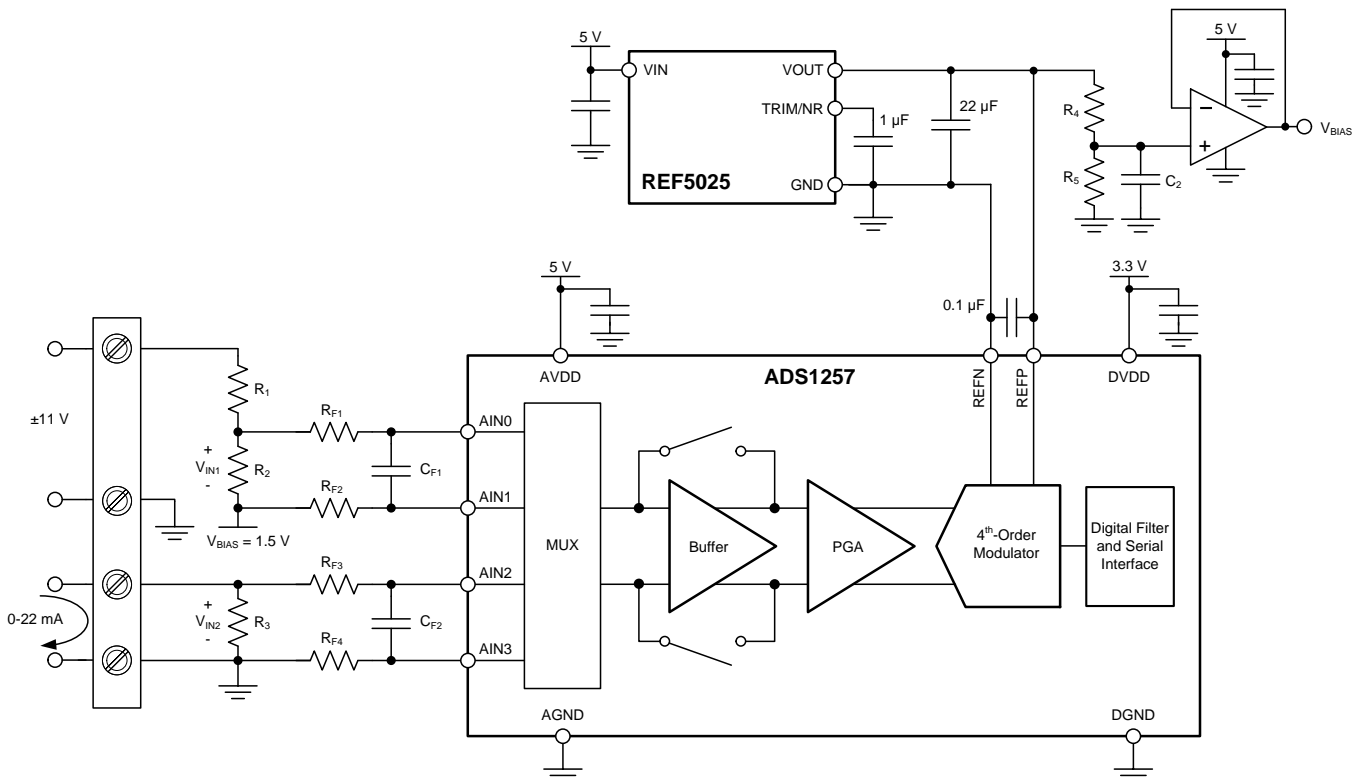

Figure 65. ±10-V and 4-20-mA Inputs for Programmable Logic Controller (PLC) Module

10.2.1 Design Requirements

Table 28. Design Requirements

DESIGN PARAMETER	VALUE
Supply voltages	5.0-V analog (unipolar) and 3.3-V digital
Data rate	10 SPS (simulataneous 50 / 60 Hz rejection)
Voltage input	±10 V (±10% overrange)[1] Input impedance ≥ 200 kΩ
Current input	4 mA to 20 mA (±10% overrange)[2]
Calibrated accuracy at T_A = 25°C	±0.01%

(1) See the *Voltage Input Design Variations* section for other possible voltage ranges.
(2) See the *Current Input Design Variations* section for other possible current ranges.

Product Folder Links: *ADS1257*

10.2.2 Detailed Design Procedure

10.2.2.1 Detailed Design Procedure for ±10-V Input

The following sections discuss the design of the PLC voltage input circuitry.

10.2.2.1.1 Absolute Input Voltage Range

A resistor divider attenuates and level shifts a ±10-V input signal to within the ADC input range, to create a linear relationship between the input signal voltage and ADC output code. Before designing the input circuitry, the ADC absolute and differential input voltage ranges are considered.

The input range of the ADS1257 depends on the analog supply voltage, the reference voltage, the state of the internal buffer (enabled or disabled), and the PGA gain. Input voltages must be within the absolute input voltage range of the ADC. The largest absolute input voltage range is achieved when the internal buffer is disabled, allowing for input signals between AGND – 0.1 V and AVDD + 0.1 V. However, the ADC input impedance is low when the buffer is disabled, causing the ADC to load input signals that have a high source impedance and are not buffered. Enable the buffer to increase the ADC input impedance, and significantly reduce the loading on the input signal. When the internal buffer is enabled, the input signal range is limited to voltages between AGND and AVDD – 2 V.

In the circuit shown in Figure 65, the voltage divider uses large-value resistors to reduce loading of the transmitted signal; therefore, the ADS1257 internal buffer is enabled to significantly reduce loading on the resistor divider. As a result, input signals to the ADC are limited to voltages between 0 V to 3 V (AVDD = 5 V, buffer enabled). Therefore, a level-shifted, single-ended input signal allows for a bipolar signal with maximum amplitude of ±1.5 V. Some additional headroom may be required to allow for analog supply-voltage tolerance.

10.2.2.1.2 Differential Input Voltage Range

The input voltage (V_{IN1}) must not exceed the differential input voltage range so that the ADC can provide an output code for every input voltage and avoid clipped output codes. The differential input voltage range is limited, in part by the absolute input voltage range, but also by the reference voltage and PGA gain. The differential input voltage range of the ADS1257 is given by Equation 5.

$$V_{IN} \leq \pm 2 \cdot V_{REF} / \text{Gain} \tag{5}$$

Using a nominal reference voltage of 2.5 V, the PGA gain is selected to allow for the largest input signal range and lowest ADC input-referred noise. The ratio of input signal to ADC noise is calculated as the number of noise-free bits, using Equation 6.

$$\text{Noise-Free Bits} = \log_2(V_{IN\_PP} / V_{NOISE\_RTI\_PP})$$

where

- V_{IN_PP} is the peak-to-peak input signal voltage range
- $V_{NOISE\_RTI\_PP}$ is the peak-to-peak input-referred noise ($V_{PP} \approx 6.6 \cdot V_{RMS}$)   (6)

The maximum achievable noise-free bit resolution is calculated for various PGA gains as shown in Table 29.

Table 29. Voltage Resolution Comparison for Various PGA Gains

PGA GAIN (V/V)	MAXIMUM DIFFERENTIAL INPUT VOLTAGE	INPUT-REFERRED NOISE AT 10 SPS [1]	NOISE-FREE BITS
1	±1.5 V[2]	2.24 µV$_{PP}$	20.4
2	±1.5 V[2]	1.41 µV$_{PP}$	21.0
4	±1.25 V[3]	0.91 µV$_{PP}$	21.4
8	±0.625 V[3]	0.70 µV$_{PP}$	20.8

(1) Peak-to-peak noise is estimated by multiplying RMS noise (as specified in Table 1) by a crest factor of 6.6.
(2) Limited by the absolute input voltage range; discussed in the *Absolute Input Voltage Range* section.
(3) Limited by the differential input voltage range; discussed in the *Differential Input Voltage Range* section.
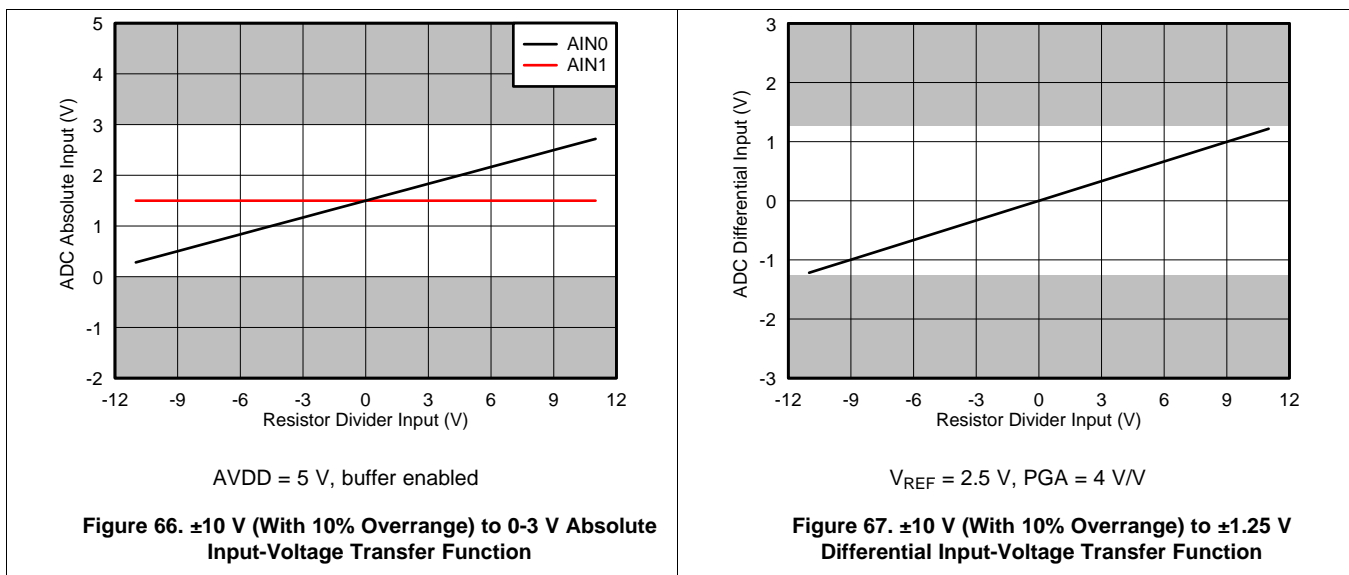
A PGA gain of 4 V/V is selected to achieve the highest voltage resolution; therefore, the differential input voltage must be limited to ±1.25 V to avoid overranging the ADC input. With the ADC differential input voltage range defined, the attenuation ratio of the resistor divider can be calculated.

10.2.2.1.3 Level-Shifted Resistor Divider Sizing

To attenuate the ±10-V signal (with 10% overrange) down to ±1.25 V, the resistor divider must have a gain less than 1.25 / 11 = 1 / 8.8 = 0.113 V/V. To achieve this attenuation, R_1 must be ≥ 9.8 · R_2. Additionally, the input impedance of the resistor divider ($R_1 + R_2$) must be ≥ 200 kΩ. Solving these requirements determines that R_2 must be ≥ 22.73 kΩ. Standard resistor values of 24.9 kΩ for R_2, and 200 kΩ for R_1 are chosen to satisfy the design requirements. Larger resistor values can also be used, but result in increased resistor thermal noise. Resistor noise must not exceed the ADC input-referred noise, or resolution degrades. Additionally, select resistors R_1 and R_2 to have low temperature coefficients in order to reduce the gain error drift of the resistor divider.

To level-shift the input signal and satisfy the ADS1257 absolute input range, R_2 is connected to a 1.5-V bias voltage. This bias voltage is derived from another resistor divider (R_4 and R_5) connected to the REF5025 output. Use values of 2 kΩ for R_4, and 3 kΩ for R_5 in order to provide the 1.5-V bias output. This voltage is buffered to avoid loading and provide a stable common-mode input voltage for the ADS1257.

Figure 66 and Figure 67 show the input transfer functions with respect to the ADC absolute and differential input voltage ranges, respectively.

AVDD = 5 V, buffer enabled

Figure 66. ±10 V (With 10% Overrange) to 0-3 V Absolute Input-Voltage Transfer Function

V_{REF} = 2.5 V, PGA = 4 V/V

Figure 67. ±10 V (With 10% Overrange) to ±1.25 V Differential Input-Voltage Transfer Function

10.2.2.1.4 Input Filtering

The differential RC filters are chosen to set the –3-dB corner frequency to be 1000 times wider than the ADC digital filter bandwidth in order to allow for fast RC settling and common component values. The selected ADS1257 sampling rate of 10 SPS results in a –3-dB digital filter bandwidth of 4.4 Hz. The –3-dB filter corner frequency for the input RC filter is set to approximately 5 kHz. Analog input currents of the ADC cause a voltage drop across the filter resistors that results in an offset error if either the bias currents or filter resistors are not equal. These resistors are limited to several kΩ in order to reduce resistor thermal noise and dc offset errors due to input bias currents. These resistors also provide a certain amount of input fault protection in case of an input overvoltage event. R_{F1} and R_{F2} are chosen to be 1.5 kΩ. The input filter differential capacitor (C_{F1}) is calculated from the selected cutoff frequency (f_{-3dB_DIFF}), as shown in Equation 7.

$$f_{-3dB\_DIFF} = 1 / (2 \cdot \pi \cdot C_{F1} \cdot (R_{F1} + R_{F2})) \tag{7}$$

After calculating the capacitance of C_{F1}, the capacitor is chosen to be a standard value of 10 nF.

10.2.2.1.5 Register Settings for ±10-V Input

The register settings for the PLC voltage measurement are shown in Table 30.

Table 30. Register Settings for ±11-V Input

REGISTER	NAME	SETTING	DESCRIPTION
00h	STATUS	0Ah	MSB first, buffer enabled
01h	MUX	01h	Select AIN0 = AIN$_P$ and AIN1 = AIN$_N$
02h	ADCON	02h	CLKOUT OFF, sensor detect OFF, gain = 4 V/V
03h	DRATE	23h	Data rate = 10 SPS

10.2.2.1.6 Voltage Input Design Variations

The level-shifted resistor divider is sized to allow for input signals up to ±10 V (with 10% overrange); however, different resistor values may be chosen to optimize the circuit for other common input voltage ranges, such as ±5 V, ±2.5 V, ±1 V, 0 V to 10 V, 0 V to 5 V, 0 V to 2.5 V, and 0 V to 1 V. For unipolar input ranges, remove the OPA188 and bias voltage resistor divider (R_4 and R_5) and connect the bias voltage (V_{BIAS}) to AGND.

10.2.2.2 Detailed Design Procedure for 4-mA to 20-mA Input

The following sections discuss the design of the PLC current input circuitry.

10.2.2.2.1 PGA Gain Selection

The previous *Absolute Input Voltage Range* and *Differential Input Voltage Range* considerations for the PLC voltage input circuitry also apply to the 4-mA to 20-mA current input design. However, the current-sense resistor is not level-shifted and input signals to the ADC are limited to positive voltages between 0-3 V (for buffer enabled, PGA gain = 1 V/V). Therefore, the noise-free bit resolution is recalcuted for the modified input signal range for various PGA gains, as shown in Table 31.

Table 31. Current Resolution Comparison for Various PGA Gains

PGA GAIN (V/V)	INPUT SIGNAL RANGE	INPUT-REFERRED NOISE AT 10 SPS[1]	NOISE-FREE BITS
1	0 to 3 V [2]	2.24 µV$_{PP}$	20.4
2	0 to 2.5 V [3]	1.41 µV$_{PP}$	20.8
4	0 to 1.25 V [3]	0.91 µV$_{PP}$	20.4
8	0 to 0.625 V [3]	0.70 µV$_{PP}$	19.8

(1) Peak-to-peak noise is estimated by multiplying RMS noise (as specified in Table 1) by a crest factor of 6.6.
(2) Limited by the absolute input voltage range; discussed in the *Absolute Input Voltage Range* section.
(3) Limited by the differential input voltage range; discussed in the *Differential Input Voltage Range* section.

A PGA gain of 2 V/V is selected to achieve the highest input current resolution. Therefore, the differential input voltage is limited to voltages between 0 V and 2.5 V.
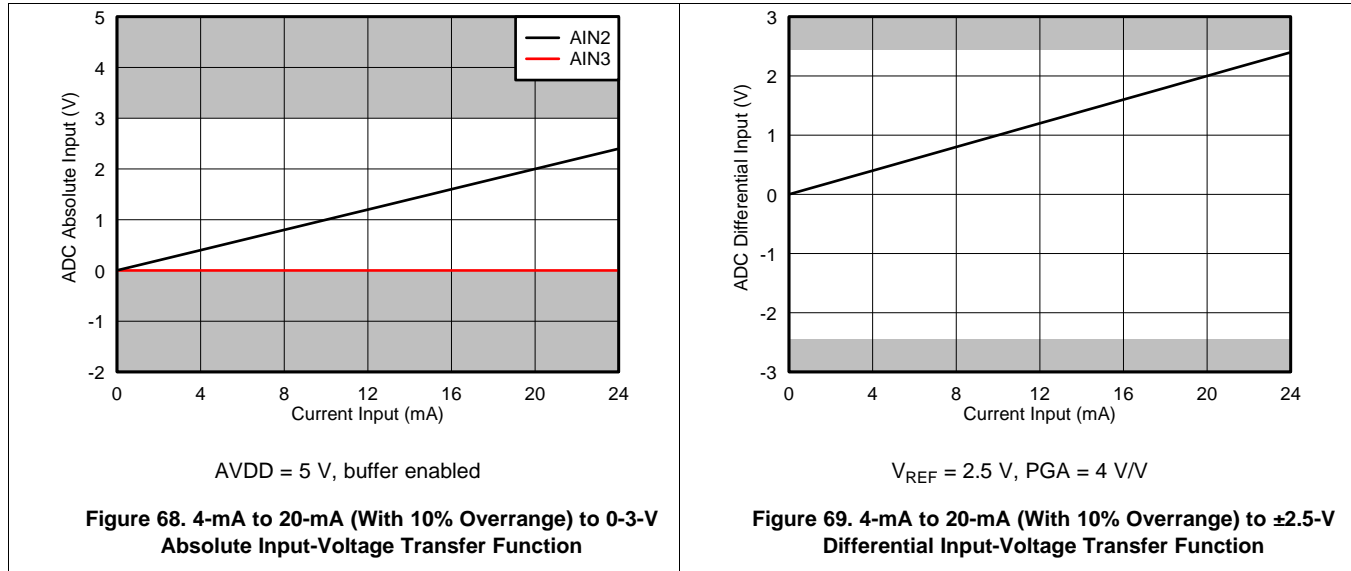
10.2.2.2.2 Current-Sense Resistor Sizing

To convert the 0-mA to 22-mA current into an input voltage between 0 V and 2.5 V, the current-sense resistor (R_3) must be ≤ 113.6 Ω. A standard resistor value of 100 Ω with a low temperature coefficient is chosen for R_3.

In addition to the resistance, make sure to consider the power dissipation. Resistor power dissipation (P_D) is given by Equation 8.

$$P_D = I_{MAX}^2 \cdot R \tag{8}$$

Product Folder Links: *ADS1257*

For the maximum current of 22 mA, the R_3 resistor dissipates 48.4 mW during normal operation. However, a larger power rating is required to accommodate temperature derating and input overvoltages. A low-leakage, transient-voltage-suppression (TVS) diode in parallel with R_3 reduces the power dissipated by this resistor in case of an input overvoltage. Figure 68 and Figure 69 show the current input-transfer functions, with respect to the ADC absolute input range and differential input voltage range, respectively.

AVDD = 5 V, buffer enabled

Figure 68. 4-mA to 20-mA (With 10% Overrange) to 0-3-V Absolute Input-Voltage Transfer Function

V_{REF} = 2.5 V, PGA = 4 V/V

Figure 69. 4-mA to 20-mA (With 10% Overrange) to ±2.5-V Differential Input-Voltage Transfer Function

10.2.2.2.3 Register Settings for 4-mA to 20-mA Input

The register settings for the PLC current measurement are shown in Table 32.

**Table 32. Register Settings for 4-mA to 20-mA Input**

REGISTER	NAME	SETTING	DESCRIPTION
00h	STATUS	0Ah	MSB first, buffer enabled
01h	MUX	23h	Select AIN2 = AIN_P and AIN3 = AIN_N
02h	ADCON	01h	CLKOUT off, sensor detect off, gain = 2 V/V
03h	DRATE	23h	Data rate = 10 SPS

10.2.2.2.4 Current Input Design Variations

The R_3 current-sense resistor is sized for input currents from 4 mA to 20 mA (with 10% overrange); however, different resistor values can be chosen to optimize the circuit for other current ranges. For a bipolar current input (such as ±20 mA), R_3 can be replaced with a 50-Ω resistor and biased to 1.5 V to allow for input voltages of ±1.25 V (Gain = 4 V/V), similar to the PLC voltage input configuration.

Product Folder Links: *ADS1257*

10.2.3 Application Curves

Figure 70 shows the measurement result accuracy for the ±10-V input application example. Figure 71 shows the measurement result accuracy for the 4-mA to 20-mA input application. The measurements were taken at T_A = 25°C. Both application examples meet the required accuracy given in Table 28.

Figure 70. Accuracy vs Input Voltage for ±10-V Input

Figure 71. Accuracy vs Input Current for 4-mA to 20-mA Input
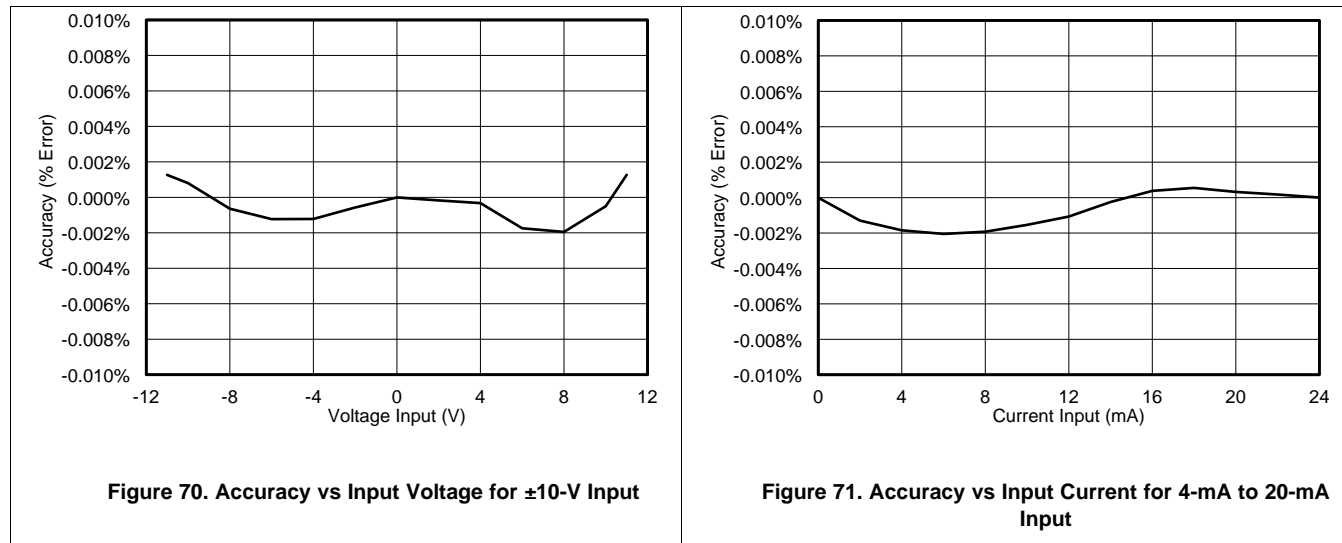
10.3 Dos and Don'ts

- Do partition the analog, digital, and power-supply circuitry into separate sections on the PCB.
- Do use a single ground plane for analog and digital grounds.
- Do place the analog components close to the ADC pins using short, direct connections.
- Do keep the SCLK pin free of glitches and noise.
- Do verify that the analog input voltages are within the specified absolute input-voltage range under all input conditions.
- Do tie unused input pins to proper voltage levels to minimize on-channel input leakage current.
- Do provide current limiting to the analog inputs to protect against overvoltage faults.
- Do use a low-dropout linear regulator (LDO) to reduce ripple voltage generated by switch-mode power supplies.
- Do not allow the analog and digital power-supply voltages to exceed the *Absolute Maximum Ratings* under any conditions, including during power-up and power-down.

Dos and Don'ts (continued)

Figure 72 shows the dos and don'ts of circuit connections for the ADS1257.
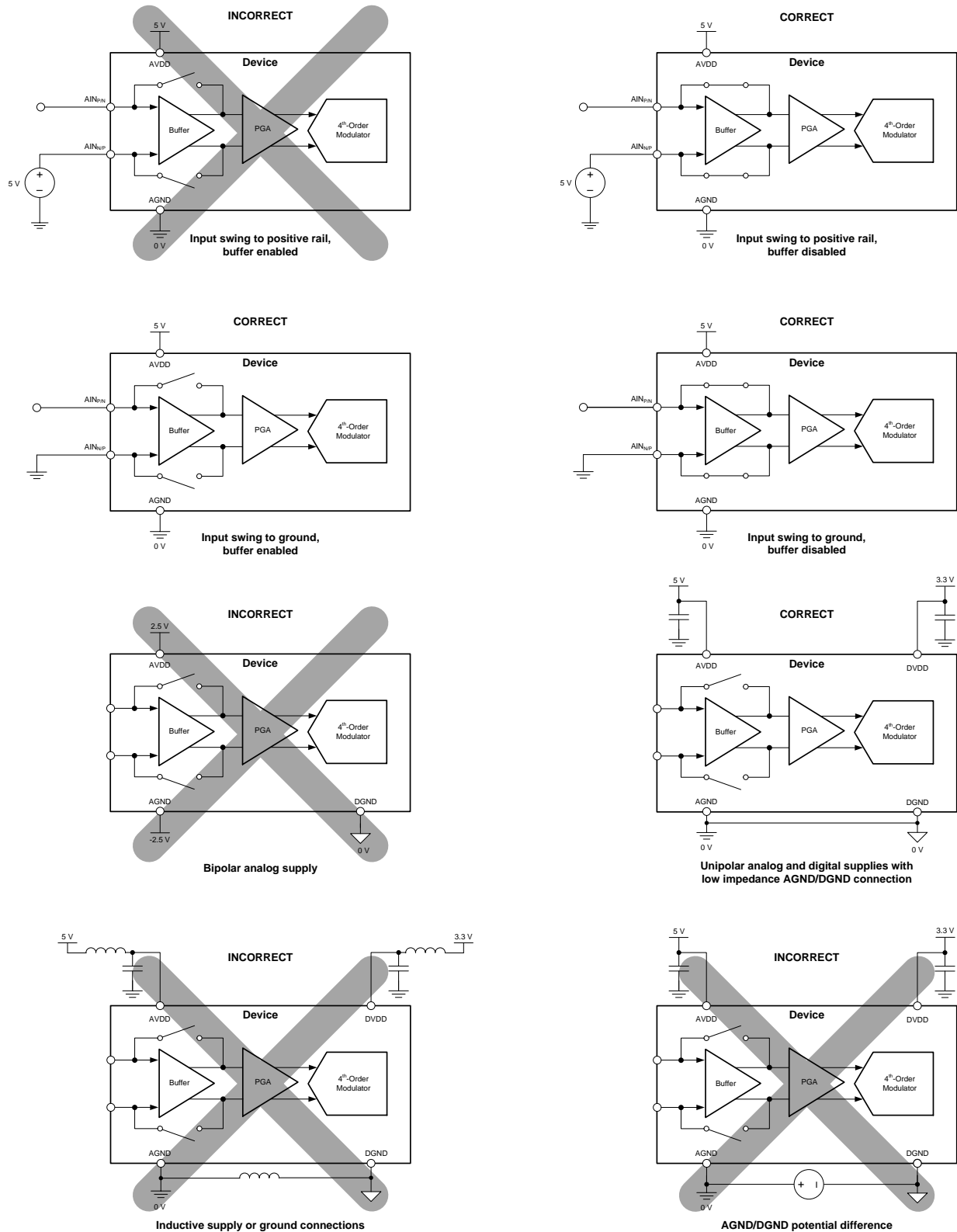

Figure 72. Do's and Don'ts Circuit Connections

11 Power Supply Recommendations

The ADS1257 requires an analog (AVDD) and digital (DVDD) power supply. The analog power supply is independent of the digital power supply. The digital supply sets the general-purpose digital I/O logic levels for D0 and D1. The analog and digital sections of the ADC are not internally isolated, and the analog and digital grounds (AGND, DGND) must be connected together. Output voltage ripple produced by switch-mode power supplies can interfere with the ADC, and result in reduced performance. Use low-dropout regulators (LDOs) to reduce the power-supply ripple voltage produced by switch-mode power supplies.

11.1 Power-Supply Sequencing

The analog and digital power supplies can be sequenced in any order during power up. Apply the external reference voltage and external clock source after the analog and digital power supplies have settled. Wait at least 8192 clock cycles (nominally 1.1 ms) before communicating with the device, and reset the device to help avoid improper operation.

NOTE

Do not apply any signal to the ADS1257 prior to power-up. In cases where applying a signal is unavoidable, limit the current in order to keep input signals within the *Absolute Maximum Ratings*.

11.2 Power-Supply Decoupling

Good power-supply decoupling is important to achieve optimum performance. AVDD and DVDD must be decoupled with at least a 0.1-µF capacitor, as shown in Figure 60. Place the bypass capacitors as close to the power-supply pins of the device as possible using low-impedance connections. Use multilayer ceramic chip capacitors (MLCCs) with low equivalent series resistance (ESR) and inductance (ESL) characteristics for power-supply decoupling. Avoid the use of vias for connecting decoupling capacitors whenever possible. If a via is required, the use of multiple vias in parallel lower the inductance of the connection; for example, when connecting to an internal ground plane layer. Connect the analog and digital ground pins together as close to the device as possible.

12 Layout

12.1 Layout Guidelines

Employ best design practices when laying out a printed circuit board (PCB) for both analog and digital components. Best design practice is to separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog multiplexers] from noise generating digital components [such as microcontrollers and switching regulators]. An example of good component placement is shown in Figure 73. Although Figure 73 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any high-resolution analog components.
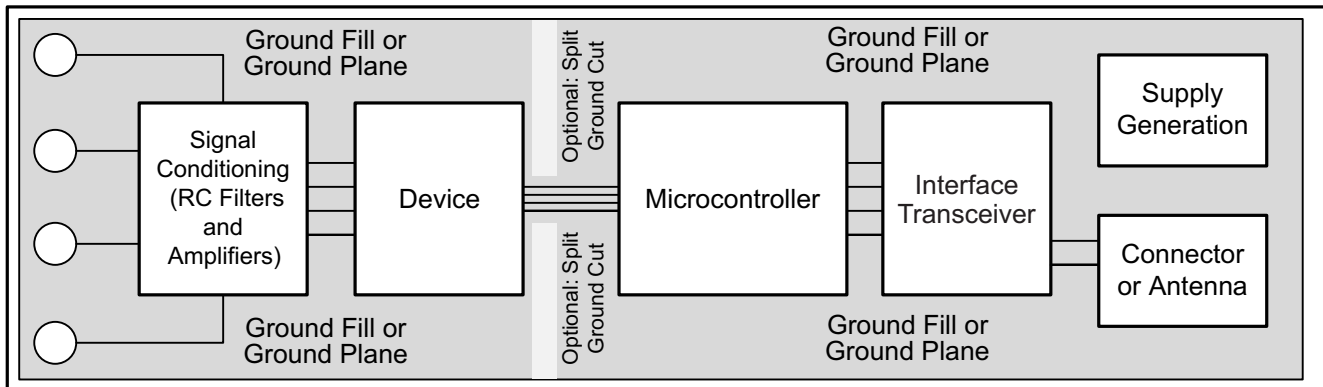

Figure 73. System Component Placement Example

The following outlines some basic recommendations for the layout of the ADS1257 to get the best possible performance of the ADC. A good design can be ruined with a bad circuit layout.

- Separate analog and digital signals. Partition the board into analog and digital sections when the layout permits. Route digital lines away from analog lines to help prevent digital noise from coupling into analog signals.
- Avoid splitting analog and digital ground planes. When possible, use a single solid ground plane for both analog and digital signals. A low impedance connection between AGND and DGND with minimal voltage difference between the ADS1257 analog and digital ground pins (AGND and DGND) is essential for optimum performance. If the system employs split digital and analog ground planes, connect the ground planes together as close to the device as possible.
- Fill void areas on signal layers with ground fill.
- Provide good ground return paths. Signal return currents follow the path of least impedance. If the ground plane is cut or has other traces that block the current from flowing adjacent to the signal trace, the current finds another path to return the source. If forced onto a longer path, the return current increases the possibility that the signal radiates or interferes with other sensitive circuitry.
- Use bypass capacitors on supplies to reduce high-frequency noise. Do not place vias between bypass capacitors and the active device. For best results, place the bypass capacitors on the same layer and as close to the active device as possible.
- Consider the resistance and inductance of the routing. Large resistance on the input traces can react with the input bias current and cause an added offset voltage. Reduce loop areas enclosed by the source signal and the return current in order to reduce input inductance and help prevent EMI pickup.
- Route all differential signal traces as matched differential pairs. When possible, use adjacent analog inputs, such as AIN0, AIN1 and AIN2, AIN3, for differential measurements.
- Analog inputs with differential connections must have a differential filtering capacitor placed across the inputs. Use high-quality differential capacitors, such as C0G (NPO) dielectric capacitors, that have stable properties and low-noise characteristics.

12.2 Layout Example

Figure 74 shows an example layout for the ADS1257 with a four layer PCB (only three layers are visible).
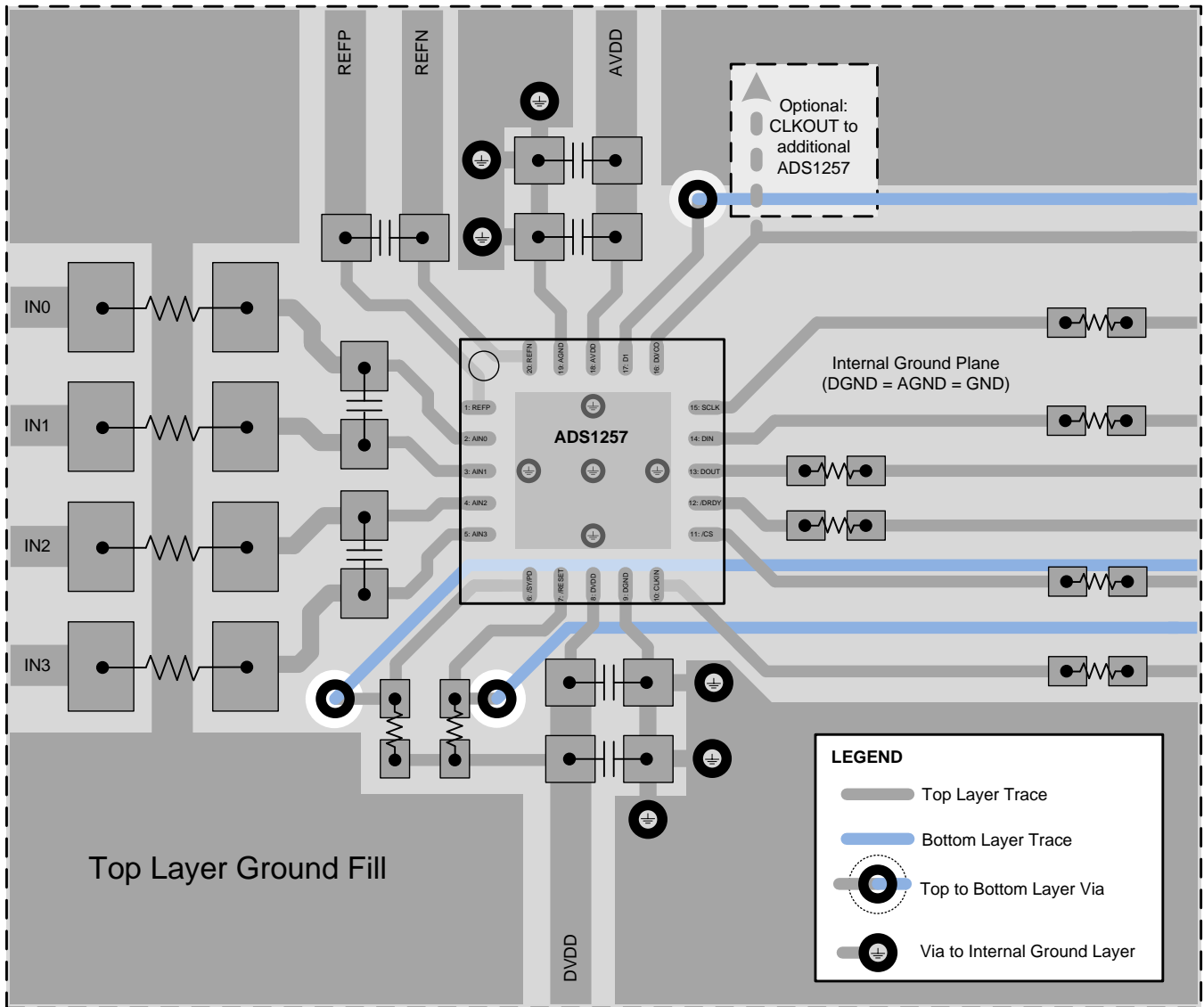

Figure 74. Four-Layer PCB Layout Example

Analog and digital grounds share a ground plane. Do not place other traces are placed on the ground plane layer. Multiple parallel vias are used to reduce ground connection impedance and connect ground planes on multiple layers. Analog and digital signals are partitioned into separate areas on the PCB (as if a ground split was made) to reduce the potential for digital noise to couple into the analog signals. Where possible, ground plane fill is used on all layers.

Supply and reference signals are shown as traces routed on the top layer; however, these signals can also be provided to the ADS1257 through an internal layer. For best performance, the negative reference signal (REFN) must be routed back to the reference source with a trace and connected to ground near the reference source, to prevent ground plane currents from coupling into this signal. Route signal traces as differential pairs to minimize noise pick-up from adjacent traces.

Layout Example (continued)

Digital signals with fast rise and fall times are subject to ringing and overshoot if not properly terminated. Series resistors placed near the driving source terminate the transmission line of the PCB trace and suppress voltage ringing. When routing digital signals, give priority to CLKIN and SCLK signals. Keep clock traces as short as possible, routed directly above a ground plane, and routed with a minimum number of vias. GPIOs and control signal traces with slower edges and less frequent switching (such as D0, $\overline{CS}$, $\overline{SYNC}/\overline{PWDN}$, and $\overline{RESET}$) are not as sensitive to layout and can be made longer and use additional vias to make room for more critical digital signals (such as CLKIN, SCLK, DIN, and DOUT). Note that when multiple ADS1257s are used, the external clock signal can be routed to CLKIN on one device, and then serially connected from CLKOUT to CLKIN on the next device to simplify layout.

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

Table 33 lists quick access links to related documentation and the associated devices. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 33. Related Documentation Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS1255	Click here	Click here	Click here	Click here	Click here
ADS1256	Click here	Click here	Click here	Click here	Click here
REF5025	Click here	Click here	Click here	Click here	Click here
OPA350	Click here	Click here	Click here	Click here	Click here
OPA188	Click here	Click here	Click here	Click here	Click here
MSP430F5529	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
SPI, QSPI are trademarks of Motorola, Inc.
Microwire is a trademark of National Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1257IRGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS1257	Samples
ADS1257IRGWT	ACTIVE	VQFN	RGW	20	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	ADS1257	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
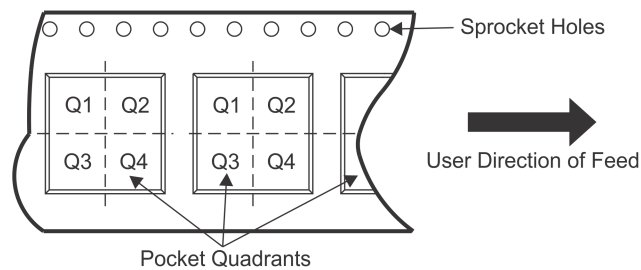
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1257IRGWR	VQFN	RGW	20	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
ADS1257IRGWT	VQFN	RGW	20	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1257IRGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
ADS1257IRGWT	VQFN	RGW	20	250	210.0	185.0	35.0

RGW (S-PVQFN-N20)　　　　　　PLASTIC QUAD FLATPACK NO-LEAD

PIN 1 INDEX AREA
TOP AND BOTTOM

$\frac{5,15}{4,85}$

$\frac{5,15}{4,85}$

$\frac{1,00}{0,80}$

0,20 REF.

SEATING PLANE

$\boxed{0,08}$

$\frac{0,05}{0,00}$

20X $\frac{0,65}{0,45}$

$\boxed{0,65}$

1

5

20

THERMAL PAD

6

SIZE AND SHAPE
SHOWN ON SEPARATE SHEET

16

10

15

11

20X $\frac{0,38}{0,23}$

$\boxed{2,60}$

$\boxed{\oplus \;\; \varnothing\; 0,10 \;\; \text{Ⓜ}}$

4204100/C 07/11
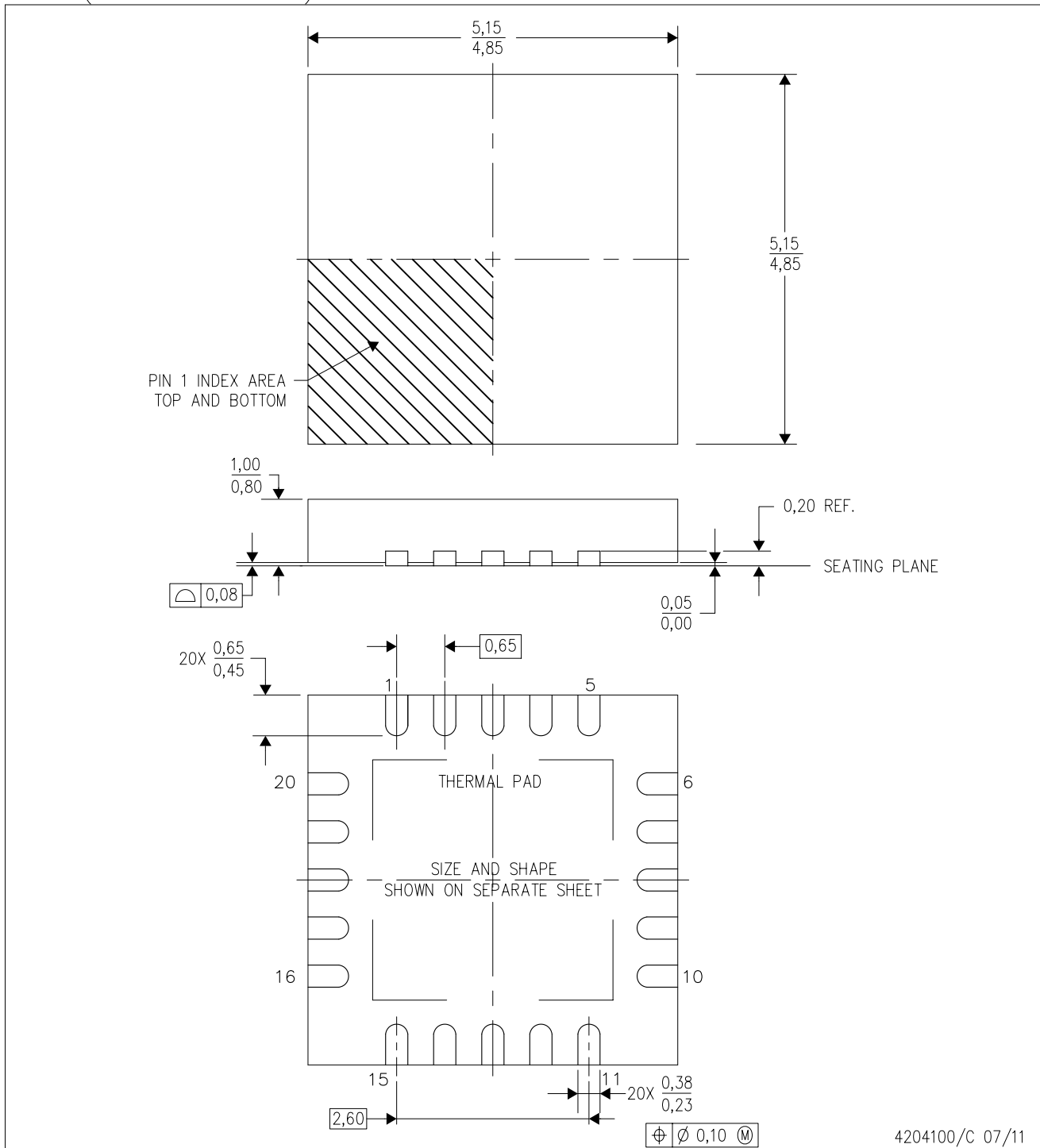
NOTES:　A.　All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
　　　　B.　This drawing is subject to change without notice.
　　　　C.　Quad Flat pack, No-leads (QFN) package configuration
　　　　D.　The package thermal pad must be soldered to the board for thermal and mechanical performance.
　　　　E.　See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
　　　　F.　Falls within JEDEC MO-220.

RGW (S−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.
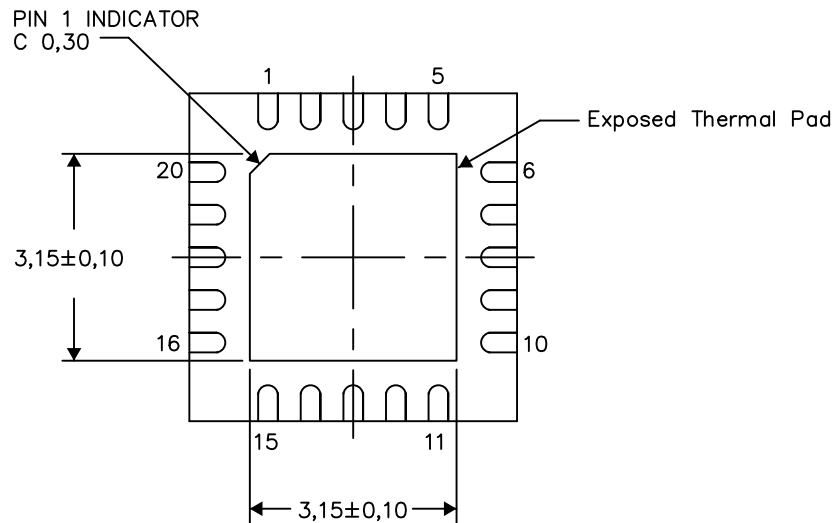
Bottom View

Exposed Thermal Pad Dimensions

4206352−2/M 06/15

NOTE: All linear dimensions are in millimeters

RGW (S−PVQFN−N20)   PLASTIC QUAD FLATPACK NO−LEAD
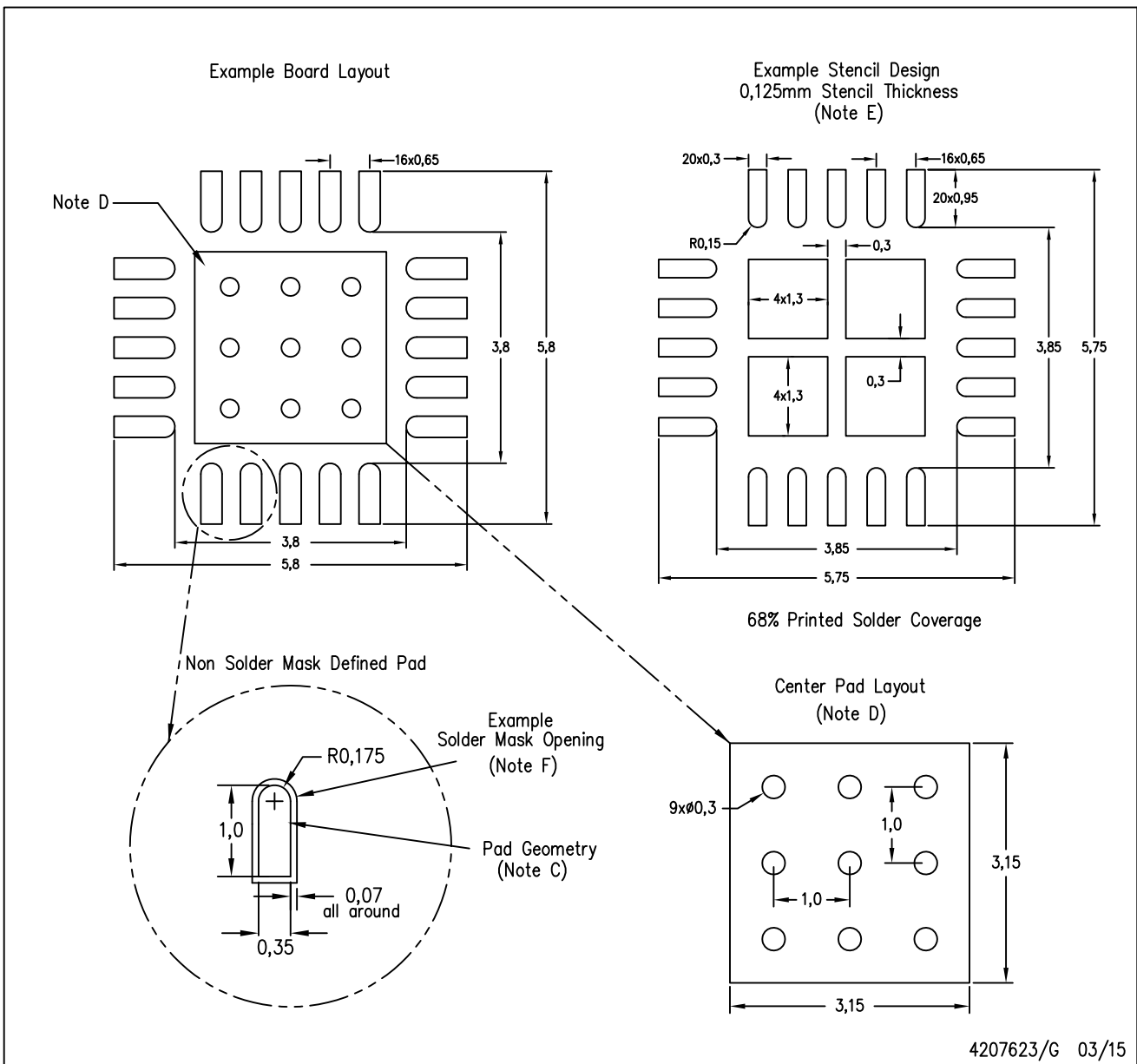
Example Board Layout

Note D

16x0,65

3,8   5,8

3,8

5,8

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

R0,175

1,0

Pad Geometry
(Note C)

0,07
all around

0,35

Example Stencil Design
0,125mm Stencil Thickness
(Note E)

20x0,3   16x0,65

20x0,95

R0,15   0,3

4x1,3

3,85   5,75

4x1,3   0,3

3,85

5,75

68% Printed Solder Coverage

Center Pad Layout
(Note D)

9xØ0,3

1,0

3,15

1,0

3,15

4207623/G 03/15

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Publication IPC−7351 is recommended for alternate designs.
        D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN
            Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
            for specific thermal information, via requirements, and recommended board layout. These documents are available at
            www.ti.com <http://www.ti.com>.
        E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
            contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
        F. Customers should contact their board fabrication site for solder mask tolerances.

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