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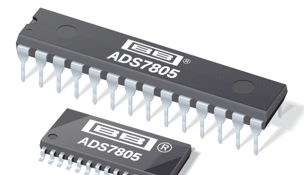


ADS7805

SBAS020D – JANUARY 1996 – REVISED OCTOBER 2006

16-Bit, 10μs Sampling, CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

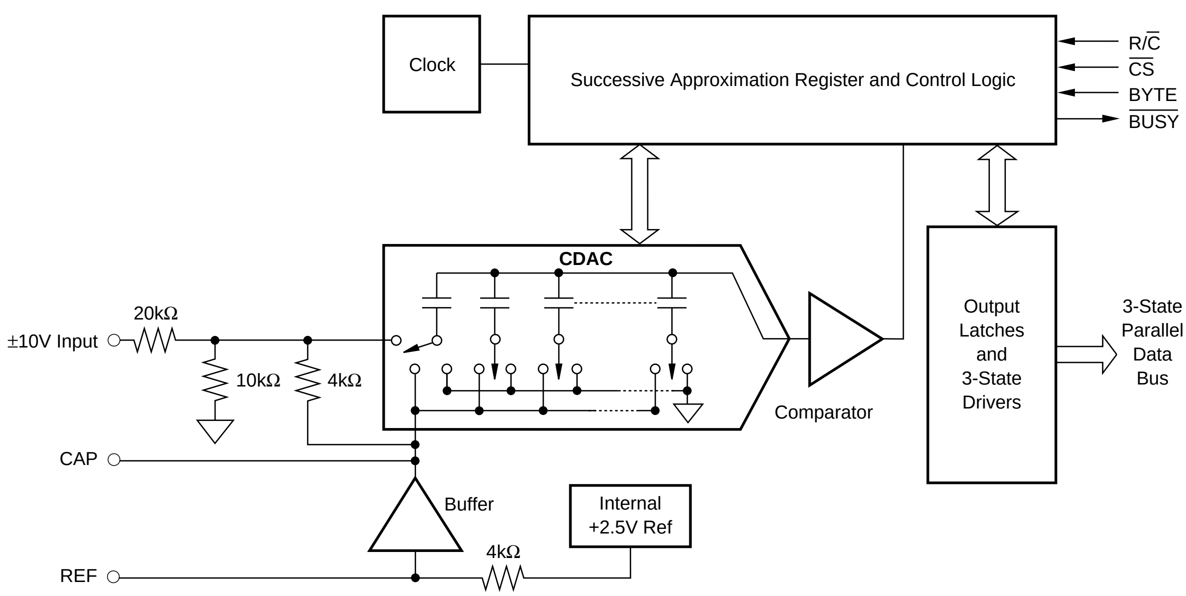
- 100kHz min SAMPLING RATE
- STANDARD ±10V INPUT RANGE
- 86dB min SINAD WITH 20kHz INPUT
- ±3.0 LSB max INL
- DNL: 16 Bits No Missing Codes
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7804
- USES INTERNAL OR EXTERNAL REFERENCE
- FULL PARALLEL DATA OUTPUT
- 100mW max POWER DISSIPATION
- 0.3" DIP-28 AND SO-28

DESCRIPTION

The ADS7805 is a complete 16-bit sampling, Analog-to-Digital (A/D) converter using state-of-the-art CMOS structures. It contains a complete 16-bit, capacitor-based, Successive Approximation Register (SAR) A/D converter with Sample-and-Hold (S/H), reference, clock, interface for microprocessor use, and 3-state output drivers.

The ADS7805 is specified at a 100kHz sampling rate and ensured over the full temperature range. Laser-trimmed scaling resistors provide an industry-standard ±10V input range while the innovative design allows operation from a single +5V supply, with power dissipation under 100mW.

The ADS7805 is available in a 0.3" DIP-28 and an SO-28 package. Both are fully specified for operation over the industrial –25°C to +85°C range; however, they will function over the –40°C to +85C temperature range.



ABSOLUTE MAXIMUM RATINGS[1]

Analog Inputs: V_{IN}	±25V
REF	$+V_{ANA}$ + 0.3V to AGND2 – 0.3V
CAP	Indifinite Short to AGND2 Momentary Short to V_{ANA}
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
V_{ANA}	7V
V_{DIG} to V_{ANA}	+0.3V
V_{DIG}	7V
Digital Inputs	–0.3V to $+V_{DIG}$ + 0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7805P	±4	83	DIP-28	NT	–25°C to +85°C	NT	ADS7805P	Tube, 13
ADS7805PB	±3	86	DIP-28	NT	–25°C to +85°C	NT	ADS7805PB	Tube, 13
ADS7805U	±4	83	SO-28	DW	–25°C to +85°C	DW	ADS7805U	Tube, 28
ADS7805U	±4	83	SO-28	DW	–25°C to +85°C	DW	ADS7805U/1K	Tape and Reel, 1000
ADS7805UB	±3	86	SO-28	DW	–25°C to +85°C	DW	ADS7805UB	Tube, 28
ADS7805UB	±3	86	SO-28	DW	–25°C to +85°C	DW	ADS7805UB/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ELECTRICAL CHARACTERISTICS

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			16	Bits
ANALOG INPUT								
Voltage Ranges			±10			±10		V
Impedance			23			23		kΩ
Capacitance			35			35		pF
THROUGHPUT SPEED								
Conversion Cycle	Acquire and Convert			10			10	µs
Throughput Rate		100			100			kHz
DC ACCURACY								
Integral Linearity Error				±4			±3	LSB[1]
No Missing Codes		15			16			Bits
Transition Noise[2]			1.3			1.3		LSB
Full-Scale Error[3,4]				±0.5			±0.25	%
Full-Scale Error Drift			±7			±5		ppm/°C
Full-Scale Error[3,4]	Ext. 2.5000V Ref			±0.5			±0.25	%
Full-Scale Error Drift	Ext. 2.5000V Ref		±2			±2		ppm/°C
Bipolar Zero Error[3]				±10			±10	mV
Bipolar Zero Error Drift			±2			±2		ppm/°C
Power Supply Sensitivity (V_{DIG} = V_{ANA} = V_D)	+4.75V < V_D < +5.25V			±8			±8	LSB
AC ACCURACY								
Spurious-Free Dynamic Range	f_{IN} = 20kHz	90			94			dB[5]
Total Harmonic Distortion	f_{IN} = 20kHz			–90			–94	dB
Signal-to-(Noise+Distortion)	f_{IN} = 20kHz	83			86			dB
	–60dB Input		30			32		dB
Signal-to-Noise	f_{IN} = 20kHz	83			86			dB
Full-Power Bandwidth[6]			250			250		kHz
SAMPLING DYNAMICS								
Aperture Delay			40			40		ns
Transient Response	FS Step			2			2	µs
Overvoltage Recovery[7]			150			150		ns

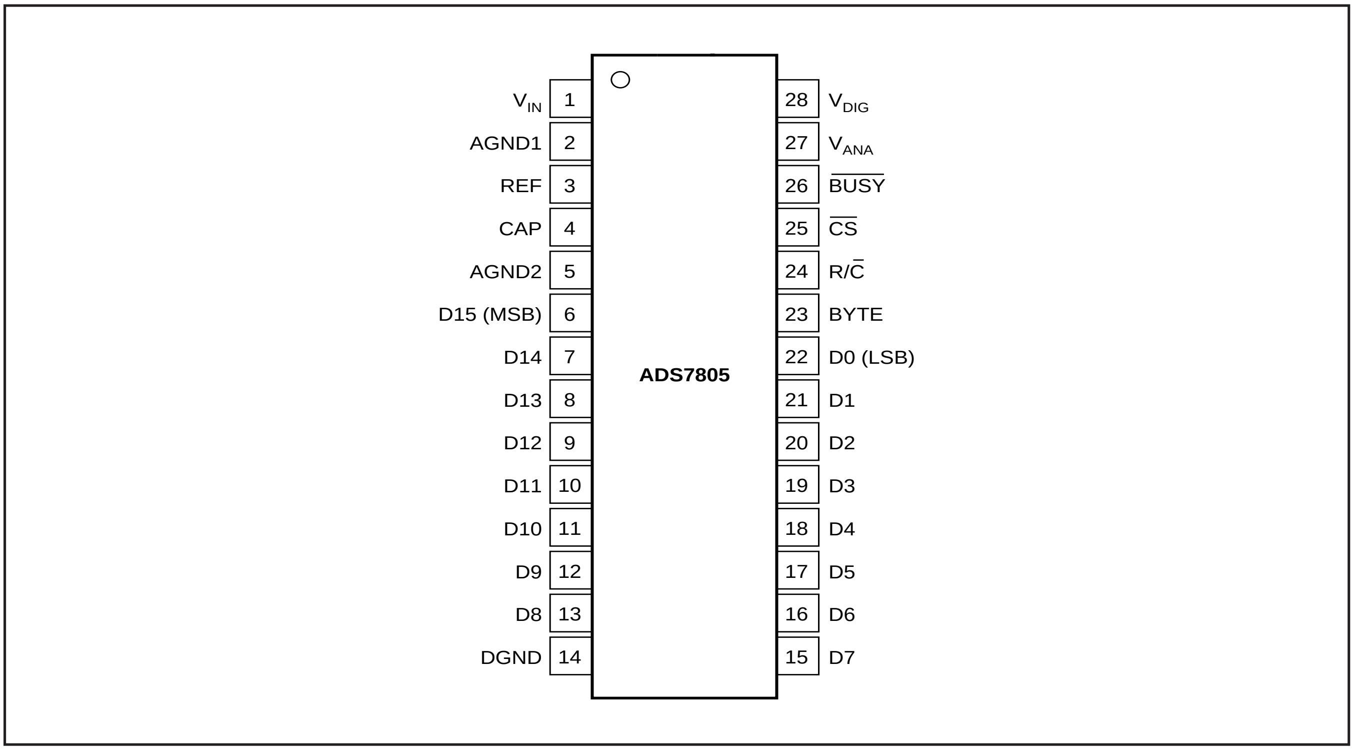
ELECTRICAL CHARACTERISTICS (Cont.)

T_A = –25°C to +85°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7805P, U			ADS7805PB, UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE								
Internal Reference Voltage		2.48	2.5	2.52	2.48	2.5	2.52	V
Int. Ref. Source Current (must use external buffer)			1			1		µA
Internal Reference Drift			8			8		ppm/°C
Ext. Ref. Voltage Range for Specified Linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
External Reference Current Drain	Ext. 2.5000V Ref			100			100	µA
DIGITAL INPUTS								
Logic Levels								
V_{IL}		–0.3		+0.8	–0.3		+0.8	V
V_{IH}		+2.0		V_D + 0.3V	+2.0		V_D + 0.3V	V
I_{IL}				±10			±10	µA
I_{IH}				±10			±10	µA
DIGITAL OUTPUTS								
Data Format		Parallel 16 Bits						
Data Coding		Binary Two's Complement						
V_{OL}	I_{SINK} = 1.6mA			+0.4			+0.4	V
V_{OH}	I_{SOURCE} = 500µA	+4			+4			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5			±5	µA
Output Capacitance	High-Z State			15			15	pF
DIGITAL TIMING								
Bus Access Time				83			83	ns
Bus Relinquish Time				83			83	ns
POWER SUPPLIES								
Specified Performance								
V_{DIG}	Must be ≤ V_{ANA}	+4.75	+5	+5.25	+4.75	+5	+5.25	V
V_{ANA}		+4.75	+5	+5.25	+4.75	+5	+5.25	V
I_{DIG}			0.3			0.3		mA
I_{ANA}			16			16		mA
Power Dissipation	f_S = 100kHz			100			100	mW
TEMPERATURE RANGE								
Specified Performance		–25		+85	–25		+85	°C
Operating Temperature(8)		–40		+85	–40		+85	°C
Derated Performance		–55		+125	–55		+125	°C
Storage		–65		+150	–65		+150	°C
Thermal Resistance (θ_{JA})								
DIP-28			75			75		°C/W
SO-28			75			75		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 16-bit, ±10V input ADS7805, one LSB is 305µV.
(2) Typical rms noise at worst case transitions and temperatures.
(3) As measured with fixed resistors, see Figure 4. Adjustable to zero with external potentiometer.
(4) Full-scale error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error.
(5) All specifications in dB are referred to a full-scale ±10V input.
(6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB, or 10 bits of accuracy.
(7) Recovers to specified performance after 2 • FS input overvoltage.
(8) Functionality test at –40°C.

PIN CONFIGURATION

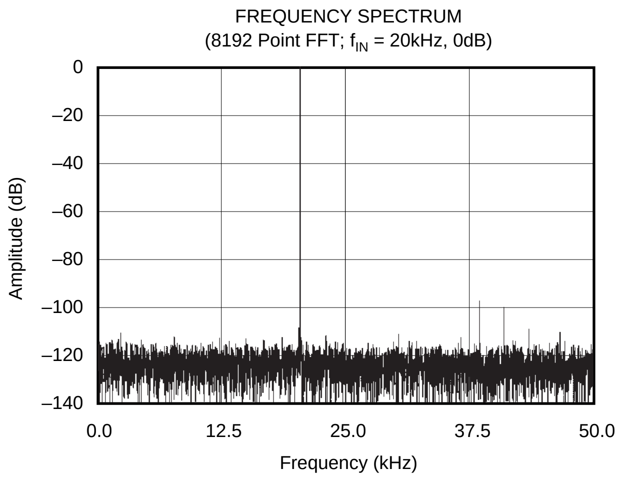


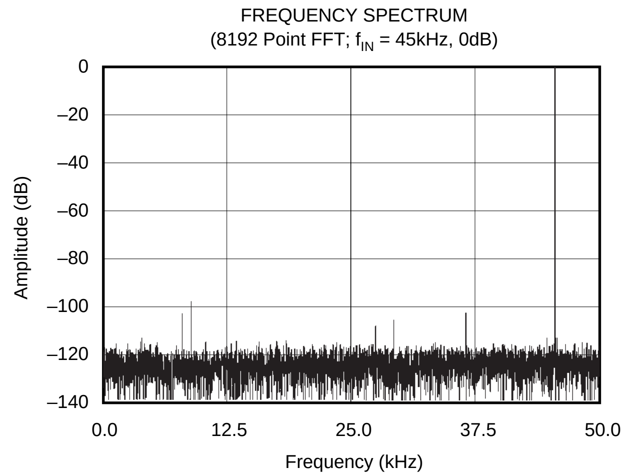
PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. See Figure 7.
2	AGND1		Analog Ground. Used internally as ground reference point.
3	REF		Reference Input/Output. 2.2µF tantalum capacitor to ground.
4	CAP		Reference Buffer Capacitor. 2.2µF tantalum capacitor to ground.
5	AGND2		Analog Ground
6	D15 (MSB)	O	Data Bit 15. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
7	D14	O	Data Bit 14. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
8	D13	O	Data Bit 13. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
9	D12	O	Data Bit 12. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
10	D11	O	Data Bit 11. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
11	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
12	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
13	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
14	DGND		Digital Ground
15	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
16	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
17	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
18	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
19	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
20	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
21	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
22	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW.
23	BYTE	I	Selects 8 most significant bits (LOW) or 8 least significant bits (HIGH).
24	R/$\overline{C}$	I	With $\overline{CS}$ LOW and $\overline{BUSY}$ HIGH, a Falling Edge on R/$\overline{C}$ Initiates a new conversion. With $\overline{CS}$ LOW, a rising edge on R/$\overline{C}$ enables the parallel output.
25	$\overline{CS}$	I	Internally OR'd with R/$\overline{C}$. If R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ initiates a new conversion.
26	$\overline{BUSY}$	O	At the start of a conversion, $\overline{BUSY}$ goes LOW and stays LOW until the conversion is completed and the digital outputs have been updated.
27	V_{ANA}		Analog Supply Input. Nominally +5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
28	V_{DIG}		Digital Supply Input. Nominally +5V. Connect directly to pin 27. Must be $\leq V_{ANA}$.

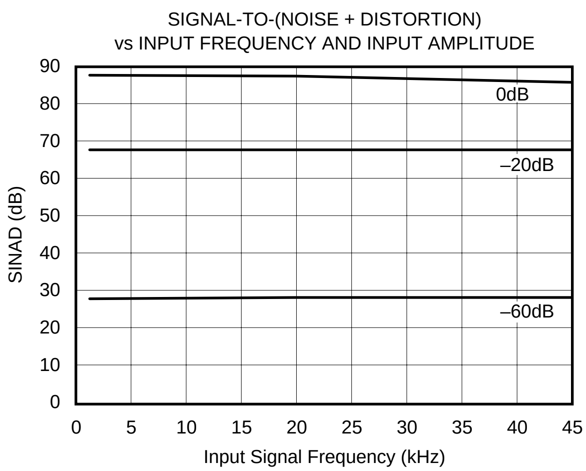
TABLE I. Pin Assignments.

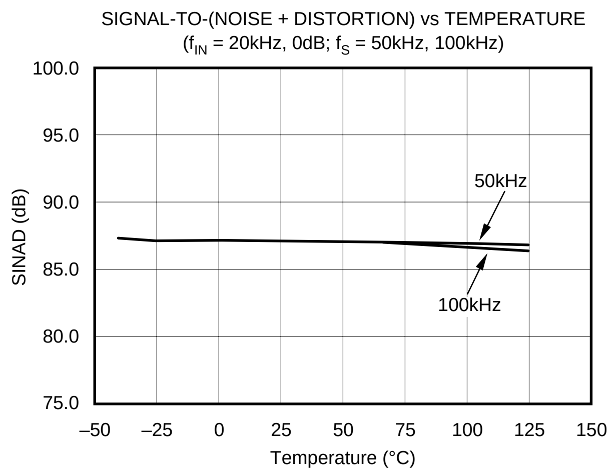
TYPICAL CHARACTERISTICS

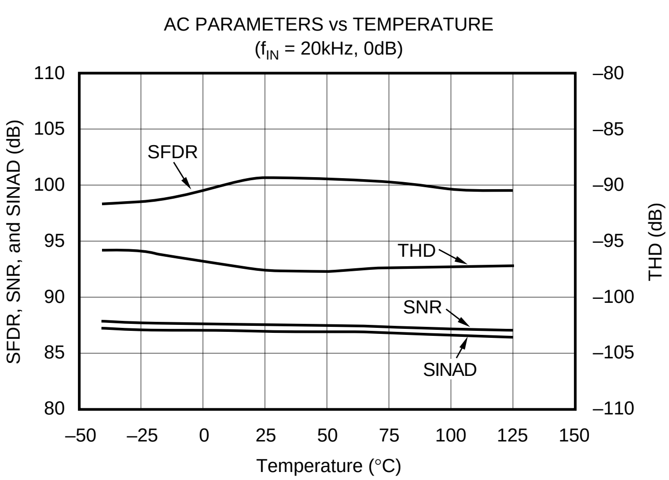
T_A = +25°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 6b, unless otherwise specified.

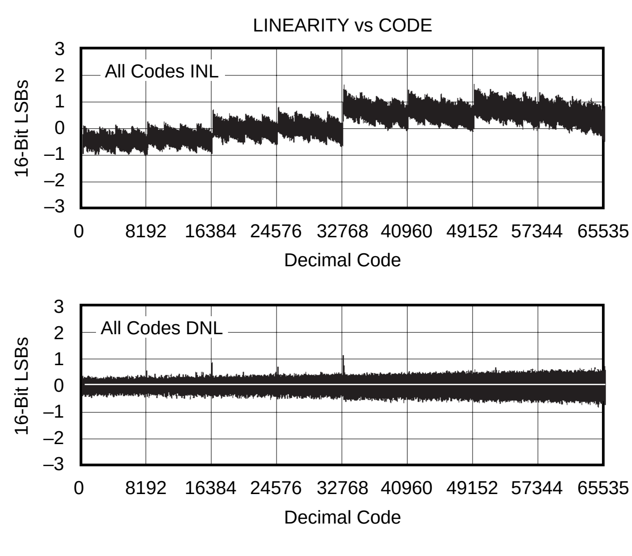




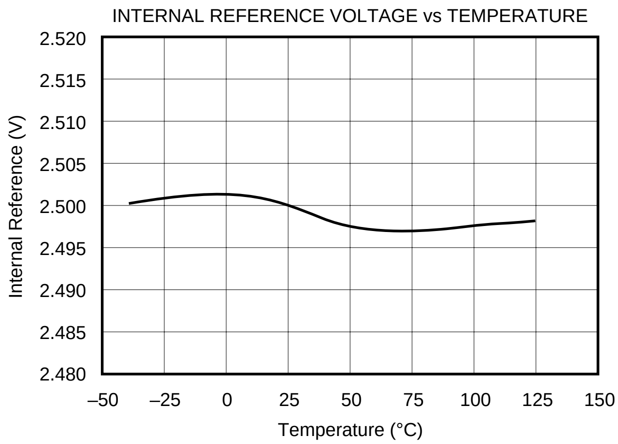


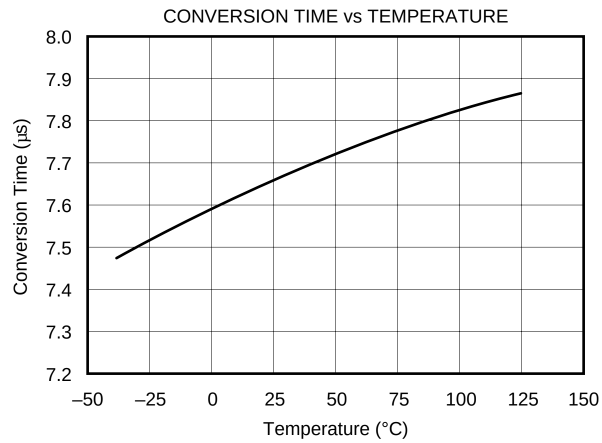


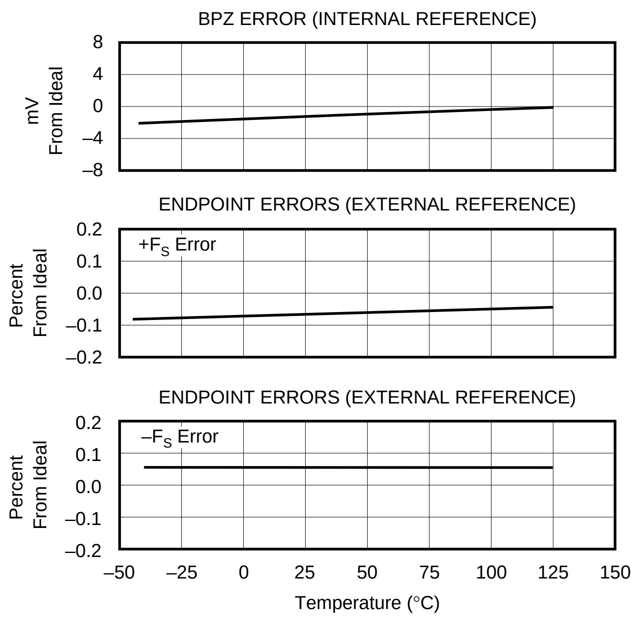




T_A = +25°C, f_S = 100kHz, V_{DIG} = V_{ANA} = +5V, using internal reference and fixed resistors shown in Figure 6b, unless otherwise specified.







BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7805 with a full parallel data output. Taking R/$\overline{\text{C}}$ (pin 24) LOW for a minimum of 40ns (7µs max) will initiate a conversion. $\overline{\text{BUSY}}$ (pin 26) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on pin 6. $\overline{\text{BUSY}}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{\text{BUSY}}$ is LOW.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the "Calibration" section).

STARTING A CONVERSION

The combination of $\overline{\text{CS}}$ (pin 25) and R/$\overline{\text{C}}$ (pin 24) LOW for a minimum of 40ns immediately puts the sample-and-hold of the ADS7805 in the hold state and starts conversion 'n'. $\overline{\text{BUSY}}$ (pin 26) will go LOW and stay LOW until conversion 'n' is completed and the internal output register has been updated. All new convert commands during $\overline{\text{BUSY}}$ LOW will be ignored. $\overline{\text{CS}}$ and/or R/$\overline{\text{C}}$ must go HIGH before $\overline{\text{BUSY}}$ goes HIGH or a new conversion will be initiated without sufficient time to acquire a new signal.

The ADS7805 will begin tracking the input signal at the end of the conversion. Allowing 10µs between convert commands assures accurate acquisition of a new signal. Refer to Table II for a summary of $\overline{\text{CS}}$, R/$\overline{\text{C}}$, and $\overline{\text{BUSY}}$ states and Figures 3 through 5 for timing diagrams.

$\overline{\text{CS}}$ and R/$\overline{\text{C}}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If, however, it is critical that $\overline{\text{CS}}$ or R/$\overline{\text{C}}$ initiates conversion 'n', be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{\text{CS}}$ can be tied LOW using R/$\overline{\text{C}}$ to control the read and convert modes. This will have no effect when using the internal data clock in the serial output mode. However, the parallel output will become active whenever R/$\overline{\text{C}}$ goes HIGH. Refer to the "Reading Data" section.

$\overline{\text{CS}}$	R/$\overline{\text{C}}$	$\overline{\text{BUSY}}$	OPERATION
1	X	X	None. Databus is in Hi-Z state.
↓	0	1	Initiates conversion "n". Databus remains in Hi-Z state.
0	↓	1	Initiates conversion "n". Databus enters Hi-Z state.
0	1	↑	Conversion "n" completed. Valid data from conversion "n" on the databus.
↓	1	1	Enables databus with valid data from conversion "n".
↓	1	0	Enables databus with valid data from conversion "n-1"(1). Conversion n in progress.
0	↑	0	Enables databus with valid data from conversion "n-1"(1). Conversion "n" in progress.
0	0	↑	New conversion initiated without acquisition of a new signal. Data will be invalid. $\overline{\text{CS}}$ and/or R/$\overline{\text{C}}$ must be HIGH when $\overline{\text{BUSY}}$ goes HIGH.
X	X	0	New convert commands ignored. Conversion "n" in progress.

NOTE: (1) See Figures 3 and 4 for constraints on data valid from conversion "n-1".

Table II. Control Line Functions for "Read" and "Convert".

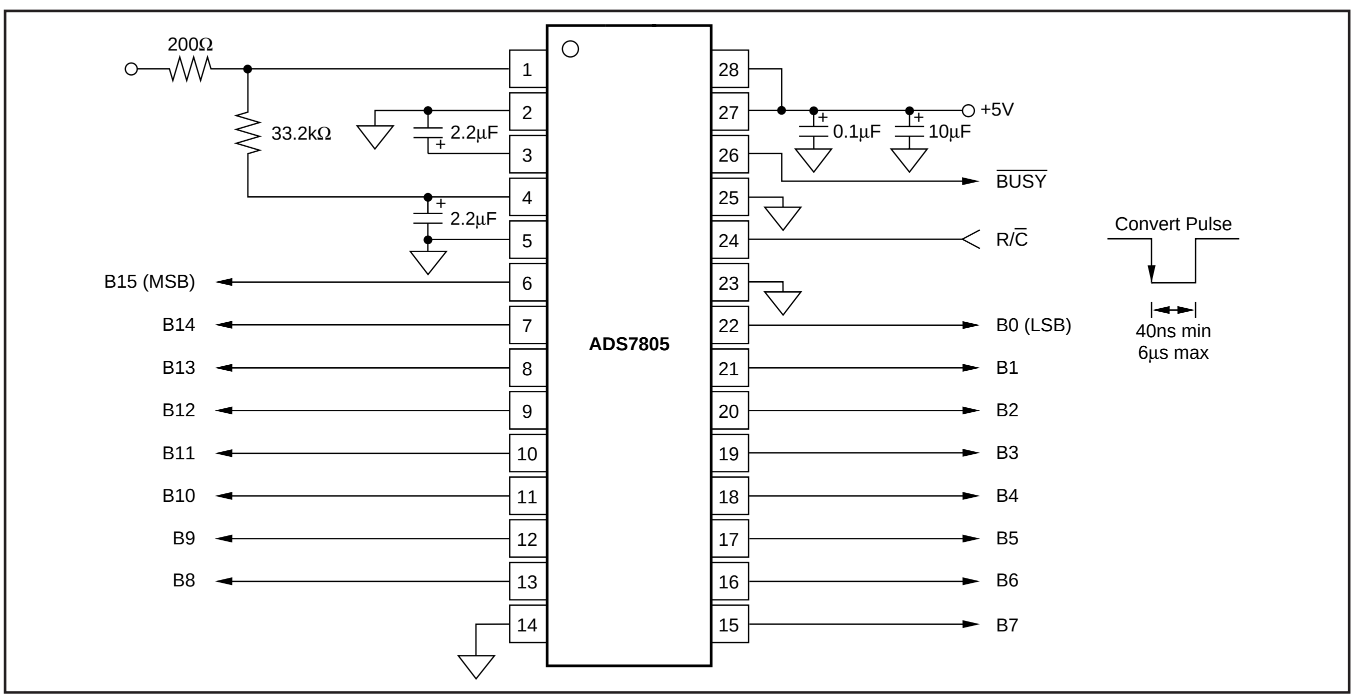


FIGURE 1. Basic Operation.

READING DATA

The ADS7805 outputs full or byte-reading parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 24) is HIGH and $\overline{CS}$ (pin 25) is LOW. Any other combination of $\overline{CS}$ and R/$\overline{C}$ will tri-state the parallel output. Valid conversion data can be read in a full parallel, 16-bit word or two 8-bit bytes on pins 6-13 and pins 15-22. BYTE (pin 23) can be toggled to read both bytes within one conversion cycle. Refer to Table III for ideal output codes and Figure 2 for bit locations relative to the state of BYTE.

DESCRIPTION	ANALOG INPUT	DIGITAL OUTPUT BINARY TWO'S COMPLEMENT	
		BINARY CODE	HEX CODE
Full-Scale Range	±10V		
Least Significant Bit (LSB)	305µV		
+Full Scale (10V – 1LSB)	9.999695V	0111 1111 1111 1111	7FFF
Mid-scale	0V	0000 0000 0000 0000	0000
One LSB below Mid-scale	–305µV	1111 1111 1111 1111	FFFF
–Full Scale	–10V	1000 0000 0000 0000	8000

Table III. Ideal Input Voltages and Output Codes.

PARALLEL OUTPUT (After a Conversion)

After conversion 'n' is completed and the output registers have been updated, $\overline{BUSY}$ (pin 26) will go HIGH. Valid data from conversion 'n' will be available on D15-D0 (pins 6-13 and 15-22). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table IV and Figures 3 to 5 for timing specifications.

PARALLEL OUTPUT (During a Conversion)

After conversion 'n' has been initiated, valid data from conversion 'n – 1' can be read and will be valid up to 7µs after the start of conversion 'n'. Do not attempt to read data from 7µs after the start of conversion 'n' until $\overline{BUSY}$ (pin 26) goes HIGH; this may result in reading invalid data. Refer to Table IV and Figures 3 to 5 for timing specifications.

Note! For the best possible performance, data should not be read during a conversion. The switching noise of the asynchronous data transfer can cause digital feedthrough degrading the converter's performance.

The number of control lines can be reduced by tying $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter (see Figure 3).

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		7000	ns
t_2	Data Valid Delay after R/$\overline{C}$ LOW			8	µs
t_3	$\overline{BUSY}$ Delay from R/$\overline{C}$ LOW			65	ns
t_4	$\overline{BUSY}$ LOW			8	µs
t_5	$\overline{BUSY}$ Delay after End of Conversion		220		ns
t_6	Aperture Delay		40		ns
t_7	Conversion Time		7.6	8	µs
t_8	Acquisition Time			2	µs
t_9	Bus Relinquish Time	10	35	83	ns
t_{10}	$\overline{BUSY}$ Delay after Data Valid	50	200		ns
t_{11}	Previous Data Valid after R/$\overline{C}$ LOW		7.4		µs
$t_7 + t_6$	Throughput Time		9	10	µs
t_{12}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{13}	Time Between Conversions	10			µs
t_{14}	Bus Access Time and BYTE Delay	10		83	ns

TABLE IV. Conversion Timing.

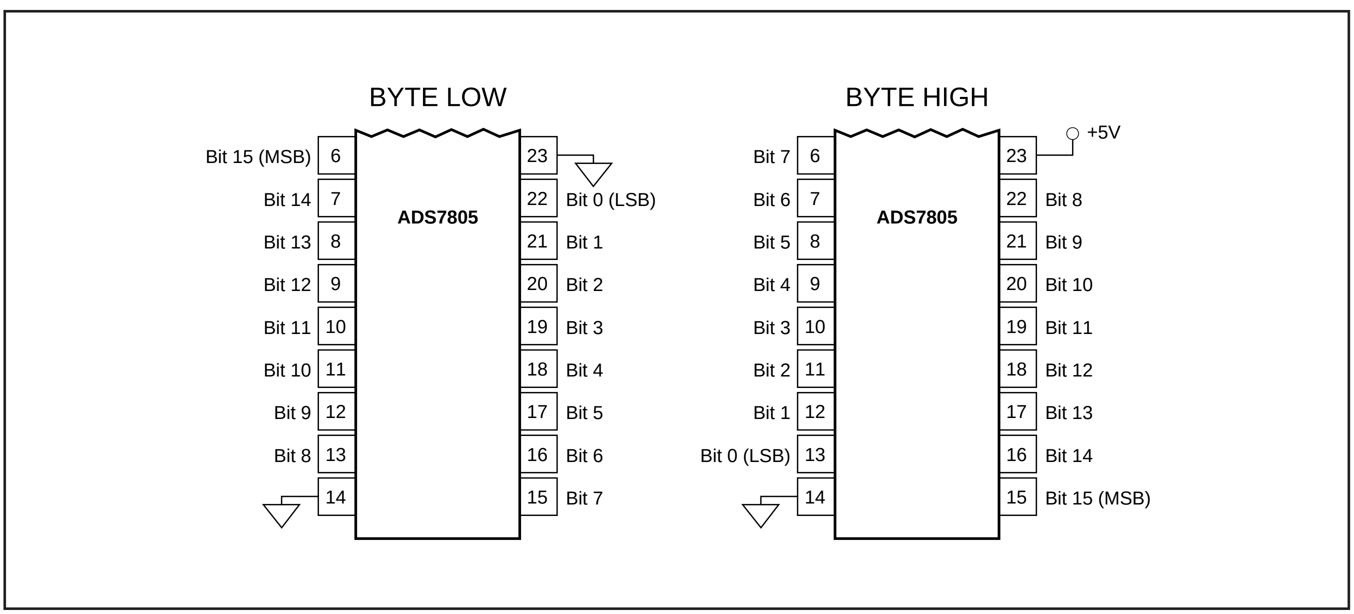


FIGURE 2. Bit Locations Relative to State of BYTE (pin 23).

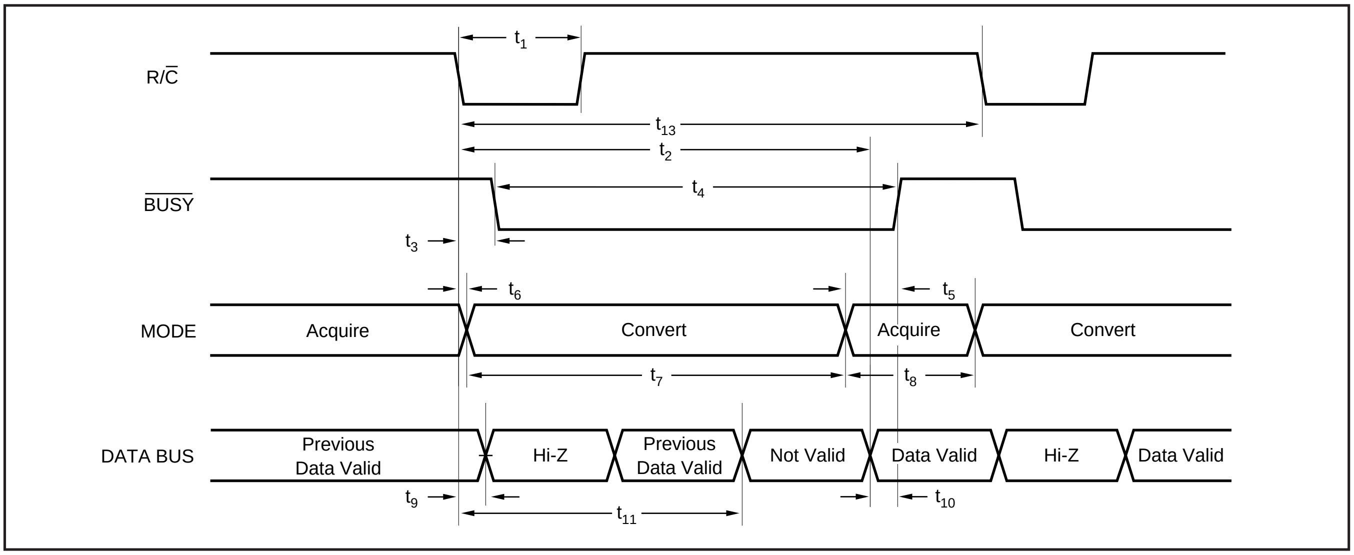


FIGURE 3. Conversion Timing with Outputs Enabled after Conversion ($\overline{CS}$ Tied LOW).

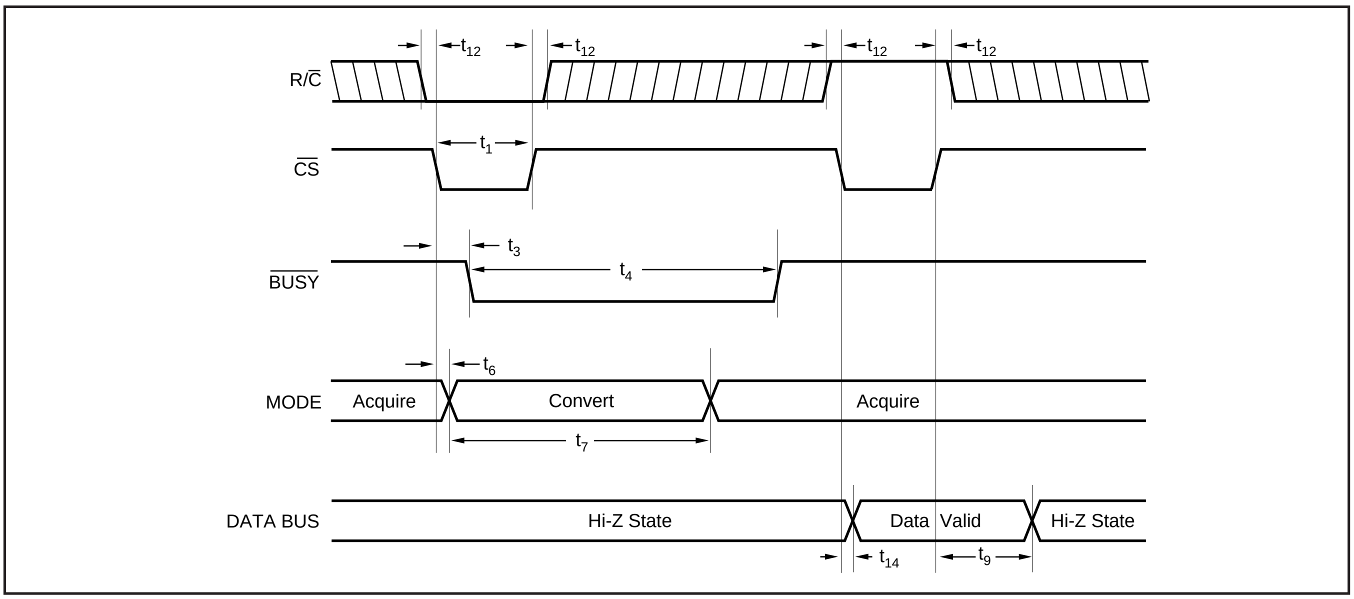


FIGURE 4. Using $\overline{CS}$ to Control Conversion and Read Timing.

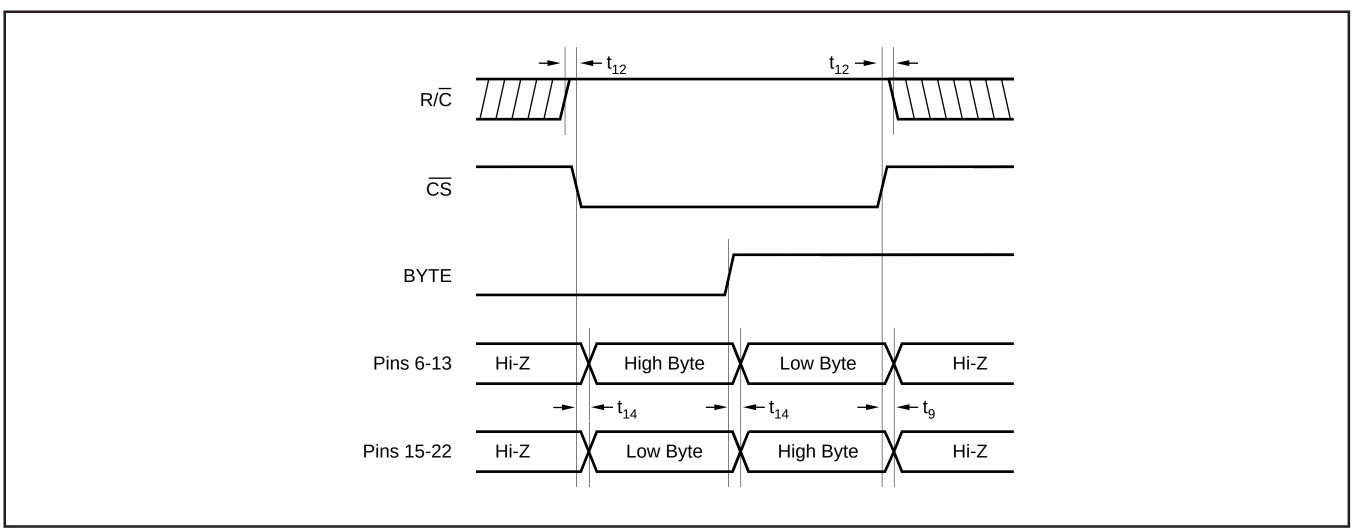


FIGURE 5. Using $\overline{CS}$ and BYTE to Control Data Bus.

INPUT RANGES

The ADS7805 offers a standard ±10V input range. Figure 6 shows the necessary circuit connections for the ADS7805 with and without hardware trim. Offset and full-scale error(1) specifications are tested and specified with the fixed resistors shown in Figure 6b. Adjustments for offset and gain are described in the "Calibration" section of this data sheet.

The offset and gain are adjusted internally to allow external trimming with a single supply. The external resistors compensate for this adjustment and can be left out if the offset and gain will be corrected in software (refer to the "Calibration" section).

The nominal input impedance of 23kΩ results from the combination of the internal resistor network shown on the front page of the product data sheet and the external resistors. The input resistor divider network provides inherent overvoltage protection ensured to at least ±25V. The 1% resistors used for the external circuitry do not compromise the accuracy or drift of the converter. They have little influence relative to the internal resistors, and tighter tolerances are not required.

NOTE: (1) Full-scale error includes offset and gain errors measured at both +FS and –FS.

CALIBRATION

The ADS7805 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain. To achieve optimum performance, several iterations may be required.

HARDWARE CALIBRATION

To calibrate the offset and gain of the ADS7805, install the proper resistors and potentiometers as shown in Figure 6a. The calibration range is ±15mV for the offset and ±60mV for the gain.

SOFTWARE CALIBRATION

To calibrate the offset and gain of the ADS7805 in software, no external resistors are required. See the "No Calibration" section for details on the effects of the external resistors. Range of offset and gain errors with and without external resistors is shown in Table V.

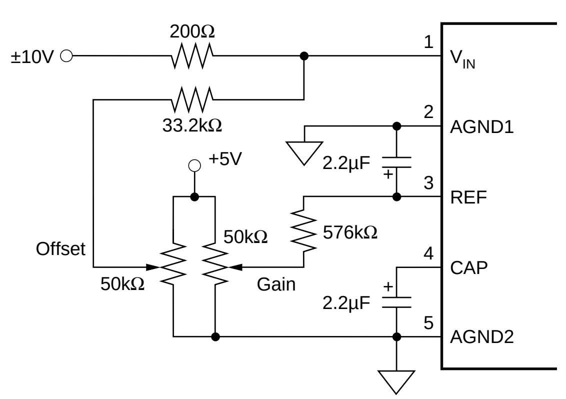
NO CALIBRATION

Figure 6b shows circuit connections. The external resistors shown in Figure 6b may not be necessary in some applications. These resistors provide compensation for an internal adjustment of the offset and gain which allows calibration with a single supply. The nominal transfer function of the ADS7805 will be bound by the shaded region (see Figure 7) with a typical offset of –30mV and a typical gain error of –1.5%. Refer to Table V for range of offset and gain errors with and without external resistors.

	WITH EXTERNAL RESISTORS	WITHOUT EXTERNAL RESISTORS	UNITS
BP0	–10 < BPO < 10 –30 < BPO < 30	–50 < BPO < –15 –150 < BPO < –45	mV LSBs
Gain Error	–0.5 < error < 0.5	–2 < error < –1	% of FSR

TABLE V. Offset and Gain Errors With and Without External Resistors.

a) ±10V With Hardware Trim



NOTE: Use 1% metal film resistors.

b) ±10V Without Hardware Trim

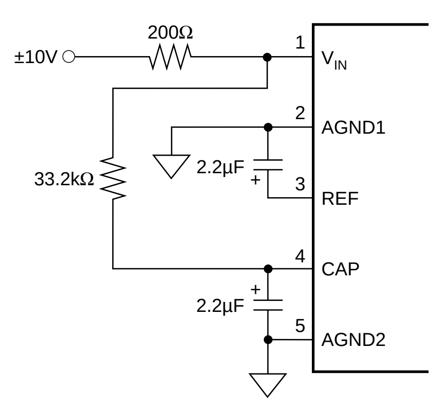


FIGURE 6. Circuit Diagram With and Without External Resistors.

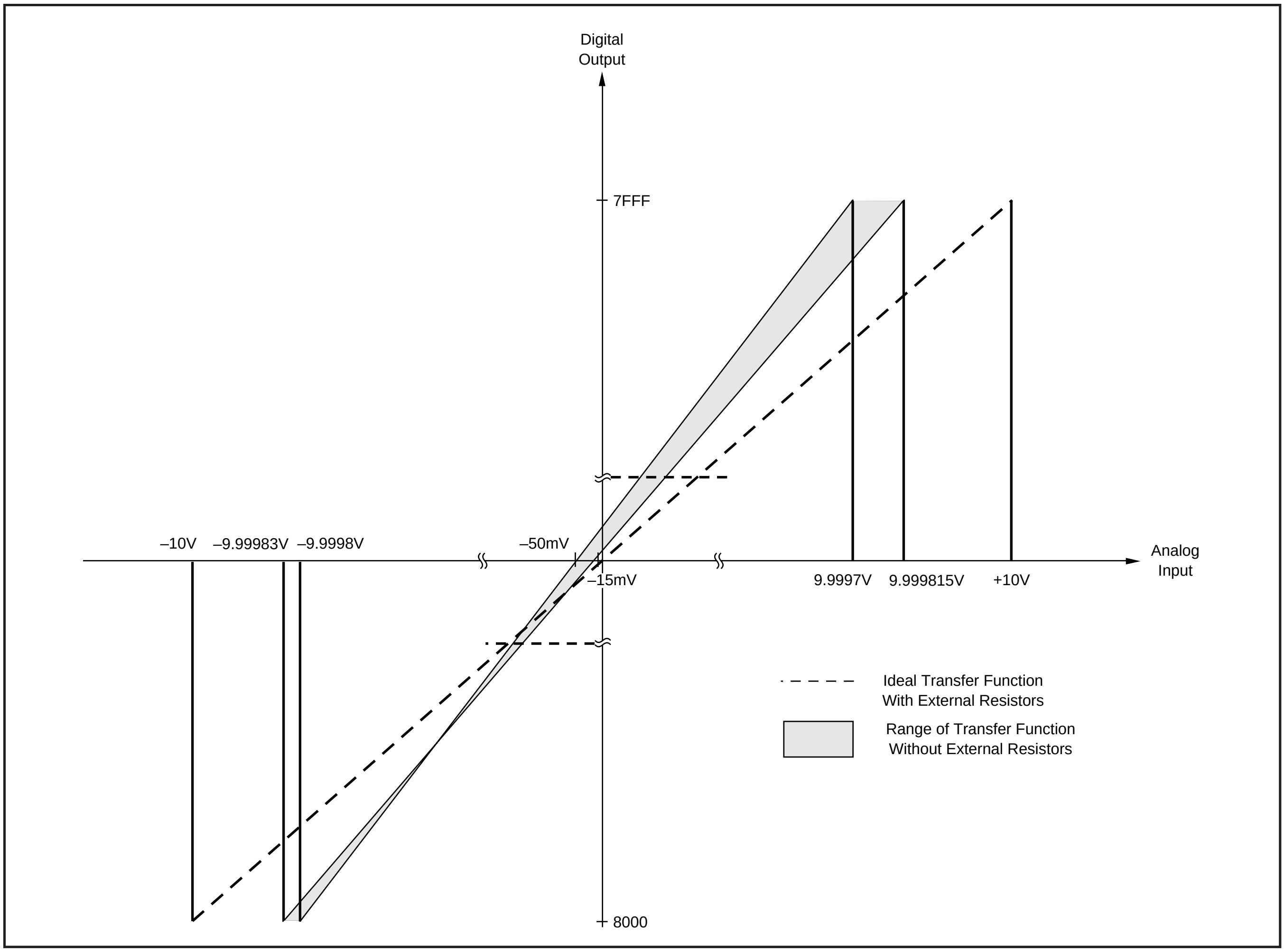


FIGURE 7. Full-Scale Transfer Function.

REFERENCE

The ADS7805 can operate with its internal 2.5V reference or an external reference. By applying an external reference to pin 5, the internal reference can be bypassed. The reference voltage at REF is buffered internally with the output on CAP (pin 4).

The internal reference has an 8 ppm/°C drift (typical) and accounts for approximately 20% of the full-scale error (FSE = ±0.5% for low grade, ±0.25% for high grade).

REF

REF (pin 3) is an input for an external reference or the output for the internal 2.5V reference. A 2.2µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low-pass filter to bandlimit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

The range for the external reference is 2.3V to 2.7V and determines the actual LSB size. Increasing the reference voltage will increase the full-scale range and the LSB size of the converter which can improve the SNR.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 2.2µF capacitor should be placed as close to the CAP pin as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the internal buffer. Using a capacitor any smaller than 1µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 2.2µF will have little effect on improving performance.

The output of the buffer is capable of driving up to 2mA of current to a DC load. DC loads requiring more than 2mA of current from the CAP pin will begin to degrade the linearity of the ADS7805. Using an external buffer will allow the internal reference to be used for larger DC loads and AC loads. Do not attempt to directly drive an AC load with the output voltage on CAP. This will cause performance degradation of the converter.

LAYOUT

POWER

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the electrical specifications, the ADS7805 uses 90% of its power for the analog circuitry. The ADS7805 should be considered as an analog component.

The +5V power for the A/D converter should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 28) directly to a digital supply can reduce converter performance due to switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7805. DGND is the digital supply ground. AGND2 is the analog supply ground. AGND1 is the ground which all analog signals internal to the A/D converter are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the A/D converter should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample-and-hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7805, compared to the FET switches on other CMOS A/D converters, releases 5%-10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the anti-alias filter on the front end. Any op amp sufficient for the signal in an application will be sufficient to drive the ADS7805.

The resistive front end of the ADS7805 also provides an ensured ±25V overvoltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7805 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversion, the tri-state outputs can be used to isolate the A/D converter from other peripherals on the same bus. Tri-state outputs can also be used when the A/D converter is the only peripheral on the data bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7805 has an internal LSB size of 38µV. Transients from fast switching signals on the parallel port, even when the A/D converter is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/06	D	3	Absolute Maximum Ratings	CAP and REF were switched.
8/06	C	2	Package/Ordering Information	Corrected typos in ordering table.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7805U	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		ADS7805U B	Samples
ADS7805U/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		ADS7805U B	Samples
ADS7805U/1KE4	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-25 to 85	ADS7805U B	Samples
ADS7805UB	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		ADS7805U B	Samples
ADS7805UB/1K	ACTIVE	SOIC	DW	28	1000	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		ADS7805U B	Samples
ADS7805UBE4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR	-25 to 85	ADS7805U B	Samples
ADS7805UBG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		ADS7805U B	Samples
ADS7805UG4	ACTIVE	SOIC	DW	28	20	Green (RoHS & no Sb/Br)	NIPDAU-DCC	Level-3-260C-168 HR		ADS7805U B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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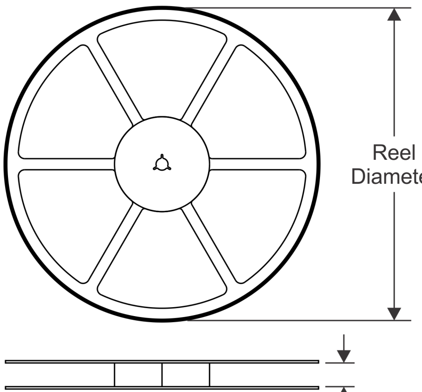
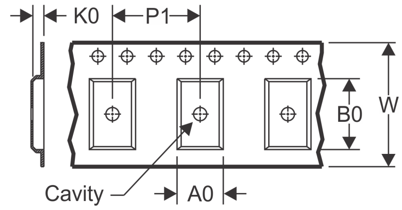
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

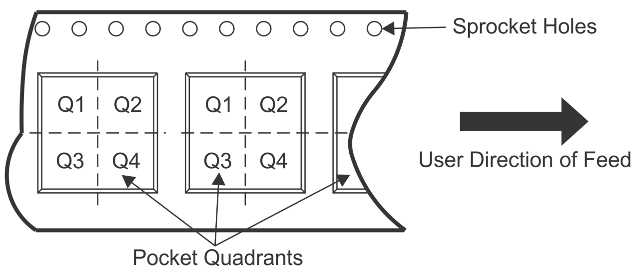


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

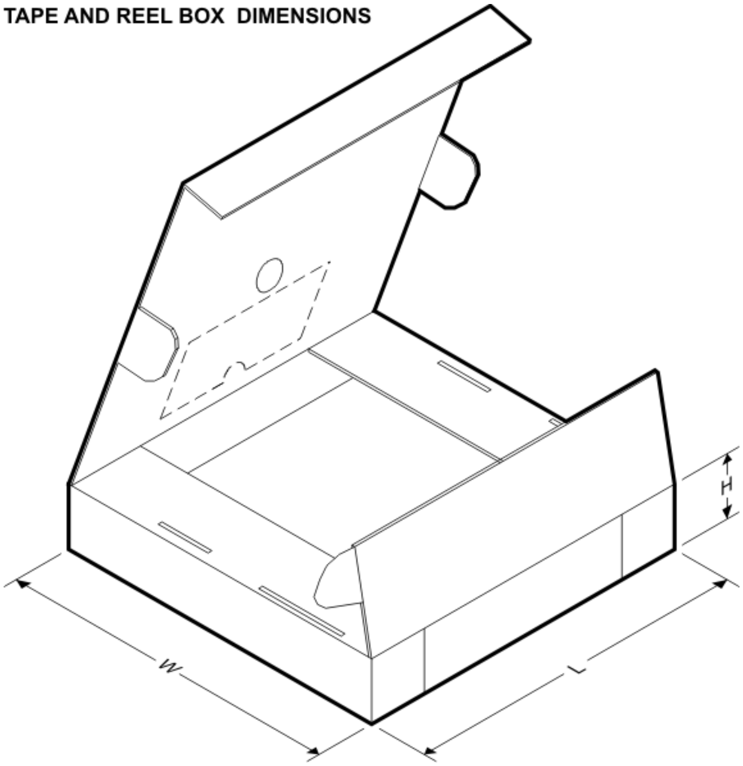
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7805U/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
ADS7805UB/1K	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

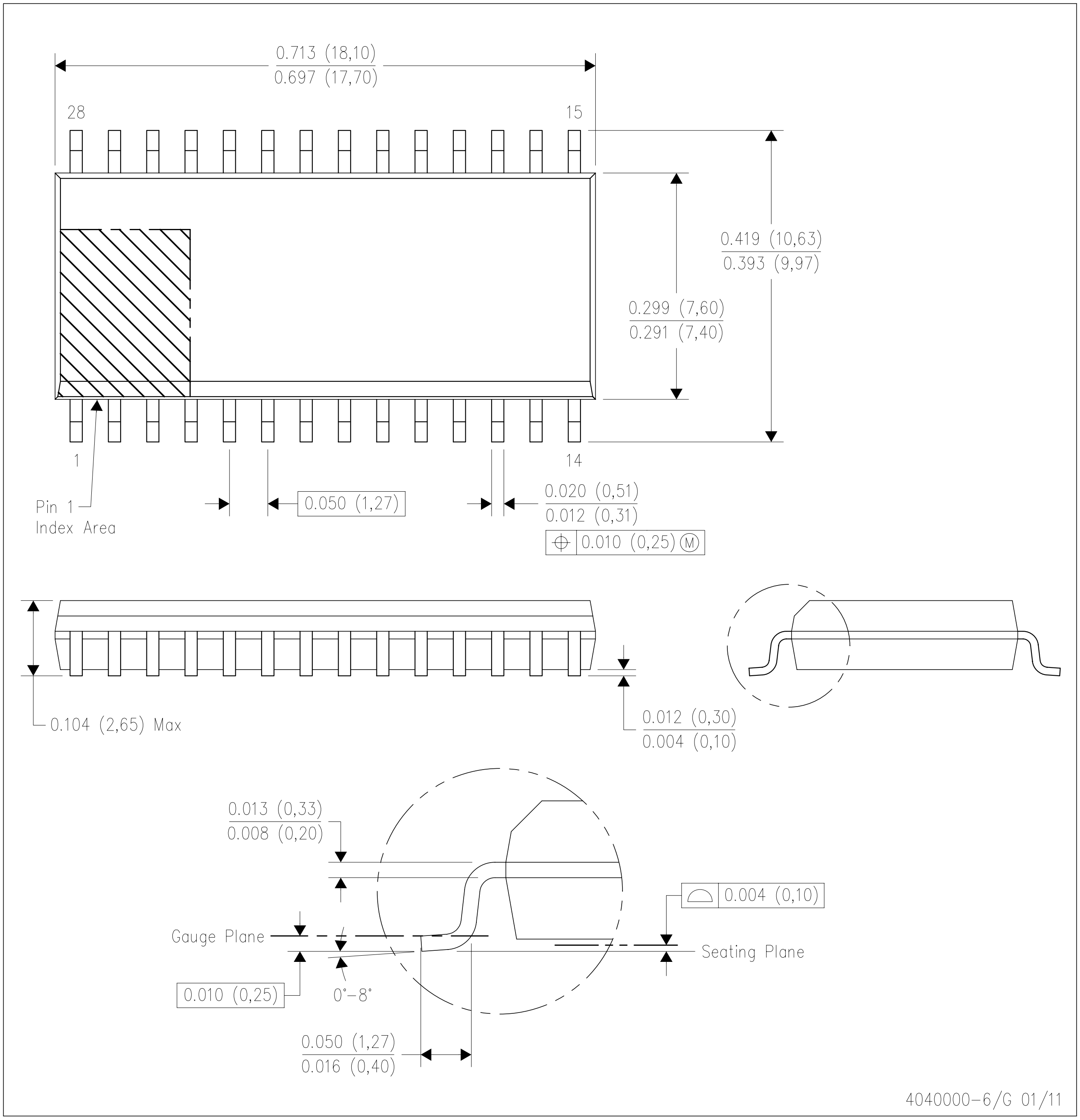
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

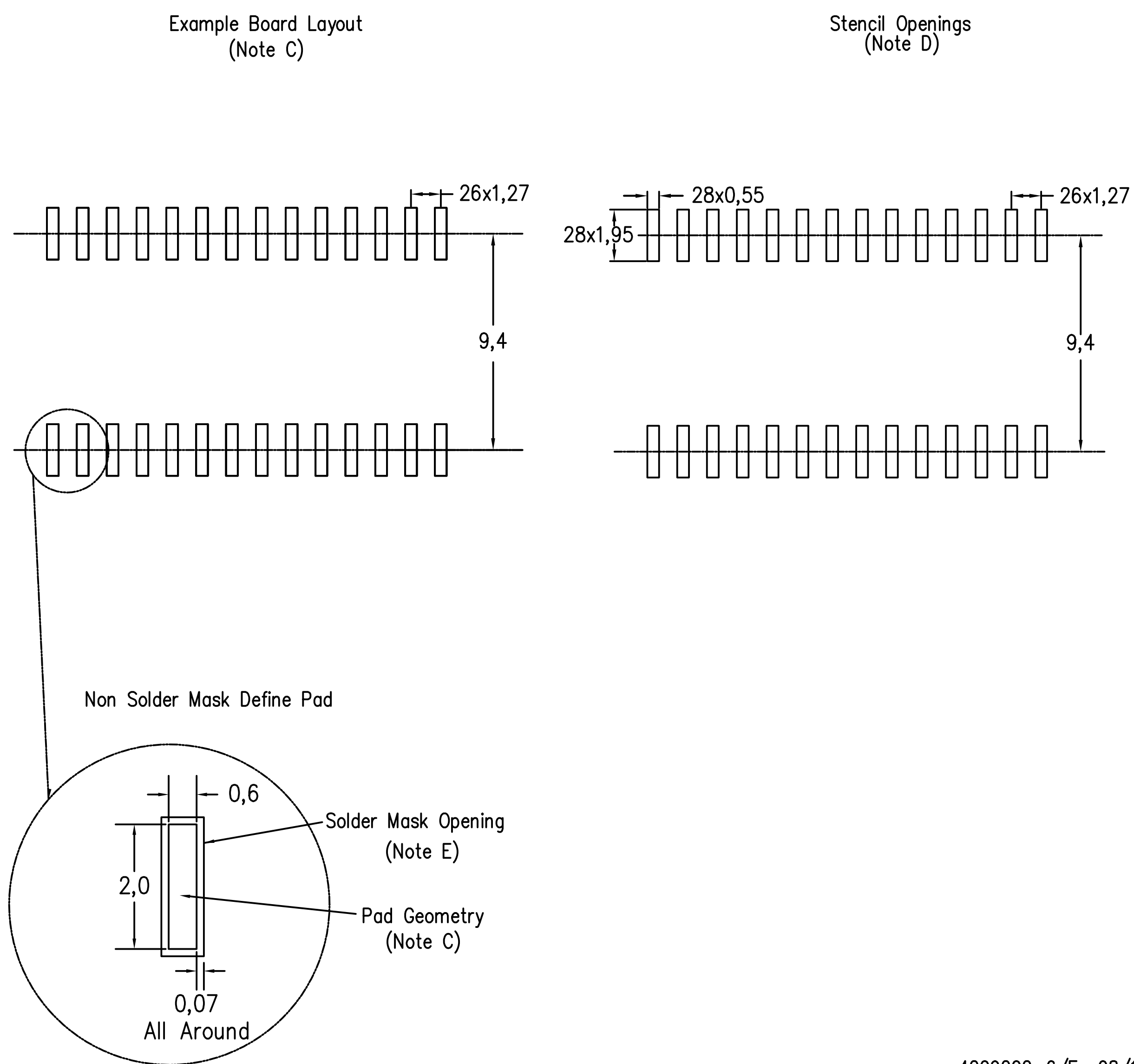
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7805U/1K	SOIC	DW	28	1000	350.0	350.0	66.0
ADS7805UB/1K	SOIC	DW	28	1000	350.0	350.0	66.0

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AE.

DW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.