Dual, 1.5MSPS, 12-Bit, 2 + 2 Channel, Simultaneous Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **Four Fully- or Six Pseudo-Differential Inputs**
- **SINAD: 70dB (min), THD: –75dB (max)**
- **Programmable and Buffered Internal 2.5V Reference**
- **Flexible Power-Down Features**
- **Variable Power Supply Ranges**
- **Low Power Operation: 40mW at 5V**
- **Operating Temperature Range: –40°C to +125°C**
- **Pin-Compatible with ADS7861 and ADS8361 (SSOP package)**

APPLICATIONS

- **Motor Control**
- **Multi-Axis Positioning Systems**
- **Three-Phase Power Control**

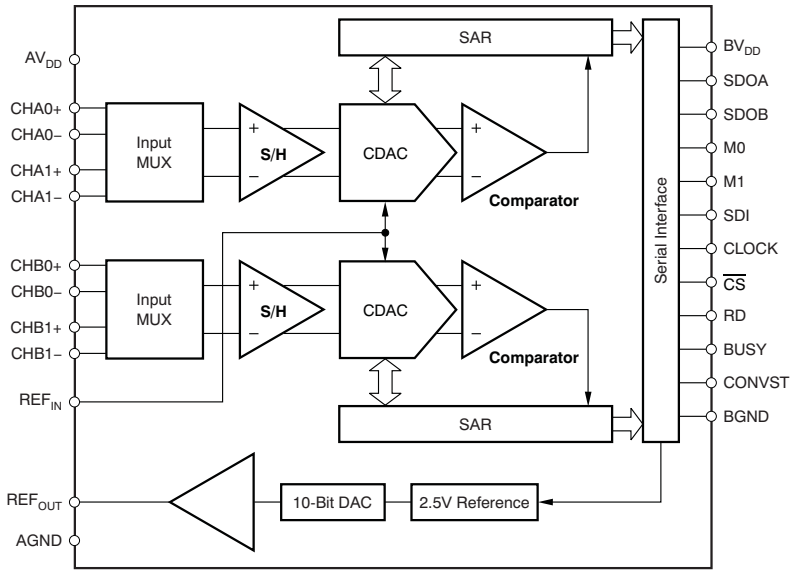
DESCRIPTION

The ADS7863 is a dual, 12-bit, 1.5MSPS, analog-to-digital converter (ADC) with four fully differential input channels grouped into two pairs for high-speed, simultaneous signal acquisition. Inputs to the sample-and-hold (S/H) amplifiers are fully differential and are maintained differential to the input of the ADC. This architecture provides excellent common-mode rejection of 80dB at 50kHz, which is a critical performance characteristic in noisy environments.

The ADS7863 is pin-compatible with the ADS8361, but offers additional features such as a programmable reference output, flexible supply voltage (2.7V to 5.5V for AV_{DD} and 1.65V to 5.5V for BV_{DD}), a pseudo-differential input multiplexer with three channels per ADC, and several power-down features.

The high-speed, dual serial interface is also pin-compatible with the ADS7861 while offering additional flexibility. The ADS7863 is offered in an SSOP-24 and a 4x4mm QFN-24 package. It is specified over the extended operating temperature range of –40°C to +125°C.

PRODUCT PREVIEW



Functional Block Diagram

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7863I	SSOP-24	DBQ	ADS7863IDBQ	Tube, 56
			ADS7863IDBQR	Tape and Reel, 2500
	4x4 QFN-24	RGE	ADS7863IRGE	Tape and Reel, 250
			ADS7863IRGER	Tape and Reel, 3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document or see the TI web site at www.ti.com

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

	ADS7863	UNIT
Supply voltage, AV_{DD} to AGND	–0.3 to +6	V
Supply voltage, BV_{DD} to BGND	–0.3 to +6	V
Supply voltage, BV_{DD} to AV_{DD}	$1.5 \times AV_{DD}$	V
Analog and reference input voltage with respect to AGND	AGND – 0.3 to AV_{DD} + 0.3	V
Digital input voltage with respect to BGND	BGND – 0.3 to BV_{DD} + 0.3	V
Ground voltage difference |AGND – BGND|	+0.3	V
Input current to any pin except supply pins	–10 to +10	mA
Operating virtual junction temperature range, T_J	–40 to +150	°C
Storage temperature range, T_{STG}	–65 to +150	°C
Lead temperature 1.6mm (1/16in) from case for 10s	+250	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range, unless otherwise noted.

PARAMETER		ADS7863			UNIT
		MIN	NOM	MAX	
Supply voltage, AV_{DD} to AGND		2.7	5.0	5.5	V
Supply voltage, BV_{DD} to BGND	Low voltage levels	1.65		3.6	V
	5V logic levels	4.5	5.0	5.5	
Reference input voltage on REF_{IN}		0.5	2.5	2.525	V
Analog differential input voltage (CHxx+) – (CHxx–)		$–V_{REF}$		$+V_{REF}$	mV
Operating ambient temperature range, T_A		–40		+125	°C

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING	T_A = +125°C POWER RATING
SSOP-24	10mW/°C	1250mW	800mW	650mW	250mW
QFN-24 (4mm x 4mm)	22mW/°C	2740mW	1750mW	1420mW	540mW

THERMAL CHARACTERISTICS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			SSOP-24	QFN-24	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance	99.8	45.6	°C/W
		High-K thermal resistance	61.0	33.1	
θ_{JC}	Junction-to-case thermal resistance		23.3	35	°C/W
P_{DISS}	Device power dissipation at 5V		40	40	mW

(1) Tested in accordance with the Low-K or High-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +125°C, and AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = 2.5V (internal), f_{CLK} = 24MHz, and f_{SAMPLE} = 1.5MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7863 MIN	ADS7863 TYP(1)	ADS7863 MAX	UNIT
RESOLUTION			12			Bits
ANALOG INPUT						
FSR	Full-scale differential input range	(CHxx+) – (CHxx–)	$–V_{REF}$		$+V_{REF}$	V
V_{IN}	Absolute input voltage	CHxx+ or CHxx+ to AGND	–0.1		AV_{DD} + 0.1	V
C_{IN}	Input capacitance	CHxx+ or CHxx– to AGND		2		pF
C_{ID}	Differential input capacitance			4		pF
I_{IL}	Input leakage current		–1		+1	nA
CMRR	Common-mode rejection ratio			80		dB
DC ACCURACY						
INL	Integral nonlinearity		–1		+1	LSB
INL match						LSB
DNL	Differential nonlinearity(2)		–1		+1	LSB
DNL match						LSB
V_{OS}	Input offset error		–1		+1	LSB
V_{OS} match		Asynchronous to Synchronous				LSB
dV_{OS}/dT	Input offset thermal drift					µV/°C
G_{ERR}	Gain error(2)				0.25	%
G_{ERR} match						%
G_{ERR}/dT	Gain error thermal drift					ppm/°C
PSRR	Power-supply rejection ratio	2.7V < AV_{DD} < 5.5V		70		dB
AC ACCURACY						
SINAD	Signal-to-noise + distortion	V_{IN} = $5V_{PP}$ at 100kHz	70			dB
SNR	Signal-to-noise ratio	V_{IN} = $5V_{PP}$ at 100kHz				dB
THD	Total harmonic distortion	V_{IN} = $5V_{PP}$ at 100kHz			–75	dB
SFDR	Spurious-free dynamic range	V_{IN} = $5V_{PP}$ at 100kHz	75			dB
SAMPLING DYNAMICS						
t_{CONV}	Conversion time per ADC	1MHz < f_{CLK} ≤ 24MHz	0.542		13	µs
t_{ACQ}	Acquisition time		125			ns
t_{DATA}	Throughput rate	1MHz < f_{CLK} ≤ 24MHz	62.5		1500	kSPS
t_A	Aperture delay				6	ns
t_A match				50		ps
t_{AJIT}	Aperture jitter			50		ps
f_{CLK}	Clock frequency on CLOCK		1		24	MHz
INTERNAL VOLTAGE REFERENCE						
Resolution	Reference output DAC resolution		10			Bits
V_{REFOUT}	Reference output voltage	Over 20%...100% DAC range	0.496		2.520	V
		DAC = 0x3FF, –40°C < T_A < +125°C	2.480	2.500	2.520	V
		DAC = 0x3FF at +25°C	2.485	2.500	2.515	V
dV_{REFOUT}/dT	Reference voltage drift			±10		ppm/°C
DNL_{DAC}	DAC differential nonlinearity		–9.76		9.76	mV
			–4		4	LSB
INL_{DAC}	DAC integral nonlinearity		–9.76		9.76	mV
			–4		4	LSB
V_{OSDAC}	DAC offset error	V_{REFOUT} = 0.5V			9.76	mV
					4	LSB

(1) All typical values at T_A = +25°C.
(2) Ensured by design, not production tested.

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ELECTRICAL CHARACTERISTICS (continued)

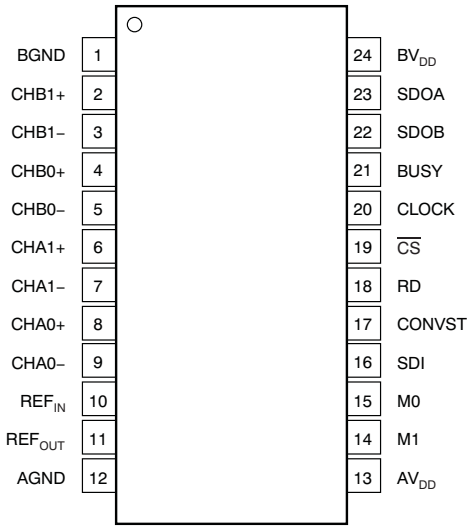
At T_A = –40°C to +125°C, and AV_{DD} = 5V, BV_{DD} = 3.3V, V_{REF} = 2.5V (internal), f_{CLK} = 24MHz, and f_{SAMPLE} = 1.5MSPS, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7863			UNIT
			MIN	TYP(1)	MAX	
INTERNAL VOLTAGE REFERENCE, continued						
PSRR	Power-supply rejection ratio					dB
I_{REFOUT}	Reference output dc current				1	mA
I_{REFSC}	Reference output short-circuit current					mA
t_{REFON}	Reference output settling time				100	µs
VOLTAGE REFERENCE INPUT						
V_{REF}	Reference input voltage range		0.5	2.5	2.525	V
I_{REF}	Reference input current			50		µA
C_{REF}	Reference input capacitance			10		pF
DIGITAL INPUTS						
Logic family				CMOS		
V_{IH}	High-level input voltage		0.7 × BV_{DD}		BV_{DD} + 0.3	V
V_{IL}	Low-level input voltage		–0.3		0.3 × BV_{DD}	V
I_{IN}	Input current	V_{IN} = BV_{DD} to BGND	–50		+50	nA
C_{IN}	Input capacitance			5		pF
DIGITAL OUTPUTS						
Logic family				CMOS		
V_{OH}	High-level output voltage	I_{OH} = –100µA	BV_{DD} – 0.2			V
V_{OL}	Low-level output voltage	I_{OH} = 100µA			0.2	V
I_{OZ}	High-impedance-state output current	V_{IN} = BV_{DD} to BGND	–50		+50	nA
C_{OUT}	Output capacitance			5		pF
C_{LOAD}	Load capacitance				30	pF
POWER SUPPLY						
AV_{DD}	Analog supply voltage	AV_{DD} to AGND	2.7	5.0	5.5	V
BV_{DD}	Buffer I/O supply voltage	BV_{DD} to BGND	1.65	3.3	5.5	V
AI_{DD}	Analog supply current	AV_{DD} = 3V		6	7	µA
		AV_{DD} = 5.5V		7	8	
		AV_{DD} = 3V, NAP power-down				
		AV_{DD} = 5.5V, NAP power-down				
		AV_{DD} = 3V, deep power-down				
		AV_{DD} = 5.5V, deep power-down				
BI_{DD}	Buffer I/O supply current					µA
P_{DISS}	Power dissipation	AV_{DD} = 3V			18.9	µW
		AV_{DD} = 5.5V			40	

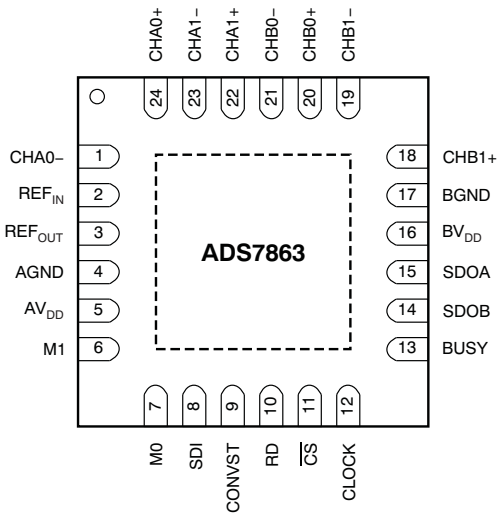
PRODUCT PREVIEW

DEVICE INFORMATION

ADS7863IDBQ
SSOP-24 (DBQ)
(TOP VIEW)



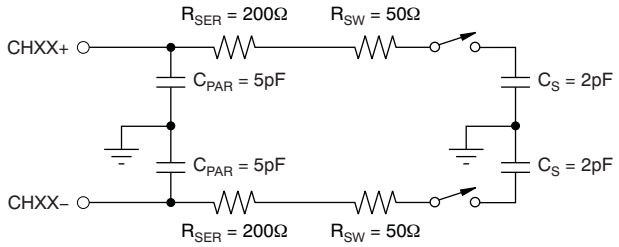
ADS7863IRG
4 x 4 QFN-24 (RGE)
(TOP VIEW)



PIN DESCRIPTIONS

PIN NUMBER			
SSOP	QFN	NAME	DESCRIPTION
1	17	BGND	Buffer I/O ground. Connect to digital ground plane.
2	18	CHB1+	Noninverting analog input channel B1
3	19	CHB1–	Inverting analog input channel B1
4	20	CHB0+	Noninverting analog input channel B0
5	21	CHB0–	Inverting analog input channel B0
6	22	CHA1+	Noninverting analog input channel A1
7	23	CHA1–	Inverting analog input channel A1
8	24	CHA0+	Noninverting analog input channel A0
9	1	CHA0–	Inverting analog input channel A0
10	2	REF_{IN}	Reference voltage input. A ceramic capacitor of 470nF (min) is required at this terminal.
11	3	REF_{OUT}	Reference voltage output. The programmable internal voltage reference output is available on this pin.
12	4	AGND	Analog ground. Connect to analog ground plane.
13	5	AV_{DD}	Analog power supply, 2.7V to 5.5V. Decouple to AGND with a 1µF ceramic capacitor.
14	6	M1	Mode pin 1. Selects between the SDOx digital outputs (see Table 7).
15	7	M0	Mode pin 0. Selects between analog input channels (see Table 7).
16	8	SDI	Serial data input. This pin allows the additional features of the ADS7863 to be used but can also be used in ADS7861-compatible manner.
17	9	CONVST	Conversion start. The ADC switches from the sample into the hold mode on the rising edge of CONVST, independent of the status of CLOCK.
18	10	RD	Read data. Synchronization pulse for the SDOx outputs and SDI input. RD only triggers when $\overline{CS}$ is low.
19	11	$\overline{CS}$	Chip select. When low, the SDOx outputs are active; when high, the SDOx outputs are tri-stated.
20	12	CLOCK	External clock input
21	13	BUSY	ADC busy indicator. BUSY goes high when the inputs are in hold mode and returns to low after the conversion has been finished.
22	14	SDOB	Serial data output for converter B. Data are valid on the falling edge of CLOCK.
23	15	SDOA	Serial data output for converter A. When M1 is high, both SDOA and SDOB are active. Data are valid on the falling edge of CLOCK.
24	16	BV_{DD}	Buffer I/O supply, 1.65V to 5.5V. Decouple to BGND with a 1µF ceramic capacitor.

Equivalent Input Circuit



TIMING CHARACTERISTICS

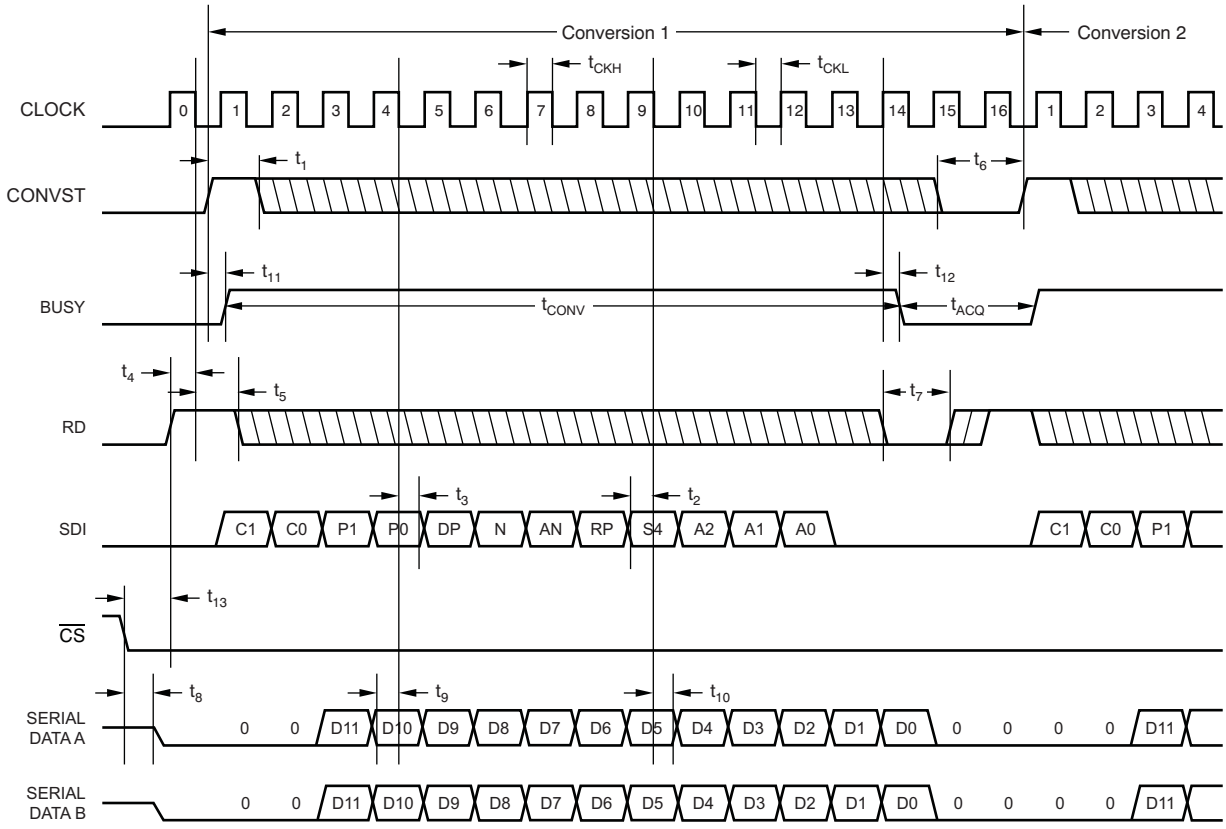
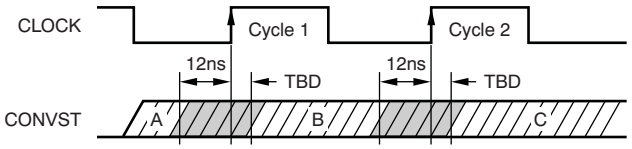


Figure 1. Detailed Timing Diagram (Mode I)

PRODUCT PREVIEW

TIMING CHARACTERISTICS (continued)



NOTE: All CONVST commands that occur more than 12ns before the rising edge of cycle '1' of the external clock (Region 'A') initiate a conversion on the rising edge of cycle '1'. All CONVST commands that occur **TBD**ns after the rising edge of cycle '1' or 12ns before the rising edge of cycle 2 (Region 'B') initiate a conversion on the rising edge of cycle '2'. All CONVST commands that occur **TBD**ns after the rising edge of cycle '2' (Region 'C') initiate a conversion on the rising edge of the next clock period.
The CONVST pin should never be switched from LOW to HIGH in the region 12ns prior to the rising edge of the CLOCK and **TBD**ns after the rising edge (gray areas). If CONVST is toggled in this gray area, the conversion could begin on either the same rising edge of the CLOCK or the following edge.

Figure 2. CONVST Timing

TIMING REQUIREMENTS(1)

Over recommended operating free-air temperature range at –40°C to +125°C, AV_{DD} = 5V, and BV_{DD} = 2.7V to 5V, unless otherwise noted.

SYMBOL	PARAMETER	COMMENTS	ADS7863		UNIT
			MIN	MAX	
t_{CONV}	Conversion time	f_{CLOCK} = 24MHz	541.67		ns
t_{ACQ}	Acquisition time	f_{CLOCK} = 24MHz	125		ns
f_{CLOCK}	CLOCK frequency	See Figure 1	1	24	MHz
T_{CLOCK}	CLOCK period	See Figure 1	41.67	1000	ns
t_{CKL}	CLOCK low time	See Figure 1	5		ns
t_{CKH}	CLOCK high time	See Figure 1	5		ns
t_1	CONVST high time	See Figure 1	15		ns
t_2	SDI setup time to CLOCK falling edge	See Figure 1	10		ns
t_3	SDI hold time to CLOCK falling edge	See Figure 1	5		ns
t_4	RD high setup time to CLOCK falling edge	See Figure 1	10		ns
t_5	RD high hold time to CLOCK falling edge	See Figure 1	5		ns
t_6	CONVST low time	See Figure 1	15		ns
t_7	RD low time relative to CLOCK falling edge	See Figure 1	15		ns
t_8	$\overline{CS}$ low to SDOx valid	See Figure 1	20		ns
t_9	SDOx data setup time to CLOCK falling edge	See Figure 1		25	ns
t_{10}	SDOx data hold time to CLOCK falling edge	See Figure 1	5		ns
t_{11}	CONVST setup time to rising edge of CLOCK	See Figure 1	12		ns
t_{12}	CLOCK rising edge to BUSY low delay	See Figure 1	3		ns
t_{13}	$\overline{CS}$ low to RD high delay	See Figure 1	10		ns

(1) All input signals are specified with $t_R = t_F$ = 1.5ns (10% to 90% of BV_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

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TYPICAL CHARACTERISTICS

At T_A = +25°C, $+V_A$ + V_D = +5V, and V_{REF} = 2.5V (internal), f_{CLK} = 8MHz, and f_{SAMPLE} = 2MHz, unless otherwise noted.

NEED TITLE vs NEED TITLE

Figure 3.

NEED TITLE vs NEED TITLE

Figure 4.

NEED TITLE vs NEED TITLE

Figure 5.

NEED TITLE vs NEED TITLE

Figure 6.

NEED TITLE vs NEED TITLE

Figure 7.

NEED TITLE vs NEED TITLE

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, $+V_A$ + V_D = +5V, and V_{REF} = 2.5V (internal), f_{CLK} = 8MHz, and f_{SAMPLE} = 2MHz, unless otherwise noted.

NEED TITLE vs NEED TITLE

Figure 9.

NEED TITLE vs NEED TITLE

Figure 10.

NEED TITLE vs NEED TITLE

Figure 11.

NEED TITLE vs NEED TITLE

Figure 12.

NEED TITLE vs NEED TITLE

Figure 13.

NEED TITLE vs NEED TITLE

Figure 14.

APPLICATIONS INFORMATION

GENERAL DESCRIPTION

The ADS7863 includes two 12-bit analog-to-digital converters (ADCs) that operate based on the successive-approximation register (SAR) principle. The ADCs sample and convert simultaneously. Conversion time can be as low as 541.67ns. Adding the acquisition time of 125ns results in a maximum conversion rate of 1.5MSPS.

Each ADC has a fully differential, 2:1 multiplexer front-end. In many common applications, all negative input signals remain at the same constant voltage (for example, 2.5V). In this type of application, the multiplexer can be used in a pseudo-differential 3:1 mode, where CHx0– functions as a common pin and the remaining three inputs (CHx0+, CHx1–, and CHx1+) operate as separate inputs referred to the common pin.

The ADS7863 also includes a 2.5V internal reference. The reference drives a 10-bit digital-to-analog converter (DAC), allowing the voltage at the REF_{OUT} pin to be adjusted via the serial interface in 2.44mV steps. A low-noise operational amplifier with unity gain buffers the DAC output voltage and drives the REF_{OUT} pin.

The ADS7863 offers a serial interface that is compatible with the ADS7861. However, instead of the A0 pin of the ADS7861 that controls the channel selection, the ADS7863 offers a serial data input (SDI) pin that supports additional functions described in the Digital section of this data sheet.

ANALOG

This section addresses the analog input circuit, the ADCs, and the reference design of the device.

Analog Inputs

Each ADC is fed by an input multiplexer; see Figure 15. Each multiplexer is either used in a fully-differential 2:1 configuration (as described in Table 1) or a pseudo-differential 3:1 configuration (as shown in Table 2). The channel selection is performed using bits C1 and C0 in the SDI Register (see also the Serial Data Input section).

The input path for the converter is fully differential and provides a common-mode rejection of 80dB at 50kHz. The high CMRR also helps suppress noise in harsh industrial environments.

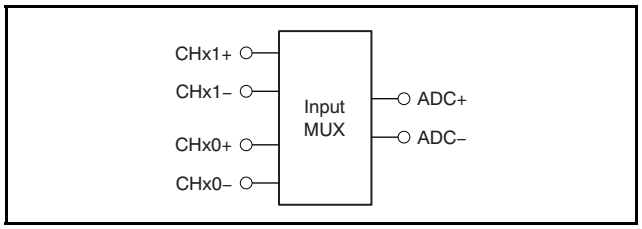

Figure 15. Input Multiplexer Configuration

Table 1. Fully Differential 2:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0+	CHx0–
1	1	CHx1+	CHx1–

Table 2. Pseudo-Differential 3:1 Multiplexer Configuration

C1	C0	ADC+	ADC–
0	0	CHx0+	CHx0–
0	1	CHx1–	CHx0–
1	1	CHx1+	CHx0–

Each of the of 2pF sample-and-hold capacitors (shown as C_S in the Equivalent Input Circuit) is connected via switches to the multiplexer output. Opening the switches holds the sampled data during the conversion process. After finishing the conversion, both capacitors are pre-charged for the duration of one clock cycle to the voltage present at the REF_{IN} pin. After the pre-charging, the multiplexer outputs are connected to the sampling capacitors again. The voltage at the analog input pin is usually different from the reference voltage; therefore, the sample capacitors must be charged to within one-half LSB for 12-bit accuracy during the acquisition time t_{ACQ} (see the Timing Characteristics).

Acquisition time is indicated with the BUSY signal being held low. It starts by closing the input switches (after finishing the previous conversion and pre-charging) and finishes with the rising edge of the CONVST signal. If the ADS7863 operates at full speed, the acquisition time is typically 125ns.

The minimum –3dB bandwidth of the driving operational amplifier can be calculated as shown in Equation 1, with *n* = 12 being the resolution of the ADS7863:

$$f_{-3dB} = \frac{\ln(2) \times (n + 1)}{2\pi \times t_{ACQ}} \quad (1)$$

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With t_{ACQ} = 125ns, the minimum bandwidth of the driving amplifier is 11.5MHz. The required bandwidth can be lower if the application allows a longer acquisition time.

A gain error occurs if a given application does not fulfill the settling requirement shown in Equation 1. As a result of precharging the capacitors, linearity and THD are not directly affected.

The OPA365 from Texas Instruments is recommended; in addition to offering the required bandwidth, it provides a low offset and also offers excellent THD performance.

The phase margin of the driving operational amplifier is usually reduced by the ADC sampling capacitor. A resistor placed between the capacitor and the amplifier limits this effect; therefore, an internal 200Ω resistor (R_{SER}) is placed in series with the switch. The switch resistance (R_{SW}) is typically 50Ω (see Equivalent Input Circuit).

The differential input voltage range of the ADC is $\pm V_{REF}$, the voltage at the REF_{IN} pin.

It is important to keep the voltage to all inputs within the 0.3V limit below AGND and above AV_{DD} while not allowing dc current to flow through the inputs. Current is only necessary to recharge the sample-and-hold capacitors.

Analog-to-Digital Converter (ADC)

The ADS7863 includes two SAR-type, 1.5MSPS, 12-bit ADCs (shown in the Functional Block Diagram on the front page of this data sheet).

CONVST

The analog inputs are held with the rising edge of the CONVST (conversion start) signal. The setup time of CONVST referred to the next rising edge of CLOCK (system clock) is 12ns (minimum). The conversion automatically starts with the rising CLOCK edge. CONVST should not be issued during a conversion, that is, when BUSY is high.

RD (read data) and CONVST can be shorted to minimize necessary software and wiring. The RD signal is triggered by the ADS7863 on the falling edge of CLOCK. Therefore, the combined signals must be activated with the rising CLOCK edge. The conversion then starts with the subsequent rising CLOCK edge.

CLOCK

The ADC uses an external clock in the range of 1MHz to 24MHz. 12 clock cycles are needed for a complete conversion; one additional clock cycle is used for pre-charging the sample capacitors. With a minimum of 16 clocks required per conversion, three clock cycles are used for sampling.

The CLOCK duty cycle should be 50%. However, the ADS7863 functions properly with a duty cycle between 30% and 70%.

RESET

The ADS7863 features an internal power-on reset (POR) function. However, an external reset can also be issued using SDI Register bits A[2:0] (see the Digital section).

REF_{IN}

The reference input is not buffered and is directly connected to the ADC. The converter generates spikes on the reference input voltage because of internal switching. Therefore, an external capacitor to the analog ground (AGND) should be used to stabilize the reference input voltage. This capacitor should be at least 470nF. Ceramic capacitors (X5R type) with values up to 1µF are commonly available as SMD in 0402 size.

REF_{OUT}

The ADS7863 includes a low-drift, 2.5V internal reference source. This source feeds a 10-bit string DAC that is controlled via the serial interface. As a result of this architecture, the voltage at the REF_{OUT} pin is programmable in 2.44mV steps and can be adjusted to specific application requirements without the use of additional external components.

However, the DAC output voltage should not be programmed below 0.5V to ensure the correct functionality of the reference output buffer. This buffer is connected between the DAC and the REF_{OUT} pin, and is capable of driving the capacitor at the REF_{IN} pin. A minimum of 470nF is required to keep the reference stable (see the previous discussion of REF_{IN} above). For applications that use an external reference source, the internal reference can be disabled using bit RP in the SDI Register (see the Digital section). The settling time of the REF_{OUT} pin is 100µs. The default value of the REF_{OUT} pin after power-up is 2.5V.

For operation with a 2.7V analog supply and a 2.5V reference, the internal reference buffer requires a rail-to-rail input and output. Such buffers typically contain two input stages; when the input voltage passes the mid-range area, a transition occurs at the output because of switching between the two input stages. In this voltage range, rail-to-rail amplifiers generally show a very poor power-supply rejection.

As a result of this poor performance, the ADS7863 buffer has a fixed transition at DAC code 496 (0x1F0). At this code, the DAC may show a jump of up to 10mV in its transfer function.

DIGITAL

This section addresses the timing and control of the ADS7863 serial interface.

Serial Data Input (SDI)

The serial data input or SDI pin (corresponding to pin A0 on the ADS7861) is coupled to RD and clocked into the ADS7863 on each falling edge of CLOCK. The data word length of the SDI Register is 12 bits. Table 3 shows the register structure. The data must be transferred MSB-first. Table 4 through Table 6 describe specific bits of this register. The default value of this register after power-up is 0x000.

Table 3. SDI Register Contents

SDI REGISTER BIT											
11	10	9	8	7	6	5	4	3	2	1	0
C1	C0	P1	P0	DP	N	AN	RP	S4	A2	A1	A0

Table 4. C1 and C0: Channel Selection

C1	C0	ADC A/B	
		POSITIVE INPUT	NEGATIVE INPUT
0	0	CHA0+ / CHB0+	CHA0– / CHB0–
0	1	CHA1– / CHB1–	CHA0– / CHB0–
1	0	CHA1+ / CHB1+	CHA0– / CHB0–
1	1	CHA1+ / CHB1+	CHA1– / CHB1–

Table 5. P1 and P0: Additional Features Enable

P1	P0	FUNCTION
0	0	Convert both CHx0 channels
0	1	Activate additional features
1	0	Reserved for factory test (do not use)
1	1	Convert both CHx1 channels

DP: Deep power-down enable ('1' = device in deep power-down mode)

N: Nap power-down enable ('1' = device in Nap power-down mode)

AN: AutoNap power-down enable ('1' = device in AutoNap power-down mode)

RP: Reference power-down ('1' = reference turned off)

S4: Special read mode for Modes II and IV ('1' = special mode enabled)

Table 6. A2, A1, and A0: DAC Control and Device Reset

A2	A1	A0	FUNCTION
0	0	0	No action
0	0	1	DAC write with next access
0	1	0	No action
0	1	1	DAC read with next access
1	0	0	No action
1	0	1	Device reset
1	1	0	No action
1	1	1	No action

All additional features become active with the rising edge of the 12th CLOCK signal after issuing the RD pulse.

Timing and Control

IMPORTANT:

Consider the Detailed Timing Diagram (Figure 1) and CONVST timing diagram (Figure 2) shown in the Timing Characteristics section. For maximum data throughput, the descriptions and diagrams given in this data sheet assume that the CONVST and RD pins are tied together. Note that they can also be controlled independently.

The operation of the ADS7863 can be configured in four different modes by using the mode pins M0 and M1, as shown in Table 7.

Pin M0 sets either manual or automatic channel selection. In manual mode, the SDI pin is used to select between channels CHx0 and CHx1; in automatic operation, the SDI pin is ignored and channel selection is controlled by the device after each conversion. Pin M1 selects between serial data being transmitted simultaneously on both outputs SDOA and SDOB for each channel respectively, or using only the SDOA output for transmitting data from both channels (see Figure 16 through Figure 23 and the associated text for more information).

Table 7. M1/M0 Truth Table

M0	M1	CHANNEL SELECTION	SDOx USED
0	0	Manual (via SDI)	SDOA and SDOB
0	1	Manual (via SDI)	SDOA only
1	0	Automatic	SDOA and SDOB
1	1	Automatic	SDOA only

Additionally, the SDI pin is used for controlling device functionality; see the Serial Data Input section for details.

Converted data on the SDOx pins becomes valid with the third falling CLOCK edge after generating an RD pulse. The following sections explain the four different modes of operation in detail.

MODE I

With the M0 and M1 pins both set to '0', the ADS7863 enters manual channel control operation. The SDI pin is used to switch between the channels. A conversion is initiated by bringing CONVST high.

16 clock cycles are required to perform a single conversion. With the rising edge of CONVST, the ADS7863 switches asynchronously to the external CLOCK from sample to hold mode.

After some delay (t_{12}), the BUSY output pin goes high and remains high for the duration of the conversion cycle. On the falling edge of the second CLOCK cycle, the ADS7863 latches in the channel for the next conversion cycle, depending on the status of the SDI pin. $\overline{CS}$ must be brought low to enable both serial outputs. Data are valid on the falling edge of every 16 clock cycles per conversion. The first two bits are set to '0'. The subsequent data contain the 12-bit conversion result (the most significant bit is transferred first), followed by two '0's (see Figure 1 and Figure 16).

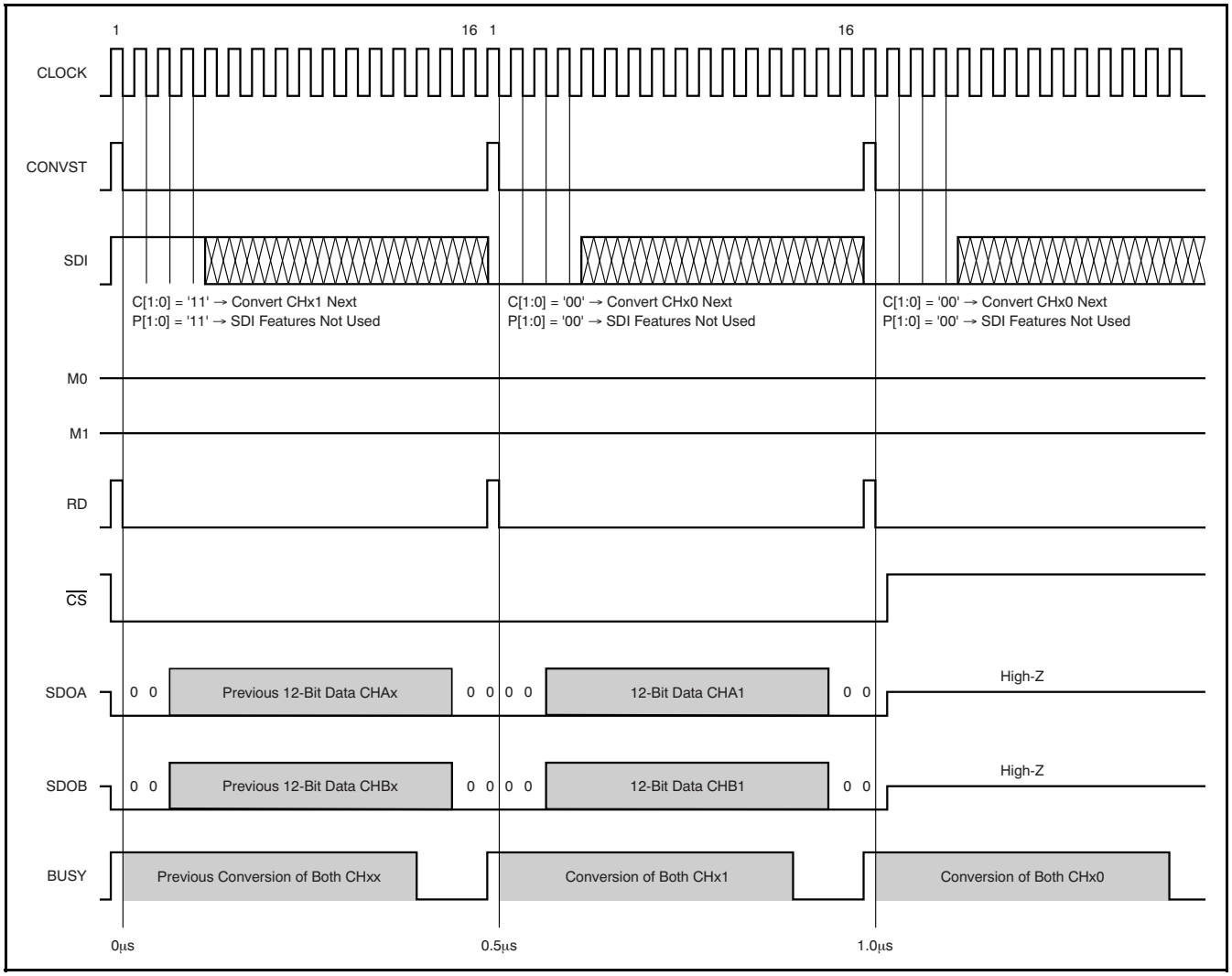


Figure 16. Mode I Timing Diagram (M0 = 0; M1 = 0)

PRODUCT PREVIEW

MODE II

With M0 = 0 and M1 set to '1', the ADS7863 also operates in manual channel control mode and outputs data on the SDOA pin only while SDOB is set to tri-state. All other pins function in the same manner as they do in Mode I. Because it takes 32 clock cycles to output the results from both ADCs (instead of 16 cycles, if M1 = 0), the ADS7863 requires 1µs to perform a complete conversion/read cycle. If the CONVST signal is issued every 0.5µs (which is required for the RD signal) as in Mode I, every second pulse is ignored; see Figure 17.

The output data consist of a '0' followed by an ADC indicator ('0' for CHAx or '1' for CHBx), 12 bits of conversion results, and another '00'.

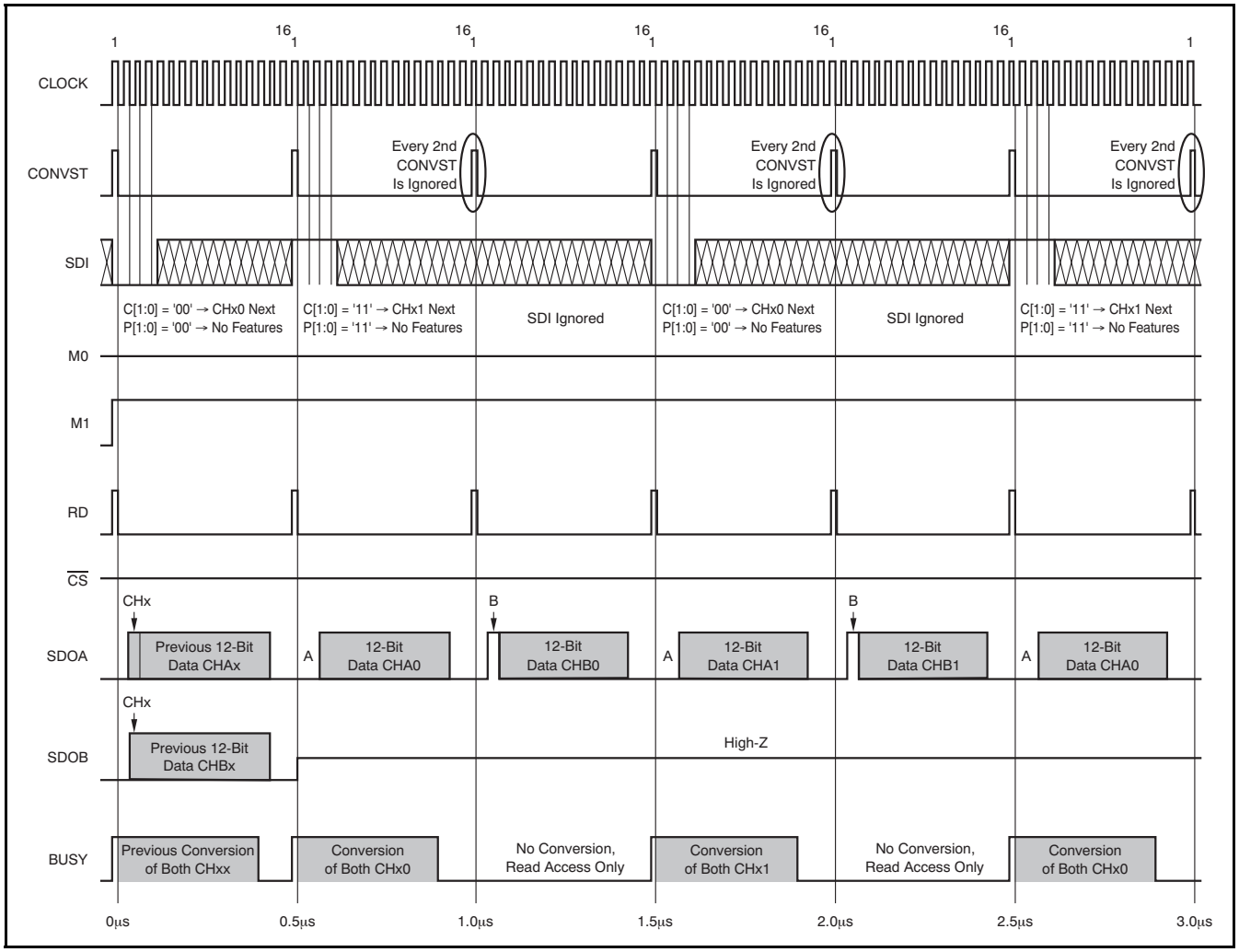


Figure 17. Mode II Timing Diagram (M0 = 0; M1 = 1)

PRODUCT PREVIEW

MODE III

With M0 set to '1' and M1 = 0, the ADS7863 automatically cycles between the multiplexer inputs (ignoring the SDI pin) while offering the conversion result of CHAx on SDOA and the conversion result of CHBx on SDOB (see Figure 18).

Output data consist of a channel indicator ('0' for CHx0 or '1' for CHx1), followed by a '0', 12 bits of conversion results, and another '00'.

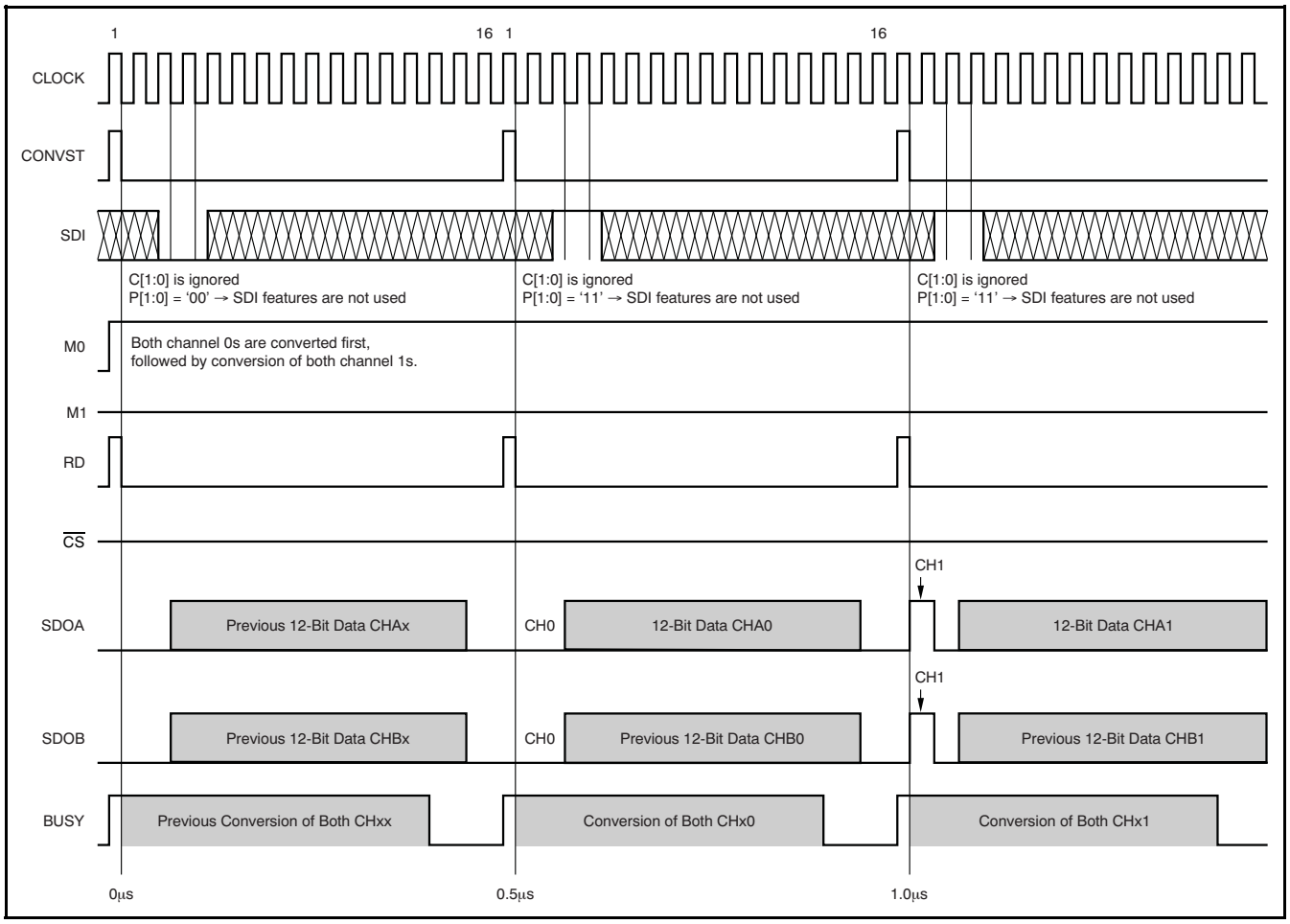


Figure 18. Mode III Timing Diagram (M0 = 1; M1 = 0)

MODE IV

In the same way as Mode II, Mode IV uses the SDOA output line exclusively to transmit data while the multiplexer channels are switched automatically. Following the first conversion after M1 goes high, the SDOB output tri-states (see Figure 19).

Output data consist of a channel indicator ('0' for CHx0 or '1' for CHx1), followed by the ADC indicator ('0' for CHAx or '1' for CHBx), 12 bits of conversion results, and ends with '00'.

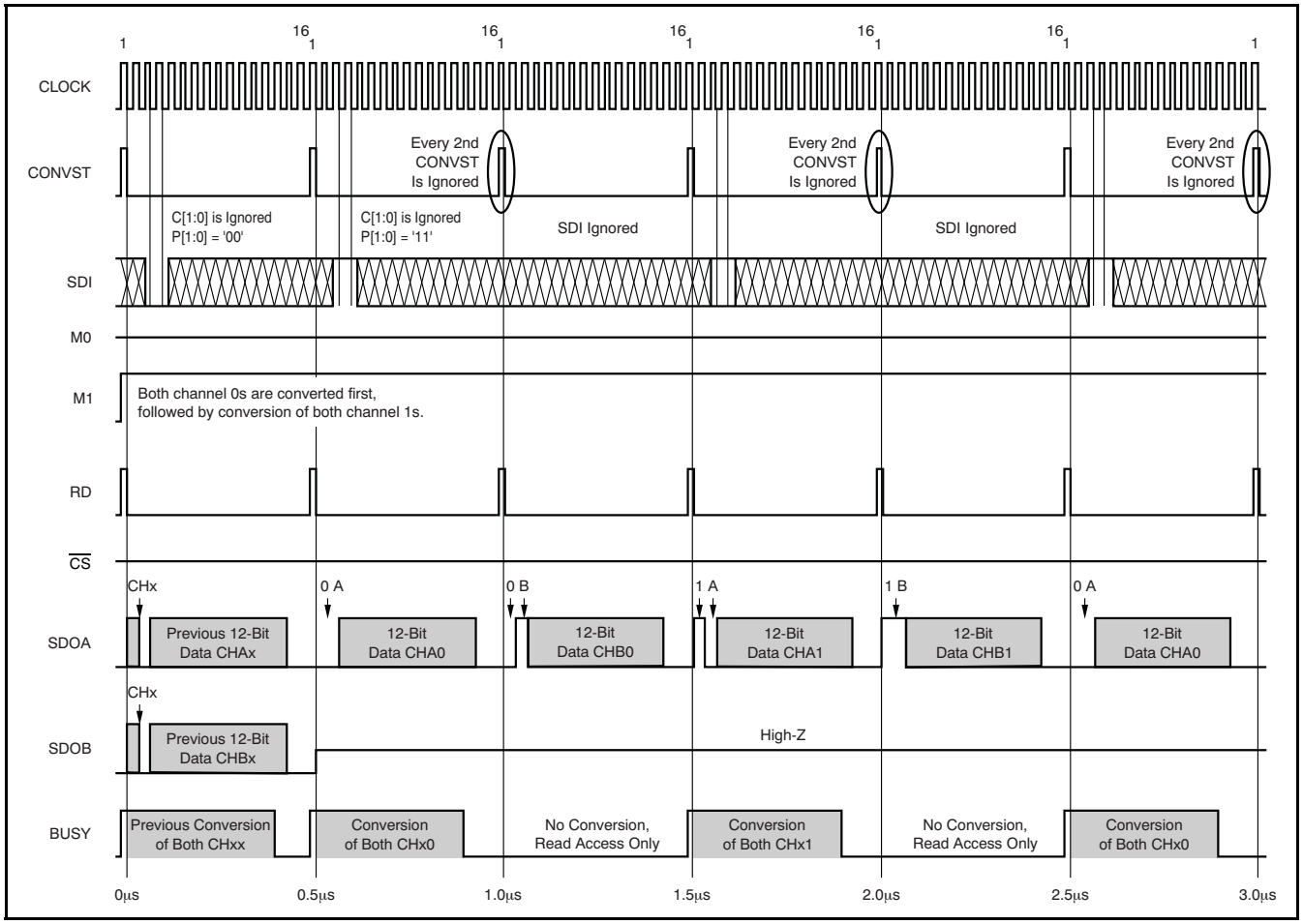


Figure 19. Mode IV Timing Diagram (M0 = 1 ; M1 = 1)

PRODUCT PREVIEW

SPECIAL MODE II (Not ADS7861-Compatible)

For Mode II, a special read mode is available in the ADS7863 where both data results can be read out, triggered by a single RD pulse. To activate this mode, bit S4 in the SDI Register must be set to '1' (see also the Serial Data Input section).

The CONVST and RD pins can still be tied together, but do not need to be issued every 16 CLOCK cycles. Output data are presented on both terminals, SDOA and SDOB.

The special read mode is not available in Mode I or Mode III. Figure 20 illustrates the special read mode.

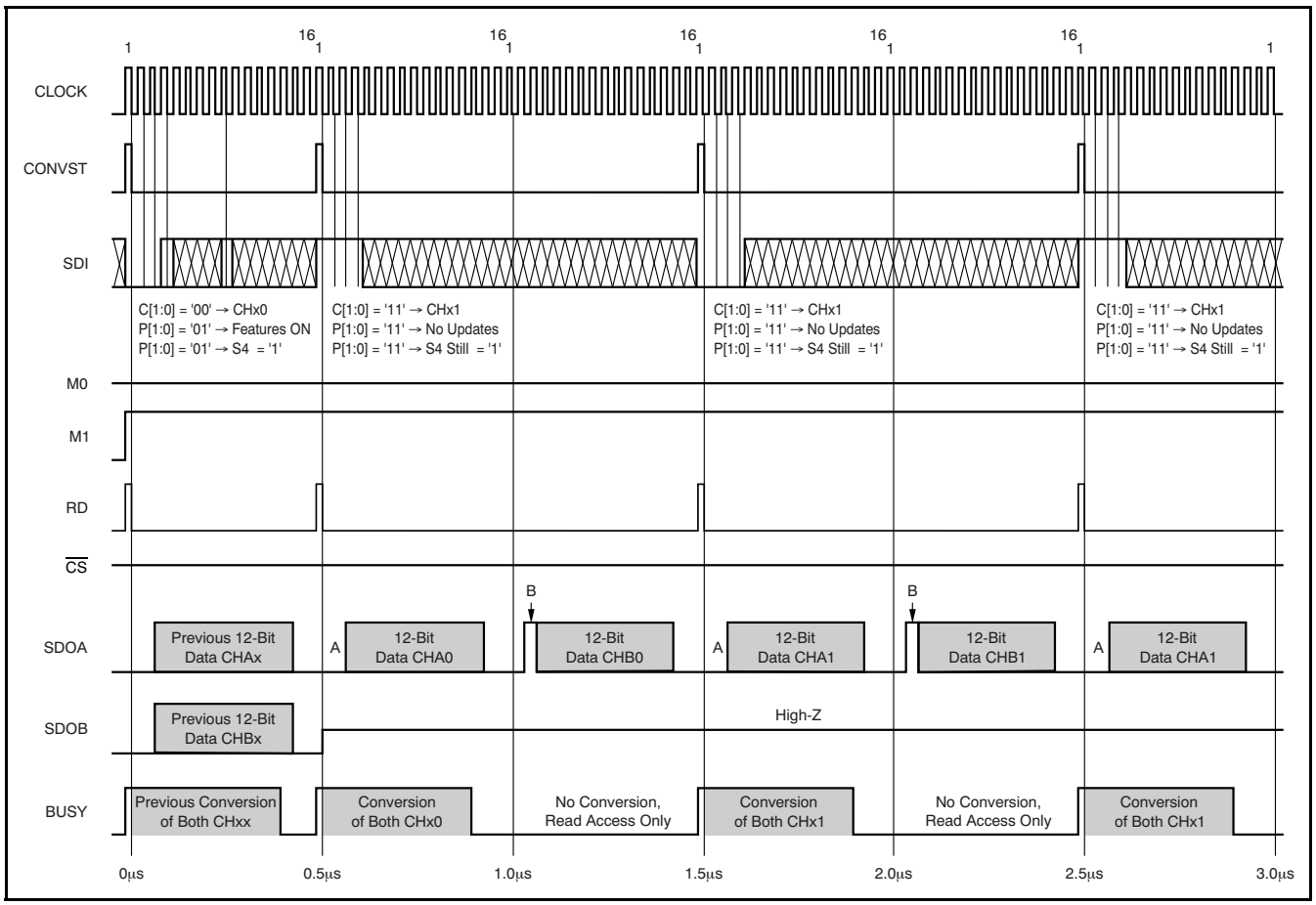


Figure 20. Special Mode II Timing Diagram (M0 = 0; M1 = 1; S4 = 1)

PRODUCT PREVIEW

SPECIAL MODE IV (Not ADS7861-Compatible)

Analogous to Special Mode II, the ADS7863 also offers a special read mode for Mode IV in which both data results of a conversion can be read, triggered by a single RD pulse. In this case as well, bit S4 in the SDI Register must be set to '1' while the CONVST and RD pins can still be tied together .

As with Special Mode II, these two pins do not need to be issued every 16 CLOCK cycles. Data are available on the SDOA pin.

This special read mode (shown in Figure 21) is not available in Mode I or Mode III.

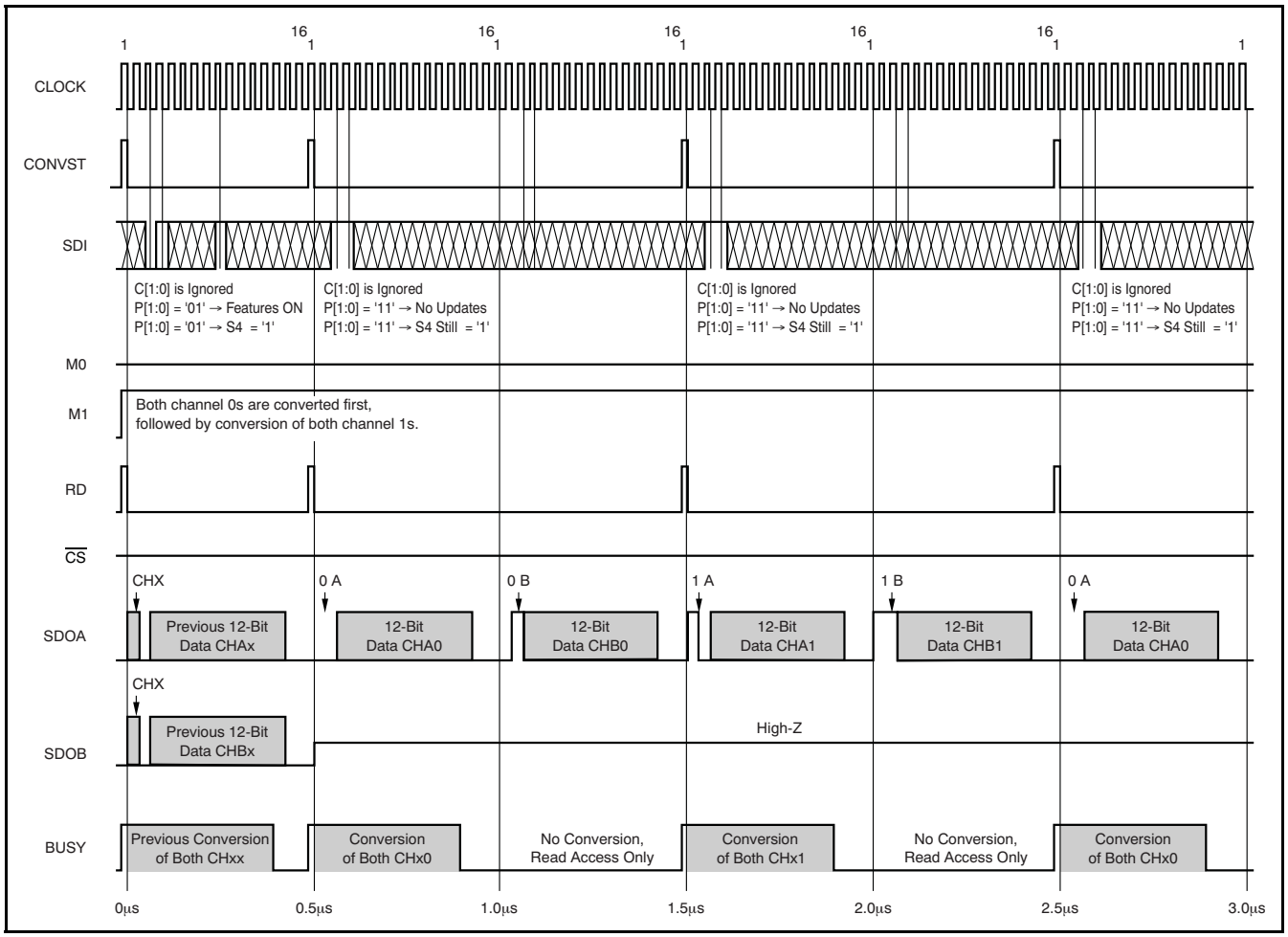


Figure 21. Special Mode IV Timing Diagram (M0 = 1; M1 = 1; S4 = 1)

PRODUCT PREVIEW

PSEUDO-DIFFERENTIAL MODE I (Not ADS7861-Compatible)

In Mode I, the ADS7863 input multiplexers can also operate in a pseudo-differential manner. In this case, SDI bits C[1:0] are used to choose the channels accordingly.

For more details, see the Serial Data Input section. Data are available on both output terminals, SDOA and SDOB.

The input multiplexer cannot be used for pseudo-differential signals in Mode III or Mode IV.

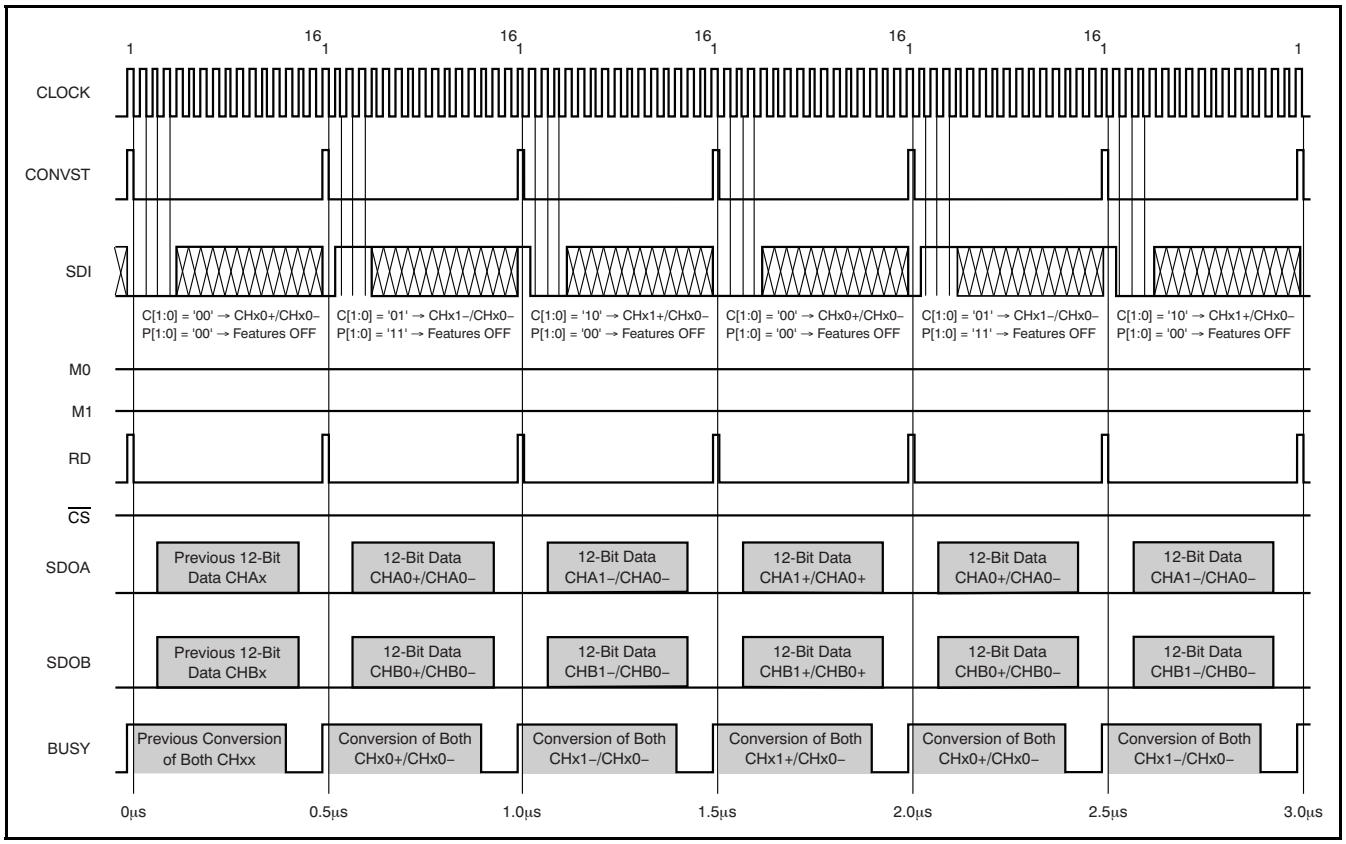


Figure 22. Pseudo-Differential Mode I (M0 = 0; M1 = 0)

PRODUCT PREVIEW

PSEUDO-DIFFERENTIAL MODE II (Not ADS7861-Compatible)

In Mode II, the ADS7863 input multiplexers can also operate in a pseudo-differential configuration. In this case, output data are available on terminal SDOA only, while SDOB is held in tri-state.

Channel switching is performed by setting the C[1:0] bits in the SDI Register accordingly (see also the Serial Data Input section).

The input multiplexer cannot be used for pseudo-differential signals in Mode III or Mode IV.

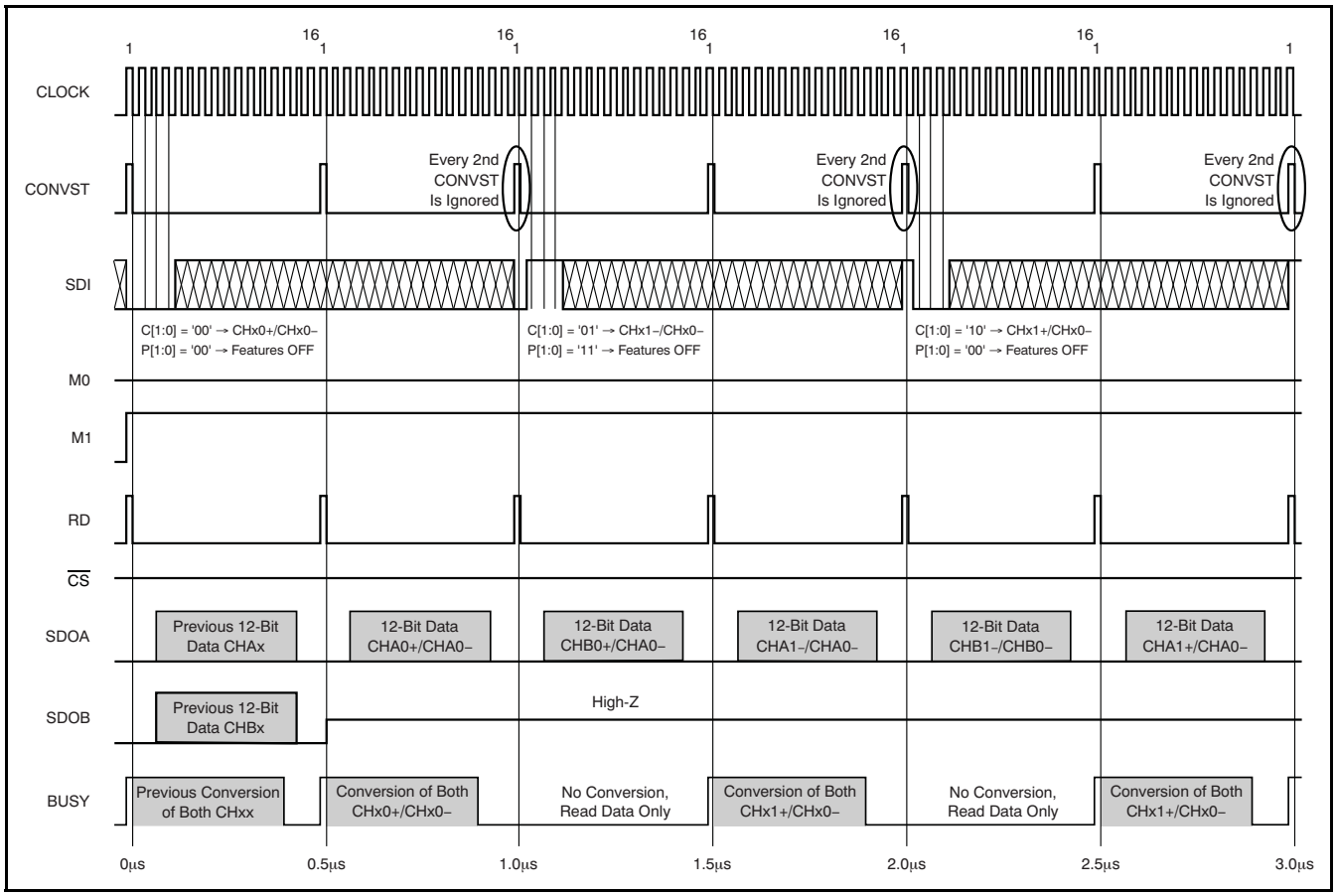


Figure 23. Pseudo-Differential Mode II (M0 = 0; M1 = 1)

PRODUCT PREVIEW

Programming the Reference DAC (Not ADS7861-Compatible)

The internal reference DAC can be set by issuing an RD pulse while providing an SDI word with P[1:0] = '01' and A[2:0] = '001'. Thereafter, a second RD pulse must be generated with an SDI word starting with '00' followed by the actual 10-bit DAC value (see Figure 24). During the second access, the first two '00' bits are not interpreted as channel selection bits.

To verify the DAC setting, an RD pulse must be generated while providing an SDI word containing P[1:0] = '01' and A[2:0] = '011' to initialize the DAC read access. Triggering the RD line again causes the SDOA output to send '0000' followed by the 10-bit DAC value and another '00'. During the second RD access, data present on SDI are ignored, while in Mode I and Mode III valid conversion data for channel B are present on SDOB. The default value of the DAC register after power-up is 0x3FF, corresponding to a reference voltage of 2.5V on the REF_{OUT} pin.

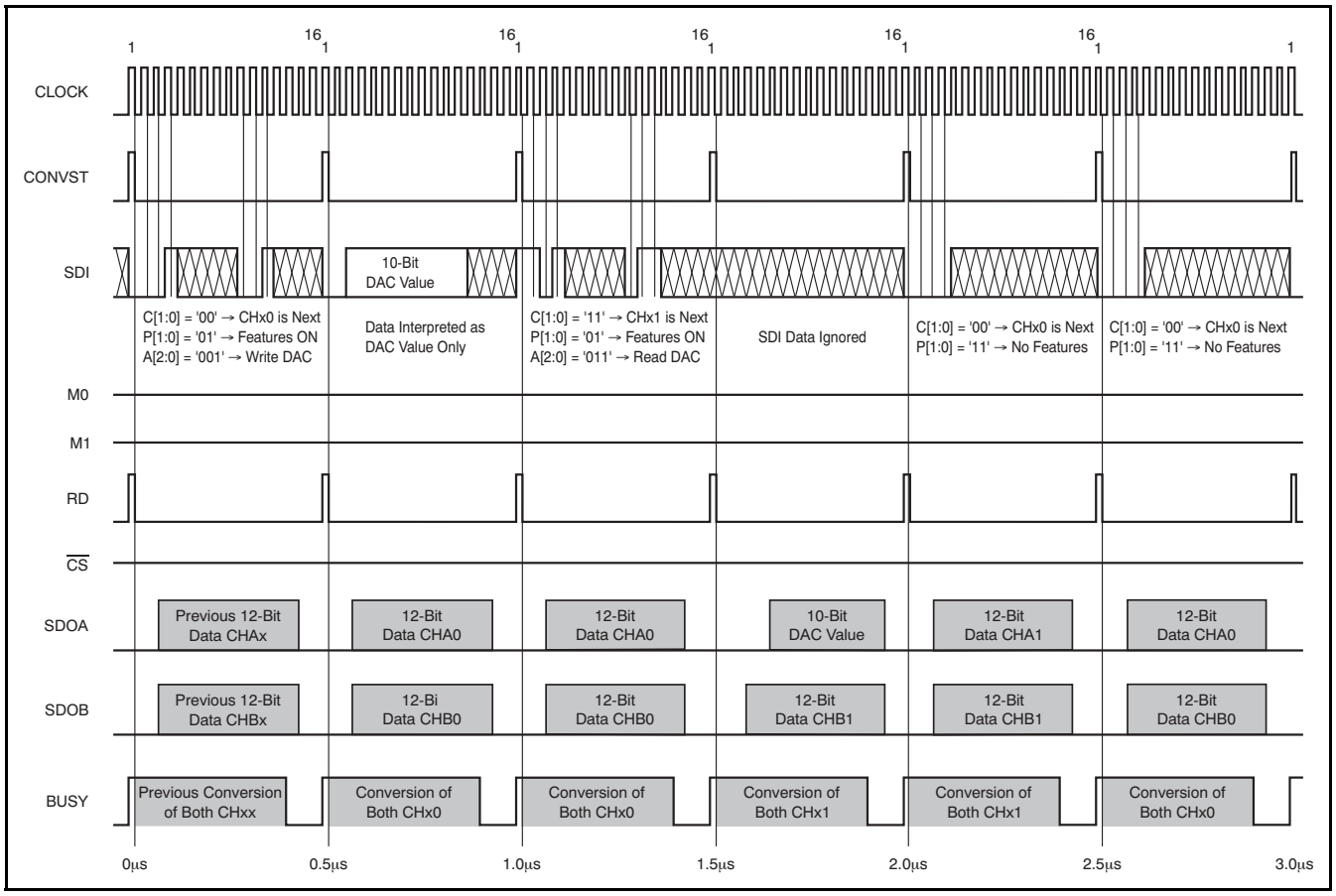


Figure 24. DAC Write and Read Access Timing Diagram

Power-Down Modes and Reset (Not ADS7861-Compatible)

The ADS7863 has a comprehensive built-in power-down feature. There are three power-down modes: deep power-down, nap power-down, and auto-nap power-down. All three power-down modes are activated with the 12th falling CLOCK edge of the SDI access, during which the related bit asserts (DP = '1', N = '1', or AN = '1'). All modes are deactivated by de-asserting the respective bit in the SDI Register. Contents of the SDI Register are not affected by any of the power-down modes. Any ongoing conversion aborts when deep or nap power-down is initiated. Table 8 lists the differences among the three power-down modes.

In ***deep power-down mode,*** all functional blocks except the digital interface are disabled. The analog block has its bias currents and the internal oscillator turned off. In this mode, the power dissipation reduces to 1µA within 2µs. The wake-up time from deep power-down mode is 1µs.

In ***nap power-down mode,*** the ADS7863 turns off the biasing of the comparator and the mid-voltage buffer. In this mode, power dissipation reduces to approximately 0.3mA within 200ns. The device goes into nap power-down mode regardless of the conversion state.

The ***auto-nap power-down mode*** is almost identical to the nap mode. The only difference is the time required to power down and the method of waking up the device. The SDI Register bit AN is only used to enable/disable this feature. If the auto-nap mode is enabled, the ADS7863 turns off the biasing automatically after finishing a conversion; thus, the end of conversion actually activates the auto-nap power-down. Device power dissipation reduces to about 0.3mA within 200ns in this mode, as well. Triggering a new conversion by applying a CONVST pulse puts the device back into normal operation.

To issue a ***device reset***, an RD pulse must be generated along with an SDI word containing A[2:0] = '101'. With the 12th falling edge after generating the RD pulse, the entire device—including the serial interface—is forced into reset. After approximately 20ns, the serial interface becomes active again.

Table 8. Power-Down Modes

POWER-DOWN TYPE	POWER DISSIPATION	ENABLED BY	ACTIVATED BY	ACTIVATION TIME	RESUMED BY	REACTIVATION TIME	DISABLED BY
Deep	1µA	DP = ‘1’	12th clock	2µs	DP = ‘0’	1µs	DP = ‘0’
Nap	300µA	N = ‘1’	12th clock	200ns	N = ‘0’	3 clocks	N = ‘0’
Auto-nap	300µA	AN = ‘1’	Each end of conversion	200ns	CONVST pulse	3 clocks	AN = ‘0’

PRODUCT PREVIEW

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7863 circuitry. This condition is particularly true if the CLOCK input is approaching the maximum throughput rate. The basic SAR architecture is quite sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, driving any single conversion for an *n*-bit SAR converter, there are *n* windows in which large external transient voltages can affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, or high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. These errors can change if the external event also changes in time with respect to the CLOCK input.

With this possibility in mind, power to the ADS7863 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor is recommended. If needed, an even larger capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

If the reference voltage is external and originates from an operational amplifier, be sure that it can drive the bypass capacitor or capacitors without oscillation.

Grounding

The xGND pins should be connected to a clean ground reference. These connections should be kept as short as possible to minimize the inductance of its path. It is recommended to use vias connecting the pads directly to the ground plane. In designs without ground planes, the ground trace should be kept as wide as possible. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor.

Depending on the circuit density on the board, placement of the analog and digital components, and the related current loops, a single solid ground plane for the entire printed circuit board (PCB) or a dedicated analog ground area may be used. In an instance of a separated analog ground area, ensure a low-impedance connection between the analog and digital ground of the ADC by placing a bridge underneath (or next) to the ADC. Otherwise, even short undershoots on the digital interface with a value lower than –300mV will lead to conduction of ESD diodes, causing current flow through the substrate and degrading the analog performance.

During the PCB layout, care should also be taken to avoid any return currents crossing any sensitive analog areas or signals. No signal must exceed the limit of –300mV with respect to the according ground plane.

Supply

The ADS7863 has two separate supplies, the BV_{DD} pin for the digital interface and the AV_{DD} pin for all remaining (analog) circuits.

BV_{DD} can range from 1.65V to 5.5V, allowing the ADS7863 to interface with all state-of-the-art processors and controllers. To limit the injection of noise energy from external digital circuitry, BV_{DD} should be filtered properly. Bypass capacitors of 0.1µF and 10µF should be placed between the BV_{DD} pin and the ground plane.

AV_{DD} is used to supply the internal analog circuitry. For optimum performance, a linear regulator (for example, the UA7805 family) is recommended to generate the analog supply voltage in the range of 2.7V to 5.5V for the ADS7863 and the necessary analog front-end circuitry.

Bypass capacitors should be connected to the ground plane such that the current is allowed to flow through the pad of the capacitor (that is, the vias should be placed on the opposite side of the connection between the capacitor and the power-supply pin of the ADC).

Digital Interface

To further optimize device performance, a resistor of 10Ω to 100Ω can be used on each digital pin of the ADS7863. In this way, the slew rate of the input and output signals is reduced, limiting the noise injection from the digital interface.

PACKAGING INFORMATION

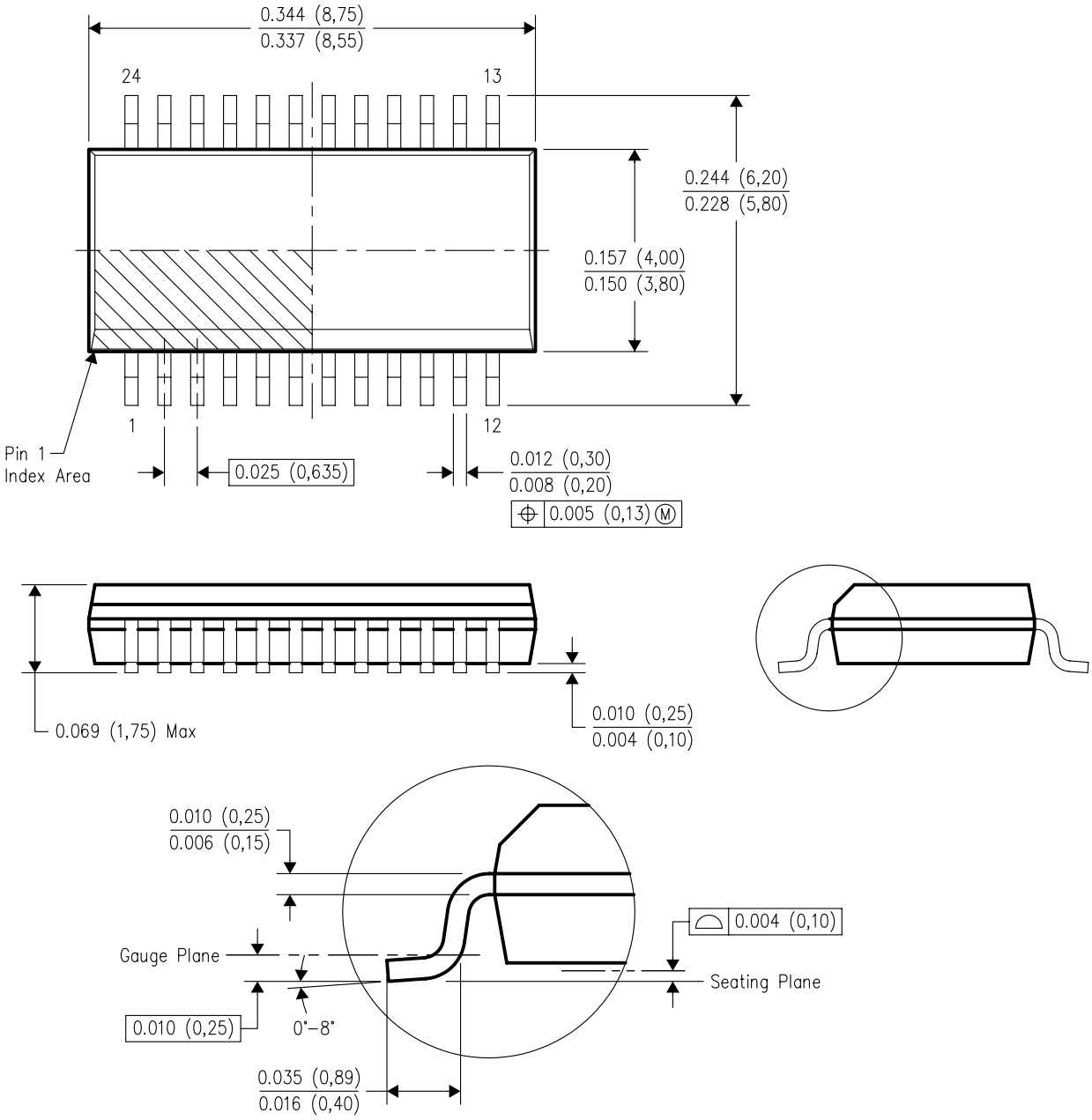
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
ADS7863IDBQ	PREVIEW	SSOP/ QSOP	DBQ	24	56	TBD	Call TI	Call TI
ADS7863IDBQR	PREVIEW	SSOP/ QSOP	DBQ	24	2500	TBD	Call TI	Call TI
ADS7863IRGER	PREVIEW	QFN	RGE	24	3000	TBD	Call TI	Call TI
ADS7863IRGET	PREVIEW	QFN	RGE	24	250	TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

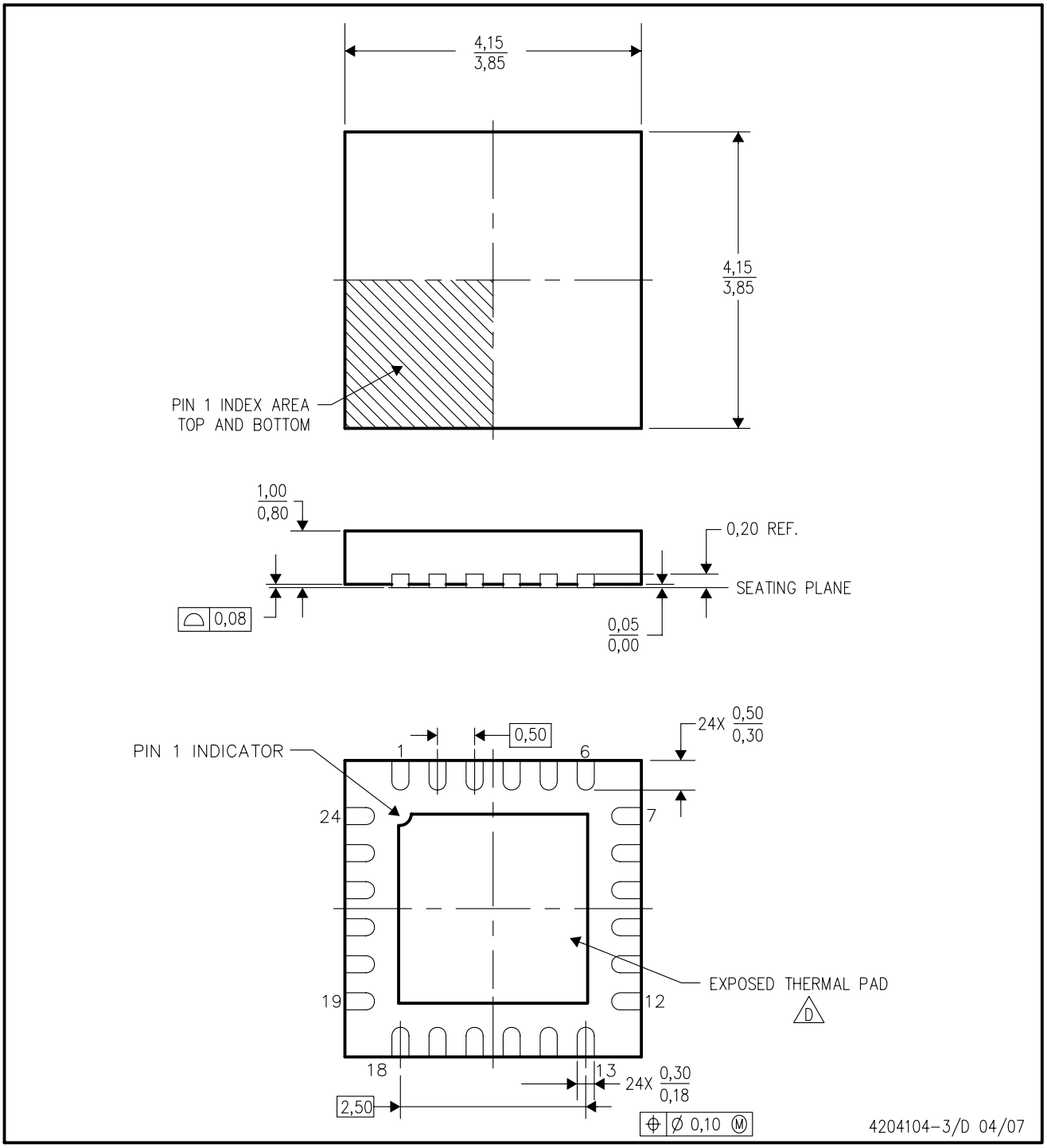
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AE.

RGE (S–PQFP–N24) PIN 1 OPTION PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

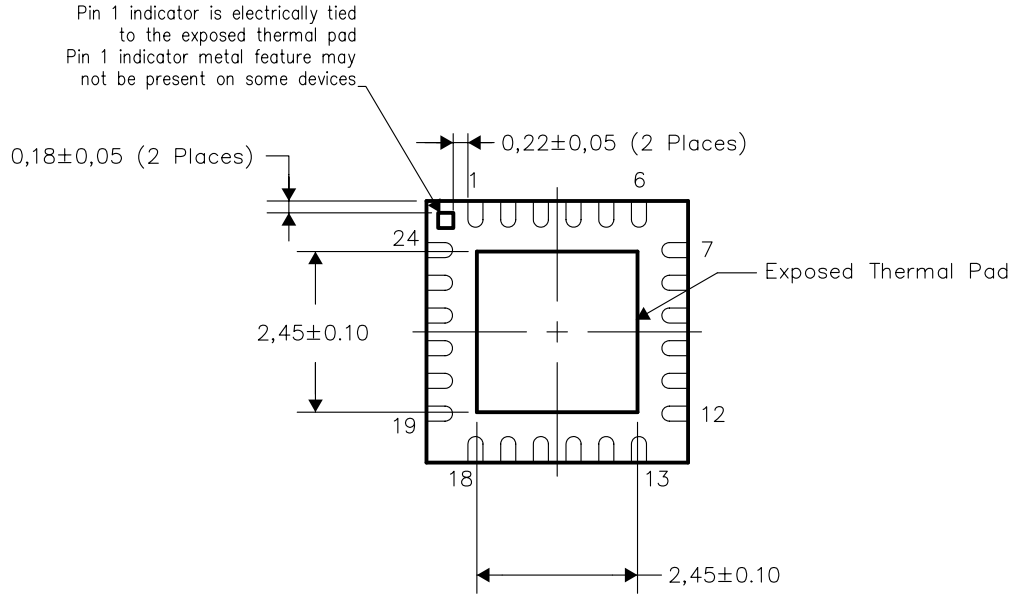
RGE (S–PQFP–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground or power plane (whichever is applicable), or alternatively, a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

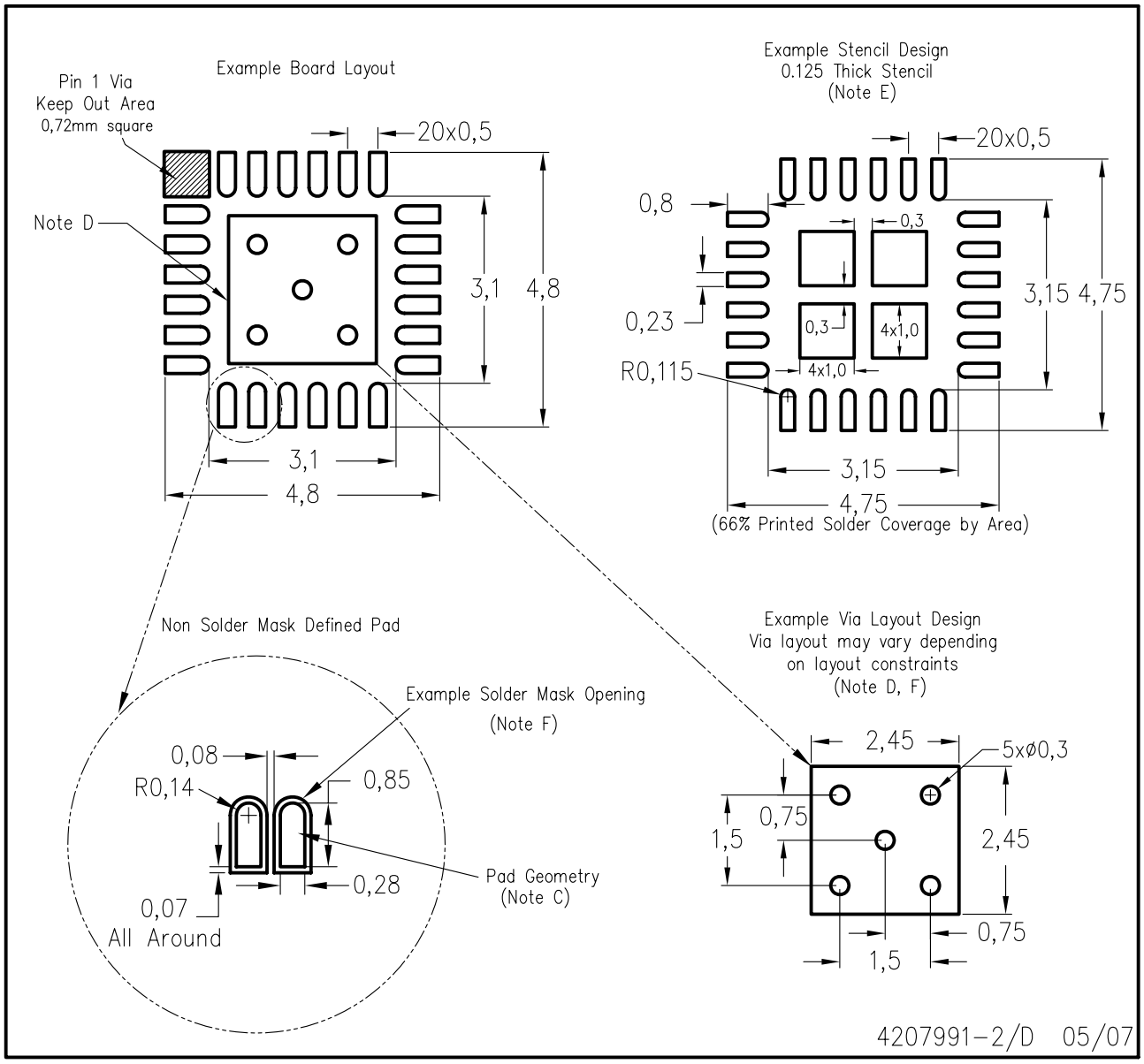


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGE (S–PQFP–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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