12-BIT, 3-MSPS, MICROPOWER, MINIATURE SAR ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **3-MHz Sample Rate Serial Device**
- **12-Bit Resolution**
- **Zero Latency**
- **48-MHz Serial Interface**
- **Supply Range: 2.7 V to 5.5 V**
- **Low Power Dissipation:**
  - **6.45 mW at 3-V V_{DD}, 2 MSPS**
  - **13.5 mw at 5-V V_{DD}, 3 MSPS**
- **±0.6 LSB INL, ±0.5 LSB DNL**
- **72 dB SINAD, –84 dB THD**
- **Unipolar Input Range: 0 V to V_{DD}**
- **Power-Down Current: 1 µA**
- **Wide Input Bandwidth: 30 MHz at 3 dB**
- **6-Pin SOT23 Package**

APPLICATIONS

- **Base Band Converters in Radio Communication**
- **Motor Current/Bus Voltage Sensors in Digital Drives**
- **Optical Networking (DWDM, MEMS Based Switching)**
- **Optical Sensors**
- **Battery Powered Systems**
- **Medical Instrumentations**
- **High-Speed Data Acquisition Systems**
- **High-Speed Closed-Loop Systems**

DESCRIPTION

The ADS7883 is a 12-bit, 3-MSPS analog-to-digital converter (ADC). The device includes a capacitor based SAR A/D converter with inherent sample and hold. The serial interface in the device is controlled by the $\overline{CS}$ and SCLK signals for glueless connections with microprocessors and DSPs. The input signal is sampled with the falling edge of $\overline{CS}$, and SCLK is used for conversion and serial data output.

The device operates from a wide supply range from 2.7 V to 5.5 V. The low power consumption of the device makes it suitable for battery-powered applications. The device also includes a power saving power-down feature for when the device is operated at lower conversion speeds.

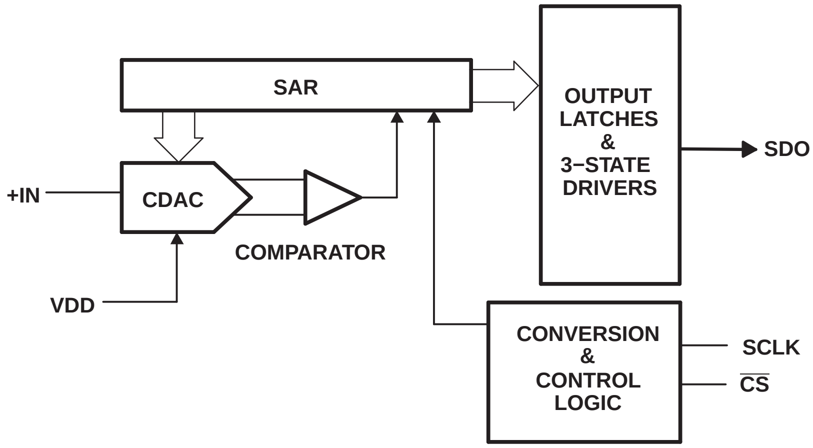
The high level of the digital input to the device is not limited to device V_{DD}. Therefore the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are received from another circuit with different supply levels. This also reduces restrictions on power-up sequencing.

The ADS7883 is available in a 6-pin SOT23 package and is specified for operation from –40°C to 125°C.

MicroPower Miniature SAR Converter Family

BIT	< 300 KSPS	300 KSPS – 1.25 MSPS	3 MSPS	
12-Bit	ADS7866 (1.2 V_{DD} to 3.6 V_{DD})	ADS7886 (2.35 V_{DD} to 5.25 V_{DD})	ADS7883	3 MSPS for 4.5 V_{DD} to 5.5 V_{DD}
				2 MSPS for 2.7 V_{DD} to 4.5 V_{DD}
10-Bit	ADS7867 (1.2 V_{DD} to 3.6 V_{DD})	ADS7887 (2.35 V_{DD} to 5.25 V_{DD})	ADS7884 (2.7 V_{DD} to 5.5 V_{DD})	
8-Bit	ADS7868 (1.2 V_{DD} to 3.6 V_{DD})	ADS7888 (2.35 V_{DD} to 5.25 V_{DD})	ADS7885 (2.7 V_{DD} to 5.5 V_{DD})	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.



PACKAGE/ORDERING INFORMATION[1]

DEVICE	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	PACKAGE MARKING	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS7883SB	±1	±1	12	6-Pin SOT23	DBV	–40°C to 125°C	7883	ADS7883SBDBVT	Small Tape and Reel 250
							7883	ADS7883SBDBVR	Large Tape and Reel 3000
ADS7883S	±2	±2	11				7883	ADS7883SDBVT	Small Tape and Reel 250
							7883	ADS7883SDBVR	Large Tape and Reel 3000

(1) For most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS[1]

		UNIT
+IN to AGND		–0.3 V to +V_{DD} +0.3 V
+V_{DD} to AGND		–0.3 V to 7.0 V
Digital input voltage to GND		–0.3 V to (7.0 V)
Digital output to GND		–0.3 V to (+V_{DD} + 0.3 V)
Operating temperature range		–40°C to 125°C
Storage temperature range		–65°C to 150°C
Junction temperature (T_J Max)		150°C
Power dissipation, SOT23 package		(T_J Max–T_A)/θ_{JA}
Thermal impedance, θ_{JA}	SOT23	295.2°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses above those listed under *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTRICAL SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, T_A = –40°C to 125°C, f_{sample} = 2 MSPS for V_{DD} = 2.7 V to 4.5 V, f_{sample} = 3 MSPS for V_{DD} = 4.5 V to 5.5 V

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT							
	Full-scale input voltage span(1)			0		V_{DD}	V
	Absolute input voltage range		+IN	–0.2		V_{DD}+0.2	V
C_I	Input capacitance(2)				27		pF
I_{Ilkg}	Input leakage current		T_A = 125°C		40		nA
SYSTEM PERFORMANCE							
	Resolution				12		Bits
	No missing codes	ADS7883SB		12			Bits
		ADS7883S		11			
INL	Integral nonlinearity	ADS7883SB		–1	±0.6	1	LSB(3)
		ADS7883S		–2	±0.75	2	
DNL	Differential nonlinearity	ADS7883SB		–1	±0.5	1	LSB
		ADS7883S		–2	±0.75	2	
E_O	Offset error(4)(5)(6)			–3	±0.2	3	LSB
E_G	Gain error(5)			–3.5	±0.3	3.5	LSB
SAMPLING DYNAMICS							
	Conversion time		32-MHz SCLK, V_{DD} = 3 V	398	422		ns
			48-MHz SCLK, V_{DD} = 5 V	265	281		
	Acquisition time		32-MHz SCLK, V_{DD} = 3 V	78			ns
			48-MHz SCLK, V_{DD} = 5 V	52			
	Maximum throughput rate		32-MHz SCLK, V_{DD} = 2.7 V to 4.5 V			2	MHz
			48-MHz SCLK, V_{DD} = 4.5 V to 5.5 V			3	
	Aperture delay				10		ns
DYNAMIC CHARACTERISTICS							
THD	Total harmonic distortion(7)		f_I = 100 kHz		–84		dB
SINAD	Signal-to-noise and distortion		f_I = 100 kHz, ADS7883SB	69	72		dB
			f_I = 100 kHz, ADS7883S	68	70		
SFDR	Spurious free dynamic range		f_I = 100 kHz		86		dB
	Full power bandwidth		At –3 dB	30			MHz
DIGITAL INPUT/OUTPUT							
Logic family — CMOS							
V_{IH}	High-level input voltage		V_{DD} = 2.7 V to 3.6 V	1.5		5.5	V
			V_{DD} = 3.6 V to 5.5 V	2.2		5.5	
V_{IL}	Low-level input voltage		V_{DD} = 2.7 V to 3.6 V			0.4	V
			V_{DD} = 3.6 V to 5.5 V			0.8	
V_{OH}	High-level output voltage		At I_{source} = 200 µA	V_{DD}–0.2			V
V_{OL}	Low-level output voltage		At I_{sink} = 200 µA			0.4	
POWER SUPPLY REQUIREMENTS							
+V_{DD}	Supply voltage			2.7	3.3	5.5	V

(1) Ideal input span; does not include gain or offset error
(2) Refer to Figure 24 for details on sampling circuit
(3) LSB means least significant bit
(4) Measured relative to an ideal full-scale input
(5) Offset error and gain error ensured by characterization
(6) First transition of 000H to 001H at ($V_{ref}/2^{10}$)
(7) Calculated on the first nine harmonics of the input frequency

ELECTRICAL SPECIFICATIONS (continued)

V_{DD} = 2.7 V to 5.5 V, T_A = –40°C to 125°C, f_{sample} = 2 MSPS for V_{DD} = 2.7 V to 4.5 V, f_{sample} = 3 MSPS for V_{DD} = 4.5 V to 5.5 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply current (normal mode)	At V_{DD} = 3 V, 2-MSPS throughput		2.15	3	mA
	At V_{DD} = 3 V, Static state		1.8		
	At V_{DD} = 5 V, 3-MSPS throughput		2.7	4	
	At V_{DD} = 5 V, Static state		2		
Power-down state supply current	SCLK off			1	μA
	SCLK on (48 MHz)		90	250	
Power dissipation	V_{DD} = 5 V, 3 MSPS		13.5	20	mW
	V_{DD} = 3 V, 2 MSPS		6.45		
Power dissipation in static state	V_{DD} = 5 V		10	12.5	mW
	V_{DD} = 3 V		5.4		
Power-down time				0.1	μs
Power-up time				0.8	μs
TEMPERATURE RANGE					
Specified performance		–40		125	°C

TIMING REQUIREMENTS (see Figure 21)

All specifications typical at T_A = –40°C to 125°C, V_{DD} = 2.7 V to 5.5 V, unless otherwise specified.

PARAMETER		TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
t_{conv}	Conversion time	V_{DD} = 3 V			13.5 × t_{SCLK}	ns
		V_{DD} = 5 V			13.5 × t_{SCLK}	
t_{acq}	Aquisition time	V_{DD} = 3 V	78			ns
		V_{DD} = 5 V	52			
t_q	Minimum quiet time needed from bus 3-state to start of next conversion	V_{DD} = 3 V	10			ns
		V_{DD} = 5 V	10			
t_{d1}	Delay time, $\overline{CS}$ low to first data (0) out	V_{DD} = 3 V		9	15	ns
		V_{DD} = 5 V		8	11	
t_{su1}	Setup time, $\overline{CS}$ low to SCLK low	V_{DD} = 3 V	7			ns
		V_{DD} = 5 V	5			
t_{d2}	Delay time, SCLK falling to SDO	V_{DD} = 3 V		11	20	ns
		V_{DD} = 5 V		9	12	
t_{h1}	Hold time, SCLK falling to data valid(2)	V_{DD} < 3 V	5.5			ns
		V_{DD} > 5 V	4			
t_{d3}	Delay time, 16th SCLK falling edge to SDO 3-state	V_{DD} = 3 V		9	15	ns
		V_{DD} = 5 V		8	11	
t_{w1}	Pulse duration, $\overline{CS}$	V_{DD} = 3 V	10			ns
		V_{DD} = 5 V	10			
t_{d4}	Delay time, $\overline{CS}$ high to SDO 3-state,	V_{DD} = 3 V		9	15	ns
		V_{DD} = 5 V		8	11	
t_{wH}	Pulse duration, SCLK high	V_{DD} = 3 V	0.45 × t_{SCLK}			ns
		V_{DD} = 5 V	0.45 × t_{SCLK}			
t_{wL}	Pulse duration, SCLK low	V_{DD} = 3 V	0.45 × t_{SCLK}			ns
		V_{DD} = 5 V	0.45 × t_{SCLK}			

(1) 3-V Specifications apply from 2.7 V to 3.6 V, and 5-V specifications apply from 4.5 V to 5.5 V.
(2) With 10-pf load.

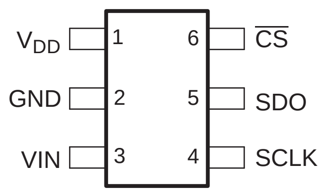
TIMING REQUIREMENTS (see Figure 21) (continued)

All specifications typical at T_A = –40°C to 125°C, V_{DD} = 2.7 V to 5.5 V, unless otherwise specified.

	PARAMETER	TEST CONDITIONS(1)	MIN	TYP	MAX	UNIT
	Frequency, SCLK	V_{DD} = 2.7 V to 4.5 V			32	MHz
		V_{DD} = 4.5 V to 5.5 V			48	
t_{d5}	Delay time, second falling edge of clock and $\overline{CS}$ to enter in powerdown (use min spec not to accidently enter in powerdown) see Figure 22	V_{DD} = 3 V	–2		4	ns
		V_{DD} = 5 V	–2		3	
t_{d6}	Delay time, $\overline{CS}$ and 10th falling edge of clock to enter in powerdown (use max spec not to accidently enter in powerdown) see Figure 22	V_{DD} = 3 V	–2		4	ns
		V_{DD} = 5 V	–2		3	

DEVICE INFORMATION

SOT23 PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{DD}	1	–	Power supply input, also acts like a reference voltage to ADC.
GND	2	–	Ground for power supply, all analog and digital signals are referred with respect to this pin.
VIN	3	I	Analog signal input
SCLK	4	I	Serial clock
SDO	5	O	Serial data out
$\overline{CS}$	6	I	Chip select signal, active low

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SUPPLY VOLTAGE

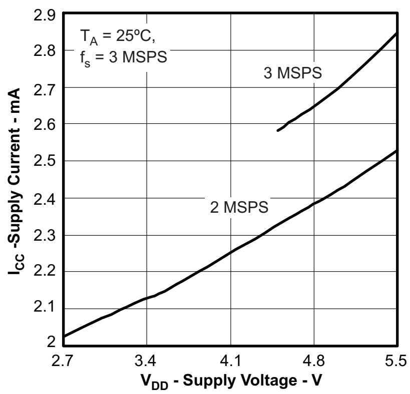


Figure 1.

SUPPLY CURRENT vs SCLK FREQUENCY

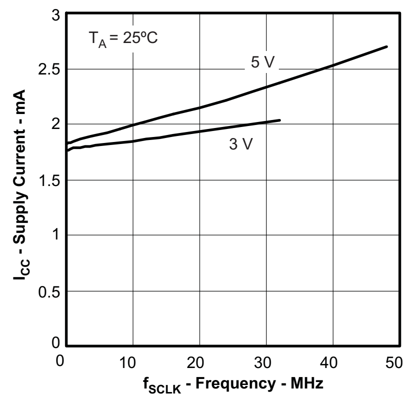


Figure 2.

SUPPLY CURRENT vs SAMPLE RATE

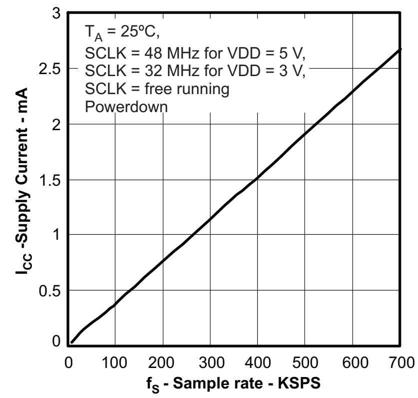


Figure 3.

INPUT LEAKAGE CURRENT vs FREE-AIR TEMPERATURE

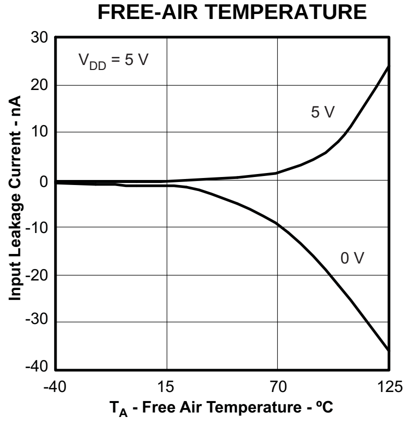


Figure 4.

SIGNAL-TO-NOISE RATIO vs INPUT FREQUENCY

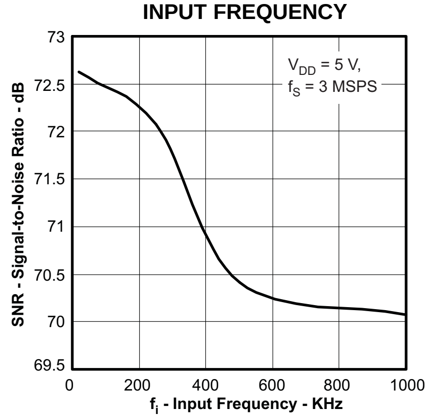


Figure 5.

SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

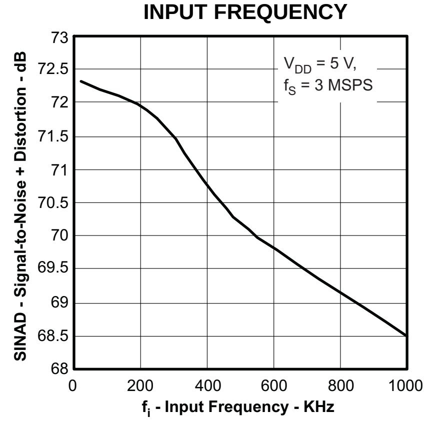


Figure 6.

TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

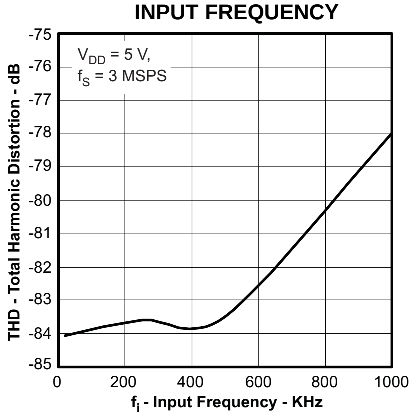


Figure 7.

SIGNAL-TO-NOISE + DISTORTION vs SUPPLY VOLTAGE

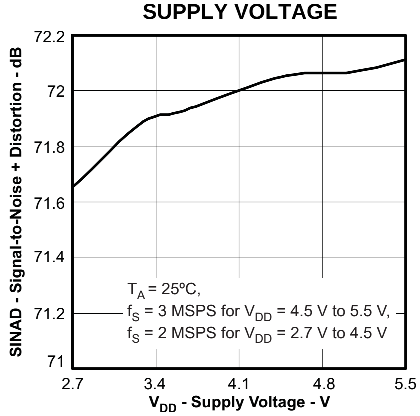


Figure 8.

SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE

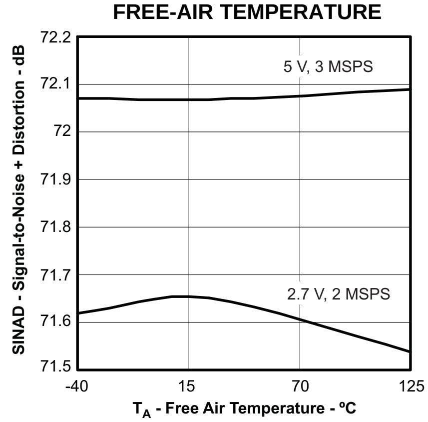


Figure 9.

TYPICAL CHARACTERISTICS (continued)

DIFFERENTIAL NONLINEARITY vs FREE-AIR TEMPERATURE

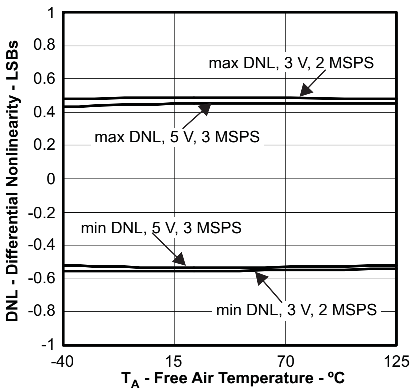


Figure 10.

INTEGRAL NONLINEARITY vs FREE-AIR TEMPERATURE

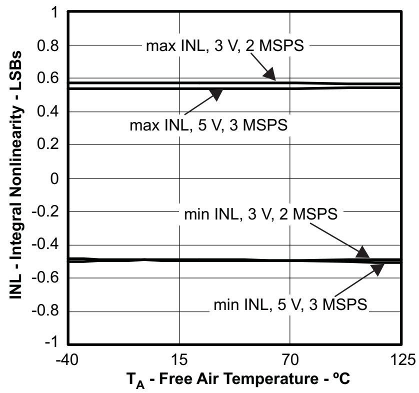


Figure 11.

DIFFERENTIAL NONLINEARITY vs SUPPLY VOLTAGE

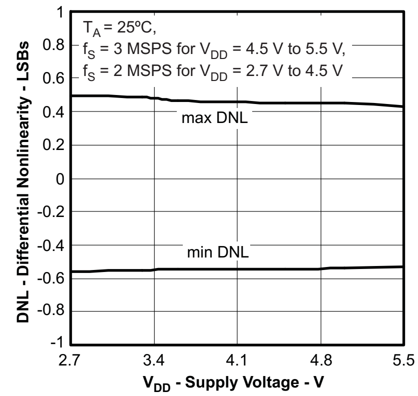


Figure 12.

INTEGRAL NONLINEARITY vs SUPPLY VOLTAGE

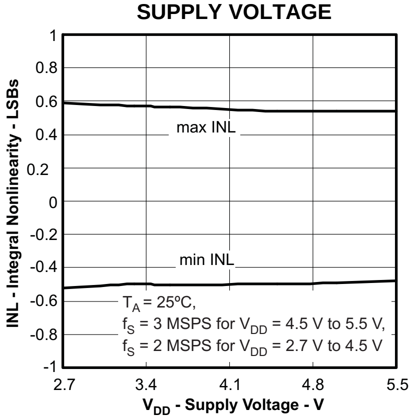


Figure 13.

OFFSET ERROR vs SUPPLY VOLTAGE

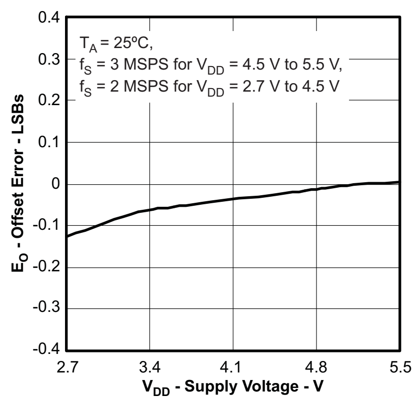


Figure 14.

OFFSET ERROR vs FREE-AIR TEMPERATURE

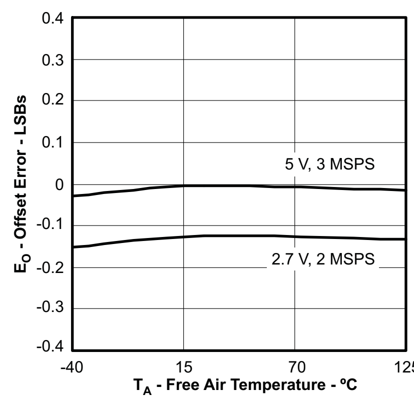


Figure 15.

GAIN ERROR vs SUPPLY VOLTAGE

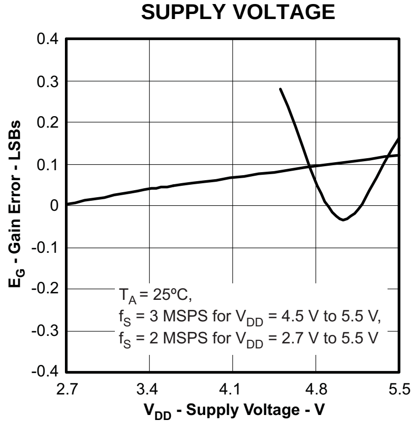


Figure 16.

GAIN ERROR vs FREE-AIR TEMPERATURE

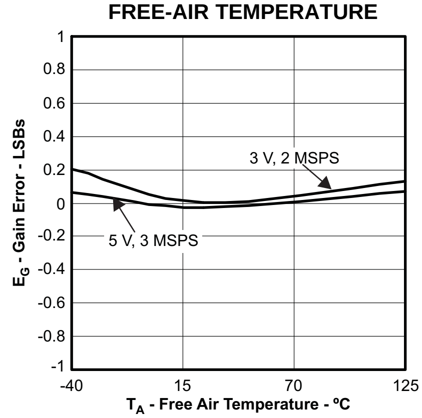


Figure 17.

TYPICAL CHARACTERISTICS (continued)

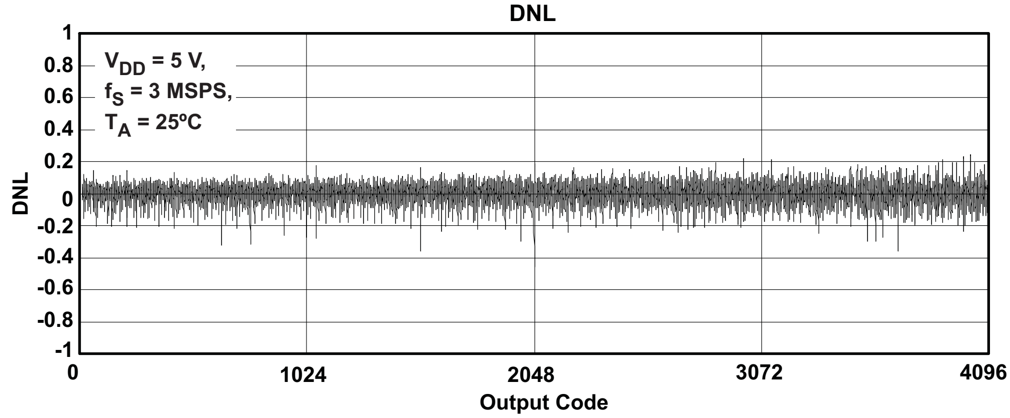


Figure 18.

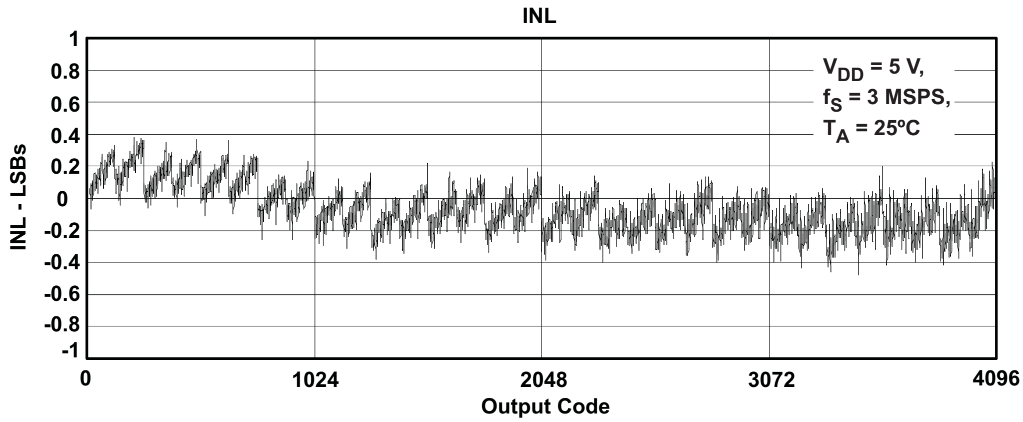


Figure 19.

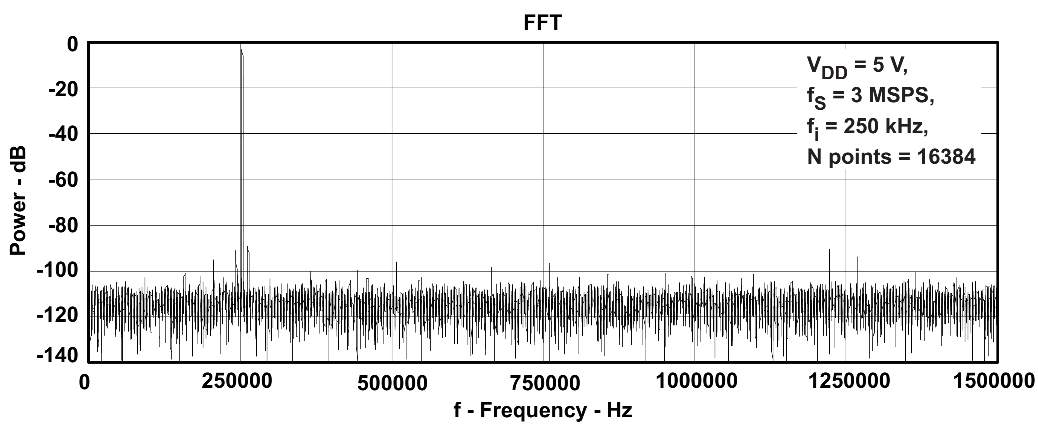


Figure 20.

NORMAL OPERATION

The cycle begins with the falling edge of $\overline{CS}$. This point is indicated as **a** in Figure 21. With the falling edge of $\overline{CS}$, the input signal is sampled and the conversion process is initiated. The device outputs data while the conversion is in progress. The data word contains two leading zeros, followed by 12-bit data in MSB first format and padded by two lagging zeros.

The falling edge of $\overline{CS}$ clocks out the first zero, and a second zero is clocked out on the first falling edge of the clock. Data is in MSB first format with the MSB being clocked out on the 2nd falling edge. Data is padded with two lagging zeros as shown in Figure 21. The conversion ends on the first rising edge of SCLK after the 13th falling edge. At this point the device enters the acquisition phase. This point is indicated by **b** in Figure 21.

Figure 21 shows the device data is read in a sixteen clock frame. However, $\overline{CS}$ can be asserted (pulled high) any time after point **b**. SDO goes to 3-state with the $\overline{CS}$ high level. The next conversion should not be started (by pulling $\overline{CS}$ low) until the end of the quiet sampling time (t_q) after SDO goes to 3-state or until the minimum acquisition time (t_{acq}) has elapsed. To continue normal operation, it is necessary that $\overline{CS}$ is not pulled high until point **b**. Without this, the device does not enter the acquisition phase and no valid data is available in the next cycle. (Also refer to the Power-Down Mode section for more details.) $\overline{CS}$ going high any time during the conversion aborts the ongoing conversion and SDO goes to 3-state.

The high level of the digital input to the device is not limited to device V_{DD}. This means the digital input can go as high as 5.5 V when the device supply is 2.7 V. This feature is useful when digital signals are received from another circuit with different supply levels. Also, this relaxes the restriction on power-up sequencing. However, the digital output levels (V_{OH} and V_{OL}) are governed by V_{DD} as listed in the Electrical Specifications table.

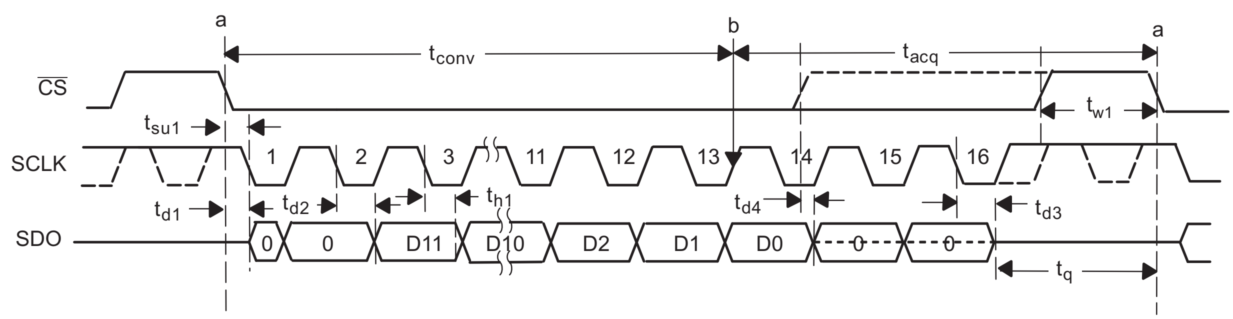


Figure 21. Interface Timing Diagram

POWER-DOWN MODE

The device enters power-down mode if $\overline{CS}$ goes high anytime after the 2nd SCLK falling edge to before the 10th SCLK falling edge. An ongoing conversion stops and SDO goes to 3-state under this power-down condition as shown in Figure 22.

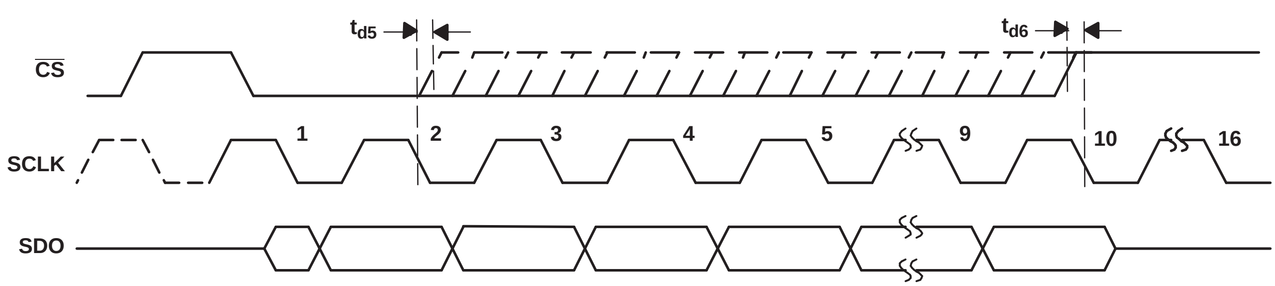


Figure 22. Entering Power-Down Mode

A dummy cycle with $\overline{CS}$ low for more than 10 SCLK falling edges brings the device out of power-down mode. For the device to reach the fully powered up condition requires 0.8 µs. $\overline{CS}$ can be pulled high any time after the 10th falling edge as shown in Figure 23. Note that the power-up time of 0.8 µs is more than a single conversion cycle at 3-MSPS speed. This means the device requires three dummy conversion frames at 3-MSPS speed or one elongated dummy conversion frame. The data during the dummy conversion frames is invalid.

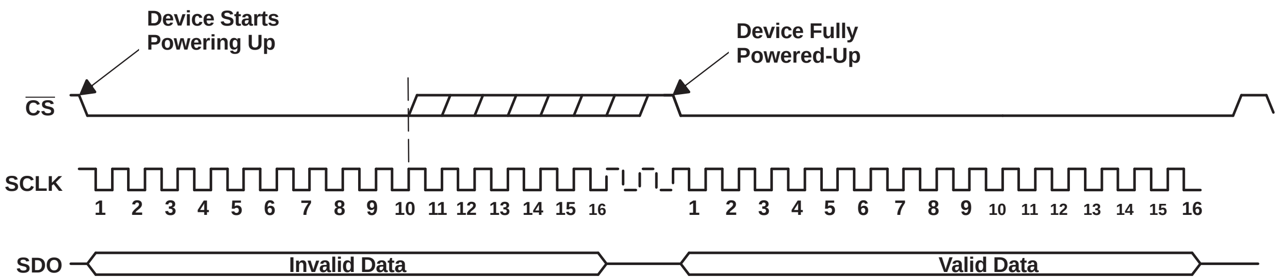


Figure 23. Exiting Power-Down Mode

APPLICATION INFORMATION

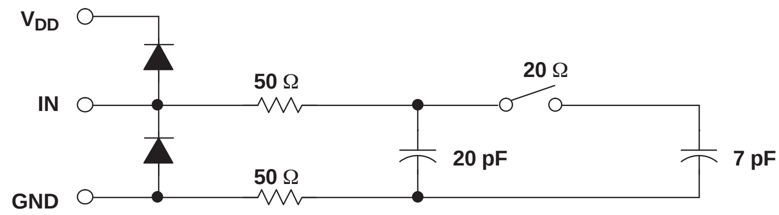


Figure 24. Typical Equivalent Sampling Circuit

Driving the VIN and V_{DD} Pins

The VIN input to the ADS7883 should be driven with a low impedance source. In most cases additional buffers are not required. In cases where the source impedance exceeds 200 Ω, using a buffer would help achieve the rated performance of the converter. The THS4031 is a good choice for the driver amplifier buffer.

The reference voltage for the ADS7883 A/D converter is derived from the supply voltage internally. The device offers limited low-pass filtering functionality on-chip. The supply to these converters should be driven with a low impedance source and should be decoupled to the ground. A 1-µF storage capacitor and a 10-nF decoupling capacitor should be placed close to the device. Wide, low impedance traces should be used to connect the capacitor to the pins of the device. The ADS7883 draws very little current from the supply lines. The supply line can be driven by either:

- Directly from the system supply.
- A reference output from a low drift and low drop out reference voltage generator like the REF5030 or REF5050. The ADS7883 can operate with a wide range of supply voltages. The actual choice of the reference voltage generator depends upon the system. Figure 26 shows one possible application circuit.
- A low-pass filtered version of the system supply followed by a buffer like the zero-drift OPA735 can also be used in cases where the system power supply is noisy. Care should be taken to ensure that the voltage at the V_{DD} input does not exceed 7 V (especially during power up) to avoid damage to the converter. This can be done easily using single supply CMOS amplifiers like the OPA735. Figure 27 shows one possible application circuit.

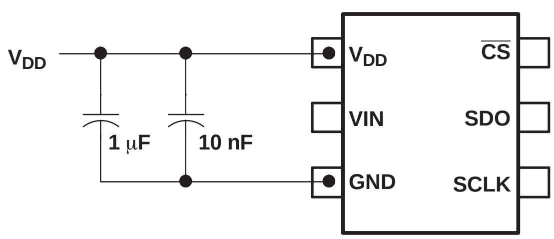


Figure 25. Supply/Reference Decoupling Capacitors

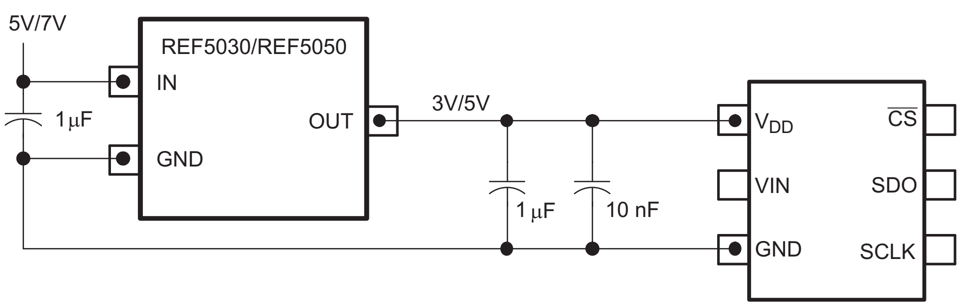


Figure 26. Using the REF5030/REF5050 Reference

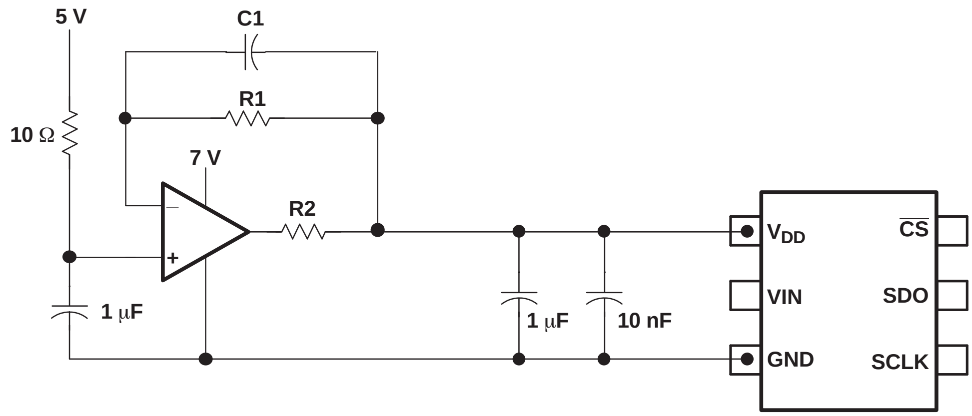


Figure 27. Buffering with the OPA735

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7883SBDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	7883	Samples
ADS7883SBDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	7883	Samples
ADS7883SDBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	7883	Samples
ADS7883SDBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	SN	Level-2-260C-1 YEAR	-40 to 125	7883	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

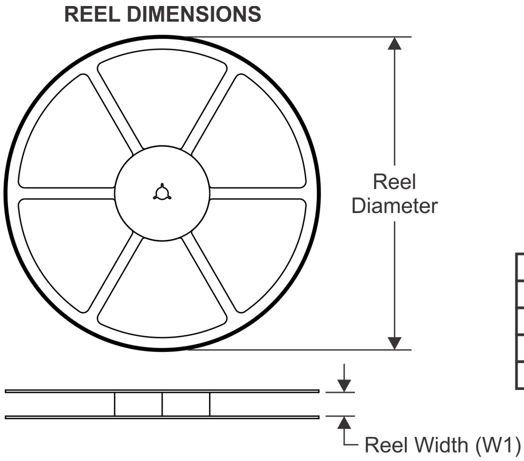
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

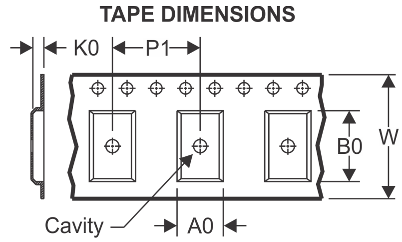
Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

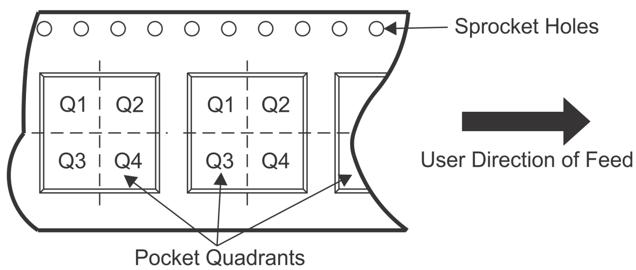
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION





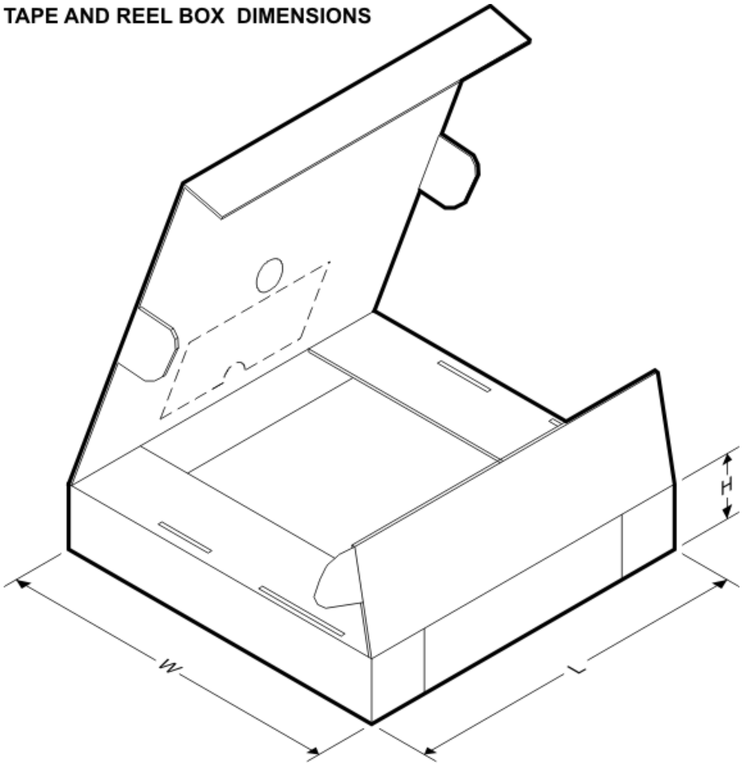
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

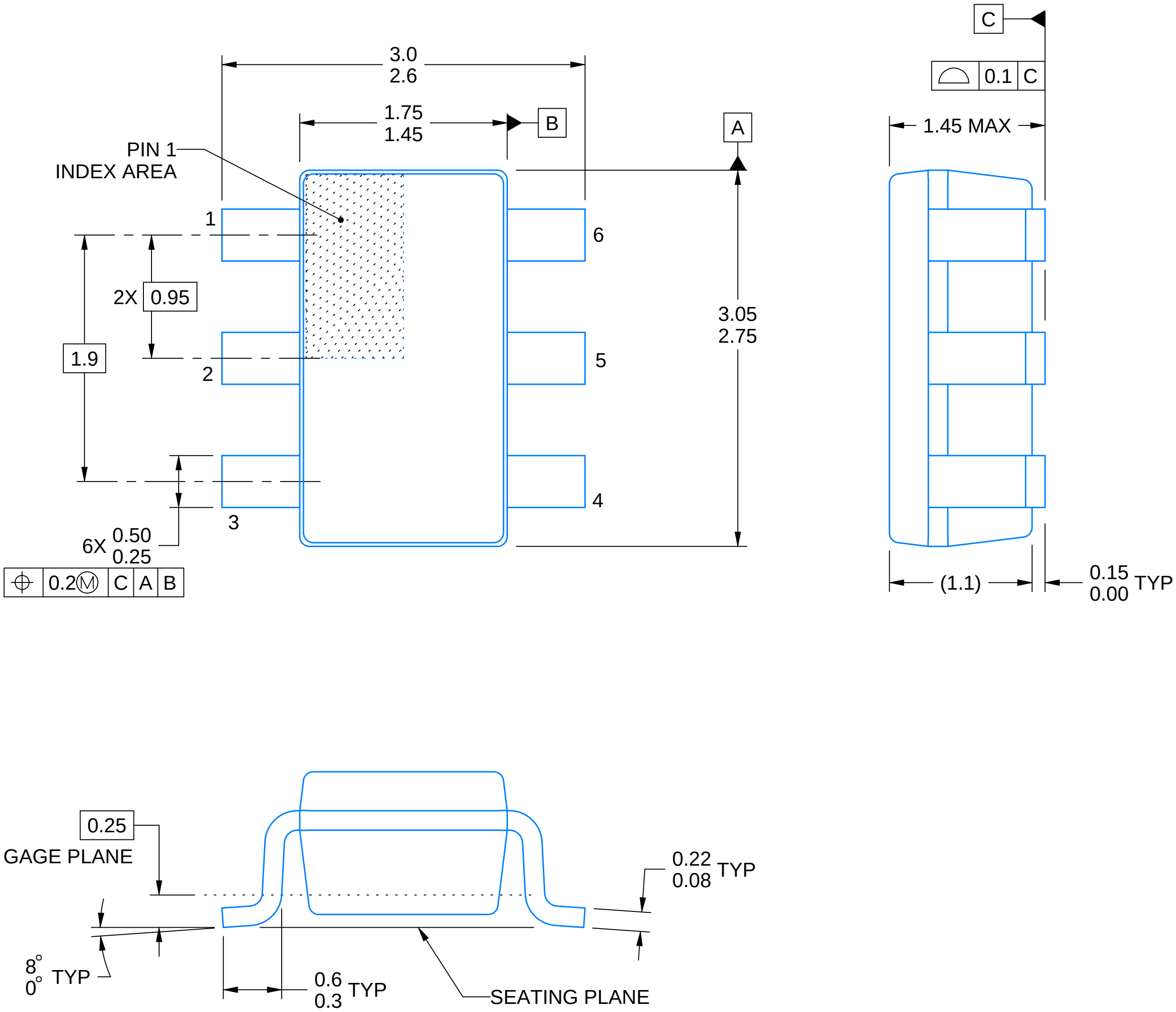
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7883SBDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SBDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADS7883SDBVT	SOT-23	DBV	6	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

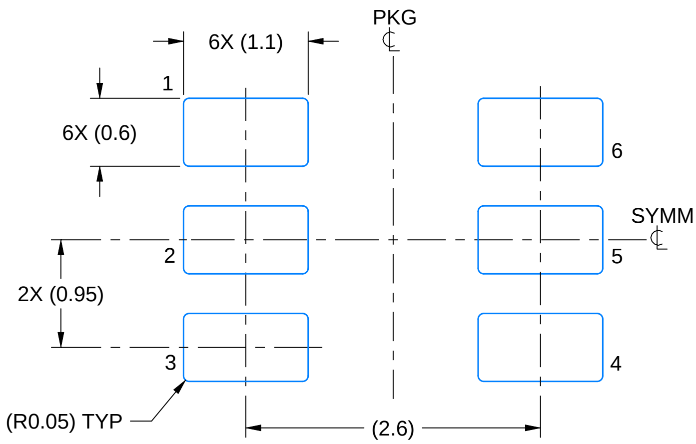
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7883SBDBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
ADS7883SBDBVT	SOT-23	DBV	6	250	195.0	200.0	45.0
ADS7883SDBVR	SOT-23	DBV	6	3000	195.0	200.0	45.0
ADS7883SDBVT	SOT-23	DBV	6	250	195.0	200.0	45.0



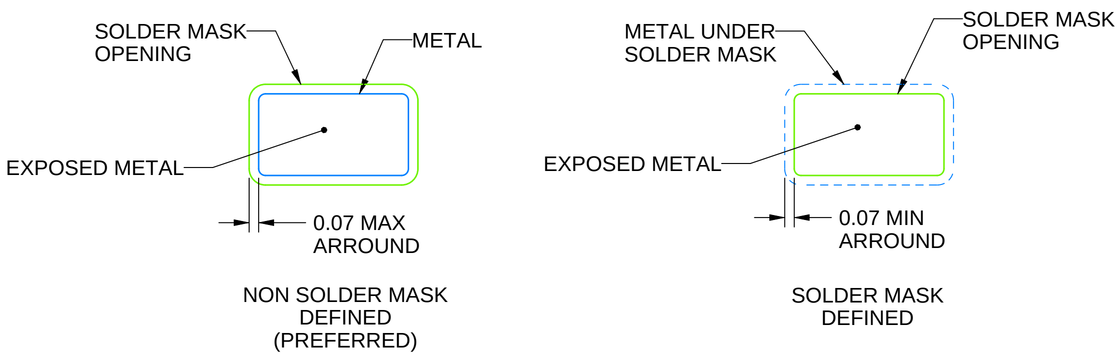
4214840/B 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

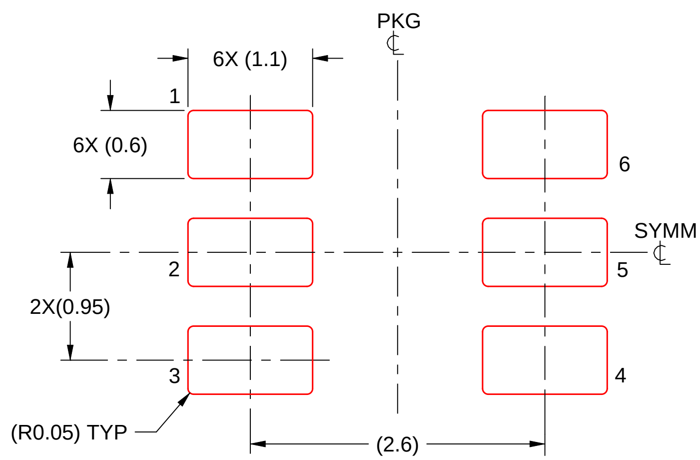


SOLDER MASK DETAILS

4214840/B 03/2018

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/B 03/2018

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER