ADT7351

Data Sheet

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Revision History

Rev. Number	Date	Rev. Contents
0.0	2011. 10. 31	Initial version

General Description

The ADT7351 is a step-down converter with integrated switching MOSFET. It operates wide input supply voltage range from 4.5V to 28V with 3A continuous output current. It includes current limiting protection and thermal shutdown.

It reduces design complexity and external component count. The ADT7351 is available in small outline SOP8-PP(with Exposed pad) package.

Package outline of the ADT7351

Features

- Current mode buck regulator with 925kHz fixed frequency
- Input voltage range : 4.5V to 28V
- Adjustable output range : 0.92V to 21V
- Continuous output current : 3A
- Up to 92% efficiency
- Integrated Power MOSFET switch : 80mΩ
- 10㎂ shutdown mode
- Thermal shutdown & current limit protection
- Under Voltage LOckout

Applications

- Distributed Power Systems
- Set-Top Boxes (STB)
- Surveillance Camera Modules
- Pre-regulator for Linear regulators
- Cigarette Lighter Powered Devices
- Battery Chargers

Typical Application Circuit

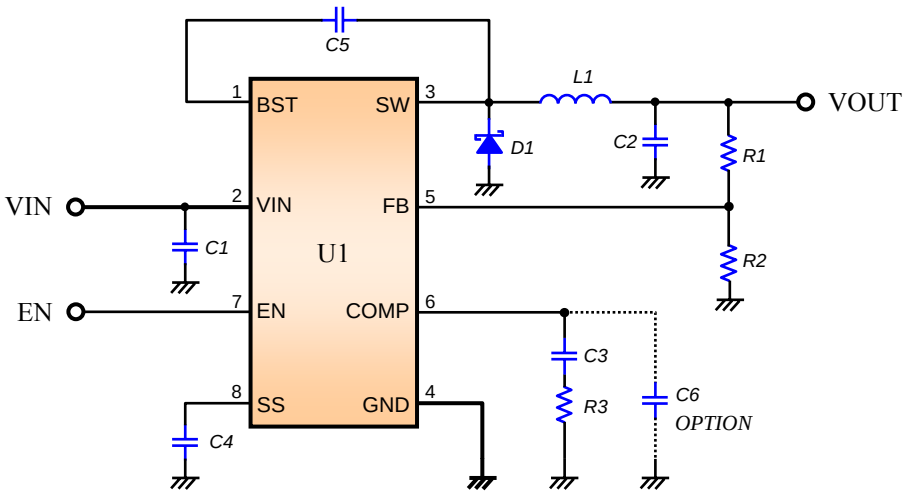

Figure 1. Typical Application Circuit (3.3V output)

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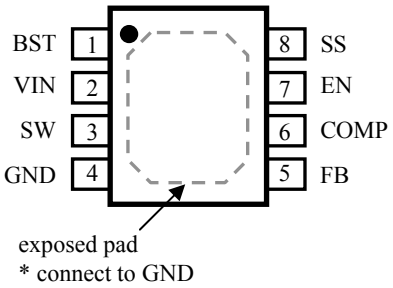
Part List

Component	Type	Value (Model)	Manufacturer
U1	IC	ADT7351	ADTech
D1	Schottky Barrier Diode	B330A	DIODES
L1	Chip inductor	4.7uH / 3.6A	TDK
C1	MLCC	10㎌ / 50V	-
C2	MLCC	47㎌ / 6.3V	-
C3	MLCC	10㎋	-
C4	MLCC	100㎋	-
C5	MLCC	10㎋	-
R1	Chip resistor	28kΩ / 1%	-
R2	Chip resistor	11kΩ / 1%	-
R3	Chip resistor	7.5kΩ / 5%	-

Pin Description

Pin No.	Name	Description
1	BST	High-Side Gate Drive Boost Input. This pin acts as the power supply of high-side gate driving blocks. Connect a 10nF or greater capacitor between SW and BST pin.
2	VIN	Power supply input. Bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3	SW	Switching node. The free-wheeling diode is connected between SW and GND.
4	GND	Ground. Connect the exposed pad on backside to GND.
5	FB	Feedback voltage input. The regulated FB voltage is 0.92V typically.
6	COMP	Compensation node. COMP is used to compensate the regulation control loop.
7	EN	Chip enable input. Also this pin functions UVLO input.
8	SS	Soft start control node. This pin controls the soft start period.



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Functional Block Diagram

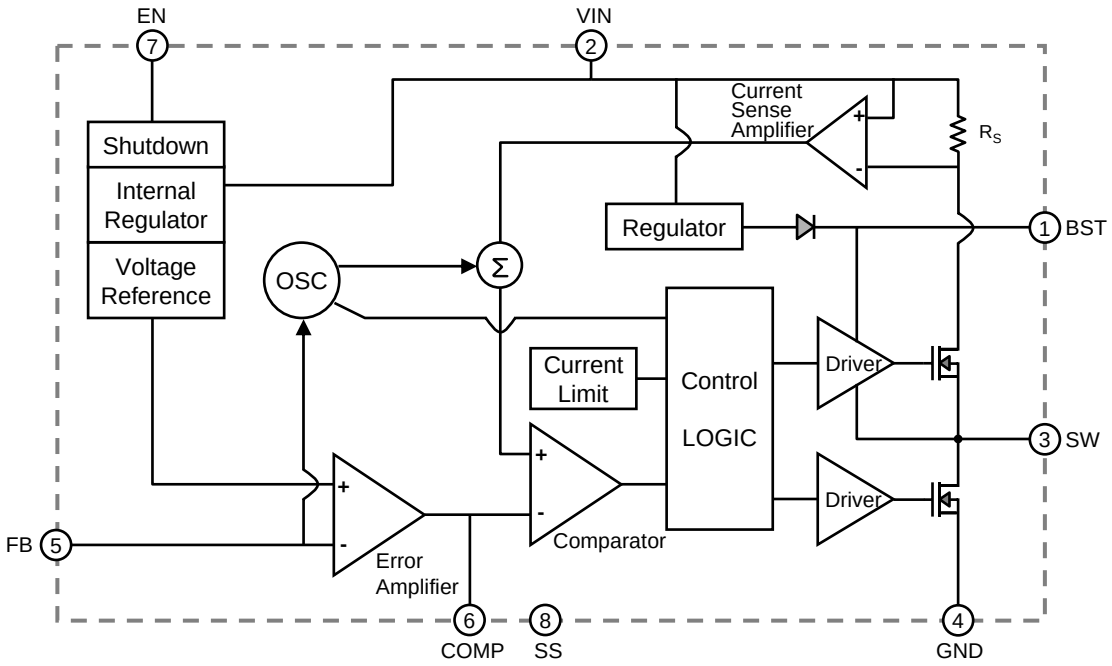

Figure 2. Functional Block Diagram

Absolute Maximum Ratings (Note1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{IN}	-0.3	-	30	V
SW pin voltage	V_{SW}	-0.5	-	V_{IN} + 0.3	V
BST pin voltage	V_{BST}	-0.3	-	V_{SW} + 6	V
All Other Pins	-	-0.3	-	+6	V
Max. power dissipation (Ta=25℃) (Note2)	P_D	-	-	2.08	W
Thermal resistance (Note3)	Θ_{JA}	-	60	-	℃/W
Storage temperature	T_{STG}	-65	-	+150	℃
Junction temperature	$T_{J.MAX}$	-	-	+150	℃

Note1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
Note2. Derate 17mW/℃ above +25℃. This is recommended to operate under this power dissipation specification.
Note3. Measured on JESD51-7, 4-layer PCB

Operating Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{IN}	4.5	12.0	28.0	V
Output voltage	V_{OUT}	0.92	-	21	V
Operating temperature	T_{OPR}	-40	-	+85	℃
Junction temperature	T_J	-	-	+125	℃

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Electrical Characteristics (Ta=25℃, V_{IN}=12V, unless otherwise noted)

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply current (shutdown)	I_{OFF}	V_{EN} = 0V	-	10	19	μA
Supply current (quiescent)	I_Q	V_{EN} = 3V, V_{FB} = 1.4V	-	0.7	1.0	mA
Feedback voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 28V, V_{COMP} < 2V	0.890	0.920	0.950	V
Error Amplifier Voltage Gain	A_{EA}	-	-	750	-	V/V
Error Amplifier Transconductance	G_{EA}	ΔI_{COMP} = ±10μA	-	750	-	μA/V
High-Side Switch On Resistance (Note4)	$R_{ON.H}$	-	-	80	-	mΩ
Low-Side Switch On Resistance (Note4)	$R_{ON.L}$	-	-	10	-	Ω
High-Side Switch Leakage Current		V_{EN} = 0V , V_{SW} = 0V	-	0.1	10	μA
Current Limit (Note4)		-	-	5.5	-	A
Current sense to COMP transconductance	G_{CS}	-	-	6	-	A/V
Oscillator frequency	F_{SW}	-	-	925	-	kHz
Fold-back frequency		V_{FB} = 0V	-	125	-	kHz
Maximum Duty cycle	D_{MAX}	V_{FB} = 0.8V	76	81	99	%
Minimum On time	T_{ON}	-	-	100	-	ns
UVLO rising threshold		V_{EN} rising	2.00	2.35	2.70	V
UVLO threshold hysteresis		-	-	250	-	mV
EN threshold voltage		-	0.8	1.1	1.4	V
Enable pull-up current		V_{EN} = 0V	0.5	2.0	3.5	μA
Soft-Start Period		C4 = 100nF, L1=4.7uH C2=47uF, IO=3A (CC)	-	7.5	-	ms
Thermal shutdown (Note4)		-	-	148	-	℃

Note4. guaranteed by design.

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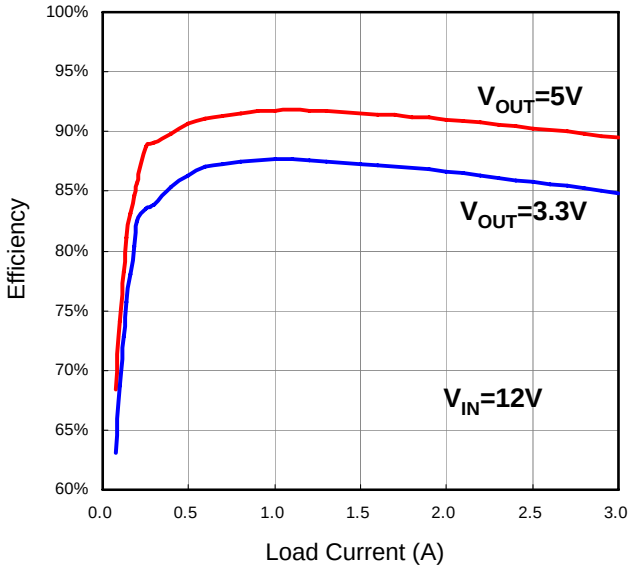
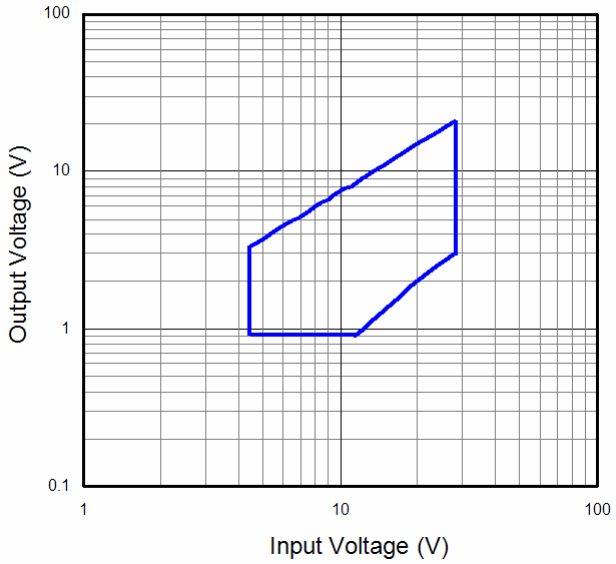
Typical Operating Characteristics

VIN=12V, C1=10uF, C2=2 x 22uF, L1=10uH and Ta=25℃, unless otherwise noted

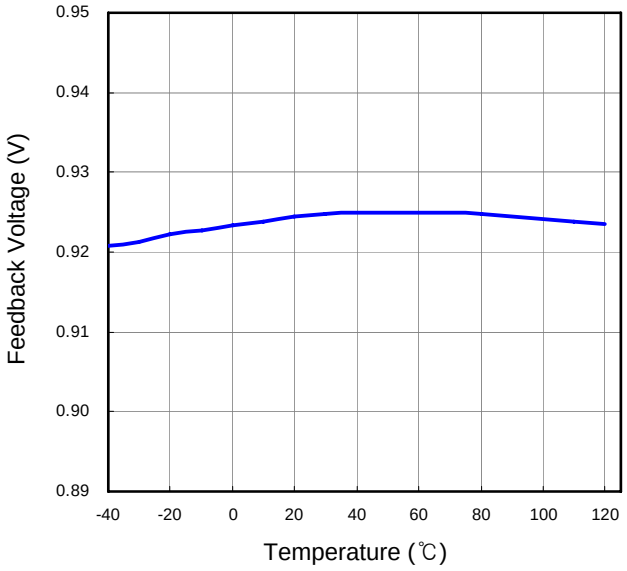
Efficiency



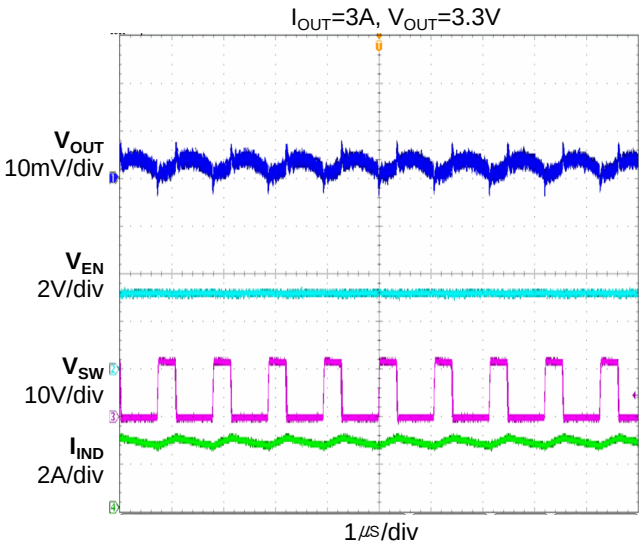
Operating Range



VFB vs Die Temperature



Steady State Operation



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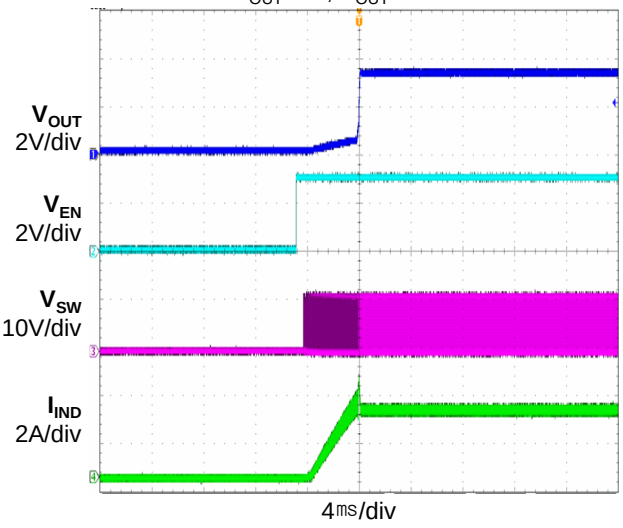
Typical Operating Characteristics (continued)

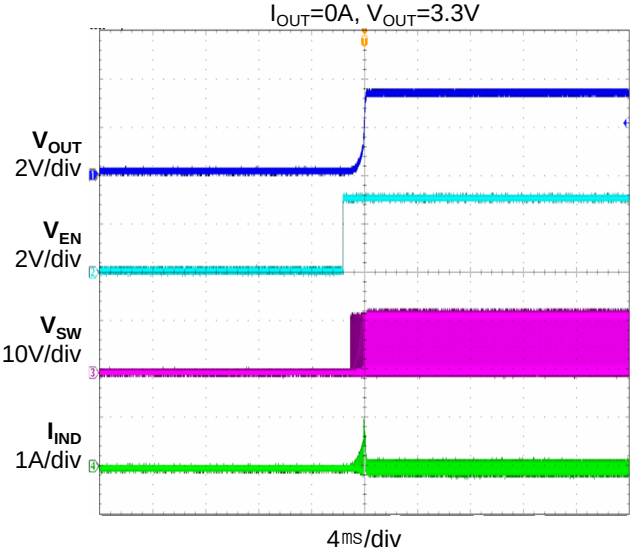
Startup Through Enable

I_{OUT}=3A, V_{OUT}=3.3V



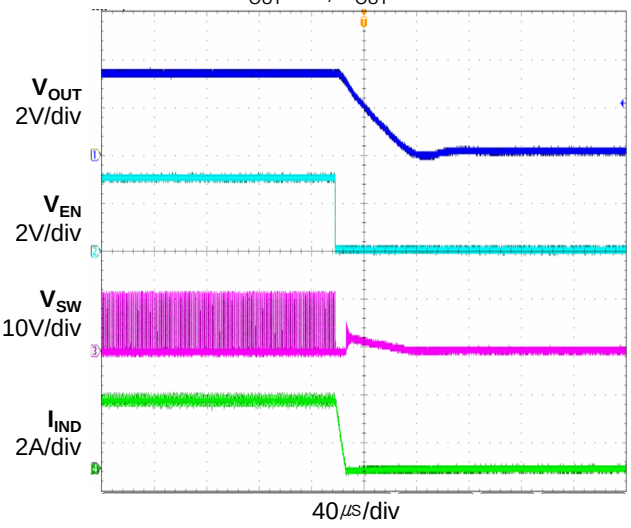
Startup Through Enable

I_{OUT}=0A, V_{OUT}=3.3V

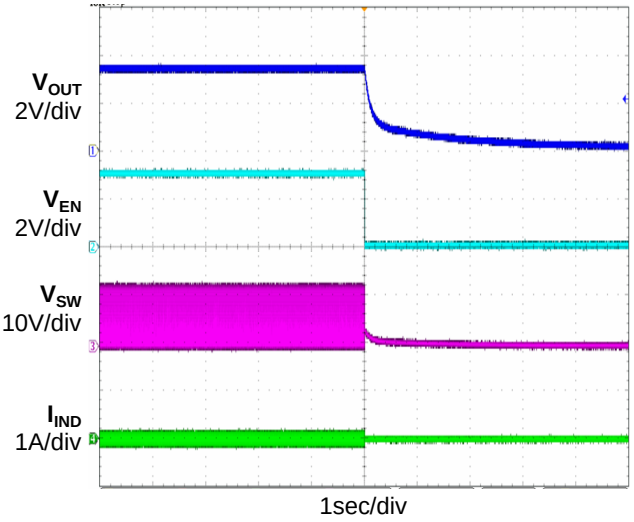


Shutdown Through Enable

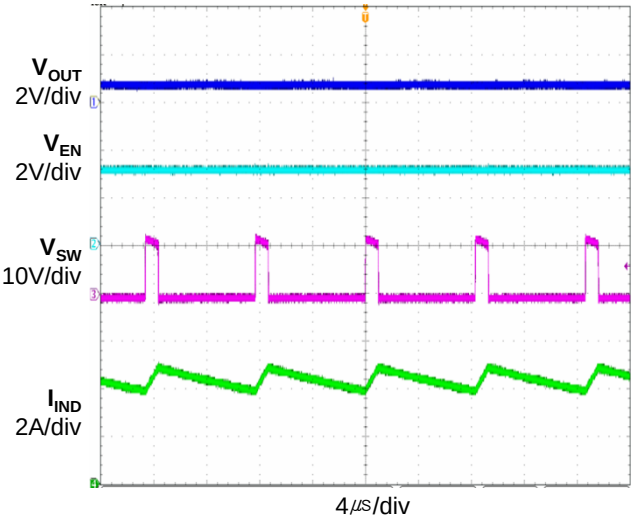
I_{OUT}=3A, V_{OUT}=3.3V



Shutdown Through Enable



SHORT



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OVERVIEW

The ADT7351 is a current mode step-down converter with integrated high side NMOS power switch. It operates from a 4.5V to 28V input voltage range and supplies up to 3A of load current. Features include enable control, under voltage lockout, programmable soft start, current limit and thermal shutdown protection. The ADT7351 uses current mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal error amplifier. The error amplifier output voltage is compared to the internally sensed load current and consequently generated PWM signal. The PWM signal has the information of the input and output voltage relationship and therefore output voltage is regulated by its PWM signal control function.

DETAILED DESCRIPTION

Enable and Soft Start

EN pin of the ADT7351 operates both chip enable and UVLO function. EN pin voltage under 800mV shuts down all the chip function except for pulling up EN pin. When the EN pin voltage exceeds 1.1V, the internal regulator will be enabled and the soft start capacitor will begin to charge. A EN pin voltage over 2.7V enables all the operations including switching function. When the EN pin is floating, EN voltage is high for its pull-up function.

The soft start function is adjustable. When the EN pin becomes high, a tens of μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The soft start time is adjusted by changing capacitance of C4 and the typical soft start time is 7.5msec at 100nF of C4.

Switching Frequency

The ADT7351 switching frequency is fixed and set by an internal oscillator. The practical switching frequency could range from 777kHz to 1050kHz due to device variation. If the FB voltage is under 0.3V, the switching frequency is changed to 125kHz for reducing abrupt inrush current.

Power Boosting

The ADT7351 uses an internal NMOS power switch to step-down the input voltage to the regulated output voltage. Since the NMOS power switch requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BST drives the gate. The capacitor is internally charged when SW is low.

Error Amplifier

The high gain error amplifier extracts the difference between the reference voltage and the feedback voltage. This extracted difference, called error signal, amplified and fed into the COMP, which is for compensation. The feedback voltage is regulated to the reference voltage, typical 0.92V for the ADT7351.

Current Sensing

The current sensing output is proportional to the current flowing into the inductor, This output goes to the comparator to make a proper PWM control signal. This output waveform resembles normally ramp shape.

Current Limit Protection

The output over-current protection (OCP) is implemented using a cycle-by-cycle peak detect control circuit. The switch current is monitored by measuring the high side NMOS switch current. The measured switch current is compared against a preset voltage which represents the current limit, between 3.3A and 7A. When the output current is more than current limit, the high side switch will be turned off and PWM duty is reduced. The output current is monitored in the same manner at each cycle and finally the power switch almost turned off not to be damaged under fault conditions.

APPLICATION INFORMATION

Figure 1 is the typical ADT7351 application circuit. And Figure 2 is the functional block diagram of the ADT7351. For the application information, refer to the Figure 1 & 2 unless otherwise noted.

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better divider resistors. output voltage is calculated by the below equation.

$$V_{OUT} = 0.92 \times \left(1 + \frac{R_1}{R_2}\right)$$

Usually, a design is started by setting a fixed R_2 value and calculating the required R_1 with upper equation. Some standard value of R_1, R_2 and most frequently used output voltage values are listed in below Table.

Table 1. Standard Output Voltage Setting

VOUT (V)	R1 (kΩ)	R2 (kΩ)
1.0	1.0	11
1.2	3.4	11
1.8	10.5	11
2.5	18.7	11
3.3	28.0	11
4.2	39.0	11
5.0	48.7	11
12.0	133.0	11

To improve efficiency at very light loads consider using larger value resistors. Note too high of resistance will be more susceptible to noise and voltage errors from the FB input current will be more noticeable.

Inductor

The inductor required to supply constant current to the output load when it is driven by a switching voltage. For given input and output voltage, inductance and switching frequency together decide the inductor ripple current, that is:

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The peak inductor current is:

$$I_{L.peak} = I_{OUT} + \frac{\Delta I_L}{2}$$

Higher inductance gives low inductor ripple current but requires larger size inductor to avoid saturation. Low ripple current reduces inductor core losses. Also it reduces RMS current through inductor and switches, which results in less conduction loss. Usually, peak to peak ripple current on inductor is designed to be 20% to 30% of the output current limit. Make sure it is capable to handle the peak current without saturation.

Surface mount inductors in different shape and styles are available from TDK, TOKO and Murata. Shielded inductors are small and radiate less EMI noise. But they cost more than unshielded inductors. The choice depends on EMI requirement, price and size.

Output Freewheeling Diode

When the high side switch is off, freewheeling diode supplies the current to the inductor. The forward voltage and reverse recovery times of the freewheeling diode are the key loss factors, so schottky diode is mostly used for the freewheeling diode. Choose a diode whose maximum reverse voltage rating is greater than the maximum input voltage, and whose current rating is greater than the maximum load current.

APPLICATION INFORMATION (continued)

Input Capacitor

The input capacitor is used to filter out discontinuous, pulsed input current and to maintain input voltage stable. Therefore input capacitor should be able to supply the AC current to the step-down converter. Its input ripple voltage can be estimated by:

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where, CIN is input capacitor value.

The voltage rating of input capacitor must be greater than the maximum input voltage plus ripple voltage.

Since the input capacitor absorbs the input switching current, it requires an proper ripple current rating. The RMS current in the input capacitor can be approximated by:

$$I_{CIN\_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worst-case condition occurs at $V_{IN}=2 \times V_{OUT}$ (50% duty condition), and its worst RMS current is approximately half of the I_{OUT}. For reliable operation and best performance, the input capacitors must have current rating higher than I_{CIN_RMS} at worst operating conditions. Ceramic capacitors are preferred for input capacitors because of their low ESR and high current rating. When selecting ceramic capacitors, X5R or X7R type dielectric ceramic capacitors should be used for their better temperature and voltage characteristics.

Output Capacitor

The output capacitor is required to maintain the DC output voltage. In a step-down converter circuit, output ripple voltage is determined by the inductor value, switching frequency, output capacitor value and ESR. That is:

$$\Delta V_{OUT} = \Delta I_L \times \left(ESR + \frac{1}{8 \times F_{SW} \times C_O}\right)$$

where,

C_O is output capacitor value,

ESR is the equivalent series resistance of the output capacitor.

Low ESR capacitors are preferred to keep the output voltage ripple low. When low ESR ceramic capacitor is used as output capacitor, its ESR value can be waived. So, the impedance at the switching frequency is dominated by the capacitance. Therefore the output voltage ripple is:

$$\Delta V_{OUT} = \Delta I_L \times \left(\frac{1}{8 \times F_{SW} \times C_O}\right)$$

On the other hand, in the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. In this case, the output voltage ripple is:

$$\Delta V_{OUT} = \Delta I_L \times (ESR)$$

In a step-down converter, output capacitor current is continuous. Usually, the ripple current rating of the output capacitor is not concerned because of its low ripple current.

APPLICATION INFORMATION (continued)

Loop Compensation

The ADT7351 uses a fixed frequency, peak current mode control scheme to provide easy compensation and fast transient response. Peak current mode control eliminate the double pole effect of the output LC filter. Therefore, the step-down converter can be simplified to be a one-pole system in frequency domain.

The goal of compensation design is to shape the converter transfer function to get the desired gain and phase. System stability is provided with the addition of a simple series capacitor-resistor from COMP to GND. This pole-zero combination serves to adjust the desired response of the closed-loop system.

The DC gain of the voltage feedback loop is given by:

$$A_{VDC} = \frac{V_{FB}}{V_{OUT}} \times A_{EA} \times G_{CS} \times R_L$$

Where A_{EA} is the error amplifier voltage gain. G_{CS} is the current sense transconductance and R_L is the load resistor value.

The system has two dominant poles. One is made by the combination of both the output resistor of the error amplifier and the compensation capacitor (C3). And the other is due to the output capacitor and the load resistor. These poles are expressed as:

$$f_{P1} = \frac{G_{EA}}{2\pi \times C3 \times A_{EA}}$$

$$f_{P2} = \frac{1}{2\pi \times C_O \times R_L}$$

where, GEA is the error amplifier transconductance.

For a stable one-pole converter system, one of two dominant poles needs to be eliminated by one zero. One zero made by the series capacitor-resistor (R3-C3) cancels f_{P2} out. This zero is:

$$f_{Z1} = \frac{1}{2\pi \times C3 \times R3}$$

If the output capacitor has a large capacitance and/or a high ESR value, unwanted zero is generated to the location of:

$$f_{Z2} = \frac{1}{2\pi \times C_O \times ESR}$$

In this case, third pole is needed to compensate f_{Z2}. This pole, f_{P3}, is made by the R3 and the selectively added optional capacitor (C6) between COMP to GND. f_{P3} is expressed to:

$$f_{P3} = \frac{1}{2\pi \times C6 \times R3}$$

The system crossover frequency (Fc), where the feedback loop has the unity gain, is important. The system crossover frequency is called the converter bandwidth. Generally higher Fc means faster transient response and load regulation. However, higher Fc could cause system unstable. A standard rule of thumb sets the crossover frequency to be equal or less than 1/10 of switching frequency (for the ADT7351, this is approximately 80kHz for the 925kHz fixed switching frequency).

Table 2 lists the typical values of compensation components for some standard output voltages. The values of the compensation components have been optimized for fast transient response and good stability at given conditions.

APPLICATION INFORMATION (continued)

Table 2. Compensation values for standard output voltage/capacitor combinations

VOUT (V)	R3 (kΩ)	C3 (nF)	C6 (pF)	L1 (uH)	C2 (μF)
1.0	1.5	18	None	1	47
1.2	2.4	12	None	1	47
1.8	3.9	10	None	2.2	47
2.5	5.1	10	None	2.2 ~ 4.7	47
3.3	7.5	10	None	2.2 ~ 4.7	47
4.2	8.2	10	None	4.7	47
5.0	15	8.2	51	4.7 ~ 6.8	2 x 22
12.0	22	5.6	51	6.8 ~ 10	2 x 22

A general procedure to choose the compensation components for conditions is following:

1. Select the desired crossover frequency. Set the crossover frequency to be equal or less than 1/10 of switching frequency. For the ADT7351, this is approximately 80kHz for the 925kHz fixed switching frequency.

2. Select R3 (compensation resistor) to operate the desired crossover frequency in a given condition. R3 value is calculated by the following equation:

$$R3 = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times F_C \times C2 \times (ESR + R_L)}{G_{EA} \times G_{CS} \times R_L}$$

For R_L much greater than ESR of the output capacitor (C2), the equation can be simplified as follows:

$$R3 = \frac{V_{OUT}}{V_{FB}} \times \frac{2\pi \times F_C \times C2}{G_{EA} \times G_{CS}}$$

Most cases, especially for the ceramic capacitors, ESR of the output capacitor is much lower than R_L, so this equation is good approximation.

3. Select C3 (compensation capacitor) to achieve the desired loop phase margin. C3 determines the desired first system zero, f_{Z1}. Typically, set f_{Z1} below 1/4 of the Fc to provides sufficient phase margin. C3 value is calculated by:

$$C3 \geq \frac{4}{2\pi \times F_C \times R3}$$

4. If the ESR output zero (f_{Z2}) is located at less than one-half the switching frequency, use the (optional) secondary compensation capacitor (C6) to cancel it. As $f_{P3}=f_{Z2}$, then:

$$C6 = \frac{C2 \times ESR}{R3}$$

APPLICATION INFORMATION (continued)

Thermal Management

The ADT7351 contains an internal thermal sensor that limits the total power dissipation in the device and protects it in the event of an extended thermal fault condition. When the die temperature exceeds +148°C typically, the thermal sensor shuts down the device, turning off the DC-DC converter to allow the die to cool. After the die temperature falls by 6°C typically, the device automatically restarts, using the soft-start sequence.

The ADT7351 is available in a thermally enhanced SOP package and can dissipate up to 1.25W at Ta=50°C (T_J=125°C). The exposed pad should be connected to GND externally, preferably soldered to a large ground plane to maximize thermal performance. Maximum available power dissipation should be de-rated by 17mW/℃ above Ta=25℃ not to damage the device.

PCB Layout Consideration

PCB layout is very important to achieve clean and stable operation. It is highly recommended to follow below guidelines for good PCB layout.

1. Input capacitor (C1) should be placed as near as possible to the IC and connected with direct traces.

2. Keep the high current paths as short and wide as possible.

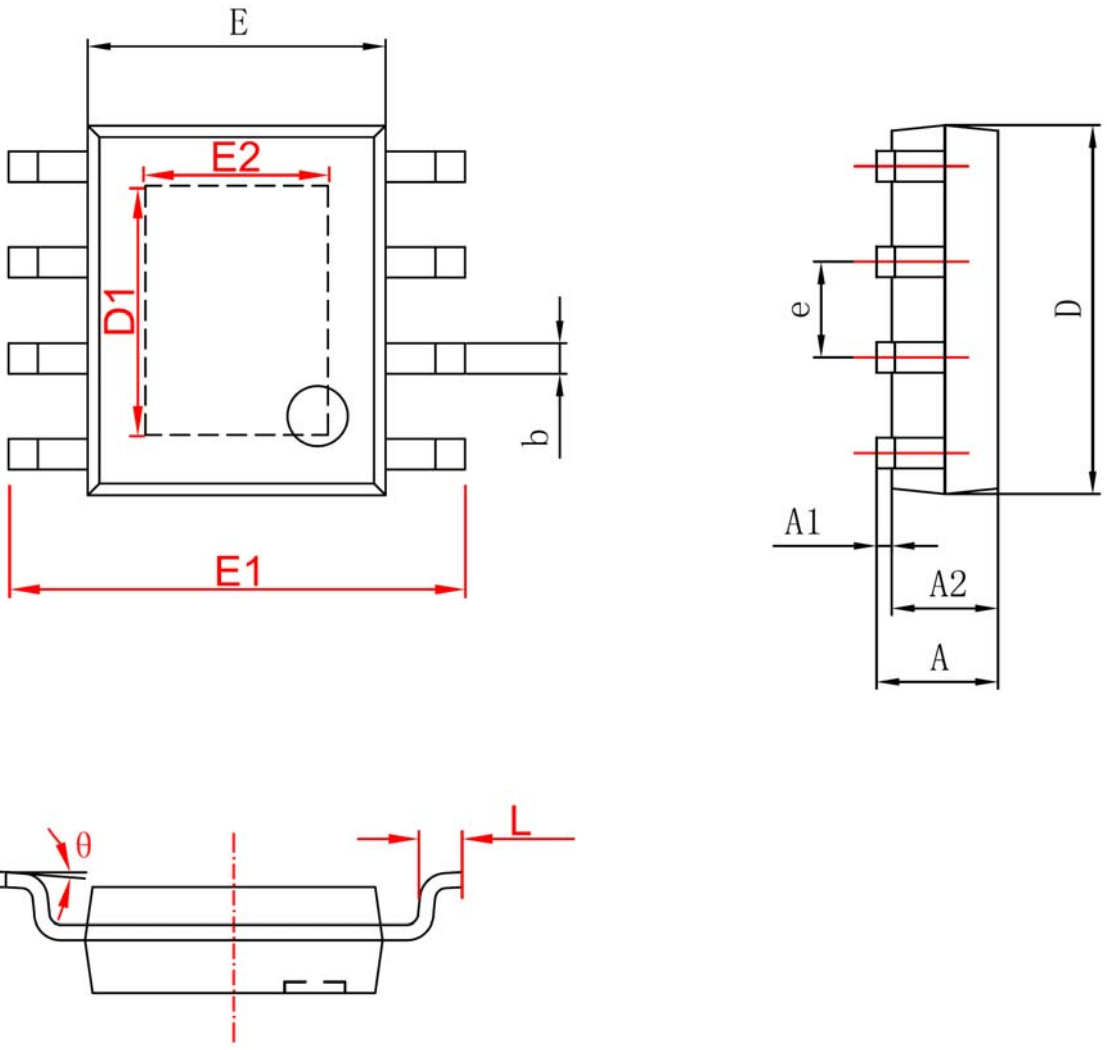
3. Keep the switching current path short and minimize the loop area, formed by SW, the output capacitors and the input capacitors.

4. Route high-speed switching nodes (such as SW and BST) away from sensitive analog areas (such as FB and COMP).

5. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close as possible to the IC.

6. Exposed pad of device must be connected to GND with solder. For single layer, do not solder exposed pad of the IC.

Package ; SOP8-PP , 4.9mm x 3.94mm body (units : mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0 °	8 °	0 °	8 °

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