Dual Port, Xpressview, 225 MHz HDMI Receiver

Data Sheet

ADV7612

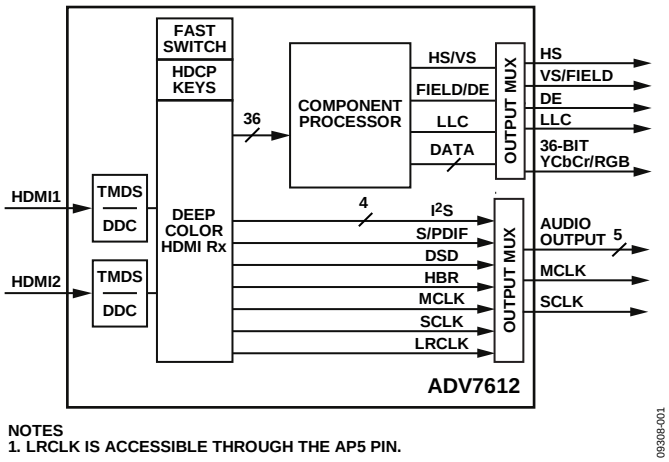
FEATURES

- High-Definition Multimedia Interface (HDMI®) 1.4a features supported
  - All mandatory and additional 3D video formats supported
  - Extended colorimetry, including sYCC601, Adobe RGB, Adobe YCC 601, xvYCC extended gamut color
  - CEC 1.4-compatible
- HDMI receiver
  - 225 MHz maximum TMDS clock frequency
  - Xpressview fast switching of HDMI ports
  - 36-/30-bit Deep Color and 24-bit color support
  - High-bandwidth Digital Content Protection (HDCP) 1.4 support with internal HDCP keys
  - HDCP repeater support
    - Up to 127 KSVs supported
  - Integrated CEC controller
  - Programmable HDMI equalizer
  - 5 V detect and Hot Plug assert for each HDMI port
- Audio support
  - Audio support including high bit rate (HBR) and direct stream digital (DSD)
  - S/PDIF (IEC 60958-compatible) digital audio support
  - Supports up to four I²S outputs
  - Advanced audio mute feature
  - Dedicated, flexible audio output port
  - Super audio CD (SACD) with DSD output interface
  - HBR audio
    - Dolby® TrueHD
    - DTS-HD Master Audio™
- General
  - Interrupt controller with two interrupt outputs
  - Standard Identification (STDI) circuit
  - Highly flexible 36-bit pixel output interface
  - Internal EDID RAM
  - Any-to-any 3 × 3 color space conversion (CSC) matrix
  - 2-layer PCB design supported
  - 100-lead LQFP_EP, 14 mm × 14 mm package
  - Qualified for Automotive Applications

APPLICATIONS

- Projectors
- Automotive
- Video conferencing
- HDTVs
- AVR, HTiB
- Soundbars
- Video switches

FUNCTIONAL BLOCK DIAGRAM



NOTES
1. LRCLK IS ACCESSIBLE THROUGH THE AP5 PIN.

Figure 1.

Advantiv
Advanced Television Solutions by Analog Devices

Rev. E Document Feedback

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GENERAL DESCRIPTION

The ADV7612 is offered in automotive, professional (no HDCP), and industrial versions. The operating temperature range is −40°C to +85°C.

The UG-216 contains critical information that must be used in conjunction with the ADV7612.

The ADV7612 is a high quality Xpressview™ fast switching HDMI®-capable receiver. It incorporates a dual input HDMI-capable receiver that supports all mandatory 3D TV formats defined in HDMI 1.4a specification, HDTV formats up to 1080p 36-bit Deep Color, and display resolutions up to UXGA (1600 × 1200 at 60 Hz).

It integrates a CEC controller that supports the capability discovery and control (CDC) feature.

The ADV7612 incorporates Xpressview fast switching on both input HDMI ports. Using Analog Devices, Inc., hardware-based HDCP engine that minimizes software overhead, Xpressview technology allows fast switching between both HDMI input ports in less than 1 second.

Each HDMI port has dedicated 5 V detect and Hot Plug™ assert pins. The HDMI receiver also includes an integrated programmable equalizer that ensures robust operation of the interface with long cables.

The ADV7612 offers a flexible audio output port for audio data extraction from the HDMI stream. HDMI audio formats, including SACD via DSD and HBR, are supported by ADV7612. The HDMI receiver has advanced audio functionality, such as a mute controller that prevents audible extraneous noise in the audio output.

The ADV7612 contains one main component processor (CP) that processes the video signals from the HDMI receiver. It provides features such as contrast, brightness and saturation adjustments, STDI detection block, free run, and synchronization alignment controls.

Fabricated in an advanced CMOS process, the ADV7612 is provided in a 14 mm × 14 mm, 100-lead surface-mount LQFP_EP, RoHS-compliant package, and is specified over the −40°C to +85°C temperature range.

DETAILED FUNCTIONAL BLOCK DIAGRAM

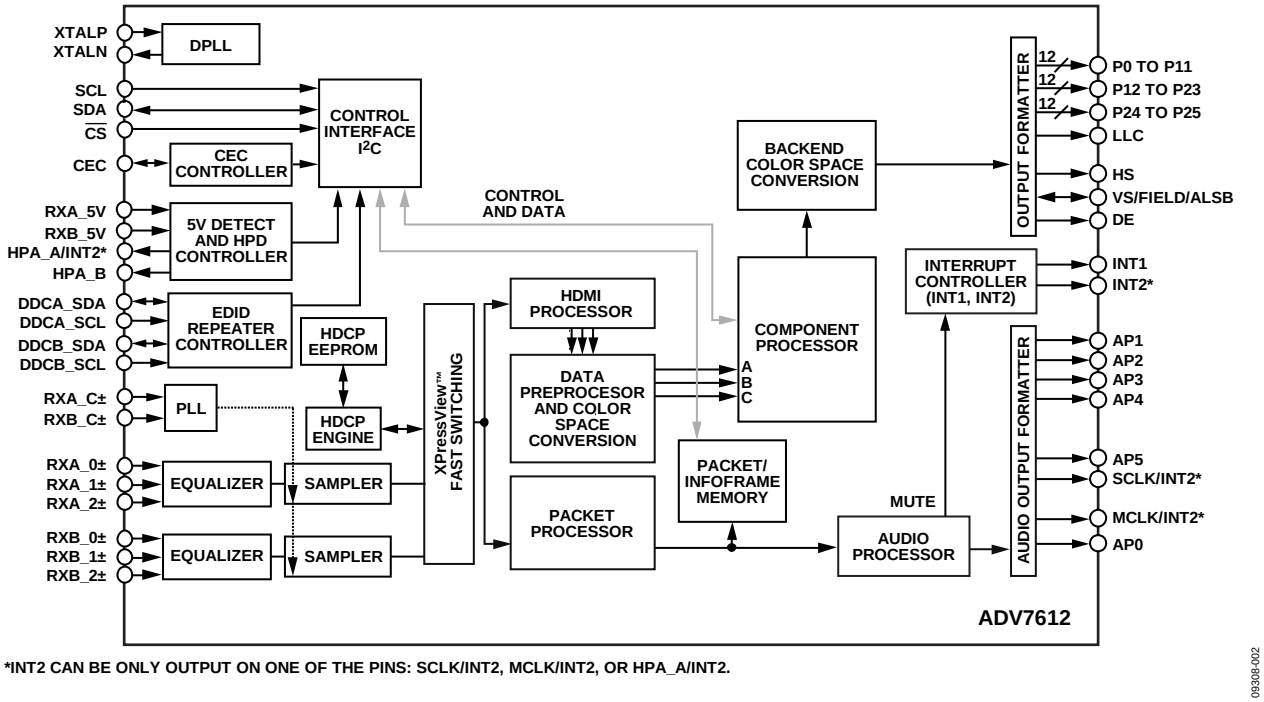

Figure 2. Detailed Functional Block Diagram

SPECIFICATIONS

At DVDD = 1.71 V to 1.89 V, DVDDIO = 3.14 V to 3.46 V, PVDD = 1.71 V to 1.89 V, TVDD = 3.14 V to 3.46 V, CVDD = 1.71 V to 1.89 V, Operating temperature range, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DIGITAL INPUTS[1]						
Input High Voltage	V_{IH}	XTALN and XTALP	1.2			V
	V_{IH}	Other digital inputs	2			V
Input Low Voltage	V_{IL}	XTALN and XTALP			0.4	V
	V_{IL}	Other digital inputs			0.8	V
Input Current	I_{IN}	$\overline{\text{RESET}}$ pin		±45	±60	µA
		$\overline{\text{CS}}$ pin		±45	±60	µA
		Other digital inputs		±10		µA
Input Capacitance	C_{IN}				10	pF
DIGITAL INPUTS (5 V TOLERANT)[1, 2]						
Input High Voltage	V_{IH}		2.6			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}		−82		+82	µA
DIGITAL OUTPUTS[1]						
Output High Voltage	V_{OH}		2.4			V
Output Low Voltage	V_{OL}				0.4	V
High Impedance Leakage Current	I_{LEAK}	VS/FIELD/ALSB pin		±35	±60	µA
		HPA_A/INT2, HPA_B pin			±82	µA
		Digital inputs other than XTALN and XTALP		±10		µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[3,4]						
Digital Core Power Supply	DVDD		1.71	1.8	1.89	V
Digital I/O Power Supply	DVDDIO		3.14	3.3	3.46	V
PLL Power Supply	PVDD		1.71	1.8	1.89	V
Terminator Power Supply	TVDD		3.14	3.3	3.46	V
Comparator Power Supply	CVDD		1.71	1.8	1.89	V
Digital Core Supply Current	I_{DVDD}	Dual 1080p60 12 bit with BG[5] port		149.5	201.9	mA
Digital I/O Supply Current	I_{DVDDIO}	Dual 1080p60 12 bit with BG[5] port		9.9	178.5	mA
PLL Supply Current	I_{PVDD}	Dual 1080p60 12 bit with BG[5] port		36.9	39.2	mA
Terminator Supply Current	I_{TVDD}	Dual 1080p60 12 bit with BG[5] port		121.4	134.5	mA
Comparator Supply Current	I_{CVDD}	Dual 1080p60 12 bit with BG[5] port		187.0	210.9	mA
POWER-DOWN CURRENTS[3,6]						
Digital Core Supply Current	I_{DVDD_PD}			0.3	0.4	mA
Digital I/O Supply Current	I_{DVDDIO_PD}			1.3	1.7	mA
PLL Supply Current	I_{PVDD_PD}			1.5	1.8	mA
Terminator Supply Current	I_{TVDD_PD}			0.1	0.3	mA
Comparator Supply Current	I_{CVDD_PD}			1.3	1.7	mA
Power-Up Time	t_{PWRUP}			25		ms

[1] Data guaranteed by characterization.
[2] The following pins are 5 V tolerant: DDCA_SCL, DDCA_SDA, DDCB_SCL, DDCB_SDA, RXA_5V, and RXB_5V.
[3] Data recorded during lab characterization
[4] Maximum current consumption values are recorded with maximum rated voltage supply levels, MoireX video pattern, and at maximum rated temperature.
[5] BG = background.
[6] Power-Down Mode 0 (IO map, Register 0x0C = 0x62), ring oscillator powered down (HDMI map, Register 0x48 = 0x01), and DDC pads off (HDMI map, Register 0x73 = 0x03).

DATA AND I²C TIMING CHARACTERISTICS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK AND CRYSTAL						
Crystal Frequency, XTALP				28.63636		MHz
Crystal Frequency Stability					±50	ppm
LLC Frequency Range			13.5		170	MHz
I²C PORTS						
SCL Frequency					400	kHz
SCL Minimum Pulse Width High[1]	t_1		600			ns
SCL Minimum Pulse Width Low[1]	t_2		1.3			µs
Start Condition Hold Time[1]	t_3		600			ns
Start Condition Setup Time[1]	t_4		600			ns
SDA Setup Time[1]	t_5		100			ns
SCL and SDA Rise Time[1]	t_6				300	ns
SCL and SDA Fall Time[1]	t_7				300	ns
Stop Condition Setup Time[1]	t_8		0.6			µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark-Space Ratio[1]	t_9:t_{10}		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS[2]						
Data Output Transition Time[1]	t_{11}	End of valid data to negative clock edge		1.0	2.2	ns
	t_{12}	Negative clock edge to start of valid data		0.0	0.3	ns
I²S PORT, MASTER MODE						
SCLK Mark-Space Ratio[1]	t_{15}:t_{16}		45:55		55:45	% duty cycle
LRCLK Data Transition Time[1]	t_{17}	End of valid data to negative SCLK edge			10	ns
	t_{18}	Negative SCLK edge to start of valid data			10	ns
I²S Data Transition Time[1]	t_{19}	End of valid data to negative SCLK edge			5	ns
	t_{20}	Negative SCLK edge to start of valid data			5	ns

[1] Data guaranteed by characterization.
[2] With the DLL block on output clock bypassed.

Timing Diagrams

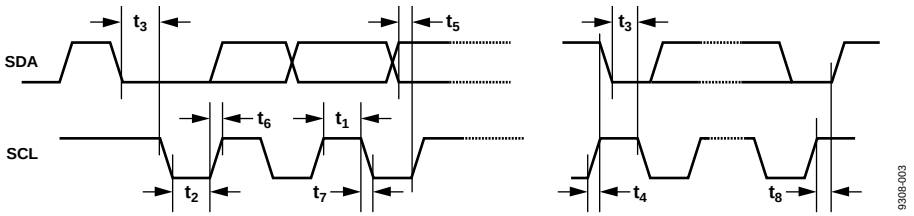

Figure 3. I²C Timing

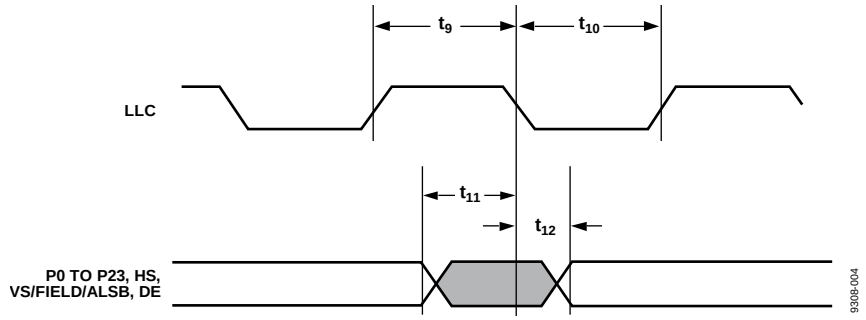

Figure 4. Pixel Port and Control SDR Output Timing

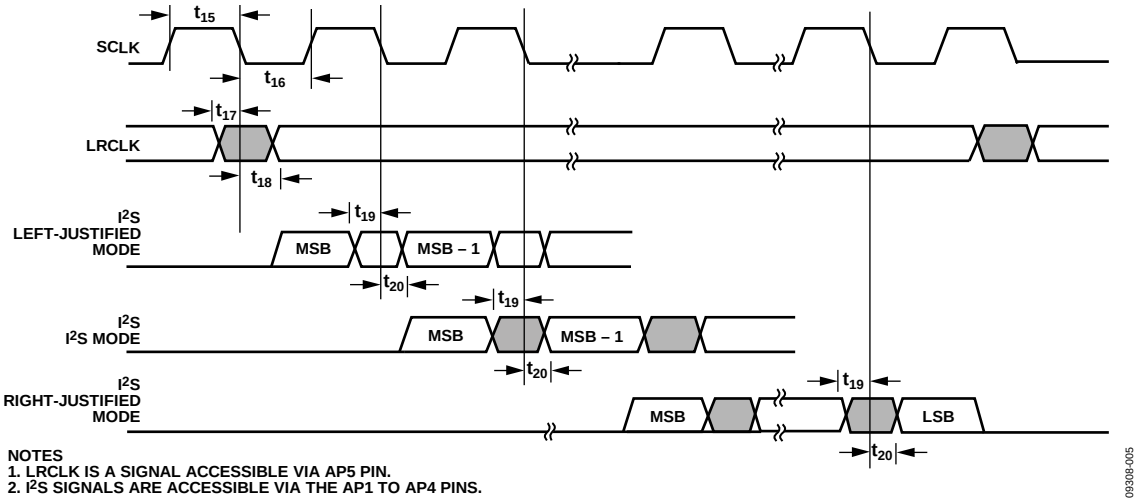

Figure 5. I²S Timing

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
DVDD to GND	2.2 V
PVDD to GND	2.2 V
DVDDIO to GND	4.0 V
CVDD to GND	2.2 V
TVDD to GND	4.0 V
Digital Inputs Voltage to GND	GND − 0.3 V to DVDDIO + 0.3 V
5 V Tolerant Digital Inputs to GND[1]	5.3 V
Digital Outputs Voltage to GND	GND − 0.3 V to DVDDIO + 0.3 V
XTALP, XTALN	−0.3 V to PVDD + 0.3 V
SCL/SDA Data Pins to DVDDIO	DVDDIO − 0.3 V to DVDDIO + 3.6 V
Maximum Junction Temperature ($T_{J\ MAX}$)	125°C
Storage Temperature Range	−60°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

[1] The following inputs are 3.3 V inputs but are 5 V tolerant: DDCA_SCL, DDCA_SDA, DDCB_SCL, and DDCB_SDA.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7612, the user is advised to turn off the unused sections of the part.

Due to the printed circuit board (PCB) metal variation and, therefore, variation in PCB heat conductivity, the value of θ_{JA} may differ for various PCBs.

The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this eliminates the variance associated with the θ_{JA} value.

The maximum junction temperature ($T_{J\ MAX}$) of 125°C must not be exceeded. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
T_S is the package surface temperature (°C).
Ψ_{JT} = 0.3°C/W for the 100-lead LQFP_EP.

W_{TOTAL} = ((PVDD × I_{PVDD}) + (0.05 × TVDD × I_{TVDD}) + (CVDD × I_{CVDD}) + (DVDD × I_{DVDD}) + (DVDDIO × I_{DVDDIO}))

where 0.05 is 5% of the TVDD power that is dissipated on the part itself.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

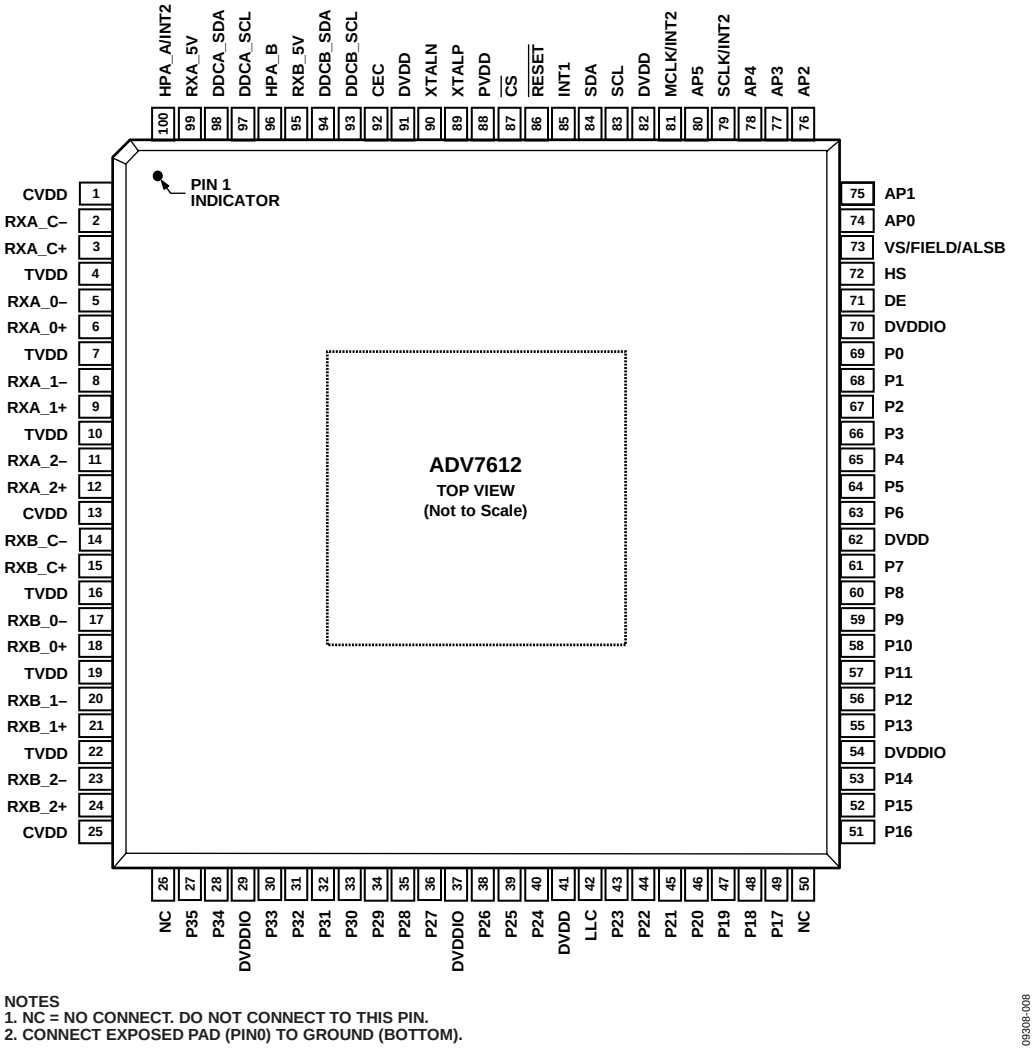

Figure 6. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
0	GND	Ground	Ground.
1	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
2	RXA_C–	HDMI input	Digital Input Clock Complement of Port A in the HDMI Interface.
3	RXA_C+	HDMI input	Digital Input Clock True of Port A in the HDMI Interface.
4	TVDD	Power	Terminator Supply Voltage (3.3 V).
5	RXA_0–	HDMI input	Digital Input Channel 0 Complement of Port A in the HDMI Interface.
6	RXA_0+	HDMI input	Digital Input Channel 0 True of Port A in the HDMI Interface.
7	TVDD	Power	Terminator Supply Voltage (3.3 V).
8	RXA_1–	HDMI input	Digital Input Channel 1 Complement of Port A in the HDMI Interface.
9	RXA_1+	HDMI input	Digital Input Channel 1 True of Port A in the HDMI Interface.
10	TVDD	Power	Terminator Supply Voltage (3.3 V).
11	RXA_2–	HDMI input	Digital Input Channel 2 Complement of Port A in the HDMI Interface.
12	RXA_2+	HDMI input	Digital Input Channel 2 True of Port A in the HDMI Interface.
13	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
14	RXB_C–	HDMI input	Digital Input Clock Complement of Port B in the HDMI Interface.

Pin No.	Mnemonic	Type	Description
15	RXB_C+	HDMI input	Digital Input Clock True of Port B in the HDMI Interface.
16	TVDD	Power	Terminator Supply Voltage (3.3 V).
17	RXB_0−	HDMI input	Digital Input Channel 0 Complement of Port B in the HDMI Interface.
18	RXB_0+	HDMI input	Digital Input Channel 0 True of Port B in the HDMI Interface.
19	TVDD	Power	Terminator Supply Voltage (3.3 V).
20	RXB_1−	HDMI input	Digital Input Channel 1 Complement of Port B in the HDMI Interface.
21	RXB_1+	HDMI input	Digital Input Channel 1 True of Port B in the HDMI Interface.
22	TVDD	Power	Terminator Supply Voltage (3.3 V).
23	RXB_2−	HDMI input	Digital Input Channel 2 Complement of Port B in the HDMI Interface.
24	RXB_2+	HDMI input	Digital Input Channel 2 True of Port B in the HDMI Interface.
25	CVDD	Power	HDMI Analog Block Supply Voltage (1.8 V).
26	NC	No connect	No connect.
27	P35	Digital video output	Video Pixel Output Port.
28	P34	Digital video output	Video Pixel Output Port.
29	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
30	P33	Digital video output	Video Pixel Output Port.
31	P32	Digital video output	Video Pixel Output Port.
32	P31	Digital video output	Video Pixel Output Port.
33	P30	Digital video output	Video Pixel Output Port.
34	P29	Digital video output	Video Pixel Output Port.
35	P28	Digital video output	Video Pixel Output Port.
36	P27	Digital video output	Video Pixel Output Port.
37	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
38	P26	Digital video output	Video Pixel Output Port.
39	P25	Digital video output	Video Pixel Output Port.
40	P24	Digital video output	Video Pixel Output Port.
41	DVDD	Power	Digital Core Supply Voltage (1.8 V).
42	LLC	Digital video output	Line-Locked Output Clock for the Pixel Data (Range is 13.5 MHz to 170 MHz).
43	P23	Digital video output	Video Pixel Output Port.
44	P22	Digital video output	Video Pixel Output Port.
45	P21	Digital video output	Video Pixel Output Port.
46	P20	Digital video output	Video Pixel Output Port.
47	P19	Digital video output	Video Pixel Output Port.
48	P18	Digital video output	Video Pixel Output Port.
49	P17	Digital video output	Video Pixel Output Port.
50	NC	No connect	No connect.
51	P16	Digital video output	Video Pixel Output Port.
52	P15	Digital video output	Video Pixel Output Port.
53	P14	Digital video output	Video Pixel Output Port.
54	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
55	P13	Digital video output	Video Pixel Output Port.
56	P12	Digital video output	Video Pixel Output Port.
57	P11	Digital video output	Video Pixel Output Port.
58	P10	Digital video output	Video Pixel Output Port.
59	P9	Digital video output	Video Pixel Output Port.
60	P8	Digital video output	Video Pixel Output Port.
61	P7	Digital video output	Video Pixel Output Port.
62	DVDD	Power	Digital Core Supply Voltage (1.8 V).
63	P6	Digital video output	Video Pixel Output Port.
64	P5	Digital video output	Video Pixel Output Port.
65	P4	Digital video output	Video Pixel Output Port.

Pin No.	Mnemonic	Type	Description
66	P3	Digital video output	Video Pixel Output Port.
67	P2	Digital video output	Video Pixel Output Port.
68	P1	Digital video output	Video Pixel Output Port.
69	P0	Digital video output	Video Pixel Output Port.
70	DVDDIO	Power	Digital I/O Supply Voltage (3.3 V).
71	DE	Miscellaneous digital	DE (data enable) is a signal that indicates active pixel data.
72	HS	Digital video output	HS is a horizontal synchronization output signal.
73	VS/FIELD/ALSB	Digital video output	VS is a vertical synchronization output signal. FIELD is a field synchronization output signal in all interlaced video modes. VS or FIELD can be configured for this pin. ALSB allows selection of the I^2C address.
74	AP0	Miscellaneous digital	Audio Output Pin. Pin AP0 to Pin AP5 can be configured to output S/PDIF digital audio output, HBR, DSD, DST, or I^2S.
75	AP1	Miscellaneous digital	Audio Output Pin. Pin AP0 to Pin AP5 can be configured to output S/PDIF digital audio output, HBR, DSD, DST, or I^2S.
76	AP2	Miscellaneous digital	Audio Output Pin. Pin AP0 to Pin AP5 can be configured to output S/PDIF digital audio output, HBR, DSD, DST, or I^2S.
77	AP3	Miscellaneous ditial	Audio Output Pin. Pin AP0 to Pin AP5 can be configured to output S/PDIF digital audio output, HBR, DSD, DST, or I^2S.
78	AP4	Miscellaneous ditial	Audio Output Pin. Pin AP0 to Pin AP5 can be configured to output S/PDIF digital audio output, HBR, DSD, DST, or I^2S.
79	SCLK/INT2	Miscellaneous digital	A dual function pin that can be configured to output an audio serial clock or an Interrupt 2 signal.
80	AP5	Miscellaneous	Audio Output Pin. Pin AP0 to Pin AP5 can be configured to output S/PDIF digital audio output, HBR, DSD, DST, or I^2S. Additionally, Pin AP5 can be configured to provide LRCLK.
81	MCLK/INT2	Miscellaneous	A dual function pin that can be configured to output an audio master clock or an Interrupt 2 signal.
82	DVDD	Power	Digital Core Supply Voltage (1.8 V).
83	SCL	Miscellaneous digital	I^2C Port Serial Clock Input. SCL is the clock line for the control port.
84	SDA	Miscellaneous digital	I^2C Port Serial Data Input/Output Pin. SDA is the data line for the control port.
85	INT1	Miscellaneous digital	Interrupt. This pin can be active low or active high. When status bits change, this pin is triggered. The events that trigger an interrupt are under user configuration.
86	$\overline{\text{RESET}}$	Miscellaneous digital	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the ADV7612 circuitry.
87	$\overline{\text{CS}}$	Miscellaneous digital	Chip Select. This pin has an internal pull-down. Pulling this line up causes I^2C state machine to ignore I^2C transmission.
88	PVDD	Power	PLL Supply Voltage (1.8 V).
89	XTALP	Miscellaneous analog	Input Pin for 28.63636 MHz Crystal or an External 1.8 V, 28.63636 MHz Clock Oscillator Source to Clock the ADV7612.
90	XTALN	Miscellaneous analog	Crystal Input. Input pin for 28.63636 MHz crystal. This pin should be left unconnected if XTALP is driven with 1.8 V clock signal.
91	DVDD	Power	Digital Core Supply Voltage (1.8 V).
92	CEC	Digital input/output	Consumer Electronic Control Channel.
93	DDCB_SCL	HDMI input	HDCP Slave Serial Clock Port B. DDCB_SCL is a 3.3 V input that is 5 V tolerant.
94	DDCB_SDA	HDMI input	HDCP Slave Serial Data Port B. DDCB_SDA is a 3.3 V input that is 5 V tolerant.
95	RXB_5V	HDMI input	5 V Detect Pin for Port B in the HDMI Interface.
96	HPA_B	Miscellaneous digital	Hot Plug assert signal output for HDMI Port B. This pin is 5 V tolerant.
97	DDCA_SCL	HDMI input	HDCP Slave Serial Clock Port A. DDCA_SCL is a 3.3 V input that is 5 V tolerant.
98	DDCA_SDA	HDMI input	HDCP Slave Serial Data Port A. DDCA_SDA is a 3.3 V input that is 5 V tolerant.
99	RXA_5V	HDMI input	5 V Detect Pin for Port A in the HDMI Interface.
100	HPA_A/INT2	Miscellaneous digital	A dual function pin that can be configured to output Hot Plug assert signal (for HDMI Port A) or an Interrupt 2 signal. This pin is 5 V tolerant.

POWER SUPPLY SEQUENCING

POWER-UP SEQUENCE

The recommended power-up sequence of the ADV7612 is to power up the 3.3 V supplies first, followed by the 1.8 V supplies. Reset should be held low while the supplies are powered up.

Alternatively, the ADV7612 may be powered up by asserting all supplies simultaneously. In this case, care must be taken while the supplies are being established to ensure that a lower rated supply does not go above a higher rated supply level.

POWER-DOWN SEQUENCE

The ADV7612 supplies may be de-asserted simultaneously as long as a higher rated supply does not go below a lower rated supply.

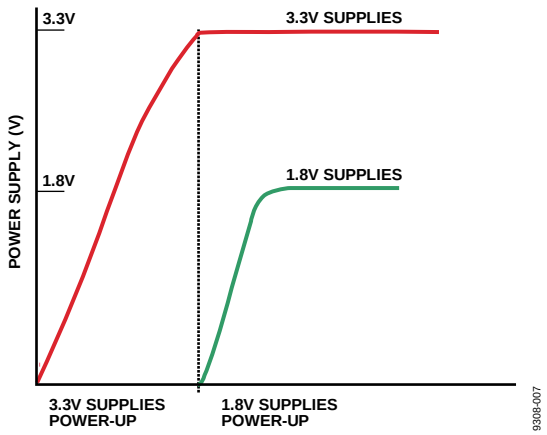

Figure 7. Recommended Power-Up Sequence

FUNCTIONAL OVERVIEW

HDMI RECEIVER

The HDMI receiver supports all mandatory and many optional 3D formats, HDTV formats up to 1080p, and all display resolutions up to UXGA (1600 × 1200 at 60 Hz).

With the inclusion of HDCP, displays can now receive encrypted video content. The HDMI interface of the ADV7612 allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 protocol.

The HDMI-compatible receiver on the ADV7612 allows programmable equalization of the HDMI data signals. This equalization compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies. It is capable of equalizing for cable lengths up to 30 meters to achieve robust receiver performance.

The ADV7612 has a synchronization regeneration block used to regenerate the DE based on the measurement of the video format being displayed, and to filter the horizontal and vertical synchronization signals to prevent glitches.

The HDMI receiver also supports TERC4 error detection, used for detection of corrupted HDMI packets following a cable disconnect.

The HDMI receiver offers advanced audio functionality. The receiver contains an audio mute controller that can detect a variety of conditions, which may result in audible extraneous noise in the audio output. On detection of these conditions, the audio signal can be ramped to prevent audio clicks or pops. Audio output can be formatted to one of the following modes:

- LPCM and IEC 61937 S/PDIF
- DSD audio
- DST audio
- HBR audio

Xpressview fast switching can be implemented with full HDCP authentication available on the background port. Synchronization measurement and status information are available for the background port.

HDMI receiver features include:

- 2:1 multiplexed HDMI receiver
- 3D format support
- 225 MHz HDMI receiver
- Integrated equalizer for cable lengths up to 30 meters
- HDCP 1.4 also on background ports
- Internal HDCP keys
- 36-/30-bit Deep Color support
- PCM, HBR, DST, and DSD audio packet support
- Repeater support
- Internal EDID RAM
- Hot Plug assert output pin for each HDMI port
- CEC controller

COMPONENT PROCESSOR

The ADV7612 has an any-to-any 3 × 3 CSC matrix. The CSC block is placed at the back of the CP section. CSC enables YPrPb-to-RGB and RGB-to-YCrCb conversions. Many other standards of color space can be implemented using the color space converter.

CP features include:

- 525i, 625i, 525p, 625p, 720p, 1080i, 1080p, and many other HDTV formats are supported
- Manual adjustments including gain (contrast) and offset (brightness), hue, and saturation
- Free run output mode that provides stable timing when no video input is present
- 170 MHz conversion rate, which supports RGB input resolutions up to 1600 × 1200 at 60 Hz
- Contrast, brightness, hue, and saturation controls
- Standard identification enabled by STDI block
- RGB that can be color space converted to YCrCb and decimated to a 4:2:2 format for video-centric back end IC interfacing
- DE output signal supplied for direct connection to HDMI/DVI transmitter

OTHER FEATURES

The ADV7612 has HS, VS, FIELD, and DE output signals with programmable position, polarity, and width.

The ADV7612 has two programmable interrupt request output pins, including INT1 and INT2 (INT2 is accessible only via one of following pins: MCLK/INT2, SCLK/INT2, or HPA_A/INT2). It also features a low power-down mode. The I^2C address of the main map is 0x98 after reset. This can be changed after reset to 0x9A if pullup is attached to VS/FIELD/ALSB pin and I^2C command SAMPLE_ALSB is issued. Refer to the Register Access and Serial Ports Description section in the UG-216.

The ADV7612 is provided in a 14 mm × 14 mm, RoHS-compliant LQFP_EP package, and is specified over the −40°C to +85°C temperature range.

PIXEL INPUT/OUTPUT FORMATTING

The output section of the ADV7612 is highly flexible. The pixel output bus can support up to 36-bit 4:4:4 YCrCb or 36-bit 4:4:4 RGB. The pixel data supports both single and double data rates modes[1]. In SDR mode, a 16-/20-/24-bit 4:2:2 or 24-/30-/36-bit 4:4:4 output is possible. In DDR mode, the pixel output port can be configured in an 8-/10-/12-bit 4:2:2 YCrCb or 12-bit 4:4:4 RGB.

Bus rotation is supported. Table 5 to Table 8 outline the different output formats that are supported. All output modes are controlled via I²C.

[1] DDR mode is only supported only up to 50 MHz (an equivalent to data rate clocked 100 MHz clock in SDR mode).

PIXEL DATA OUTPUT MODES FEATURES

The output pixel port features include the following:

- 8-/10-/12-bit ITU-R BT.656 4:2:2 YCrCb with embedded time codes and/or HS, VS, and FIELD output signals
- 16-/20-/24-bit YCrCb with embedded time codes and/or HS and VS/FIELD pin timing
- 24-/30-/36-bit YCrCb/RGB with embedded time codes and/or HS and VS/FIELD pin timing
- DDR 8-/10-/12-bit 4:2:2 YCrCb
- DDR 12-/24-/30-/36 bit 4:4:4 RGB

Table 5. SDR 4:2:2 Output Modes

	SDR 4:2:2				
OP_FORMAT_SEL[7:0]	**0x0[1]**	**0x1**	**0x2**	**0x6**	**0x0A**
Pixel Output	**8-Bit SDR ITU-R BT.656 Mode 0**	**10-Bit SDR ITU-R BT.656 Mode 0**	**12-Bit SDR ITU-R BT.656 Mode 0**	**12-Bit SDR ITU-R BT.656 Mode 1**	**12-Bit SDR ITU-R BT.656 Mode 2**
P35	High-Z	High-Z	High-Z	High-Z	Y3, Cb3, Cr3
P34	High-Z	High-Z	High-Z	High-Z	Y2, Cb2, Cr2
P33	High-Z	High-Z	High-Z	High-Z	Y1, Cb1, Cr1
P32	High-Z	High-Z	High-Z	High-Z	Y0, Cb0, Cr0
P31	High-Z	High-Z	High-Z	High-Z	High-Z
P30	High-Z	High-Z	High-Z	High-Z	High-Z
P29	High-Z	High-Z	High-Z	Y1, Cb1, Cr1	High-Z
P28	High-Z	High-Z	High-Z	Y0, Cb0, Cr0	High-Z
P27	High-Z	High-Z	High-Z	High-Z	High-Z
P26	High-Z	High-Z	High-Z	High-Z	High-Z
P25	High-Z	High-Z	High-Z	High-Z	High-Z
P24	High-Z	High-Z	High-Z	High-Z	High-Z
P23	Y7, Cb7, Cr7	Y9, Cb9, Cr9	Y11, Cb11, Cr11	Y11, Cb11, Cr11	Y11, Cb11, Cr11
P22	Y6, Cb6, Cr6	Y8, Cb8, Cr8	Y10, Cb10, Cr10	Y10, Cb10, Cr10	Y10, Cb10, Cr10
P21	Y5, Cb5, Cr5	Y7, Cb7, Cr7	Y9, Cb9, Cr9	Y9, Cb9, Cr9	Y9, Cb9, Cr9
P20	Y4, Cb4, Cr4	Y6, Cb6, Cr6	Y8, Cb8, Cr8	Y8, Cb8, Cr8	Y8, Cb8, Cr8
P19	Y3, Cb3, Cr3	Y5, Cb5, Cr5	Y7, Cb7, Cr7	Y7, Cb7, Cr7	Y7, Cb7, Cr7
P18	Y2, Cb2, Cr2	Y4, Cb4, Cr4	Y6, Cb6, Cr6	Y6, Cb6, Cr6	Y6, Cb6, Cr6
P17	Y1, Cb1, Cr1	Y3, Cb3, Cr3	Y5, Cb5, Cr5	Y5, Cb5, Cr5	Y5, Cb5, Cr5
P16	Y0, Cb0, Cr0	Y2, Cb2, Cr2	Y4, Cb4, Cr4	Y4, Cb4, Cr4	Y4, Cb4, Cr4
P15	High-Z	Y1, Cb1, Cr1	Y3, Cb3, Cr3	Y3, Cb3, Cr3	High-Z
P14	High-Z	Y0, Cb0, Cr0	Y2, Cb2, Cr2	Y2, Cb2, Cr2	High-Z
P13	High-Z	High-Z	Y1, Cb1, Cr1	High-Z	High-Z
P12	High-Z	High-Z	Y0, Cb0, Cr0	High-Z	High-Z
P11	High-Z	High-Z	High-Z	High-Z	High-Z
P10	High-Z	High-Z	High-Z	High-Z	High-Z
P9	High-Z	High-Z	High-Z	High-Z	High-Z
P8	High-Z	High-Z	High-Z	High-Z	High-Z
P7	High-Z	High-Z	High-Z	High-Z	High-Z
P6	High-Z	High-Z	High-Z	High-Z	High-Z
P5	High-Z	High-Z	High-Z	High-Z	High-Z
P4	High-Z	High-Z	High-Z	High-Z	High-Z
P3	High-Z	High-Z	High-Z	High-Z	High-Z
P2	High-Z	High-Z	High-Z	High-Z	High-Z
P1	High-Z	High-Z	High-Z	High-Z	High-Z
P0	High-Z	High-Z	High-Z	High-Z	High-Z

[1] Modes 0x00, 0x01, 0x02, 0x06 and 0x0A require additional writes to IO Map reg. 0x19[7:6]=2'b11 and IO Map reg.0x33[6]=1

Table 6. SDR 4:2:2 and 4:4:4 Output Modes

	SDR 4:2:2					SDR 4:4:4			
OP_FORMAT_SEL[7:0]	**0x80**	**0x81**	**0x82**	**0x86**	**0x8A**	**0x40**	**0x41**	**0x42**	**0x46**
Pixel Output	**16-Bit SDR ITU-R BT.656 4:2:2 Mode 0**	**20-Bit SDR ITU-R BT.656 4:2:2 Mode 0**	**24-Bit SDR ITU-R BT.656 4:2:2 Mode 0**	**24-Bit SDR ITU-R BT.656 4:2:2 Mode 1**	**24-Bit SDR ITU-R BT.656 4:2:2 Mode 2**	**24-Bit SDR 4:4:4 Mode 0**	**30-Bit SDR 4:4:4 Mode 0**	**36-Bit SDR 4:4:4 Mode 0**	**36-Bit SDR 4:4:4 Mode 1**
P35	High-Z	High-Z	High-Z	High-Z	Y3	R7	R9	R11	R9
P34	High-Z	High-Z	High-Z	High-Z	Y2	R6	R8	R10	R8
P33	High-Z	High-Z	High-Z	Cb1, Cr1	Y1	R5	R7	R9	R7
P32	High-Z	High-Z	High-Z	Cb0, Cr0	Y0	R4	R6	R8	R6
P31	High-Z	High-Z	High-Z	High-Z	Cb3, Cr3	R3	R5	R7	R5
P30	High-Z	High-Z	High-Z	High-Z	Cb2, Cr2	R2	R4	R6	R4
P29	High-Z	High-Z	High-Z	Y1	Cb1, Cr1	R1	R3	R5	R3
P28	High-Z	High-Z	High-Z	Y0	Cb0, Cr0	R0	R2	R4	R2
P27	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	R1	R3	R1
P26	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	R0	R2	R0
P25	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	R1	G7
P24	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z	R0	G6
P23	Y7	Y9	Y11	Y11	Y11	G7	G9	G11	G5
P22	Y6	Y8	Y10	Y10	Y10	G6	G8	G10	G4
P21	Y5	Y7	Y9	Y9	Y9	G5	G7	G9	G3
P20	Y4	Y6	Y8	Y8	Y8	G4	G6	G8	G2
P19	Y3	Y5	Y7	Y7	Y7	G3	G5	G7	G1
P18	Y2	Y4	Y6	Y6	Y6	G2	G4	G6	G0
P17	Y1	Y3	Y5	Y5	Y5	G1	G3	G5	B11
P16	Y0	Y2	Y4	Y4	Y4	G0	G2	G4	B10
P15	High-Z	Y1	Y3	Y3	High-Z	High-Z	G1	G3	B9
P14	High-Z	Y0	Y2	Y2	High-Z	High-Z	G0	G2	B8
P13	High-Z	High-Z	Y1	High-Z	High-Z	High-Z	High-Z	G1	G11
P12	High-Z	High-Z	Y0	High-Z	High-Z	High-Z	High-Z	G0	G10
P11	Cb7, Cr7	Cb9, Cr9	Cb11, Cr11	Cb11, Cr11	Cb11, Cr11	B7	B9	B11	B7
P10	Cb6, Cr6	Cb8, Cr8	Cb10, Cr10	Cb10, Cr10	Cb10, Cr10	B6	B8	B10	B6
P9	Cb5, Cr5	Cb7, Cr7	Cb9, Cr9	Cb9, Cr9	Cb9, Cr9	B5	B7	B9	B5
P8	Cb4, Cr4	Cb6, Cr6	Cb8, Cr8	Cb8, Cr8	Cb8, Cr8	B4	B6	B8	B4
P7	Cb3, Cr3	Cb5, Cr5	Cb7, Cr7	Cb7, Cr7	Cb7, Cr7	B3	B5	B7	B3
P6	Cb2, Cr2	Cb4, Cr4	Cb6, Cr6	Cb6, Cr6	Cb6, Cr6	B2	B4	B6	B2
P5	Cb1, Cr1	Cb3, Cr3	Cb5, Cr5	Cb5, Cr5	Cb5, Cr5	B1	B3	B5	B1
P4	Cb0, Cr0	Cb2, Cr2	Cb4, Cr4	Cb4, Cr4	Cb4, Cr4	B0	B2	B4	B0
P3	High-Z	Cb1, Cr1	Cb3, Cr3	Cb3, Cr3	High-Z	High-Z	B1	B3	R11
P2	High-Z	Cb0, Cr0	Cb2, Cr2	Cb2, Cr2	High-Z	High-Z	B0	B2	R10
P1	High-Z	High-Z	Cb1, Cr1	High-Z	High-Z	High-Z	High-Z	B1	G9
P0	High-Z	High-Z	Cb0, Cr0	High-Z	High-Z	High-Z	High-Z	B0	G8

Table 7. DDR 4:2:2 Output Modes

	DDR 4:2:2 Mode (Clock/2)					
OP_FORMAT_SEL[7:0]	**0x20**		**0x21**		**0x22**	
	8-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 0		**10-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 0**		**12-Bit DDR ITU-656 (Clock/2 Output) 4:2:2 Mode 0**	
Pixel Output	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**
P35	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P34	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P33	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P32	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P31	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P30	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P29	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P28	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P27	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P26	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P25	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P24	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P23	Cb7, Cr7	Y7	Cb9, Cr9	Y9	Cb11, Cr11	Y11
P22	Cb6, Cr6	Y6	Cb8, Cr8	Y8	Cb10, Cr10	Y10
P21	Cb5, Cr5	Y5	Cb7, Cr7	Y7	Cb9, Cr9	Y9
P20	Cb4, Cr4	Y4	Cb6, Cr6	Y6	Cb8, Cr8	Y8
P19	Cb3, Cr3	Y3	Cb5, Cr5	Y5	Cb7, Cr7	Y7
P18	Cb2, Cr2	Y2	Cb4, Cr4	Y4	Cb6, Cr6	Y6
P17	Cb1, Cr1	Y1	Cb3, Cr3	Y3	Cb5, Cr5	Y5
P16	Cb0, Cr0	Y0	Cb2, Cr2	Y2	Cb4, Cr4	Y4
P15	High-Z	High-Z	Cb1, Cr1	Y1	Cb3, Cr3	Y3
P14	High-Z	High-Z	Cb0, Cr0	Y0	Cb2, Cr2	Y2
P13	High-Z	High-Z	High-Z	High-Z	Cb1, Cr1	Y1
P12	High-Z	High-Z	High-Z	High-Z	Cb0, Cr0	Y0
P11	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P10	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P9	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P8	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P7	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P6	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P5	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P4	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P3	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P2	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P1	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z
P0	High-Z	High-Z	High-Z	High-Z	High-Z	High-Z

Table 8. DDR 4:4:4 Output Modes

	DDR 4:4:4 Mode (Clock/2)[1, 2]					
OP_FORMAT_SEL[7:0]	**0x60**		**0x61**		**0x62**	
	24-Bit DDR RGB (Clock/2 Output)		**30-Bit DDR RGB (Clock/2 Output)**		**36-Bit DDR RGB (Clock/2 Output)**	
Pixel Output	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**	**Clock Rise**	**Clock Fall**
P35	R7-0	R7-1	R9-0	R9-1	R11-0	R11-1
P34	R6-0	R6-1	R8-0	R8-1	R10-0	R10-1
P33	R5-0	R5-1	R7-0	R7-1	R9-0	R9-1
P32	R4-0	R4-1	R6-0	R6-1	R8-0	R8-1
P31	R3-0	R3-1	R5-0	R5-1	R7-0	R7-1
P30	R2-0	R2-1	R4-0	R4-1	R6-0	R6-1
P29	R1-0	R1-1	R3-0	R3-1	R5-0	R5-1
P28	R0-0	R0-1	R2-0	R2-1	R4-0	R4-1
P27	High-Z	High-Z	R1-0	R1-1	R3-0	R3-1
P26	High-Z	High-Z	R0-0	R0-1	R2-0	R2-1
P25	High-Z	High-Z	High-Z	High-Z	R1-0	R1-1
P24	High-Z	High-Z	High-Z	High-Z	R0-0	R0-1
P23	G7-0	G7-1	G9-0	G9-1	G11-0	G11-1
P22	G6-0	G6-1	G8-0	G8-1	G10-0	G10-1
P21	G5-0	G5-1	G7-0	G7-1	G9-0	G9-1
P20	G4-0	G4-1	G6-0	G6-1	G8-0	G8-1
P19	G3-0	G3-1	G5-0	G5-1	G7-0	G7-1
P18	G2-0	G2-1	G4-0	G4-1	G6-0	G6-1
P17	G1-0	G1-1	G3-0	G3-1	G5-0	G5-1
P16	G0-0	G0-1	G2-0	G2-1	G4-0	G4-1
P15	High-Z	High-Z	G1-0	G1-1	G3-0	G3-1
P14	High-Z	High-Z	G0-0	G0-1	G2-0	G2-1
P13	High-Z	High-Z	High-Z	High-Z	G1-0	G1-1
P12	High-Z	High-Z	High-Z	High-Z	G0-0	G0-1
P11	B7-0	B7-1	B9-0	B9-1	B11-0	B11-1
P10	B6-0	B6-1	B8-0	B8-1	B10-0	B10-1
P9	B5-0	B5-1	B7-0	B7-1	B9-0	B9-1
P8	B4-0	B4-1	B6-0	B6-1	B8-0	B8-1
P7	B3-0	B3-1	B5-0	B5-1	B7-0	B7-1
P6	B2-0	B2-1	B4-0	B4-1	B6-0	B6-1
P5	B1-0	B1-1	B3-0	B3-1	B5-0	B5-1
P4	B0-0	B0-1	B2-0	B2-1	B4-0	B4-1
P3	High-Z	High-Z	B1-0	B1-1	B3-0	B3-1
P2	High-Z	High-Z	B0-0	B0-1	B2-0	B2-1
P1	High-Z	High-Z	High-Z	High-Z	B1-0	B1-1
P0	High-Z	High-Z	High-Z	High-Z	B0-0	B0-1

[1] -0 = even samples.
[2] -1 = odd samples.

OUTLINE DIMENSIONS

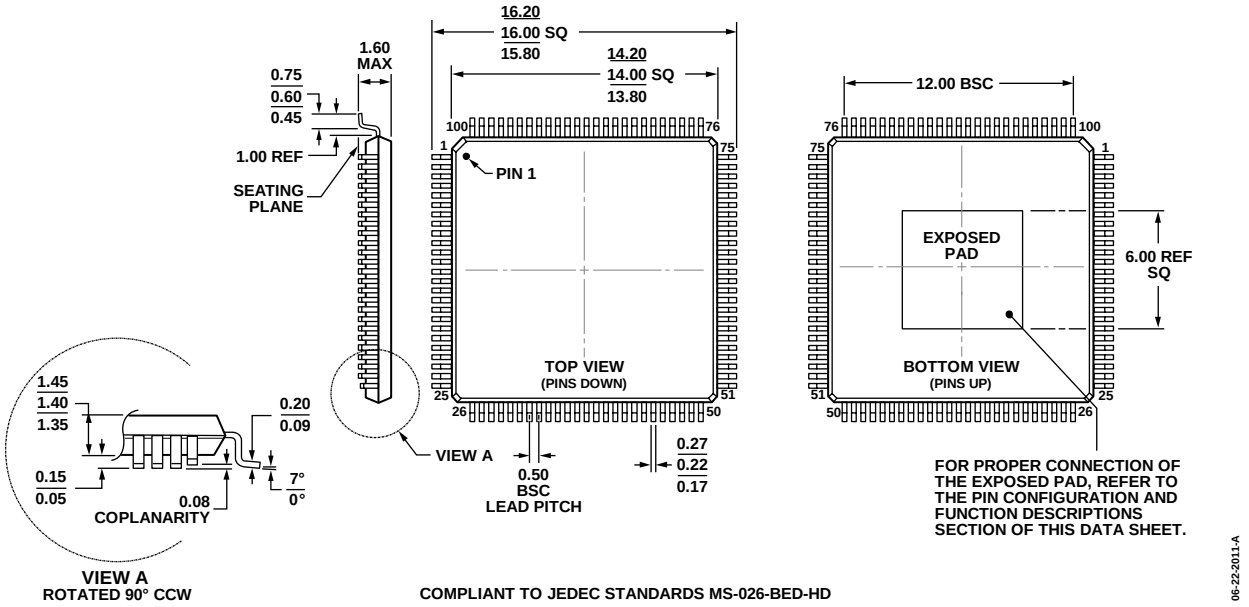

Figure 8. 100-Lead Low Profile Quad Flat Package [LQFP_EP]
SW-100-2
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2, 3]	Temperature Range	Package Description	Package Option
ADV7612BSWZ	−40°C to +85°C	100-Lead LQFP_EP	SW-100-2
ADV7612BSWZ-P	−40°C to +85°C	100-Lead LQFP_EP	SW-100-2
ADV7612WBSWZ	−40°C to +85°C	100-Lead LQFP_EP	SW-100-2
EVAL-ADV7612EB1Z		Evaluation board with HDCP keys	
EVAL-ADV7612EB2Z		Evaluation board without HDCP keys	
EVAL-ADV7612-7511		Low cost evaluation board with HDCP	
EVAL-ADV7612-7511P		Low cost evaluation board without HDCP	

[1] Z = RoHS Compliant Part.
[2] The ADV7612BSWZ-P is a non-HDCP version.
[3] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7612WBSWZ model is available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that this automotive model may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade product shown is available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for this model.

NOTES

NOTES

NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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