# 3 GHz HDMI 2:2 Crosspoint Transceiver with On-Screen Display

Data Sheet

# ADV7626

## FEATURES

- 2-input, 2-output crosspoint HDMI transceiver
- HDMI support
  - 3 GHz video support (up to 4k × 2k)
  - Audio return channel (ARC)
  - 3D TV support
  - Content type bits
  - CEC 1.4-compatible
  - Extended colorimetry
- Character- and icon-based on-screen display (OSD)
  - 3D OSD overlay on all mandatory 3D formats
  - Support for OSD overlay on 3 GHz video formats
- High-bandwidth Digital Content Protection (HDCP 1.4)
- HDCP repeater support: up to 127 KSVs supported
- 300 MHz maximum TMDS clock frequency (up to 4k × 2k)
- 48-/36-/30-bit Deep Color input modes supported
- Ultralow jitter digital PLL (100% deskew)
- 2 independent HDMI receivers
  - 3 GHz support on all inputs
  - Adaptive equalizer for cable lengths up to 30 meters
  - Flexible internal EDID RAM supports dual EDIDs
  - Replication of either dual EDID on any input port
  - 5 V detect inputs
  - Hot Plug assert control outputs
- 2 independent HDMI transmitters
  - 3 GHz support on all outputs
  - EDID data extraction
  - Hot Plug detect (HPD) inputs
  - Audio return channel (ARC) receiver per transmitter
  - 3 GHz color space converter (CSC) per transmitter
- Audio
  - HDMI-compatible audio interface
  - 2 independent 8-channel audio extraction ports
  - 2 independent 8-channel audio insertion ports
  - S/PDIF (IEC 60958-compatible) digital audio input/output
  - Super Audio CD® (SACD) with DSD input/output interface
  - High bit rate (HBR) audio
  - Dolby® TrueHD
  - DTS-HD Master Audio™
  - Full audio input and output support
- General
  - Interrupt controller
  - Standard identification (STDI) circuit
  - Software libraries, driver, and application available

## APPLICATIONS

- AVR
- Soundbar with HDMI repeater support
- Matrix switch
- Other repeater applications

## FUNCTIONAL BLOCK DIAGRAM

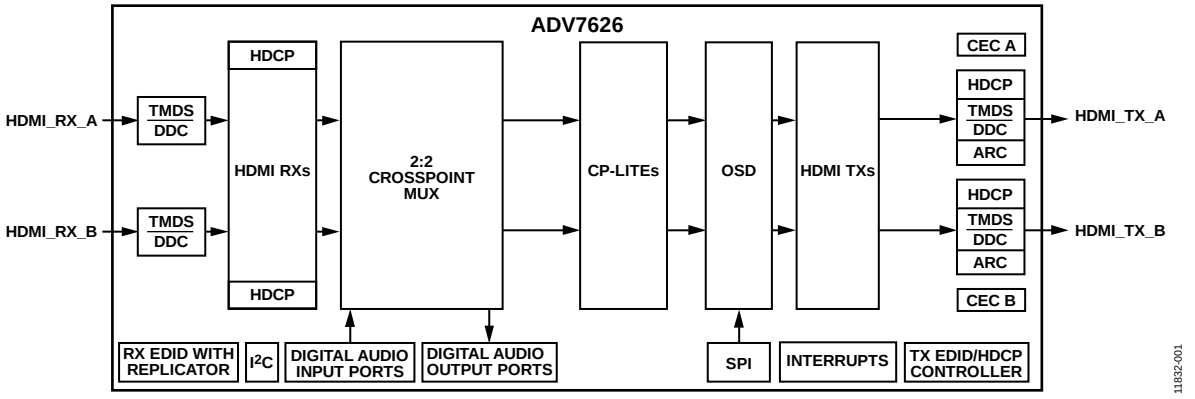



*Figure 1.*

Rev. 0

Document Feedback



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

# ADV7626* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

**Application Notes**

- AN-1299: Enabling HDMI 2.0 Using ADV8005 and ADV7625/ADV7626/ADV7627

**Data Sheet**

- ADV7626: 3 GHz HDMI 2:2 Crosspoint Transceiver with On-Screen Display Data Sheet

## REFERENCE MATERIALS

**Press**

- Crosspoint Transceivers Distribute Wide Range of Ultra-High-Definition Home and Professional Audio/Video Content

## DESIGN RESOURCES

- ADV7626 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all ADV7626 EngineerZone Discussions.

## SAMPLE AND BUY

Visit the product page to see pricing options.

## TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

## DOCUMENT FEEDBACK

Submit feedback for this data sheet.

# TABLE OF CONTENTS



## REVISION HISTORY

**12/13—Revision 0: Initial Version**

# GENERAL DESCRIPTION

The ADV7626 is a high performance, High-Definition Multimedia Interface (HDMI®) transceiver with crosspoint and splitter capabilities. The ADV7626 supports 3 GHz video and features two independent HDMI receivers, two independent HDMI transmitters, two audio output ports, and two audio input ports. The ADV7626 supports all HDCP repeater functions through fully tested Analog Devices, Inc., repeater software libraries and drivers.

The HDMI receivers and transmitters in the ADV7626 support the reception and transmission of 3 GHz video formats up to 4k × 2k at 24 Hz/25 Hz/30 Hz, in addition to all mandatory HDMI 3D TV formats. The receivers and transmitters also provide support for THX® Media Director™.

Each HDMI receiver features an integrated equalizer that ensures robust operation of the interface with cable lengths up to 30 meters. The HDMI receivers share a 768-byte volatile extended display identification data (EDID) memory, which can facilitate one or two EDIDs, one for each receiver. Each HDMI port features dedicated 5 V detect and Hot Plug™ assert pins.

Each HDMI transmitter supports audio return channel (ARC) and features an integrated HDMI CEC controller that supports capability discovery and control (CDC).

The ADV7626 offers two dedicated audio output ports and two dedicated audio input ports. Each audio port supports the extraction and insertion of up to eight channels of audio data out of or into the HDMI streams. HDMI audio formats, including $I^2S$, S/PDIF, direct stream digital (DSD), and high bit rate (HBR) audio are supported.

The ADV7626 has an integrated on-screen display (OSD) generator that enables the creation and control of high quality character- and icon-based system status and control displays. The OSD can be overlaid on 3 GHz video formats and 3D video. Customers who are interested in using OSD are provided with Blimp, the Analog Devices OSD development tool.

The ADV7626 is provided in a space-saving, 260-ball, 15 mm × 15 mm CSP_BGA surface-mount, RoHS-compliant package and is specified over the 0°C to 70°C temperature range.

# DETAILED FUNCTIONAL BLOCK DIAGRAM

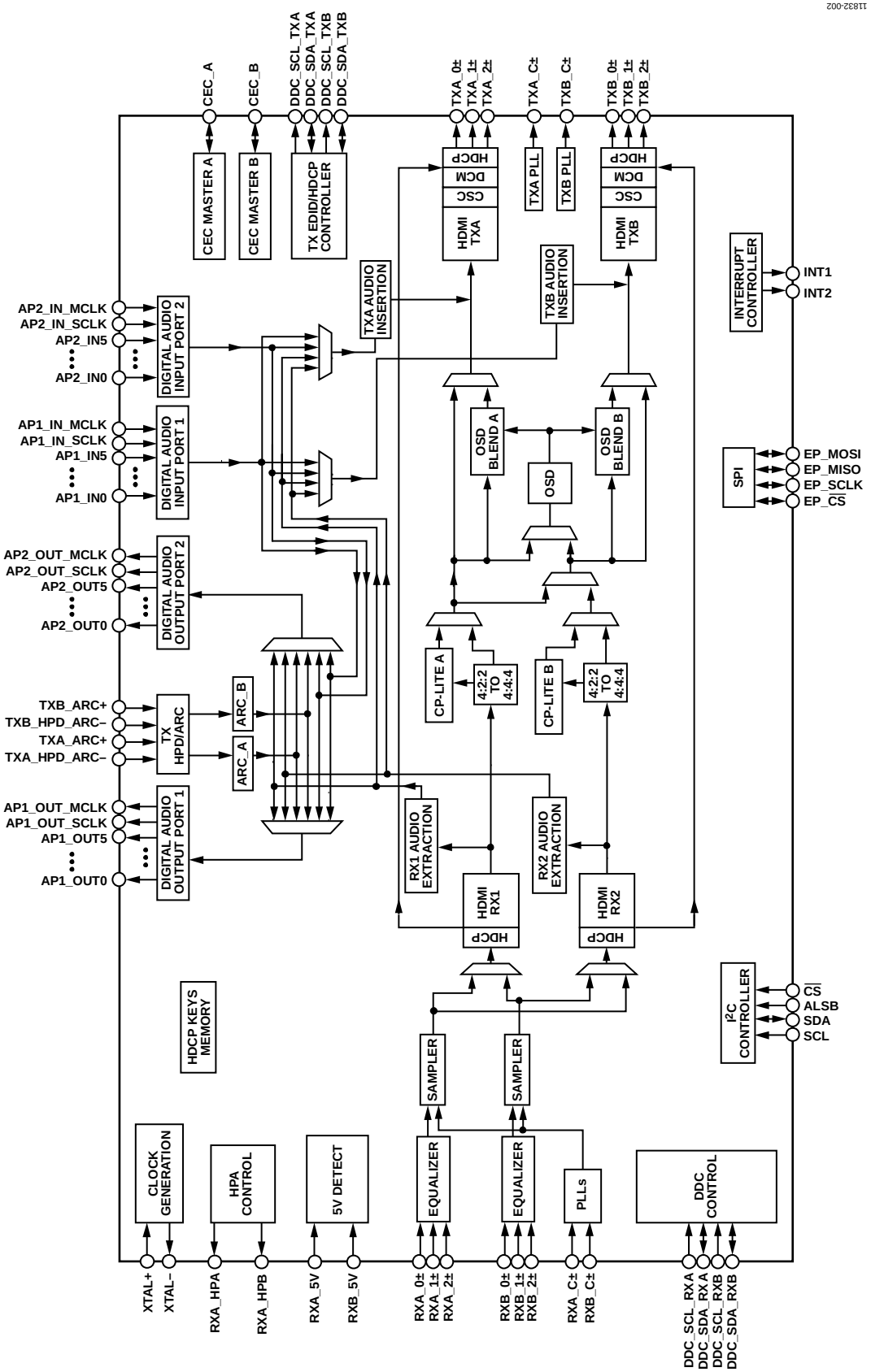



*Figure 2. Detailed Functional Block Diagram*

# SPECIFICATIONS

AVDD_TXA = 1.8 V ± 5%, AVDD_TXB = 1.8 V ± 5%, CVDD = 1.8 V ± 5%, DVDD = 1.8 V ± 5%, DVDDIO = 3.3 V ± 5%, PVDD = 1.8 V ± 5%, PVDD_TXA = 1.8 V ± 5%, PVDD_TXB = 1.8 V ± 5%, TVDD = 3.3 V ± 5%, $T_{MIN}$ to $T_{MAX}$ = 0°C to 70°C.

## DIGITAL, HDMI, AND AC SPECIFICATIONS

**Table 1.**

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| DIGITAL INPUTS | | | | | |
| Input High Voltage ($V_{IH}$) | | 2 | | | V |
| Input Low Voltage ($V_{IL}$) | | | | 0.8 | V |
| Input Leakage Current ($I_{IN}$) | | −60 | | +60 | µA |
| Input Capacitance ($C_{IN}$) | | | | 20 | pF |
| DIGITAL INPUTS (5 V TOLERANT)[1] | | | | | |
| Input High Voltage ($V_{IH}$) | | 2.85 | | | V |
| Input Low Voltage ($V_{IL}$) | | | | 0.8 | V |
| Input Leakage Current ($I_{IN}$) | RXA_5V and RXB_5V inputs | −450 | | +450 | µA |
| | All other 5 V tolerant digital inputs | −60 | | +60 | µA |
| DIGITAL OUTPUTS | | | | | |
| Output High Voltage ($V_{OH}$) | | 2.4 | | | V |
| Output Low Voltage ($V_{OL}$) | | | | 0.4 | V |
| High Impedance Leakage Current ($I_{LEAK}$) | | | 10 | | µA |
| Output Capacitance ($C_{OUT}$) | | | | 20 | pF |
| DIGITAL OUTPUTS (5 V TOLERANT)[2] | | | | | |
| Output High Voltage ($V_{OH}$) | | 4.85 | | | V |
| Output Low Voltage ($V_{OL}$) | | | | 0.4 | V |
| AC SPECIFICATIONS | | | | | |
| TMDS Input Clock Range | | 25 | | 300 | MHz |
| TMDS Output Clock Frequency | | 25 | | 300 | MHz |

[1] The following pins are 5 V tolerant inputs: DDC_SCL_RXA, DDC_SDA_RXA, DDC_SCL_RXB, DDC_SDA_RXB, RXA_5V, RXB_5V, CEC_A, DDC_SCL_TXA, DDC_SDA_TXA, TXA_HPD_ARC−, TXA_ARC+, CEC_B, DDC_SCL_TXB, DDC_SDA_TXB, TXB_HPD_ARC−, and TXB_ARC+.
[2] The following pins are 5 V tolerant outputs: RXA_HPA and RXB_HPA.

## DATA AND I²C TIMING CHARACTERISTICS

**Table 2.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VIDEO SYSTEM CLOCK AND XTAL | | | | | | |
| Crystal Nominal Frequency | | | | 27.0 | | MHz |
| Crystal Frequency Stability | | | | | ±50 | ppm |
| External Clock Source | | External crystal must operate at 1.8 V | | | | |
| Input High Voltage | $V_{IH}$ | XTAL driven with external clock source | 1.2 | | | V |
| Input Low Voltage | $V_{IL}$ | XTAL driven with external clock source | | | 0.4 | V |
| Serial Port EP_SCLK Frequency | | | | | 27 | MHz |
| Audio SCLK Frequency | | | | | 49.152 | MHz |
| Audio MCLK Frequency | | | | | 98.304 | MHz |
| Audio DSD Clock Frequency | | | | | 5.6448 | MHz |
| RESET FEATURE | | | | | | |
| Reset Pulse Width | | | 5 | | | ms |
| I²C PORTS (FAST MODE) | | | | | | |
| xCL Frequency[1] | | | | | 400 | kHz |
| xCL Minimum Pulse Width High[1] | $t_1$ | | 600 | | | ns |
| xCL Minimum Pulse Width Low[1] | $t_2$ | | 1.3 | | | µs |
| Start Condition Hold Time | $t_3$ | | 600 | | | ns |
| Start Condition Setup Time | $t_4$ | | 600 | | | ns |
| xDA Setup Time[2] | $t_5$ | | 100 | | | ns |
| xCL and xDA Rise Time[1, 2] | $t_6$ | | | | 300 | ns |
| xCL and xDA Fall Time[1, 2] | $t_7$ | | | | 300 | ns |
| Setup Time (Stop Condition) | $t_8$ | | 0.6 | | | µs |
| SERIAL PORT, MASTER MODE[3, 4] | | SPI Mode 0 | | | | |
| EP_$\overline{CS}$ Falling Edge to EP_SCLK Rising/Falling Edge | $t_9$, $t_{10}$ | | 1 × EP_SCLK periods | | 1.5 × EP_SCLK periods | ns |
| EP_SCLK Rising/Falling Edge to EP_$\overline{CS}$ Rising Edge | $t_{11}$, $t_{12}$ | | 1 × EP_SCLK periods | | 1.5 × EP_SCLK periods | ns |
| EP_$\overline{CS}$ Pulse Width[5] | $t_{13}$ | | 1000 | | | ns |
| EP_SCLK High Time | $t_{14}$ | | 40 | | 60 | % duty cycle |
| EP_SCLK Low Time | | | 40 | | 60 | % duty cycle |
| EP_MOSI Start of Data Invalid to EP_SCLK Falling Edge | $t_{15}$ | | | | 0 | ns |
| EP_$\overline{CS}$ Start of Data Invalid to EP_SCLK Falling Edge | $t_{15}$ | | | | 0 | ns |
| EP_SCLK Falling Edge to EP_MOSI End of Data Invalid | $t_{16}$ | | | | 2.15 | ns |
| EP_SCLK Falling Edge to EP_$\overline{CS}$ End of Data Invalid | $t_{16}$ | | | | 2.15 | ns |
| EP_MISO Setup Time | $t_{17}$ | Valid regardless of the EP_SCLK active edge used | 7.5 | | | ns |
| EP_MISO Hold Time | $t_{18}$ | Valid regardless of the EP_SCLK active edge used | 0 | | | ns |
| SERIAL PORT, SLAVE MODE[3, 4] | | SPI Mode 0 | | | | |
| EP_$\overline{CS}$ Falling Edge to EP_SCLK Rising Edge | $t_{20}$ | | 10 | | | ns |
| Final EP_SCLK Rising Edge to EP_$\overline{CS}$ Rising Edge | $t_{22}$ | | 10 | | | ns |
| EP_$\overline{CS}$ Pulse Width[5] | $t_{23}$ | | | 20 × EP_SCLK periods | | ns |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| EP_SCLK High Time | $t_{24}$ | | 45 | | 55 | % duty cycle |
| EP_SCLK Low Time | | | 45 | | 55 | % duty cycle |
| EP_MOSI Setup Time | $t_{25}$ | | 0.5 | | | ns |
| EP_MOSI Hold Time | $t_{26}$ | | 1.4 | | | ns |
| EP_SCLK Falling Edge to EP_MISO Start of Data Invalid | $t_{27}$ | | 5.5 | | | ns |
| EP_SCLK Falling Edge to EP_MISO End of Data Invalid | $t_{28}$ | | | | 9 | ns |
| AUDIO INPUT PORTS, I²S INPUT | | | | | | |
| APx_IN_SCLK High Time | $t_{37}$ | | 45 | | 55 | % duty cycle |
| APx_IN_SCLK Low Time | | | 45 | | 55 | % duty cycle |
| APx_IN Data Setup Time | $t_{38}$ | | 2.3 | | | ns |
| APx_IN Data Hold Time | $t_{39}$ | | 1.6 | | | ns |
| AUDIO INPUT PORTS, DSD INPUT | | | | | | |
| APx_IN_SCLK High Time | $t_{40}$ | | 45 | | 55 | % duty cycle |
| APx_IN_SCLK Low Time | | | 45 | | 55 | % duty cycle |
| APx_IN DSD Data Setup Time | $t_{41}$ | | 2.3 | | | ns |
| APx_IN DSD Data Hold Time | $t_{42}$ | | 1.6 | | | ns |
| AUDIO OUTPUT PORTS, I²S OUTPUT | | | | | | |
| APx_OUT_SCLK High Time | $t_{46}$ | | 45 | | 55 | % duty cycle |
| APx_OUT_SCLK Low Time | | | 45 | | 55 | % duty cycle |
| APx_OUT LRCLK Transition Time | $t_{47}$ | Start of invalid LRCLK to falling APx_OUT_SCLK edge | | | 10 | ns |
| APx_OUT LRCLK Transition Time | $t_{48}$ | Falling APx_OUT_SCLK edge to end of invalid LRCLK | | | 10 | ns |
| APx_OUT Data Transition Time | $t_{49}$ | Start of invalid data to falling APx_OUT_SCLK edge | | | 10 | ns |
| APx_OUT Data Transition Time | $t_{50}$ | Falling APx_OUT_SCLK edge to end of invalid data | | | 10 | ns |
| AUDIO OUTPUT PORTS, DSD OUTPUT | | | | | | |
| APx_OUT_SCLK High Time | $t_{51}$ | | 45 | | 55 | % duty cycle |
| APx_OUT_SCLK Low Time | | | 45 | | 55 | % duty cycle |
| APx_OUT DSD Data Transition Time | $t_{52}$ | Start of invalid data to falling APx_OUT_SCLK edge | | | 10 | ns |
| APx_OUT DSD Data Transition Time | $t_{53}$ | Falling APx_OUT_SCLK edge to end of invalid data | | | 10 | ns |

[1] xCL refers to SCL, DDC_SCL_RXA, and DDC_SCL_RXB.
[2] xDA refers to SDA, DDC_SDA_RXA, and DDC_SDA_RXB.
[3] SPI Mode 0 only.
[4] All serial port measurements are for CPHA = 0, CPOL = 0 (clock is low in idle state; negative edge of clock is used to transmit data and positive edge is used to sample data).
[5] Measurements guaranteed by design only.

### *Timing Diagrams*

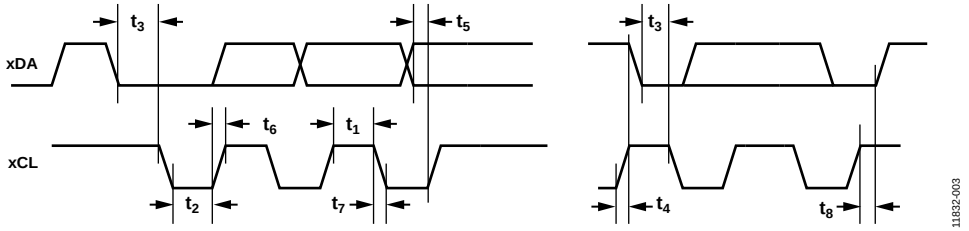



*Figure 3. I²C Timing*

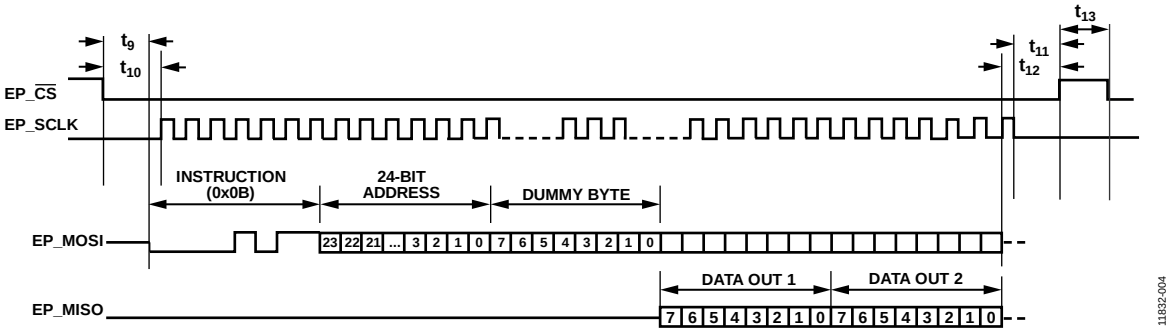



*Figure 4. Detailed SPI Master Timing Diagram (SPI Mode 0, CPOL = CPHA = 0)*

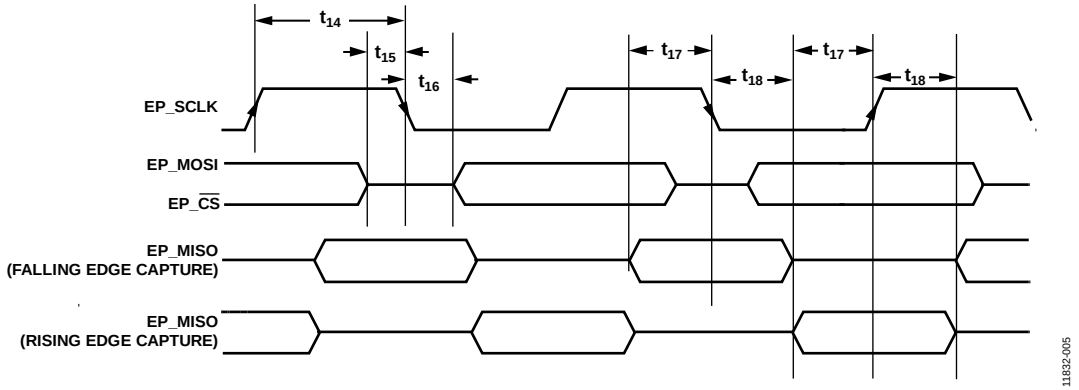



*Figure 5. SPI Master Mode Timing (SPI Mode 0)*

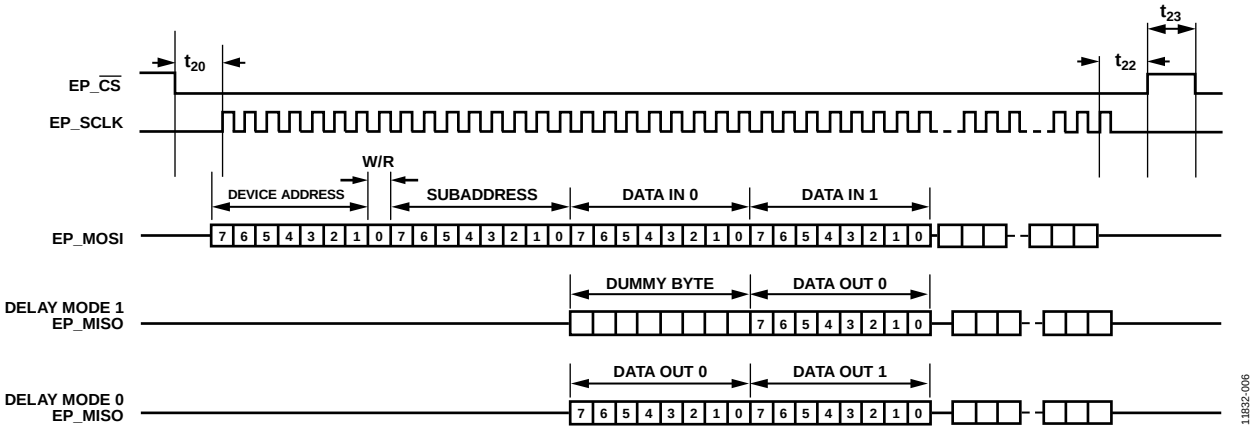



*Figure 6. Detailed SPI Slave Timing Diagram (SPI Mode 0, CPOL = CPHA = 0)*

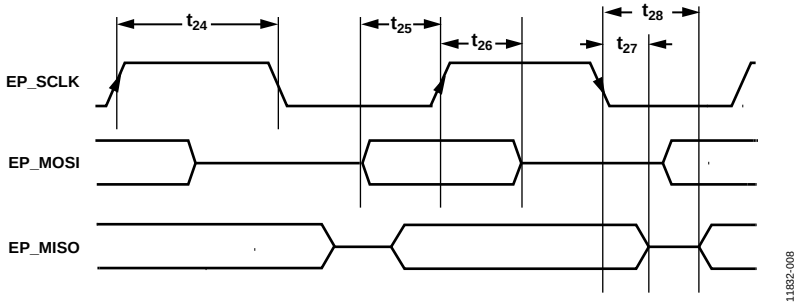
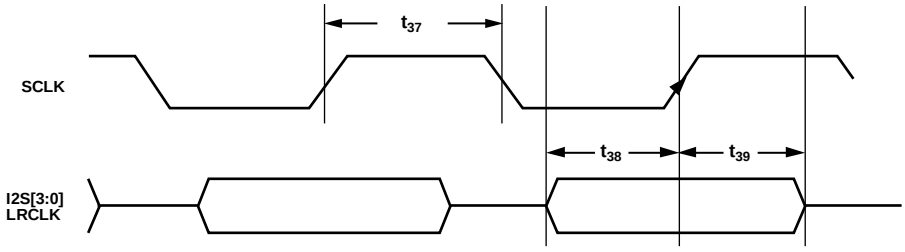



*Figure 7. SPI Slave Mode Timing (SPI Mode 0)*




**AUDIO INPUT PORTS I²S SIGNAL ASSIGNMENT**

| INPUT PORT | SCLK | LRCLK | I2S[3:0] |
|---|---|---|---|
| AP1_IN | AP1_IN_SCLK | AP1_IN5 | AP1_IN[4:1] |
| AP2_IN | AP2_IN_SCLK | AP2_IN5 | AP2_IN[4:1] |

11832-012

*Figure 8. I²S Input Timing*

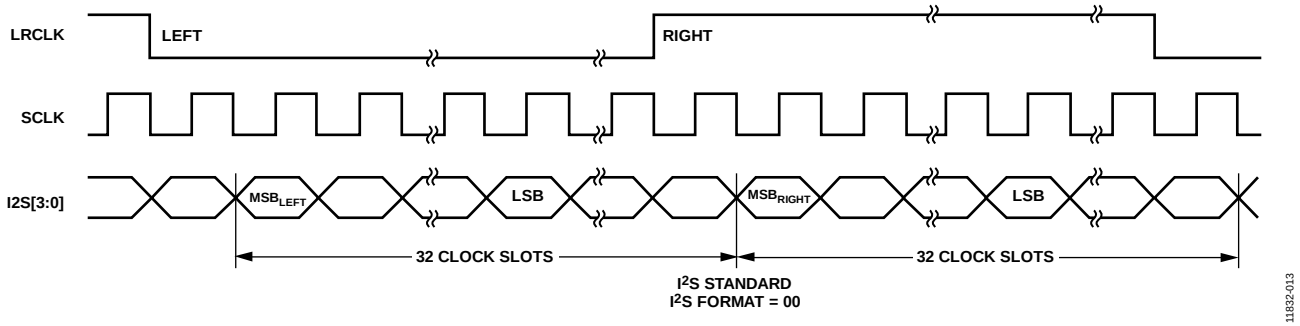



*Figure 9. I²S Standard Audio, Data Width 16 to 24 Bits per Channel*

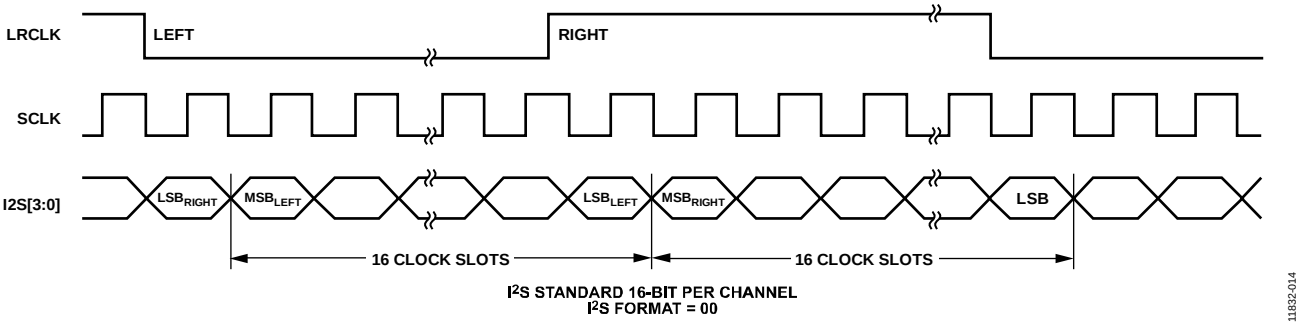



*Figure 10. I²S Standard Audio, 16-Bit Samples Only*

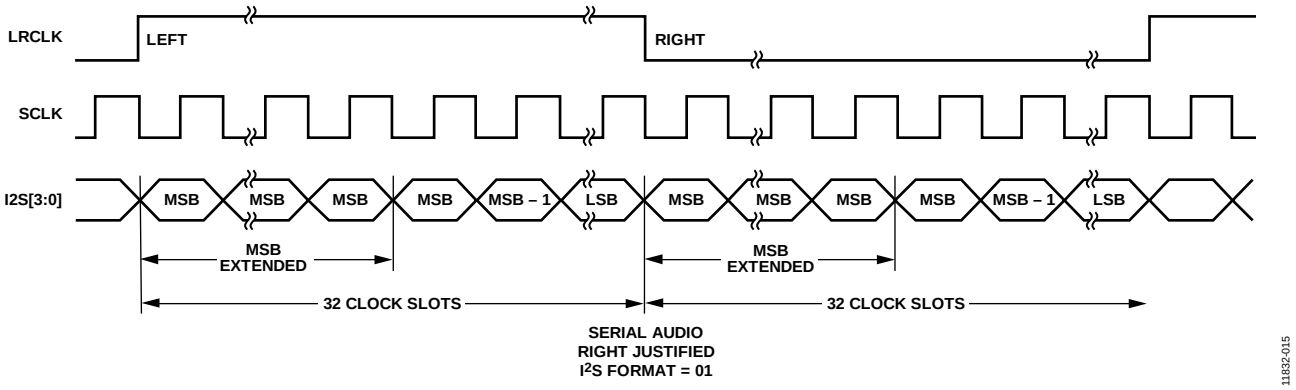



*Figure 11. Serial Audio, Right-Justified*

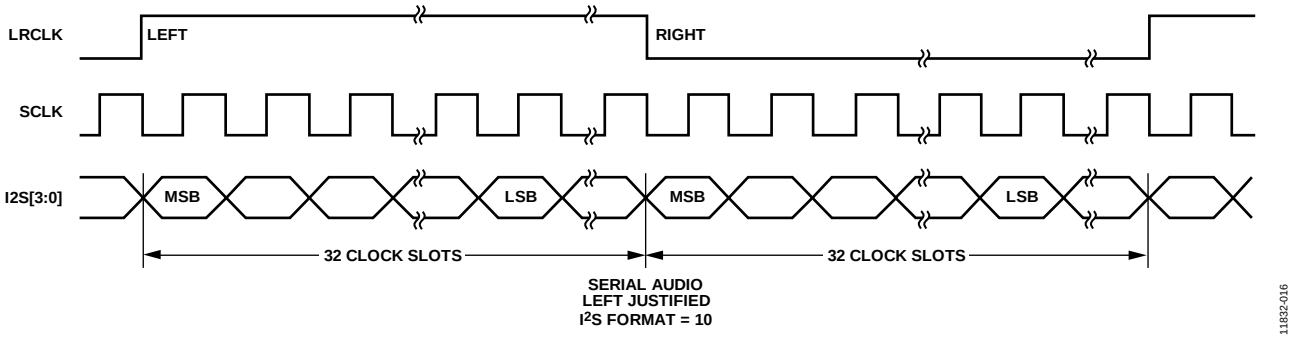



*Figure 12. Serial Audio, Left-Justified*

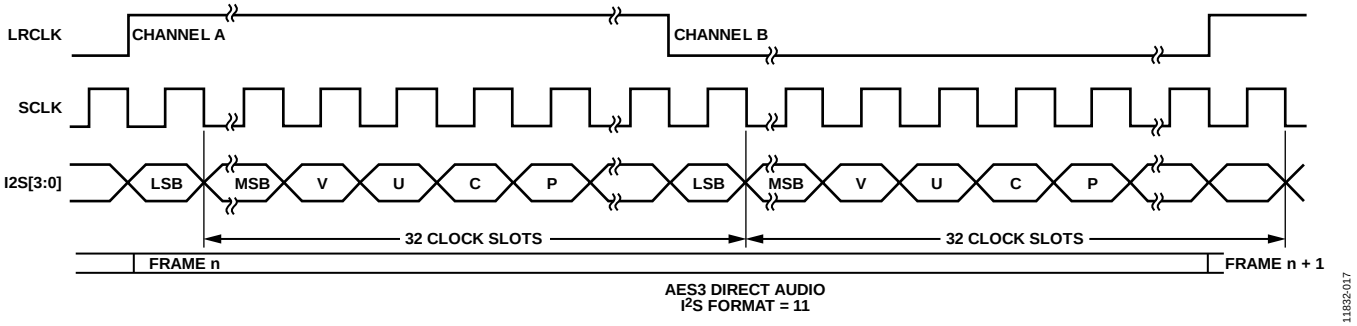



*Figure 13. AES3 Direct Audio*

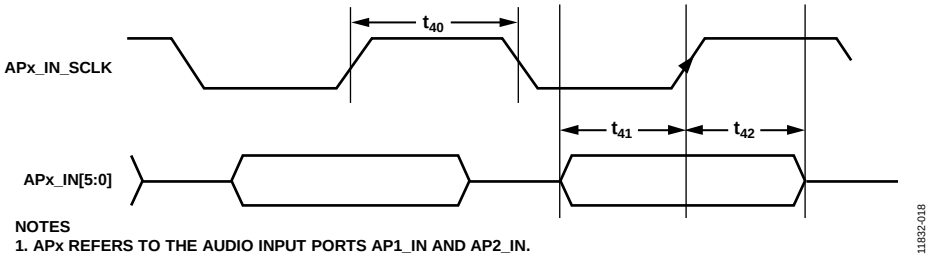
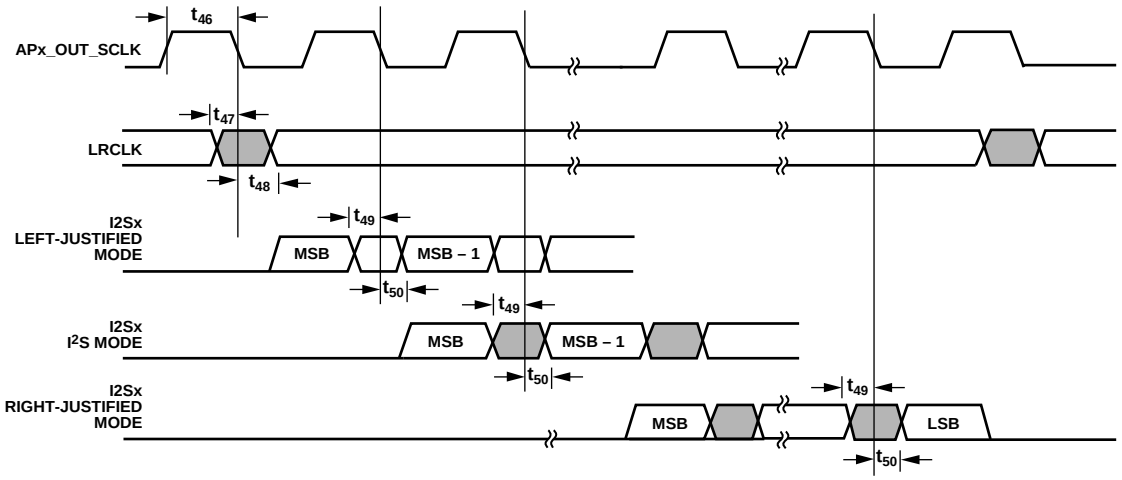
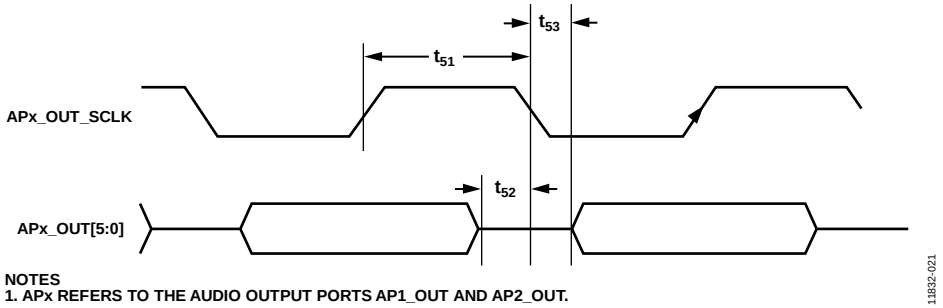



*Figure 14. DSD Input Timing*




NOTES
1. APx REFERS TO THE AUDIO OUTPUT PORTS AP1_OUT AND AP2_OUT.
2. LRCLK IS A SIGNAL ACCESSIBLE VIA APx_OUT5.
3. I2Sx ARE SIGNALS ACCESSIBLE VIA APx_OUT1 TO APx_OUT4.

*Figure 15. I²S Output Timing*




NOTES
1. APx REFERS TO THE AUDIO OUTPUT PORTS AP1_OUT AND AP2_OUT.

*Figure 16. DSD Output Timing*

## POWER SPECIFICATIONS

**Table 3.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| POWER SUPPLIES | | | | | |
| HDMI TxA Analog Power Supply | AVDD_TXA | 1.71 | 1.8 | 1.89 | V |
| HDMI TxB Analog Power Supply | AVDD_TXB | 1.71 | 1.8 | 1.89 | V |
| Comparator Power Supply | CVDD | 1.71 | 1.8 | 1.89 | V |
| Digital Power Supply | DVDD | 1.71 | 1.8 | 1.89 | V |
| Digital I/O Power Supply | DVDDIO | 3.14 | 3.3 | 3.46 | V |
| PLL Power Supply | PVDD | 1.71 | 1.8 | 1.89 | V |
| HDMI TxA PLL Power Supply | PVDD_TXA | 1.71 | 1.8 | 1.89 | V |
| HDMI TxB PLL Power Supply | PVDD_TXB | 1.71 | 1.8 | 1.89 | V |
| Termination Power Supply | TVDD | 3.14 | 3.3 | 3.46 | V |
| CURRENT CONSUMPTION—MUX MODE[1, 2] | | | | | |
| HDMI TxA Analog Power Supply | $I_{AVDD\_TXA}$ | | 23.2 | | mA |
| HDMI TxB Analog Power Supply | $I_{AVDD\_TXB}$ | | 23.2 | | mA |
| Comparator Power Supply | $I_{CVDD}$ | | 196 | | mA |
| Digital Core Power Supply | $I_{DVDD}$ | | 326.1 | | mA |
| Digital I/O Power Supply | $I_{DVDDIO}$ | | 0.1 | | mA |
| PLL Power Supply | $I_{PVDD}$ | | 69.7 | | mA |
| HDMI TxA PLL Power Supply | $I_{PVDD\_TXA}$ | | 71.5 | | mA |
| HDMI TxB PLL Power Supply | $I_{PVDD\_TXB}$ | | 71.5 | | mA |
| Termination Power Supply | $I_{TVDD}$ | | 116 | | mA |
| CURRENT CONSUMPTION—AUDIO EXTRACT/ AUDIO INSERT MODE[1, 3] | | | | | |
| HDMI TxA Analog Power Supply | $I_{AVDD\_TXA}$ | | 26.2 | | mA |
| HDMI TxB Analog Power Supply | $I_{AVDD\_TXB}$ | | 26.2 | | mA |
| Comparator Power Supply | $I_{CVDD}$ | | 184 | | mA |
| Digital Core Power Supply | $I_{DVDD}$ | | 436.0 | | mA |
| Digital I/O Power Supply | $I_{DVDDIO}$ | | 0.05 | | mA |
| PLL Power Supply | $I_{PVDD}$ | | 64 | | mA |
| HDMI TxA PLL Power Supply | $I_{PVDD\_TXA}$ | | 71.1 | | mA |
| HDMI TxB PLL Power Supply | $I_{PVDD\_TXB}$ | | 71.1 | | mA |
| Termination Power Supply | $I_{TVDD}$ | | 115 | | mA |
| CURRENT CONSUMPTION—SPLITTER MODE[1, 4] | | | | | |
| HDMI TxA Analog Power Supply | $I_{AVDD\_TXA}$ | | 26.2 | | mA |
| HDMI TxB Analog Power Supply | $I_{AVDD\_TXB}$ | | 26.2 | | mA |
| Comparator Power Supply | $I_{CVDD}$ | | 93 | | mA |
| Digital Core Power Supply | $I_{DVDD}$ | | 243.5 | | mA |
| Digital I/O Power Supply | $I_{DVDDIO}$ | | 0.05 | | mA |
| PLL Power Supply | $I_{PVDD}$ | | 33.5 | | mA |
| HDMI TxA PLL Power Supply | $I_{PVDD\_TXA}$ | | 71.1 | | mA |
| HDMI TxB PLL Power Supply | $I_{PVDD\_TXB}$ | | 71.1 | | mA |
| Termination Power Supply | $I_{TVDD}$ | | 115 | | mA |
| CURRENT CONSUMPTION—POWER-DOWN MODE 0[1, 5] | | | | | |
| HDMI TxA Analog Power Supply | $I_{AVDD\_TXA}$ | | 0.65 | | mA |
| HDMI TxB Analog Power Supply | $I_{AVDD\_TXB}$ | | 0.65 | | mA |
| Comparator Power Supply | $I_{CVDD}$ | | 0.84 | | mA |
| Digital Core Power Supply | $I_{DVDD}$ | | 0.25 | | mA |
| Digital I/O Power Supply | $I_{DVDDIO}$ | | 0.21 | | mA |
| PLL Power Supply | $I_{PVDD}$ | | 0.02 | | mA |
| HDMI TxA PLL Power Supply | $I_{PVDD\_TXA}$ | | 0.05 | | mA |
| HDMI TxB PLL Power Supply | $I_{PVDD\_TXB}$ | | 0.05 | | mA |
| Termination Power Supply | $I_{TVDD}$ | | 0.14 | | mA |

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| CURRENT CONSUMPTION—POWER-DOWN MODE 1[1, 6] | | | | | |
| HDMI TxA Analog Power Supply | $I_{AVDD\_TXA}$ | | 0.95 | | mA |
| HDMI TxB Analog Power Supply | $I_{AVDD\_TXB}$ | | 0.95 | | mA |
| Comparator Power Supply | $I_{CVDD}$ | | 0.84 | | mA |
| Digital Core Power Supply | $I_{DVDD}$ | | 0.95 | | mA |
| Digital I/O Power Supply | $I_{DVDDIO}$ | | 0.21 | | mA |
| PLL Power Supply | $I_{PVDD}$ | | 0.02 | | mA |
| HDMI TxA PLL Power Supply | $I_{PVDD\_TXA}$ | | 0.05 | | mA |
| HDMI TxB PLL Power Supply | $I_{PVDD\_TXB}$ | | 0.05 | | mA |
| Termination Power Supply | $I_{TVDD}$ | | 0.14 | | mA |
| CURRENT CONSUMPTION—EXAMPLE MAXIMUM OPERATING MODE[1, 7] | | | | | |
| HDMI TxA Analog Power Supply | $I_{AVDD\_TXA}$ | | | 31.00 | mA |
| HDMI TxB Analog Power Supply | $I_{AVDD\_TXB}$ | | | 31.00 | mA |
| Comparator Power Supply | $I_{CVDD}$ | | | 213.00 | mA |
| Digital Core Power Supply | $I_{DVDD}$ | | | 530.00 | mA |
| Digital I/O Power Supply | $I_{DVDDIO}$ | | | 0.20 | mA |
| PLL Power Supply | $I_{PVDD}$ | | | 75.00 | mA |
| HDMI TxA PLL Power Supply | $I_{PVDD\_TXA}$ | | | 80.00 | mA |
| HDMI TxB PLL Power Supply | $I_{PVDD\_TXB}$ | | | 80.00 | mA |
| Termination Power Supply | $I_{TVDD}$ | | | 128.00 | mA |

[1] Data recorded during lab characterization. Typical current consumption values are recorded with nominal voltage supply levels and at room temperature.
[2] ADV7626 configured in mux mode with two active HDMI Rx inputs and two HDMI Tx outputs in use. 4k × 2k at 30 Hz video format with pseudo random test pattern applied to each HDMI Rx input port. HDMI Rx termination closed on the two HDMI Rx input ports. HDMI Tx source termination enabled.
[3] ADV7626 configured in audio extract/audio insert mode with two active HDMI Rx inputs and two HDMI Tx outputs in use. Audio extracted from both HDMI Rx inputs and output on AP1_OUT and AP2_OUT. Audio inserted on HDMI Tx outputs from AP1_IN and AP2_IN input ports, respectively. HBR audio used. 4k × 2k at 30 Hz video format with pseudo random test pattern applied to both HDMI Rx input ports. HDMI Rx port termination closed on the two HDMI Rx input ports. HDMI Tx source termination enabled. OSD not enabled.
[4] ADV7626 configured in splitter mode with one HDMI Rx input and two HDMI Tx outputs in use. 4k × 2k at 30 Hz video format with pseudo random test pattern applied to one HDMI Rx input and output on both HDMI Tx outputs using splitter mode. HBR audio from HDMI Rx input inserted on the HDMI Tx outputs. No audio extraction. HDMI Rx port termination closed on the active HDMI Rx input port and open on the unused HDMI Rx input port. HDMI Tx source termination enabled. OSD enabled and blended on both HDMI Tx outputs using splitter mode.
[5] ADV7626 configured in Power-Down Mode 0 with two HDMI Rx inputs and two HDMI Tx outputs connected. In Power-Down Mode 0, all blocks are powered down except for the I²C slave.
[6] ADV7626 configured in Power-Down Mode 1 with two HDMI Rx inputs and two HDMI Tx outputs connected. In Power-Down Mode 1, all blocks are powered down except for the I²C slave and the CEC (to monitor wake-up interrupts).
[7] ADV7626 configured in an example maximum operating mode with two active HDMI Rx inputs and two HDMI Tx outputs in use. HBR audio from the two active HDMI Rx inputs inserted on the corresponding HDMI Tx outputs. No audio extraction. 4k × 2k at 30 Hz video format with pseudo random test pattern applied to both HDMI Rx input ports. HDMI Rx port termination closed on the two HDMI Rx input ports. HDMI Tx source termination enabled. OSD not enabled. Maximum current consumption values recorded with maximum power supply levels at device maximum operating temperature.

# ABSOLUTE MAXIMUM RATINGS

**Table 4.**

| Parameter | Rating |
|---|---|
| AVDD_TXA to GND | 2.2 V |
| AVDD_TXB to GND | 2.2 V |
| CVDD to GND | 2.2 V |
| DVDD to GND | 2.2 V |
| PVDD to GND | 2.2 V |
| PVDD_TXA to GND | 2.2 V |
| PVDD_TXB to GND | 2.2 V |
| DVDDIO to GND | 4.0 V |
| TVDD to GND | 4.0 V |
| Digital Inputs Voltage to GND | GND − 0.3 V to DVDDIO + 0.3 V up to a maximum of 4.0 V |
| 5 V Tolerant Digital Inputs to GND[1] | 5.5 V |
| Digital Outputs Voltage to GND | GND − 0.3 V to DVDDIO + 0.3 V up to a maximum of 4.0 V |
| XTAL+, XTAL− Pins | −0.3 V to PVDD + 0.3 V |
| Maximum Junction Temperature ($T_{J\,MAX}$) | 125°C |
| Storage Temperature Range | −65°C to +150°C |
| Infrared Reflow, Soldering (20 sec) | 260°C |

[1] The following inputs are 5 V tolerant: DDC_SCL_RXA, DDC_SDA_RXA, DDC_SCL_RXB, DDC_SDA_RXB, RXA_5V, RXB_5V, CEC_A, DDC_SCL_TXA, DDC_SDA_TXA, TXA_HPD_ARC−, TXA_ARC+, CEC_B, DDC_SCL_TXB, DDC_SDA_TXB, TXB_HPD_ARC−, and TXB_ARC+.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL PERFORMANCE

To reduce power consumption when using the ADV7626, the user is advised to turn off unused sections of the device.

Due to printed circuit board (PCB) metal variation and, therefore, variation in PCB heat conductivity, the value of $\theta_{JA}$ may differ for various PCBs. The most efficient measurement solution is obtained using the package surface temperature to estimate the die temperature because this solution eliminates the variance associated with the $\theta_{JA}$ value.

Do not exceed the maximum junction temperature ($T_{J\,MAX}$) of 125°C. The following equation calculates the junction temperature using the measured package surface temperature and applies only when no heat sink is used on the device under test (DUT):

$$T_J = T_S + (\Psi_{JT} \times W_{TOTAL})$$

where:
$T_S$ is the package surface temperature (°C).
$\Psi_{JT}$ = 0.41°C/W for the 260-ball CSP_BGA (based on 2s2p test board defined in the JEDEC specification).

$W_{TOTAL} = ((PVDD \times I_{PVDD}) + (PVDD\_TXA \times I_{PVDD\_TXA}) + (PVDD\_TXB \times I_{PVDD\_TXB}) + (TVDD \times I_{TVDD}) + (CVDD \times I_{CVDD}) + (AVDD\_TXA \times I_{AVDD\_TXA}) + (AVDD\_TXB \times I_{AVDD\_TXB}) + (DVDD \times I_{DVDD}) + (DVDDIO \times I_{DVDDIO}))$

Note that this calculation assumes a configuration of two active HDMI Rx inputs and two active HDMI Tx outputs, where termination is open on the unused Rx input ports.

A configuration of one active HDMI Rx input and two active HDMI Tx outputs (splitter mode) results in approximately 112 mW extra power dissipation on chip.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | GND | RXA_2+ | RXA_1+ | RXA_0+ | RXA_C+ | CVDD | RXB_2+ | RXB_1+ | RXB_0+ | RXB_C+ | CVDD | NC | NC | NC | NC | CVDD | NC | GND |
| B | GND | RXA_2– | RXA_1– | RXA_0– | RXA_C– | CVDD | RXB_2– | RXB_1– | RXB_0– | RXB_C– | CVDD | NC | NC | NC | NC | CVDD | NC | GND |
| C | GND | CVDD | CVDD | TVDD | TVDD | GND | GND | TVDD | TVDD | GND | GND | TVDD | TVDD | GND | GND | CVDD | GND | GND |
| D | INT1 | INT2 | SCL | SDA | $\overline{CS}$ | RXA_5V | RXA_HPA | DDC_ SCL_RXA | DDC_ SDA_RXA | DDC_ SCL_RXB | DDC_ SDA_RXB | RXB_HPA | RXB_5V | NC | TEST6 | TVDD | NC | NC |
| E | AP1_ OUT0 | AP1_ OUT1 | ALSB | $\overline{RESET}$ | | | | | | | | | | | NC | TVDD | NC | NC |
| F | AP1_ OUT2 | AP1_ OUT3 | AP2_ OUT0 | AP2_ OUT1 | | | | | | | | | | | NC | GND | NC | NC |
| G | AP1_ OUT4 | AP1_ OUT5 | AP2_ OUT2 | AP2_ OUT3 | | | DVDD | DVDD | DVDD | DVDD | DVDD | TEST5 | | | TEST7 | GND | NC | NC |
| H | AP1_ OUT_ MCLK | AP1_ OUT_ SCLK | AP2_ OUT4 | AP2_ OUT5 | | | DVDDIO | GND | GND | GND | GND | GND | | | NC | GND | CVDD | CVDD |
| J | AP2_ OUT_ MCLK | AP2_ OUT_ SCLK | TEST9 | TEST10 | | | DVDDIO | GND | GND | GND | GND | GND | | | TEST8 | TVDD | NC | NC |
| K | GND | GND | TEST11 | TEST12 | | | GND | GND | GND | GND | GND | GND | | | NC | TVDD | NC | NC |
| L | XTAL+ | XTAL– | TEST13 | TEST14 | | | GND | GND | GND | GND | GND | GND | | | NC | GND | NC | NC |
| M | PVDD | PVDD | TEST3 | TEST2 | | | GND | GND | GND | GND | GND | GND | | | NC | GND | NC | NC |
| N | GND | GND | PVDD_ TXA | PVDD_ TXA | | | | | | | | | | | GND | GND | CVDD | CVDD |
| P | TXA_C– | TXA_C+ | GND | R_TXA | | | | | | | | | | | TEST15 | TEST16 | TEST4 | TEST1 |
| R | TXA_0– | TXA_0+ | GND | AVDD_ TXA | TXB_ HPD_ ARC– | R_TXB | GND | TXB_ ARC+ | DDC_ SDA_TXB | DDC_ SCL_TXB | CEC_B | DVDDIO | EP_$\overline{CS}$ | AP2_IN_ SCLK | AP2_IN4 | AP2_IN2 | AP2_IN0 | TEST17 |
| T | TXA_1– | TXA_1+ | GND | AVDD_ TXA | CEC_A | GND | GND | GND | GND | AVDD_ TXB | AVDD_ TXB | DVDDIO | EP_SCLK | AP2_IN_ MCLK | AP2_IN5 | AP2_IN3 | AP2_IN1 | TEST18 |
| U | TXA_2– | TXA_2+ | GND | DDC_ SCL_ TXA | TXA_ ARC+ | PVDD_ TXB | GND | TXB_C+ | TXB_0+ | TXB_1+ | TXB_2+ | GND | EP_MOSI | AP1_IN_ SCLK | AP1_IN4 | AP1_IN2 | AP1_IN0 | GND |
| V | GND | GND | GND | DDC_ SDA_ TXA | TXA_ HPD_ ARC– | PVDD_ TXB | GND | TXB_C– | TXB_0– | TXB_1– | TXB_2– | GND | EP_MISO | AP1_IN_ MCLK | AP1_IN5 | AP1_IN3 | AP1_IN1 | GND |

11832-007

*Figure 17. Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | Mnemonic | Function | Description |
|---|---|---|---|
| A1 | GND | Ground | Ground. |
| A2 | RXA_2+ | HDMI Rx input | HDMI RxA Channel 2 True Input. |
| A3 | RXA_1+ | HDMI Rx input | HDMI RxA Channel 1 True Input. |
| A4 | RXA_0+ | HDMI Rx input | HDMI RxA Channel 0 True Input. |
| A5 | RXA_C+ | HDMI Rx input | HDMI RxA Clock True Input. |
| A6 | CVDD | Power | Comparator Power Supply (1.8 V). |
| A7 | RXB_2+ | HDMI Rx input | HDMI RxB Channel 2 True Input. |
| A8 | RXB_1+ | HDMI Rx input | HDMI RxB Channel 1 True Input. |
| A9 | RXB_0+ | HDMI Rx input | HDMI RxB Channel 0 True Input. |
| A10 | RXB_C+ | HDMI Rx input | HDMI RxB Clock True Input. |
| A11 | CVDD | Power | Comparator Power Supply (1.8 V). |
| A12 | NC | Do not connect | Leave this pin floating. |

| Pin No. | Mnemonic | Function | Description |
|---|---|---|---|
| A13 | NC | Do not connect | Leave this pin floating. |
| A14 | NC | Do not connect | Leave this pin floating. |
| A15 | NC | Do not connect | Leave this pin floating. |
| A16 | CVDD | Power | Comparator Power Supply (1.8 V). |
| A17 | NC | Do not connect | Leave this pin floating. |
| A18 | GND | Ground | Ground. |
| B1 | GND | Ground | Ground. |
| B2 | RXA_2– | HDMI Rx input | HDMI RxA Channel 2 Complement Input. |
| B3 | RXA_1– | HDMI Rx input | HDMI RxA Channel 1 Complement Input. |
| B4 | RXA_0– | HDMI Rx input | HDMI RxA Channel 0 Complement Input. |
| B5 | RXA_C– | HDMI Rx input | HDMI RxA Clock Complement Input. |
| B6 | CVDD | Power | Comparator Power Supply (1.8 V). |
| B7 | RXB_2– | HDMI Rx input | HDMI RxB Channel 2 Complement Input. |
| B8 | RXB_1– | HDMI Rx input | HDMI RxB Channel 1 Complement Input. |
| B9 | RXB_0– | HDMI Rx input | HDMI RxB Channel 0 Complement Input. |
| B10 | RXB_C– | HDMI Rx input | HDMI RxB Clock Complement Input. |
| B11 | CVDD | Power | Comparator Power Supply (1.8 V). |
| B12 | NC | Do not connect | Leave this pin floating. |
| B13 | NC | Do not connect | Leave this pin floating. |
| B14 | NC | Do not connect | Leave this pin floating. |
| B15 | NC | Do not connect | Leave this pin floating. |
| B16 | CVDD | Power | Comparator Power Supply (1.8 V). |
| B17 | NC | Do not connect | Leave this pin floating. |
| B18 | GND | Ground | Ground. |
| C1 | GND | Ground | Ground. |
| C2 | CVDD | Power | Comparator Power Supply (1.8 V). |
| C3 | CVDD | Power | Comparator Power Supply (1.8 V). |
| C4 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| C5 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| C6 | GND | Ground | Ground. |
| C7 | GND | Ground | Ground. |
| C8 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| C9 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| C10 | GND | Ground | Ground. |
| C11 | GND | Ground | Ground. |
| C12 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| C13 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| C14 | GND | Ground | Ground. |
| C15 | GND | Ground | Ground. |
| C16 | CVDD | Power | Comparator Power Supply (1.8 V). |
| C17 | GND | Ground | Ground. |
| C18 | GND | Ground | Ground. |
| D1 | INT1 | Control | Interrupt Output. This pin can be active low or high. When an unmasked status bit changes, an interrupt is generated on this pin. |
| D2 | INT2 | Control | Interrupt Output. This pin can be active low or high. When an unmasked status bit changes, an interrupt is generated on this pin. |
| D3 | SCL | $I^2C$ control | $I^2C$ Clock Input. This pin is open drain; connect this pin to a 3.3 V supply using a 4.7 kΩ resistor. |
| D4 | SDA | $I^2C$ control | $I^2C$ Data Input. This pin is open drain; connect this pin to a 3.3 V supply using a 4.7 kΩ resistor. |
| D5 | $\overline{CS}$ | Digital input | Chip Select Pin. This pin must be set low or left floating for the chip to process $I^2C$ messages that are destined for the ADV7626. The ADV7626 ignores $I^2C$ messages when this pin is high. |
| D6 | RXA_5V | HDMI Rx input | HDMI RxA 5 V Detect Pin. |

| Pin No. | Mnemonic | Function | Description |
|---|---|---|---|
| D7 | RXA_HPA | HDMI Rx output | HDMI RxA Hot Plug Assert. |
| D8 | DDC_SCL_RXA | HDMI Rx DDC | HDCP Slave Serial Clock for HDMI RxA. |
| D9 | DDC_SDA_RXA | HDMI Rx DDC | HDCP Slave Serial Data for HDMI RxA. |
| D10 | DDC_SCL_RXB | HDMI Rx DDC | HDCP Slave Serial Clock for HDMI RxB. |
| D11 | DDC_SDA_RXB | HDMI Rx DDC | HDCP Slave Serial Data for HDMI RxB. |
| D12 | RXB_HPA | HDMI Rx output | HDMI RxB Hot Plug Assert. |
| D13 | RXB_5V | HDMI Rx input | HDMI RxB 5 V Detect Pin. |
| D14 | NC | Do not connect | Leave this pin floating. |
| D15 | TEST6 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| D16 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| D17 | NC | Do not connect | Leave this pin floating. |
| D18 | NC | Do not connect | Leave this pin floating. |
| E1 | AP1_OUT0 | Audio output | Audio Output Port 1, Output 0. |
| E2 | AP1_OUT1 | Audio output | Audio Output Port 1, Output 1. |
| E3 | ALSB | $I^2C$ control | Pin to set the $I^2C$ address of the I/O register map for the device. When the ALSB pin is tied low, the I/O register map $I^2C$ address is 0xB0. When the ALSB pin is tied high, the I/O register map $I^2C$ address is 0xB2. |
| E4 | $\overline{\text{RESET}}$ | Miscellaneous digital | Reset Pin. |
| E15 | NC | Do not connect | Leave this pin floating. |
| E16 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| E17 | NC | Do not connect | Leave this pin floating. |
| E18 | NC | Do not connect | Leave this pin floating. |
| F1 | AP1_OUT2 | Audio output | Audio Output Port 1, Output 2. |
| F2 | AP1_OUT3 | Audio output | Audio Output Port 1, Output 3. |
| F3 | AP2_OUT0 | Audio output | Audio Output Port 2, Output 0. |
| F4 | AP2_OUT1 | Audio output | Audio Output Port 2, Output 1. |
| F15 | NC | Do not connect | Leave this pin floating. |
| F16 | GND | Ground | Ground. |
| F17 | NC | Do not connect | Leave this pin floating. |
| F18 | NC | Do not connect | Leave this pin floating. |
| G1 | AP1_OUT4 | Audio output | Audio Output Port 1, Output 4. |
| G2 | AP1_OUT5 | Audio output | Audio Output Port 1, Output 5. |
| G3 | AP2_OUT2 | Audio output | Audio Output Port 2, Output 2. |
| G4 | AP2_OUT3 | Audio output | Audio Output Port 2, Output 3. |
| G7 | DVDD | Power | Digital Power Supply (1.8 V). |
| G8 | DVDD | Power | Digital Power Supply (1.8 V). |
| G9 | DVDD | Power | Digital Power Supply (1.8 V). |
| G10 | DVDD | Power | Digital Power Supply (1.8 V). |
| G11 | DVDD | Power | Digital Power Supply (1.8 V). |
| G12 | TEST5 | Test pin | Test Pin 5. Leave this pin floating. |
| G15 | TEST7 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| G16 | GND | Ground | Ground. |
| G17 | NC | Do not connect | Leave this pin floating. |
| G18 | NC | Do not connect | Leave this pin floating. |
| H1 | AP1_OUT_MCLK | Audio output | Audio Output Port 1, MCLK. |
| H2 | AP1_OUT_SCLK | Audio output | Audio Output Port 1, SCLK. |
| H3 | AP2_OUT4 | Audio output | Audio Output Port 2, Output 4. |
| H4 | AP2_OUT5 | Audio output | Audio Output Port 2, Output 5. |
| H7 | DVDDIO | Power | Digital Interface Supply (3.3 V). |
| H8 | GND | Ground | Ground. |
| H9 | GND | Ground | Ground. |
| H10 | GND | Ground | Ground. |
| H11 | GND | Ground | Ground. |

| Pin No. | Mnemonic | Function | Description |
|---|---|---|---|
| H12 | GND | Ground | Ground. |
| H15 | NC | Do not connect | Leave this pin floating. |
| H16 | GND | Ground | Ground. |
| H17 | CVDD | Power | Comparator Power Supply (1.8 V). |
| H18 | CVDD | Power | Comparator Power Supply (1.8 V). |
| J1 | AP2_OUT_MCLK | Audio output | Audio Output Port 2, MCLK. |
| J2 | AP2_OUT_SCLK | Audio output | Audio Output Port 2, SCLK. |
| J3 | TEST9 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| J4 | TEST10 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| J7 | DVDDIO | Power | Digital Interface Supply (3.3 V). |
| J8 | GND | Ground | Ground. |
| J9 | GND | Ground | Ground. |
| J10 | GND | Ground | Ground. |
| J11 | GND | Ground | Ground. |
| J12 | GND | Ground | Ground. |
| J15 | TEST8 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| J16 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| J17 | NC | Do not connect | Leave this pin floating. |
| J18 | NC | Do not connect | Leave this pin floating. |
| K1 | GND | Ground | Ground. |
| K2 | GND | Ground | Ground. |
| K3 | TEST11 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| K4 | TEST12 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| K7 | GND | Ground | Ground. |
| K8 | GND | Ground | Ground. |
| K9 | GND | Ground | Ground. |
| K10 | GND | Ground | Ground. |
| K11 | GND | Ground | Ground. |
| K12 | GND | Ground | Ground. |
| K15 | NC | Do not connect | Leave this pin floating. |
| K16 | TVDD | Power | HDMI Rx Terminator Supply Voltage (3.3 V). |
| K17 | NC | Do not connect | Leave this pin floating. |
| K18 | NC | Do not connect | Leave this pin floating. |
| L1 | XTAL+ | Miscellaneous digital | ADV7626 Crystal Input. |
| L2 | XTAL− | Miscellaneous digital | ADV7626 Crystal Output. |
| L3 | TEST13 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| L4 | TEST14 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| L7 | GND | Ground | Ground. |
| L8 | GND | Ground | Ground. |
| L9 | GND | Ground | Ground. |
| L10 | GND | Ground | Ground. |
| L11 | GND | Ground | Ground. |
| L12 | GND | Ground | Ground. |
| L15 | NC | Do not connect | Leave this pin floating. |
| L16 | GND | Ground | Ground. |
| L17 | NC | Do not connect | Leave this pin floating. |
| L18 | NC | Do not connect | Leave this pin floating. |
| M1 | PVDD | Power | PLL Digital Supply (1.8 V). |
| M2 | PVDD | Power | PLL Digital Supply (1.8 V). |
| M3 | TEST3 | Test pin | Test Pin 3. Leave this pin floating. |
| M4 | TEST2 | Test pin | Test Pin 2. Leave this pin floating. |
| M7 | GND | Ground | Ground. |
| M8 | GND | Ground | Ground. |

| Pin No. | Mnemonic | Function | Description |
|---|---|---|---|
| M9 | GND | Ground | Ground. |
| M10 | GND | Ground | Ground. |
| M11 | GND | Ground | Ground. |
| M12 | GND | Ground | Ground. |
| M15 | NC | Do not connect | Leave this pin floating. |
| M16 | GND | Ground | Ground. |
| M17 | NC | Do not connect | Leave this pin floating. |
| M18 | NC | Do not connect | Leave this pin floating. |
| N1 | GND | Ground | Ground. |
| N2 | GND | Ground | Ground. |
| N3 | PVDD_TXA | Power | HDMI TxA PLL Power Supply (1.8 V). |
| N4 | PVDD_TXA | Power | HDMI TxA PLL Power Supply (1.8 V). |
| N15 | GND | Ground | Ground. |
| N16 | GND | Ground | Ground. |
| N17 | CVDD | Power | Comparator Power Supply (1.8 V). |
| N18 | CVDD | Power | Comparator Power Supply (1.8 V). |
| P1 | TXA_C− | HDMI Tx output | HDMI TxA Clock Complement Output. |
| P2 | TXA_C+ | HDMI Tx output | HDMI TxA Clock True Output. |
| P3 | GND | Ground | Ground. |
| P4 | R_TXA | HDMI Tx input | This pin sets the internal reference currents for HDMI TxA. Place a 470 Ω resistor (1% tolerance) between this pin and GND. Place the external resistor as close as possible to the ADV7626. |
| P15 | TEST15 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| P16 | TEST16 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| P17 | TEST4 | Test pin | Test Pin 4. Leave this pin floating. |
| P18 | TEST1 | Test pin | Test Pin 1. Leave this pin floating. |
| R1 | TXA_0− | HDMI Tx output | HDMI TxA Channel 0 Complement Output. |
| R2 | TXA_0+ | HDMI Tx output | HDMI TxA Channel 0 True Output. |
| R3 | GND | Ground | Ground. |
| R4 | AVDD_TXA | Power | HDMI TxA Analog Supply (1.8 V). |
| R5 | TXB_HPD_ARC− | HDMI Tx input | HDMI TxB Hot Plug Detect (HPD) Signal and Audio Return Channel Complement Input. |
| R6 | R_TXB | HDMI Tx input | This pin sets the internal reference currents for HDMI TxB. Place a 470 Ω resistor (1% tolerance) between this pin and GND. Place the external resistor as close as possible to the ADV7626. |
| R7 | GND | Ground | Ground. |
| R8 | TXB_ARC+ | HDMI Tx input | HDMI TxB Audio Return Channel True Input. |
| R9 | DDC_SDA_TXB | HDMI Tx DDC | HDCP Slave Serial Data for HDMI TxB. |
| R10 | DDC_SCL_TXB | HDMI Tx DDC | HDCP Slave Serial Clock for HDMI TxB. |
| R11 | CEC_B | HDMI Tx CEC | HDMI TxB Consumer Electronics Control (CEC). |
| R12 | DVDDIO | Power | Digital Interface Supply (3.3 V). |
| R13 | EP_$\overline{CS}$ | Serial port control | SPI Chip Select Interface for the OSD. |
| R14 | AP2_IN_SCLK | Audio input | Audio Input Port 2, SCLK. |
| R15 | AP2_IN4 | Audio input | Audio Input Port 2, Input 4. |
| R16 | AP2_IN2 | Audio input | Audio Input Port 2, Input 2. |
| R17 | AP2_IN0 | Audio input | Audio Input Port 2, Input 0. |
| R18 | TEST17 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| T1 | TXA_1− | HDMI Tx output | HDMI TxA Channel 1 Complement Output. |
| T2 | TXA_1+ | HDMI Tx output | HDMI TxA Channel 1 True Output. |
| T3 | GND | Ground | Ground. |
| T4 | AVDD_TXA | Power | HDMI TxA Analog Supply (1.8 V). |
| T5 | CEC_A | HDMI Tx CEC | HDMI TxA Consumer Electronics Control (CEC). |
| T6 | GND | Ground | Ground. |
| T7 | GND | Ground | Ground. |

| Pin No. | Mnemonic | Function | Description |
|---|---|---|---|
| T8 | GND | Ground | Ground. |
| T9 | GND | Ground | Ground. |
| T10 | AVDD_TXB | Power | HDMI TxB Analog Supply (1.8 V). |
| T11 | AVDD_TXB | Power | HDMI TxB Analog Supply (1.8 V). |
| T12 | DVDDIO | Power | Digital Interface Supply (3.3 V). |
| T13 | EP_SCLK | Serial port control | SPI Clock Interface for the OSD. |
| T14 | AP2_IN_MCLK | Audio input | Audio Input Port 2, MCLK. |
| T15 | AP2_IN5 | Audio input | Audio Input Port 2, Input 5. |
| T16 | AP2_IN3 | Audio input | Audio Input Port 2, Input 3. |
| T17 | AP2_IN1 | Audio input | Audio Input Port 2, Input 1. |
| T18 | TEST18 | Test pin | Connect this pin to ground using a 4.7 kΩ resistor. |
| U1 | TXA_2− | HDMI Tx output | HDMI TxA Channel 2 Complement Output. |
| U2 | TXA_2+ | HDMI Tx output | HDMI TxA Channel 2 True Output. |
| U3 | GND | Ground | Ground. |
| U4 | DDC_SCL_TXA | HDMI Tx DDC | HDCP Slave Serial Clock for HDMI TxA. |
| U5 | TXA_ARC+ | HDMI Tx input | HDMI TxA Audio Return Channel True Input. |
| U6 | PVDD_TXB | Power | HDMI TxB PLL Power Supply (1.8 V). |
| U7 | GND | Ground | Ground. |
| U8 | TXB_C+ | HDMI Tx output | HDMI TxB Clock True Output. |
| U9 | TXB_0+ | HDMI Tx output | HDMI TxB Channel 0 True Output. |
| U10 | TXB_1+ | HDMI Tx output | HDMI TxB Channel 1 True Output. |
| U11 | TXB_2+ | HDMI Tx output | HDMI TxB Channel 2 True Output. |
| U12 | GND | Ground | Ground. |
| U13 | EP_MOSI | Serial port control | SPI Master Output/Slave Input for OSD. |
| U14 | AP1_IN_SCLK | Audio input | Audio Input Port 1, SCLK. |
| U15 | AP1_IN4 | Audio input | Audio Input Port 1, Input 4. |
| U16 | AP1_IN2 | Audio input | Audio Input Port 1, Input 2. |
| U17 | AP1_IN0 | Audio input | Audio Input Port 1, Input 0. |
| U18 | GND | Ground | Ground. |
| V1 | GND | Ground | Ground. |
| V2 | GND | Ground | Ground. |
| V3 | GND | Ground | Ground. |
| V4 | DDC_SDA_TXA | HDMI Tx DDC | HDCP Slave Serial Data for HDMI TxA. |
| V5 | TXA_HPD_ARC− | HDMI Tx input | HDMI TxA Hot Plug Detect (HPD) Signal and Audio Return Channel Complement Input. |
| V6 | PVDD_TXB | Power | HDMI TxB PLL Power Supply (1.8 V). |
| V7 | GND | Ground | Ground. |
| V8 | TXB_C− | HDMI Tx output | HDMI TxB Clock Complement Output. |
| V9 | TXB_0− | HDMI Tx output | HDMI TxB Channel 0 Complement Output. |
| V10 | TXB_1− | HDMI Tx output | HDMI TxB Channel 1 Complement Output. |
| V11 | TXB_2− | HDMI Tx output | HDMI TxB Channel 2 Complement Output. |
| V12 | GND | Ground | Ground. |
| V13 | EP_MISO | Serial port control | SPI Master Input/Slave Output for OSD. |
| V14 | AP1_IN_MCLK | Audio input | Audio Input Port 1, MCLK. |
| V15 | AP1_IN5 | Audio input | Audio Input Port 1, Input 5. |
| V16 | AP1_IN3 | Audio input | Audio Input Port 1, Input 3. |
| V17 | AP1_IN1 | Audio input | Audio Input Port 1, Input 1. |
| V18 | GND | Ground | Ground. |

# POWER SUPPLY RECOMMENDATIONS

## POWER-UP SEQUENCE

The power-up sequence for the ADV7626 is as follows:

1. Hold the $\overline{\text{RESET}}$ pin low.
2. Power up the 3.3 V supplies (DVDDIO and TVDD).
3. After the 3.3 V supplies reach their minimum recommended value of 3.14 V, wait at least 20 ms before powering up the 1.8 V supplies.
4. Power up the 1.8 V supplies (AVDD_TXA, AVDD_TXB, CVDD, DVDD, PVDD, PVDD_TXA, and PVDD_TXB). These supplies should be powered up at the same time; that is, there should be a difference of less than 0.3 V between them.
5. Release the $\overline{\text{RESET}}$ pin after all supplies are established.

After power-up, a complete reset is recommended. This reset can be performed by the system microcontroller.

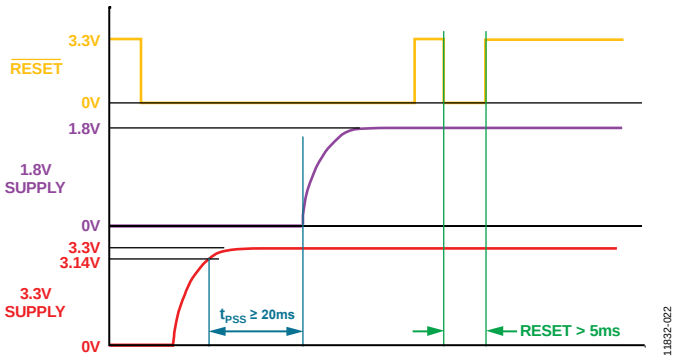



*Figure 18. ADV7626 Supply Power-Up Sequence*

## POWER-DOWN SEQUENCE

The ADV7626 supplies can be deasserted simultaneously as long as DVDDIO or TVDD does not fall below a lower rated supply.

# THEORY OF OPERATION

## HDMI RECEIVER

The ADV7626 front end incorporates two HDMI receivers capable of receiving all HDTV formats up to 3 GHz (4k × 2k at 24 Hz/25 Hz/30 Hz). The HDMI receivers also support HDMI features including 3D TV and content type bits.

Each HDMI receiver in the ADV7626 incorporates an adaptive equalizer, which compensates for the high frequency losses inherent in HDMI and DVI cabling, especially at longer lengths and higher frequencies.

The ADV7626 features a 768-byte internal EDID memory space, which can be used to store two independent EDIDs, one for each receiver. The memory can be partitioned to provide two 256-byte EDIDs or one 512-byte extended EDID and one 256-byte EDID. Either EDID can be replicated on any input port.

The two HDMI receivers offer advanced audio functionality. Each receiver supports multichannel I²S audio for up to eight channels. The receivers also support a six-DSD channel interface, with each channel carrying an oversampled 1-bit representation of the audio signal as delivered on SACD. The ADV7626 can also receive HBR audio packet streams and output them through the HBR interface in an S/PDIF format that conforms to the IEC 60958 standard. S/PDIF is supported via the HPD back channel. The receivers also contain an audio mute controller that can detect a variety of conditions that can result in audible extraneous noise in the audio output. On detection of these conditions, the audio data can be ramped to prevent audio clicks or pops.

## HDCP REPEATER FUNCTIONALITY

With the inclusion of HDCP 1.4, displays can receive encrypted video content. The HDMI interface of the ADV7626 allows authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP 1.4 protocol. Repeater support is also offered by the ADV7626.

## DIGITAL AUDIO PORTS

The ADV7626 features two independent audio input ports and two independent audio output ports. The audio input and output ports provide comprehensive muxing support for the destination of the audio (for example, to either HDMI transmitter or either audio output port) and support for the source of the audio (for example, from either HDMI receiver or from either audio input port). The extracted audio can be processed by a SHARC® processor and can be reinserted back into the HDMI output stream or output via the hardware connected to the system.

## ON-SCREEN DISPLAY

A key feature of the ADV7626 is the on-chip character- and icon-based OSD generator. The generated OSD can be converted to match the 4:2:2 or 4:4:4 input format in either the RGB or YCrCb color spaces. After the OSD is generated, it is overlaid at the output resolution (any video resolution up to 4k × 2k at 24 Hz/25 Hz/30 Hz) for best performance. The OSD portion of the image is optionally semitransparent using a 5-bit alpha blend between the input video and the OSD. The OSD font characters and icons can be stored in external SPI flash memory, read directly into RAM, or they can be loaded into the on-chip RAM via the SPI or I²C interface.

## HDMI TRANSMITTERS

The ADV7626 incorporates dual HDMI transmitters, supporting all HDTV formats up to 3 GHz (4k × 2k at 24 Hz/25 Hz/30 Hz), ARC, and all mandatory 3D TV formats. The HDMI transmitter can output any audio mode received from the HDMI receiver, including audio sample packets, HBR, or DSD.

The ARC receiver supports both single-ended and differential modes and simplifies cabling by combining an upstream audio capability in a conventional HDMI cable. Each transmitter features an on-chip MPU with an I²C master to perform HDCP operations and EDID read operations.

## I²C INTERFACE

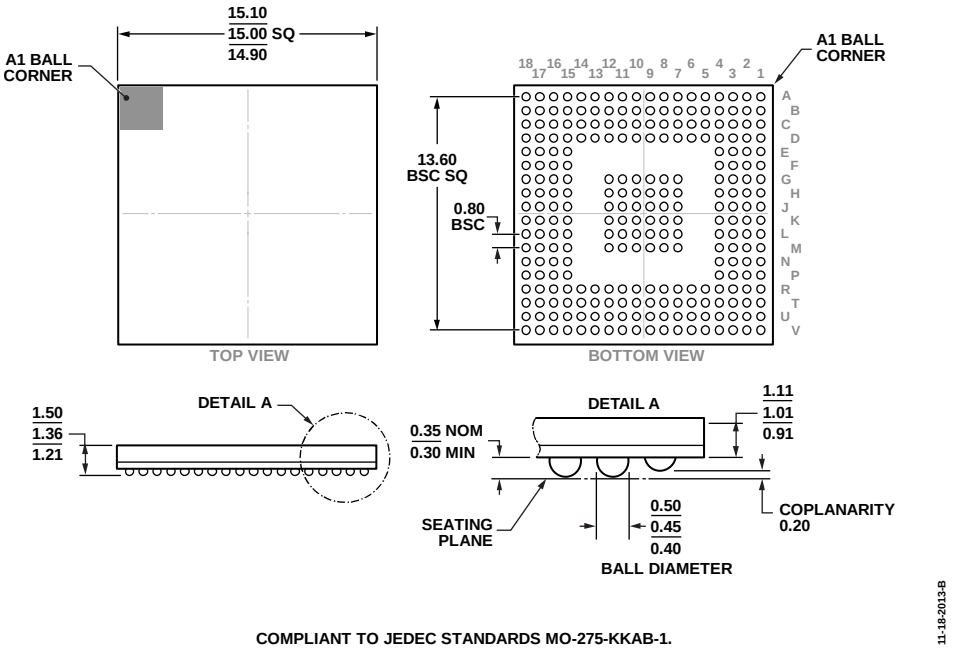
The ADV7626 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. The ADV7626 is controlled by an external I²C master device, such as a microcontroller.

## OTHER FEATURES

Other features of the ADV7626 include the following:

- Fully qualified software low level libraries, driver, and application
- Complete input and output audio support
- Programmable interrupt request output pins: INT1 and INT2
- Chip select and ALSB
- Low power consumption: 1.8 V digital core, 1.8 V analog, and 3.3 V digital input/output
- Temperature range: 0°C to 70°C
- 15 mm × 15 mm, Pb-free, 260-ball CSP_BGA

# OUTLINE DIMENSIONS




COMPLIANT TO JEDEC STANDARDS MO-275-KKAB-1.

*Figure 19. 260-Ball Chip Scale Package Ball Grid Array [CSP_BGA]*
*(BC-260-1)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1, 2] | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADV7626KBCZ-8 | 0°C to 70°C | 260-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-260-1 |
| ADV7626KBCZ-8-RL | 0°C to 70°C | 260-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-260-1 |
| EVAL-ADV7625-SMZ | | Evaluation Board | |

[1] Z = RoHS Compliant Part.
[2] This part is programmed with internal HDCP keys. Customers must have HDCP adopter status (consult Digital Content Protection, LLC, for licensing requirements) to purchase any components with internal HDCP keys.

# NOTES

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).
HDMI, the HDMI Logo, and High-Definition Multimedia Interface are trademarks or registered trademarks of HDMI Licensing LLC in the United States and other countries.


D11832-0-12/13(0)