

FEATURES

Video signal processor

- Full 12-bit, 4:4:4 YUV internal processing
- Motion adaptive de-interlacing with ultralow angle interpolation
- Multiple video processing paths
- Upscaling to 4k × 2k (ADV8003KBCZ-8x models only)
- Aspect ratio conversion/panorama scaling
- Cadence detection for the recovery of original frames from film-based content
- Dual video scalars enable simultaneous output of multiple different resolutions
- Sharpness and detail enhancement
- Noise reduction to reduce random, mosquito, and block noise
- Frame rate converter
- Support for up to 3 simultaneous video streams, including picture-in-picture (PiP) support

On-screen display (OSD)

- Internally generated bitmap-based OSD allowing overlay on one or more video outputs
- Overlay on 3D video formats
- Dedicated OSD scaler
- Alpha blending of OSD data on video data
- Disturbance free blending of OSD on either of 2 zones
- Option of external OSD
- Easy to use software tool for developing OSDs

HDMI transmitters

- Dual HDMI transmitters enabling splitter capability
- Content type bits
- CEC 1.4 controller
- Audio return channel (ARC) support
- Support of standard S/PDIF for stereo LPCM compressed audio up to 192 kHz
- 6-channel uncompressed LPCM I²S audio up to 192 kHz
- 6-channel direct stream digital (DSD) audio inputs
- Noise shaped video (NSV) six-DAC video encoder
- Six 12-bit NSV video DACs
- Multiformat video output support
 - Composite (CVBS), S-Video (Y/C), and Component YPrPb (SD, ED, and HD)
- Rovi Rev. 7.1.L1 (SD) and Rev. 1.4 (ED) compliant
- Simultaneous SD and ED/HD operation
- Professional video mode
- Capability to output up to 36-bit TTL data

APPLICATIONS

- High-end A/V receivers
- Upconverting DVD players/recorders
- Blu-ray players/recorders
- Set-top boxes
- Video conferencing
- Standalone video processors
- HDMI splitters

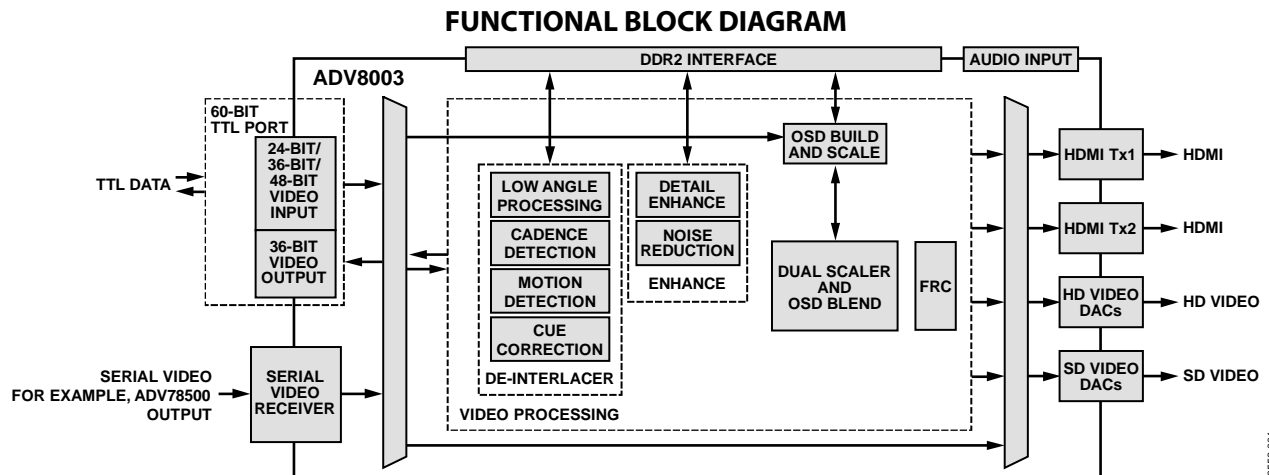


Figure 1.

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REVISION HISTORY

8/13—Revision B: Initial Version

GENERAL DESCRIPTION

The **ADV8003** is a multiple input video signal processor that can de-interlace and scale SD, ED, or HD video data to HD formats; generate a bitmap on-screen display (OSD); and output the video with OSD overlaid on two High Definition Multimedia Interface (HDMI®) transmitters and a video encoder.

Video can be input into the **ADV8003** in a number of ways: using the 48-bit TTL pixel port, using the 24-bit external OSD TTL pixel port, or from a device with an HDMI transmitter such as the **ADV7850**. The **ADV8003** supports many of the formats outlined in the CEA-861 and VESA specifications, as well as several other widely used timing formats.

Using two external DDR2 memories, the **ADV8003** can perform high performance, motion adaptive interlaced to progressive conversion on SD and HD content. Using a single DDR2 memory, the HD de-interlacing is limited to intrafield.

The **ADV8003** features primary and secondary video scalars that enable simultaneous output of multiple different resolutions. The primary video scalar of the ADV8003KBCZ-8/8B/8C models is capable of upscaling to 4k × 2k format and downscaling from 1080p. The primary video scalar of the ADV8003KBCZ-7/ADV8003KBCZ-7B/ADV8003KBCZ-7C/ADV8003KBCZ-7T models is capable of upscaling and downscaling to and from a 1080p format. The secondary video scalar facilitates up-scaling to 1080p and downscaling to 480p. Detail enhancement and image enhancing techniques such as random, mosquito, and block noise reduction allow for improved final image quality. The frame rate converter of the **ADV8003** allows the conversion between common frame rates with support to output two different frame rates simultaneously under certain conditions.

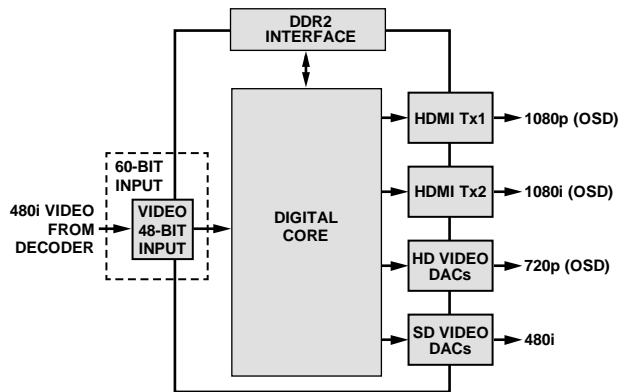


Figure 2. Sample Multiple Output Configuration

The **ADV8003** has a flexible digital core that allows the user to configure the part in several different modes; for example, using a single video processing channel, using dual video processing

channels, or displaying OSD on multiple outputs of different resolutions.

The **ADV8003** can accept OSD information from an external OSD source on the 24-bit external OSD TTL pixel data input or can internally generate a high quality, bitmap-based OSD. The internal OSD is highly flexible and allows the system designer to easily incorporate features like scrolling text and animation in various color depths up to 24-bit true color.

Analog Devices, Inc., provides an OSD development tool (Blimp) to assist in the design, debug, and emulation of the OSD prior to integration with the system application. When the design is complete, the OSD development tool automatically generates code to which system APIs can be added before integration with the system application and an OSD design resource, which must be downloaded to an external SPI flash memory.

Video can be output from the **ADV8003** using one or both of the HDMI transmitters and/or the 6-DAC SD/HD video encoder. The flexible multiplexing allows simultaneous output on the HDMI transmitters and HD formats on the HD DACs (for example, 1080p) with SD formats on the SD DACs (for example, 480i).

Both of the HDMI transmitters on the ADV8003 support all mandatory and many optional 3D video resolutions and audio return channels (ARC). Each transmitter also features a full CEC master. The **ADV8003** can receive up to six channels of I²S, S/PDIF, direct stream digital (DSD), and high bit rate (HBR).

The six 12-bit NSV® video DACs allow for composite (CVBS), S-Video (Y/C), and component (YPrPb) analog outputs in standard, enhanced, and high definition video formats. Over-sampling of 216 MHz (SD and ED) and 297 MHz (HD) removes the requirement for external output filtering.

The **ADV8003** can also support 30-bit TTL in mode and 30-bit TTL out mode for professional applications, which do not require the use of HDMI.

The **ADV8003** supports the I²C protocol for communication with the system microcontroller.

THE ADV8003 FAMILY

There are a number of derivatives within the **ADV8003** family, each featuring different capabilities; all are provided in the same 19 mm × 19 mm, 425-ball CSP_BGA package (see Table 1).

Note that the functionality of the ADV8003KBCZ-8 is described throughout this data sheet. Some sections are not relevant to other models because not all of the blocks found in the ADV8003KBCZ-8 are included in those models. Table 1 lists the functionality for each model.

Table 1. Features Sets of the ADV8003 Family ICs

| Part Number | Maximum Data Rate | Maximum Video Format | HDMI TX Outputs | Analog Outputs | Rovi Output | VSP | OSD | TTL Out |
|----------------------------|-------------------|--------------------------|-----------------|-----------------|-------------|-----|-----|---------|
| ADV8003KBCZ-8 ¹ | 3 Gbps | 4k × 2k at 30 Hz (8-bit) | 2 | Six 12-bit DACs | Yes | Yes | Yes | Yes |
| ADV8003KBCZ-8B | 3 Gbps | 4k × 2k at 30 Hz (8-bit) | 1 | No | No | Yes | Yes | No |
| ADV8003KBCZ-8C | 3 Gbps | 4k × 2k at 30 Hz (8-bit) | 2 | No | No | Yes | Yes | No |
| ADV8003KBCZ-7 ¹ | 2.25 Gbps | UXGA (162 MHz) | 2 | Six 12-bit DACs | Yes | Yes | Yes | Yes |
| ADV8003KBCZ-7B | 2.25 Gbps | UXGA (162 MHz) | 1 | No | No | Yes | Yes | No |
| ADV8003KBCZ-7C | 2.25 Gbps | UXGA (162 MHz) | 2 | No | No | Yes | Yes | No |
| ADV8003KBCZ-7T | 2.25 Gbps | UXGA (162 MHz) | 0 | No | No | Yes | Yes | Yes |

¹ Rovi enabled ICs require the buyer to be an approved licensee (authorized buyer) of ICs that are capable of outputting Rovi compliant video.

DETAILED FUNCTIONAL BLOCK DIAGRAM

800-99501

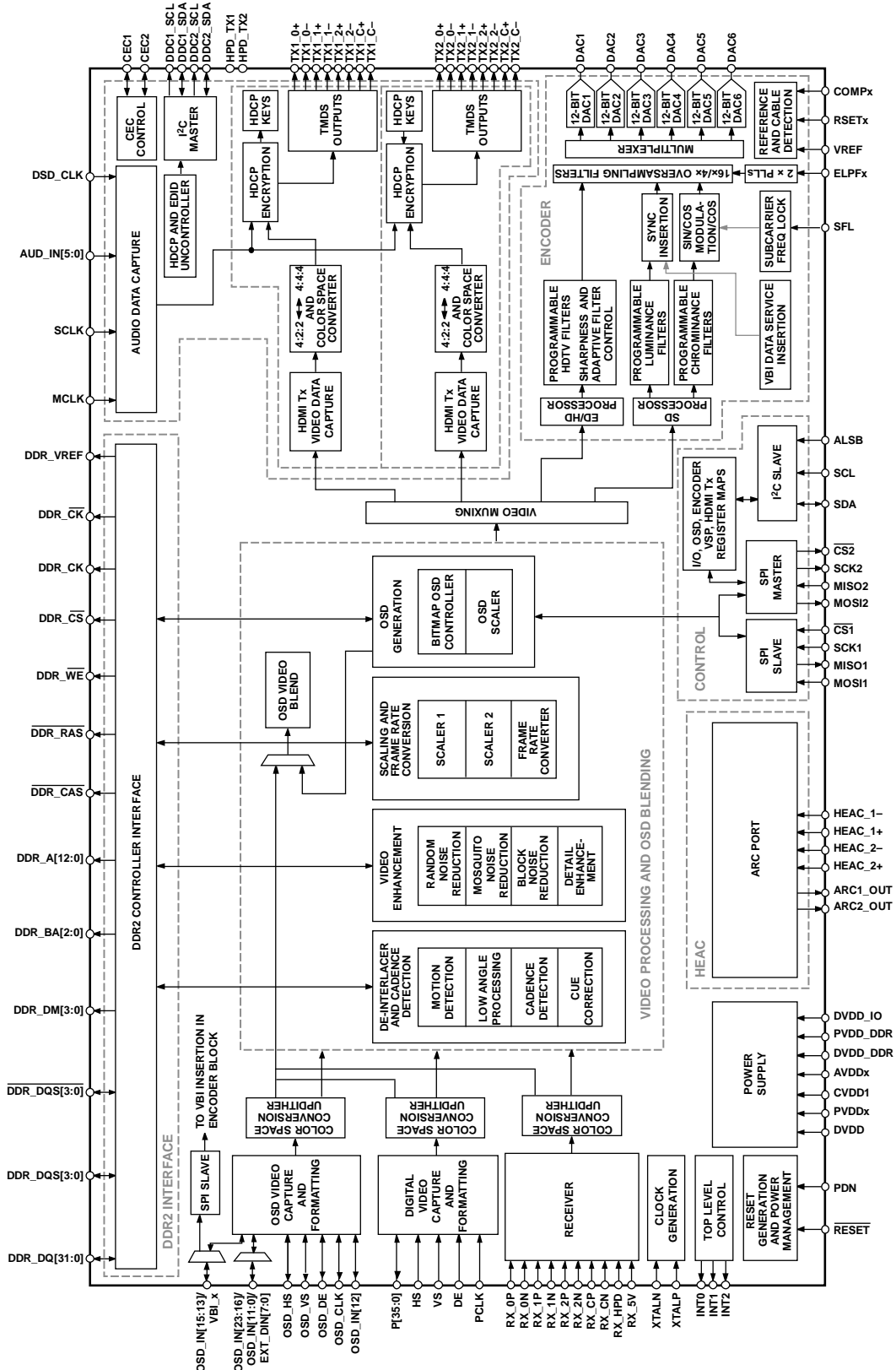


Figure 3. ADV8003KBCZ-8

SPECIFICATIONS

Measured at DVDD = 1.746 V to 1.854 V, DVDD_DDR = 1.746 V to 1.854 V, PVDD1 = 1.746 V to 1.854 V, PVDD2 = 1.746 V to 1.854 V, PVDD3 = 1.746 V to 1.854 V, PVDD5 = 1.746 V to 1.854 V, PVDD6 = 1.746 V to 1.854 V, PVDD_DDR = 1.746 V to 1.854 V, AVDD3 = 1.746 V to 1.854 V, CVDD1 = 1.746 V to 1.854 V, AVDD1 = 3.20 V to 3.40 V, AVDD2 = 3.20 V to 3.40 V, DVDD_IO = 3.20 V to 3.40 V, T_{MIN} to T_{MAX} = 0°C to 70°C, unless otherwise noted.

ELECTRICAL CHARACTERISTICS

Table 2.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|--------------------|---|------------------|--------|-------------------|----------------|
| STATIC PERFORMANCE | | | | | | |
| Resolution (Each DAC) | N | | | 12 | | Bits |
| Integral Nonlinearity, +ve ¹ | INL | DAC outputs sampled at 500 kHz | | 0.389 | | LSB |
| Integral Nonlinearity, -ve ¹ | INL | DAC outputs sampled at 500 kHz | | -0.322 | | LSB |
| Differential Nonlinearity, +ve ² | DNL | DAC outputs sampled at 500 kHz | | 0.183 | | LSB |
| Differential Nonlinearity, -ve ² | DNL | DAC outputs sampled at 500 kHz | | -0.208 | | LSB |
| DIGITAL INPUTS | | | | | | |
| Input High Voltage | V _{IH} | | 0.7 × DVDD_IO | | | V |
| Input Low Voltage | V _{IL} | | | | 0.3 × DVDD_IO | V |
| Input Leakage Current | I _{IN} | HEAC inputs DDR_DQS inputs Other digital inputs | | | ±60 ±60 ±10 | μA μA μA |
| Input Capacitance | C _{IN} | | | 13 | | pF |
| DIGITAL INPUTS (5 V TOLERANT) | | | | | | |
| Input High Voltage | V _{IH} | | 3.4 | | | V |
| Input Low Voltage | V _{IL} | | | | 0.8 | V |
| Input Leakage Current | I _{IN} | | | | ±60 | μA |
| DIGITAL OUTPUTS | | | | | | |
| Output High Voltage | V _{OH} | | 2.4 | | | V |
| Output Low Voltage | V _{OL} | | | | 0.4 | V |
| High Impedance Leakage Current | I _{LEAK} | | | | ±10 | μA |
| Output Capacitance | C _{OUT} | | | 13 | | pF |
| POWER REQUIREMENTS ^{3, 4, 5} | | | | | | |
| Digital Power Supply | DVDD | | 1.746 | 1.8 | 1.854 | V |
| PLL Analog Supply | PVDD1 | | 1.746 | 1.8 | 1.854 | V |
| PLL Digital Supply | PVDD2 | | 1.746 | 1.8 | 1.854 | V |
| Encoder PLL Supply | PVDD3 | | 1.746 | 1.8 | 1.854 | V |
| HDMI Tx1 PLL Power Supply | PVDD5 | | 1.746 | 1.8 | 1.854 | V |
| HDMI Tx2 PLL Power Supply | PVDD6 | | 1.746 | 1.8 | 1.854 | V |
| HDMI Analog Power Supply | AVDD3 | | 1.746 | 1.8 | 1.854 | V |
| Comparator Power Supply | CVDD1 | | 1.746 | 1.8 | 1.854 | V |
| HDMI Rx Inputs Analog Supply | AVDD1 | | 3.20 | 3.3 | 3.40 | V |
| Encoder Analog Power Supply | AVDD2 | | 3.20 | 3.3 | 3.40 | V |
| Digital Interface Supply | DVDD_IO | | 3.20 | 3.3 | 3.40 | V |
| Digital Power Supply Current, Including DVDD_DDR and PVDD_DDR | I _{DVDD} | Mode 1 | | 1989.0 | | mA |
| | | Mode 2 | | 1423.0 | | mA |
| | | Power-down mode | | 60.6 | | mA |
| PLL Analog Supply Current | I _{PVDD1} | Mode 1 | | 23.0 | | mA |
| | | Mode 2 | | 21.0 | | mA |
| | | Power-down mode | | 1.3 | | mA |
| PLL Digital Supply Current | I _{PVDD2} | Mode 1 | | 21.8 | | mA |
| | | Mode 2 | | 19.9 | | mA |
| | | Power-down mode | | 0.2 | | mA |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--------------------------------------|----------|--------------------------|-----|------|-----|------|
| Encoder PLL Supply Current | IPVDD3 | Mode 1 | | 8.9 | | mA |
| | | Mode 2 | | 3.8 | | mA |
| | | Power-down mode | | 0.0 | | mA |
| HDMI Tx1 PLL Supply Current | IPVDD5 | Mode 1 | | 62.2 | | mA |
| | | Mode 2 | | 49.3 | | mA |
| | | Power-down mode | | 1.8 | | mA |
| HDMI Tx2 PLL Supply Current | IPVDD6 | Mode 1 | | 62.5 | | mA |
| | | Mode 2 | | 2.1 | | mA |
| | | Power-down mode | | 1.6 | | mA |
| HDMI Analog Power Supply Current | IAVDD3 | Mode 1 | | 52.9 | | mA |
| | | Mode 2 | | 19.7 | | mA |
| | | Power-down mode | | 3.6 | | mA |
| Comparator Power Supply Current | ICVDD1 | Mode 1 | | 76.1 | | mA |
| | | Mode 2 | | 69.6 | | mA |
| | | Power-down mode | | 1.1 | | mA |
| HDMI Rx Inputs Analog Supply Current | IAVDD1 | Mode 1 | | 62.3 | | mA |
| | | Mode 2 | | 56.8 | | mA |
| | | Power-down mode | | 6.3 | | mA |
| Encoder Analog Power Supply | IAVDD2 | Mode 1 | | 36.2 | | mA |
| | | Mode 2 | | 9.2 | | mA |
| | | Power-down mode | | 1.9 | | mA |
| Digital Interface Supply Current | IDVDD_IO | Mode 1 | | 1.14 | | mA |
| | | Mode 2 | | 1.93 | | mA |
| | | Power-down mode | | 0.1 | | mA |

¹ Integral nonlinearity (INL) measures the deviation of the actual DAC transfer function from the ideal. For +ve INL, the actual line lies above the ideal line value. For -ve INL, the actual line lies below the ideal line value.

² Differential nonlinearity (DNL) measures the deviation of the actual DAC output voltage step from the ideal. For +ve DNL, the actual step value lies above the ideal step value. For -ve DNL, the actual step value lies below the ideal step value.

³ Mode 1 involves a 1080i60 input to the ADV8003 receiver and a 720p60 input to the ADV8003 TTL external OSD input. Both inputs are run through the front-end color space converters. The 1080i60 video stream is de-interlaced and upsampled to 4k × 2k at 24 Hz. The 720p video stream is input to the OSD block and is blended onto the 4k × 2k at 24 Hz video stream using the OSD block scaler. Both HDMI transmitters are then driven using the 4k × 2k at 24 Hz output.

⁴ Mode 2 involves a 1080i60 input to the ADV8003 receiver. This input is run through the front-end color space converter. The 1080i60 video stream is de-interlaced and is output to HDMI Transmitter 1. The secondary VSP is used to convert the 1080p video stream to 480i and is output using the SD encoder.

⁵ In the power-down mode, the ARC and the internal clock tree are kept active.

ANALOG SPECIFICATIONS

Table 3.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---------------------------------------|---|------|-----|-----|------|
| Low Drive Output Current (Full Scale) | $R_{SET} = 4.12 \text{ k}\Omega$, $R_L = 300 \Omega$ | 3.95 | 4.3 | 4.5 | mA |
| DAC-to-DAC Matching | DAC1 to DAC6 | | 0.9 | | % |
| Output Compliance, V_{OC} | | 0 | | 1.4 | V |
| Output Capacitance, C_{OUT} | DAC1, DAC2, DAC3 | | 9 | | pF |
| | DAC4, DAC5, DAC6 | | 9 | | pF |
| DAC Analog Output Skew | DAC1 to DAC6 | | 0.2 | | ns |

DATA AND I²C TIMING CHARACTERISTICSFor input timing measurements, V_{IH} = DVDD_IO and V_{IL} = GND.

Table 4.

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|-----------------------------------|--|----------------------|-----|----------------------|--------------|
| TMDS CLOCK | | | | | | |
| TMDS Input Clock Frequency | | ADV8003KBCZ-8, ADV8003KBCZ-8B, ADV8003KBCZ-8C | 25 | | 297 | MHz |
| | | ADV8003KBCZ-7, ADV8003KBCZ-7B, ADV8003KBCZ-7C, ADV8003KBCZ-7T | 25 | | 225 | MHz |
| TMDS Output Clock Frequency | | ADV8003KBCZ-8, ADV8003KBCZ-8B, ADV8003KBCZ-8C | 25 | | 297 | MHz |
| | | ADV8003KBCZ-7, ADV8003KBCZ-7B, ADV8003KBCZ-7C, ADV8003KBCZ-7T | 25 | | 225 | MHz |
| CLOCK AND CRYSTAL | | | | | | |
| Crystal Frequency, XTAL | | | | 27 | | MHz |
| Crystal Frequency Stability | | | | | ±50 | ppm |
| Primary Video Input Clock Frequency Range | | | 13.5 | | 162 | MHz |
| Secondary Video Input Clock Frequency Range | | | 13.5 | | 162 | MHz |
| Video Output Clock Frequency Range | | | 13.5 | | 162 | MHz |
| Serial Port 1 SCK Frequency (SCK1) | | | | | 50 | MHz |
| Serial Port 2 SCK Frequency (SCK2) | | | 11.5 | | 81 | MHz |
| Serial Port 3 SCK Frequency (VBI_SCK) | | | | | 27 | MHz |
| Audio SCLK Frequency | | | | | 49.152 | MHz |
| Audio MCLK Frequency | | | | | 98.304 | MHz |
| Audio DSD Clock Frequency | | | | | 5.6448 | MHz |
| FAST I ² C PORTS ¹ | | | | | | |
| SCL Frequency | | | | | 400 | kHz |
| SCL Minimum Pulse Width High | t ₁ | | 600 | | | ns |
| SCL Minimum Pulse Width Low | t ₂ | | 1.3 | | | μs |
| Start Condition Hold Time | t ₃ | | 600 | | | ns |
| Start Condition Setup Time | t ₄ | | 600 | | | ns |
| SDA Setup Time | t ₅ | | 100 | | | ns |
| SCL and SDA Rise Time | t ₆ | | | | 300 | ns |
| SCL and SDA Fall Time | t ₇ | | | | 300 | ns |
| Stop Condition Setup Time | t ₈ | | 0.6 | | | μs |
| SERIAL PORT ^{2,3} | | | | | | |
| Master Serial Port (Serial Port 2) | | | | | | |
| $\overline{\text{CS}}_2$ Falling Edge to SCK2 Rising/Falling Edge | t ₉ , t ₁₀ | t ₉ , t ₁₀ , depending on the values of CPHA and CPOL | 1 × SCK2 periods | | 1.5 × SCLK2 periods | ns |
| SCK2 Rising/Falling Edge to $\overline{\text{CS}}_2$ Rising Edge | t ₁₁ , t ₁₂ | t ₁₁ , t ₁₂ , depending on the values of CPHA and CPOL | 1 × SCK2 periods | | 1.5 × SCLK2 periods | ns |
| $\overline{\text{CS}}_2$ Pulse Width | t ₁₃ | | 1880 | | 1900 | ns |
| SCK2 High Time | t ₁₄ | | 0.45 × SCLK2 periods | | 0.55 × SCLK2 periods | % duty cycle |
| SCK2 Low Time | | | 0.45 × SCLK2 periods | | 0.55 × SCLK2 periods | % duty cycle |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|-----------------------------------|--|------------------------|---------------------|------------------------|--------------|
| MOSI2 Start of Data Invalid to SCK2 Falling Edge | t ₁₅ | SPI Mode 0, SPI Mode 3 | | | 1.15 | ns |
| $\overline{\text{CS}}2$ Start of Data Invalid to SCK2 Falling Edge | t ₁₅ | SPI Mode 0, SPI Mode 3 | | | 0.81 | ns |
| SCK2 Falling Edge to MOSI2 End of Data Invalid | t ₁₆ | SPI Mode 0, SPI Mode 3 | | | 1.85 | ns |
| SCK2 Falling Edge to $\overline{\text{CS}}2$ End of Data Invalid | t ₁₆ | SPI Mode 0, SPI Mode 3 | | | 2.14 | ns |
| MISO2 Setup Time | t ₁₇ | Valid regardless of the SCK2 active edge used | 14.57 | | | ns |
| MISO2 Hold Time | t ₁₈ | Valid regardless of the SCK2 active edge used | 0.0 | | | ns |
| MOSI2 Start of Data Invalid to SCK2 Rising Edge | t ₁₉ | SPI Mode 1, SPI Mode 2 | | | 1.59 | ns |
| $\overline{\text{CS}}2$ Start of Data Invalid to SCK2 Rising Edge | t ₁₉ | SPI Mode 1, SPI Mode 2 | | | 1.24 | ns |
| SCK2 Rising Edge to MOSI2 End of Data Invalid | t ₂₀ | SPI Mode 1, SPI Mode 2 | | | 1.39 | ns |
| SCK2 Rising Edge to $\overline{\text{CS}}2$ End of Data Invalid | t ₂₀ | SPI Mode 1, SPI Mode 2 | | | 1.68 | ns |
| MISO2 Setup Time | t ₂₁ | Valid regardless of the SCK2 active edge used | 14.57 | | | ns |
| MISO2 Hold Time | t ₂₂ | Valid regardless of the SCK2 active edge used | 0.0 | | | ns |
| Slave Mode (Serial Port 1) | | | | | | |
| $\overline{\text{CS}}1$ Falling Edge to SCK1 Rising/Falling Edge | t ₂₃ , t ₂₄ | t ₂₃ , t ₂₄ , depending on the values of CPHA and CPOL | | | 50.0 | ns |
| SCK1 Rising/Falling Edge to $\overline{\text{CS}}1$ Rising Edge | t ₂₅ , t ₂₆ | t ₂₅ , t ₂₆ , depending on the values of CPHA and CPOL | | | 50.0 | ns |
| $\overline{\text{CS}}1$ Pulse Width | t ₂₇ | | | 5 × SCK1 periods | | ns |
| SCK1 High Time | t ₃₀ | | 0.45 × SCK1 periods | | 0.55 × SCK1 periods | % duty cycle |
| SCK1 Low Time | | | 0.45 × SCK1 periods | | 0.55 × SCK1 periods | % duty cycle |
| MOSI1 Setup Time | t ₃₁ | SPI Mode 0, SPI Mode 3 | 0.15 | | | ns |
| MOSI1 Hold Time | t ₃₂ | SPI Mode 0, SPI Mode 3 | 1.4 | | | ns |
| SCK1 Falling Edge to MISO1 Start of Data Invalid | t ₃₃ | SPI Mode 0, SPI Mode 3 | | | 5.89 | ns |
| SCK1 Falling Edge to MISO1 End of Data Invalid | t ₃₄ | SPI Mode 0, SPI Mode 3 | | | 12.08 | ns |
| MOSI1 Setup Time | t ₃₅ | SPI Mode 1, SPI Mode 2 | 0 | | | ns |
| MOSI1 Hold Time | t ₃₆ | SPI Mode 1, SPI Mode 2 | 1.96 | | | ns |
| SCK1 Rising Edge to MISO1 Start of Data Invalid | t ₃₇ | SPI Mode 1, SPI Mode 2 | | | 5.79 | ns |
| SCK1 Rising Edge to MISO1 End of Data Invalid | t ₃₈ | SPI Mode 1, SPI Mode 2 | | | 11.97 | ns |
| Slave Mode (Serial Port 3) | | | | | | |
| VBI_SCK High Time | t ₃₉ | | 0.45 × VBI_SCK periods | | 0.55 × VBI_SCK periods | % duty cycle |
| VBI_SCK Low Time | | | 0.45 × VBI_SCK periods | | 0.55 × VBI_SCK periods | % duty cycle |
| VBI_ $\overline{\text{CS}}$ Pulse Width | | | | 5 × VBI_SCK periods | | ns |
| VBI_ $\overline{\text{CS}}$, VBI_MOSI Setup Time | t ₄₀ | SPI Mode 0 only | 0.93 | | | ns |
| VBI_ $\overline{\text{CS}}$, VBI_MOSI Hold Time | t ₄₁ | SPI Mode 0 only | 0.75 | | | ns |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|-----------------|---------------------------|-----------------------|-----|-----------------------|--------------|
| SPI Pass-Through Mode | | | | | | |
| Data Transition on SCK1 to Start of Data Invalid on SCK2 | t ₄₂ | | | | 5.17 | ns |
| Data Transition on SCK1 to End of Data Invalid on SCK2 | t ₄₃ | | | | 10.20 | ns |
| Data Transition on MOSI1 to Start of Data Invalid on MOSI2 | t ₄₂ | | | | 4.90 | ns |
| Data Transition on MOSI1 to End of Data Invalid on MOSI2 | t ₄₃ | | | | 10.85 | ns |
| Data Transition on MISO2 to Start of Data Invalid on MISO1 | t ₄₂ | | | | 5.29 | ns |
| Data Transition on MISO2 to End of Data Invalid on MISO1 | t ₄₃ | | | | 11.97 | ns |
| Data Transition on $\overline{CS1}$ to Start of Data Invalid on $\overline{CS2}$ | t ₄₂ | | | | 4.61 | ns |
| Data Transition on $\overline{CS1}$ to End of Data Invalid on $\overline{CS2}$ | t ₄₃ | | | | 8.78 | ns |
| RESET FUNCTION | | | | | | |
| Reset Pulse Width | | | 5 | | | ms |
| VIDEO DATA AND CONTROL INPUTS ³ | | | | | | |
| PCLK High Time | t ₄₄ | | 0.45 × PCLK period | | 0.55 × PCLK period | % duty cycle |
| PCLK Low Time | | | 0.45 × PCLK period | | 0.55 × PCLK period | % duty cycle |
| OSD_CLK High Time | t ₅₁ | | 0.45 × OSD_CLK period | | 0.55 × OSD_CLK period | % duty cycle |
| OSD_CLK Low Time | | | 0.45 × OSD_CLK period | | 0.55 × OSD_CLK period | % duty cycle |
| Main Video Input, SDR and DDR Mode Setup Time (Data Latched on Rising Edge) | t ₄₅ | | 1.42 | | | ns |
| Main Video Input, SDR and DDR Modes Hold Time (Data Latched on Rising Edge) | t ₄₆ | | 0.95 | | | ns |
| Main Video Input, DDR Mode Setup Time (Data Latched on Falling Edge) | t ₄₇ | | 0.72 | | | ns |
| Main Video Input, DDR Mode Hold Time (Data Latched on Falling Edge) | t ₄₈ | | 1.49 | | | ns |
| Interleaved Video Input, SDR Setup Time (Data Latched on Rising Edge) | t ₄₉ | Used for 300 MHz TTL data | 1.42 | | | ns |
| Interleaved Video Input, SDR Hold Time (Data Latched on Rising Edge) | t ₅₀ | Used for 300 MHz TTL data | 0.95 | | | ns |
| External OSD Input, SDR and DDR Mode Setup Time (Data Latched on Rising Edge) | t ₅₂ | | 1.33 | | | ns |
| External OSD Input, SDR and DDR Mode Hold Time (Data Latched on Rising Edge) | t ₅₃ | | 0.94 | | | ns |
| External OSD Input, DDR Mode Setup Time (Data Latched on Rising Edge) | t ₅₄ | | 0.57 | | | ns |
| External OSD Input, DDR Mode Hold Time (Data Latched on Rising Edge) | t ₅₅ | | 1.51 | | | ns |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|--|-----------------|--------------------------|------------------------|-----|-----------------------|--------------|
| VIDEO DATA AND CONTROL OUTPUTS³ | | | | | | |
| OSD_CLK High Time | t ₅₆ | | 0.40 × OSD_CLK period | | 0.60 × OSD_CLK period | % duty cycle |
| OSD_CLK Low Time | | | 0.40 × OSD_CLK period | | 0.60 × OSD_CLK period | % duty cycle |
| OSD_CLK Active Edge to Data and Control Start of Data Invalid (Data Latched on Falling Edge) | t ₅₇ | | | | 0.07 | ns |
| OSD_CLK Active Edge to Data and Control End of Data Invalid (Data Latched on Falling Edge) | t ₅₈ | | | | 1.56 | ns |
| OSD_CLK Active Edge to Data and Control Start of Data Invalid (Data Latched on Rising Edge) | t ₅₉ | | | | 0.41 | ns |
| OSD_CLK Active Edge to Data and Control End of Data Invalid (Data Latched on Rising Edge) | t ₆₀ | | | | 0.93 | ns |
| S/PDIF INPUT³ | | | | | | |
| MCLK High Time | t ₆₁ | | 0.45 × MCLK periods | | 0.55 × MCLK periods | % duty cycle |
| MCLK Low Time | | | 0.45 × MCLK periods | | 0.55 × MCLK periods | % duty cycle |
| S/PDIF Data Setup Time | t ₆₂ | | 0.12 | | | ns |
| S/PDIF Data Hold Time | t ₆₃ | | 1.89 | | | ns |
| I²S PORT, SLAVE MODE³ | | | | | | |
| SCLK High Time | t ₆₄ | | 0.45 × SCLK periods | | 0.55 × SCLK periods | % duty cycle |
| SCLK Low Time | | | 0.45 × SCLK periods | | 0.55 × SCLK periods | % duty cycle |
| I ² S Data Setup Time | t ₆₅ | | 0.42 | | | ns |
| I ² S Data Hold Time | t ₆₆ | | 1.38 | | | ns |
| DSD PORT³ | | | | | | |
| DSD Clock High Time | t ₆₇ | | 0.45 × DSD CLK periods | | 0.55 × DSDCLK periods | % duty cycle |
| DSD Clock Low Time | | | 0.45 × SCLK periods | | 0.55 × SCLK periods | % duty cycle |
| DSD Data Setup Time | t ₆₈ | | 0.48 | | | ns |
| DSD Data Hold Time | t ₆₉ | | 1.79 | | | ns |

¹ It is possible to run I²C at faster speeds; however, it has been characterized to run only in fast mode.
² All serial port measurements are for the default polarity and phase settings (clock low in idle state and negative edge used).
³ All measurements are guaranteed by design only.

Timing Diagrams

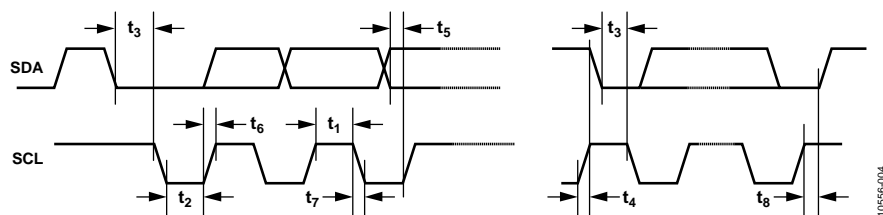


Figure 4. I²C Timing
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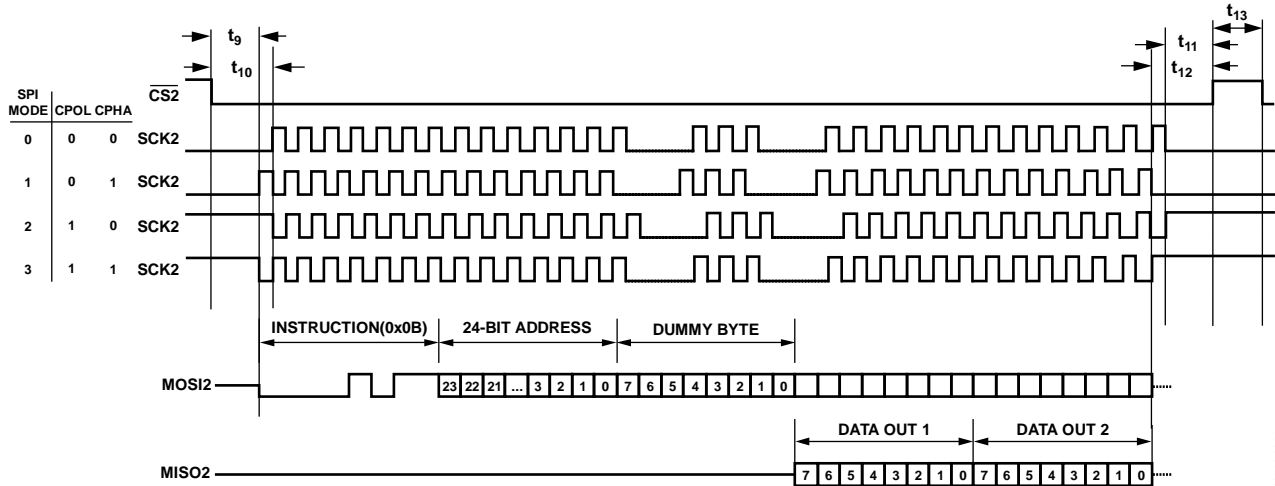


Figure 5. Detailed SPI Master Timing Diagram (Serial Port 2)

10556-005

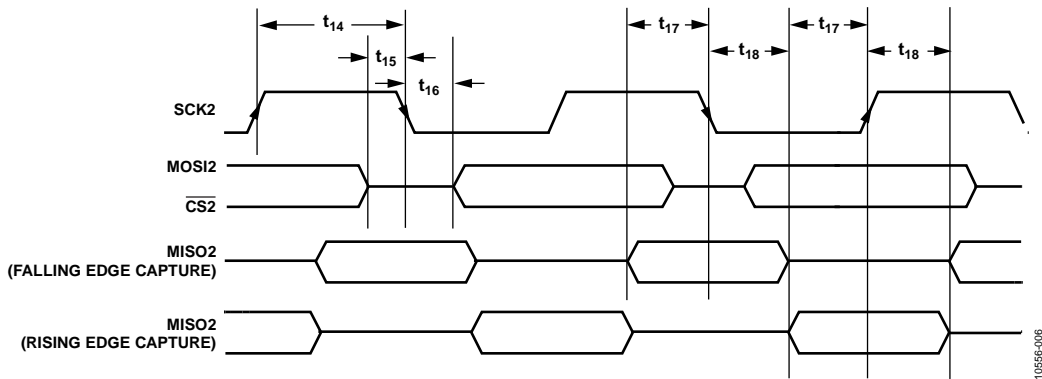


Figure 6. Serial Port 2 Master Mode Timing (SPI Mode 0 and SPI Mode 3)

10556-006

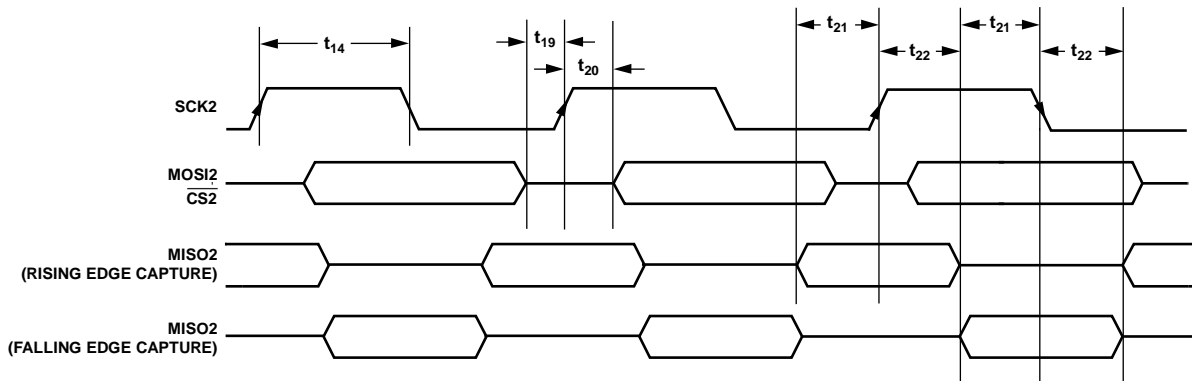


Figure 7. Serial Port 2 Master Mode Timing (SPI Mode 1 and SPI Mode 2)

10556-007

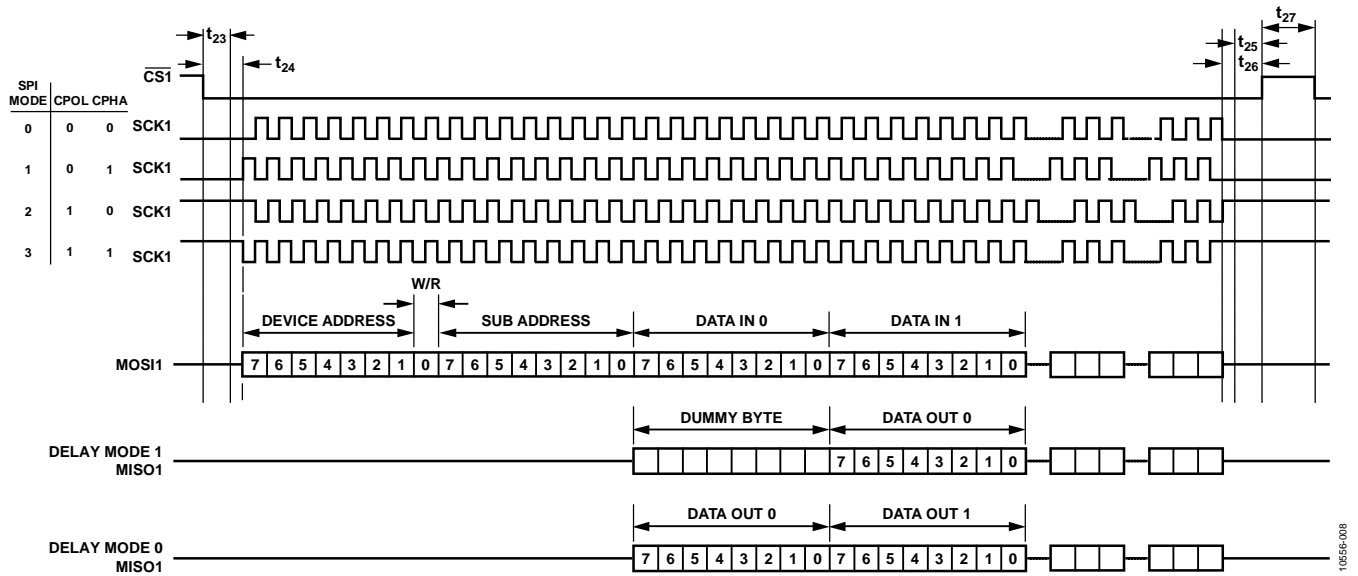


Figure 8. Detailed SPI Slave Timing Diagram (Serial Port 1)

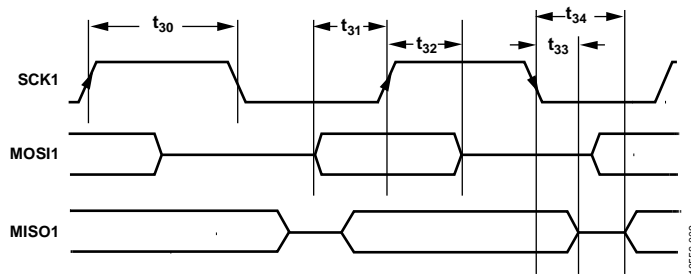


Figure 9. Serial Port 1 Slave Mode Timing (SPI Mode 0 and SPI Mode 3)

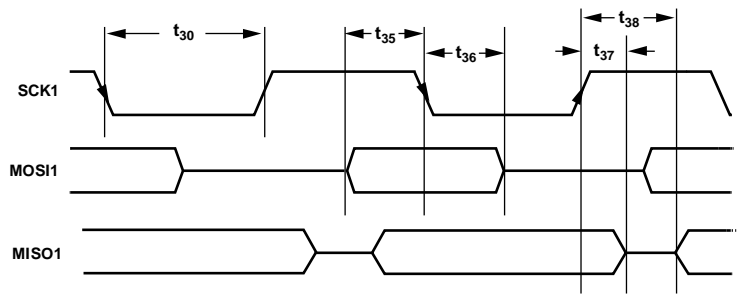


Figure 10. Serial Port 1 Slave Mode Timing (SPI Mode 1 and SPI Mode 2)

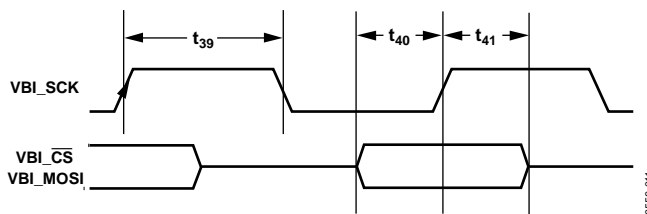


Figure 11. Serial Port 3 Slave Mode Timing (SPI Mode 0 Only)

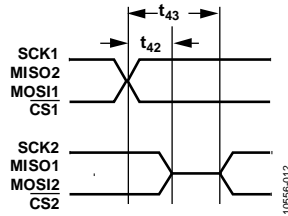


Figure 12. SPI Pass-Through Mode (Serial Port 1 and Serial Port 2)

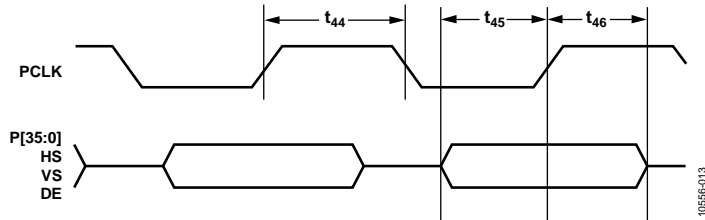


Figure 13. Main Video Input, Noninterleaved SDR Video Data and Control Timing

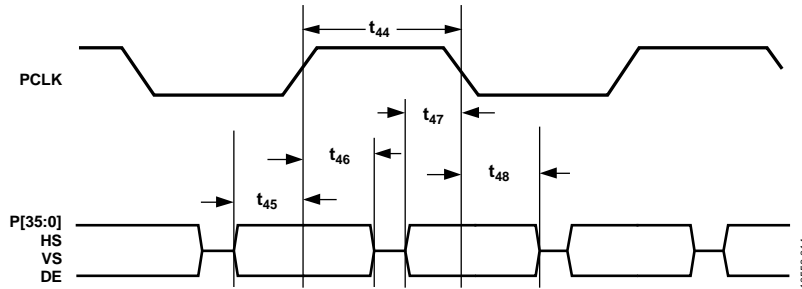


Figure 14. Main Video Input, Noninterleaved DDR Video Data and Control Timing

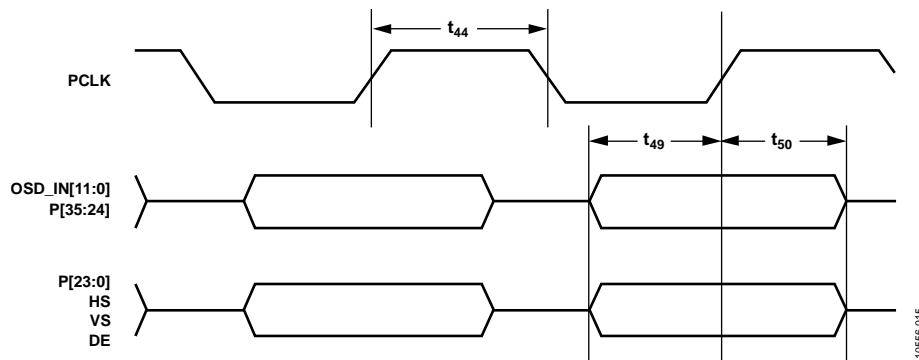


Figure 15. Interleaved SDR Video Data and Control Input Timing

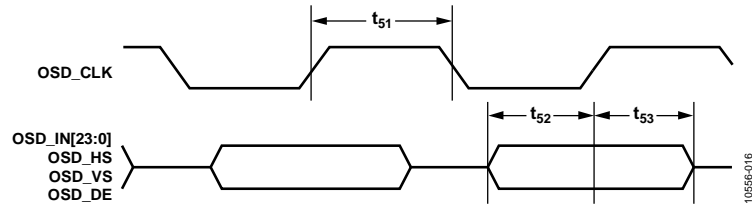


Figure 16. External OSD Input, Noninterleaved SDR Video Data and Control Timing

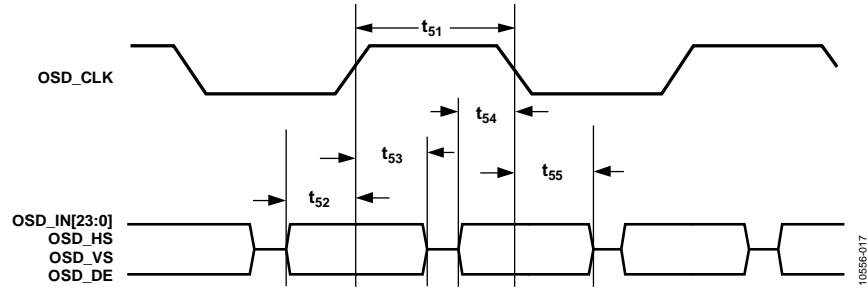


Figure 17. External OSD Input, Noninterleaved DDR Video Data and Control Timing

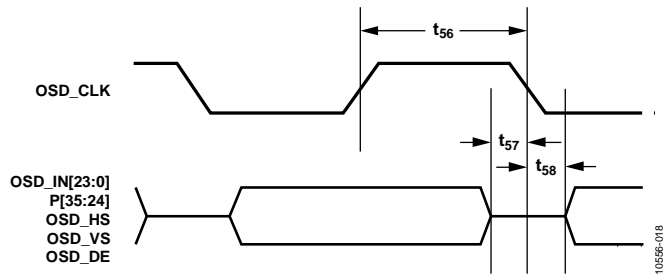


Figure 18. SDR Video Data and Control Output Timing (Data Launched on Falling Edge)

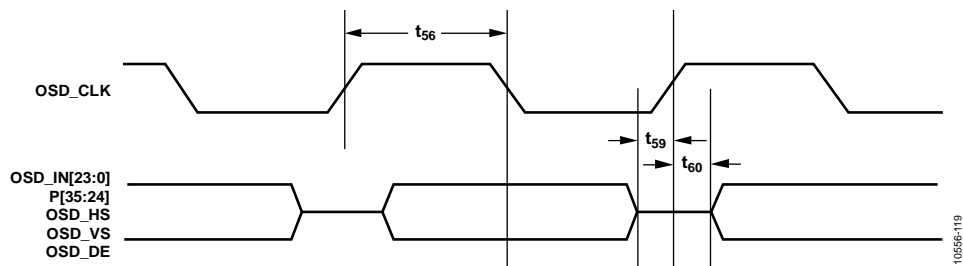


Figure 19. SDR Video Data and Control Output Timing (Data Launched on Rising Edge)

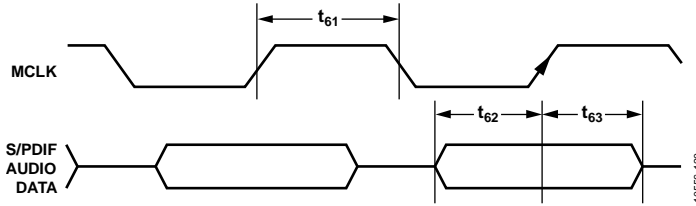


Figure 20. S/PDIF Input Timing, Data Latched on Rising Edge

10556-120

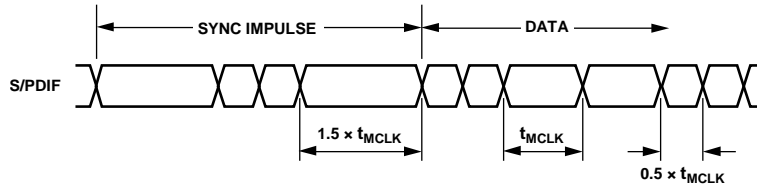


Figure 21. S/PDIF Data Timing

10556-020

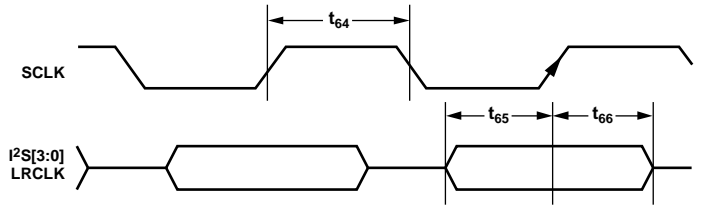


Figure 22. I²S Timing

10556-021

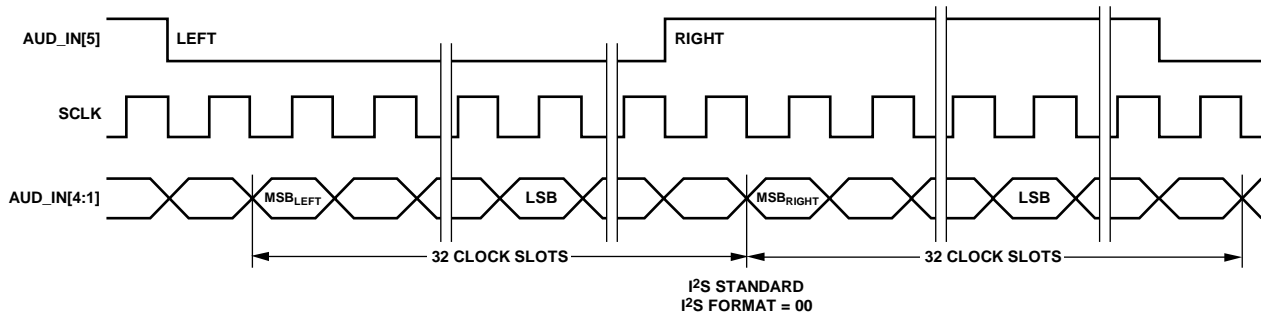


Figure 23. I²S Standard Audio—Data Width of 16 Bits to 24 Bits per Channel

10556-022

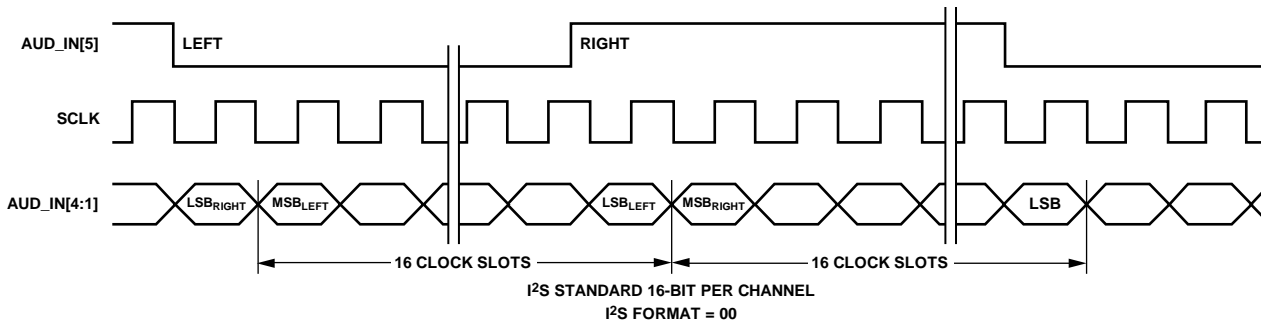


Figure 24. I²S Standard Audio—16-Bit Samples Only

10556-023

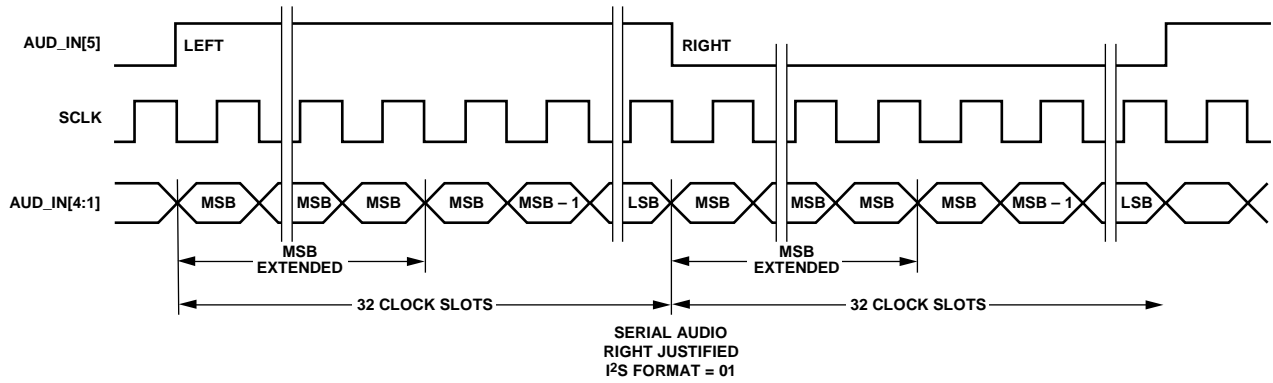


Figure 25. Serial Audio—Right-Justified

10556-024

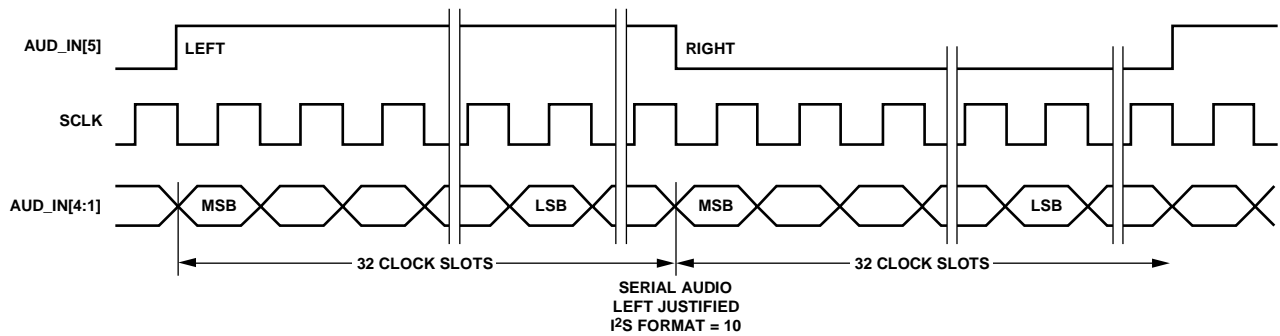


Figure 26. Serial Audio—Left-Justified

10556-125

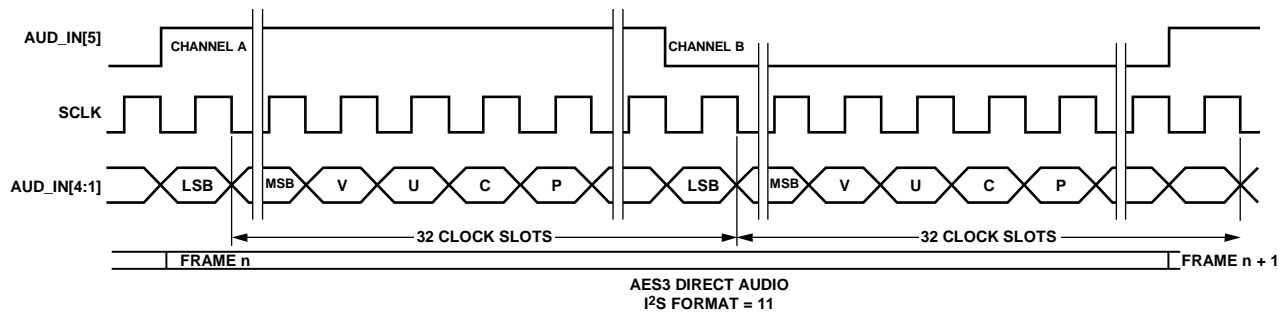


Figure 27. AES3 Direct Audio

10556-126

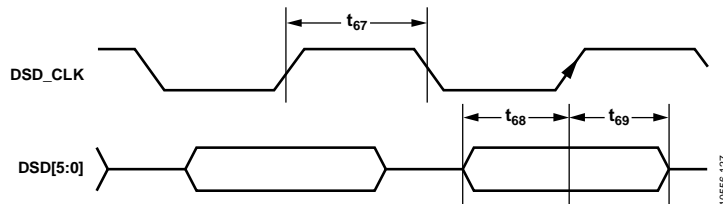


Figure 28. DSD Timing

10556-127

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|---|----------------------------|
| AVDD1, AVDD2, DVDD_IO to GND | 3.9 V |
| DVDD, PVDDx, CVDD1, AVDD3, DVDD_DDR, PVDD_DDR to GND | 2.2 V |
| DVDD to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| PVDD1 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| PVDD2 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| PVDD3 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| PVDD5 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| PVDD6 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| CVDD1 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| AVDD3 to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| DVDD_DDR to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| PVDD_DDR to Other 1.8 V Power Supplies ¹ | -0.3 V to +0.3 V |
| Digital Inputs to GND | -0.3 V to DVDD_IO + 0.3 V |
| Serial Video Inputs to GND | -0.3 V to CVDD1 + 0.3 V |
| DDR_IO and DDR_VREF to GND | -0.3 V to DVDD_DDR + 0.3 V |
| 5 V Tolerant Digital Inputs to GND ² | -0.3 V to +5.5 V |
| 1.8 V Analog Inputs to GND | -0.3 V to AVDD3 + 0.3 V |
| 3.3 V Analog Inputs to GND | -0.3 V to AVDD2 + 0.3 V |
| HDMI Digital Outputs to GND | -0.3 V to AVDD3 + 0.3 V |
| Digital Outputs Voltage to GND | -0.3 V to DVDD_IO + 0.3 V |
| Analog Outputs Voltage to GND ³ | -0.3 V to AVDD2 + 0.3 V |
| Maximum Junction Temperature (T _{J MAX}) | 125°C |
| Storage Temperature Range | -65°C to +150°C |
| Infrared Reflow Soldering (20 sec) | 260°C |

¹ 1.8 V power supplies include DVDD, PVDD1, PVDD2, PVDD3, PVDD5, PVDD6, CVDD1, AVDD3, DVDD_DDR, and PVDD_DR.

² The following inputs are 5 V tolerant: CEC1, CEC2, DDC1_SCL, DDC2_SCL, DDC1_SDA, DDC2_SDA, HEAC_1-, HEAC_1+, HEAC_2-, HEAC_2+, RX_5V, and RX_HPD.

³ Except the ELPF1 and ELPF2 outputs, which are kept to -0.3 V to PVDD3 + 0.3 V; the RTERM output, which is kept to -0.3 V to CVDD1 + 0.3 V; and the R_TX1 and R_TX2 outputs, which are kept to -0.3 V to PVDD5 + 0.3 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | | | |
|----|-----------------------|-----------------------|-----------------------|------------|------------|------------|------------|------------|-----------|----------|----------|-----------|-----------|-----------|---------|------------|------------|------------|------------|-----------|-----------|------------|-----------|---------|--------|---|
| A | OSD_IN[23]/EXT_DIN[7] | OSD_DE | OSD_CLK/EXT_CLK | AUD_IN[1] | AUD_IN[2] | AUD_IN[5] | ARC2_OUT | MOSI1 | SCK2 | CS2 | RESET | XTALN | PVDD2 | NC | NC | CVDD1 | RX_CN | RX_0N | RX_1N | RX_2N | CVDD1 | RSET1 | VREF | A | | |
| B | OSD_IN[21]/EXT_DIN[5] | OSD_IN[22]/EXT_DIN[6] | OSD_VS | AUD_IN[0] | AUD_IN[3] | SFL | ARC1_OUT | MISO1 | MOSI2 | MISO2 | ALSB | XTALP | PVDD1 | NC | NC | GND | RX_CP | RX_0P | RX_1P | RX_2P | GND | COMP1 | DAC4 | B | | |
| C | OSD_IN[19]/EXT_DIN[3] | OSD_IN[20]/EXT_DIN[4] | GND | AUD_IN[4] | DSD_CLK | SCLK | SCL | SCK1 | GND | INT0 | PDN | GND | GND | NC | NC | RX_HP | AVDD1 | GND | GND | AVDD1 | AVDD1 | DAC5 | DAC6 | C | | |
| D | OSD_IN[16]/EXT_DIN[0] | OSD_IN[17]/EXT_DIN[1] | OSD_IN[18]/EXT_DIN[2] | GND | DVDD_IO | MCLK | SDA | CS1 | GND | INT1 | INT2 | DVDD_IO | TEST1 | NC | NC | RX_5V | NC | NC | RTERM | AVDD2 | AVDD2 | DAC1 | DAC2 | D | | |
| E | OSD_IN[13]/VBI_SCK | OSD_IN[14]/VBI_MOSI | OSD_IN[15]/VBI_CS | DVDD_IO | | | | | | | | | | | | | | | | | TEST2 | GND | COMP2 | DAC3 | E | |
| F | OSD_IN[9] | OSD_IN[10] | OSD_IN[11] | OSD_IN[12] | | | | | | | | | | | | | | | | | | RSET2 | PVDD3 | GND | CEC1 | F |
| G | OSD_IN[5] | OSD_IN[6] | OSD_IN[7] | OSD_IN[8] | | GND | GND | GND | DVDD | GND | GND | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | ELPF1 | ELPF2 | GND | AVDD3 | G |
| H | OSD_IN[1] | OSD_IN[2] | OSD_IN[3] | OSD_IN[4] | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | TX1_2+ | TX1_2- | H |
| J | DE | HS | OSD_HS | OSD_IN[0] | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | DDC1_SDA | GND | TX1_1+ | TX1_1- | J | |
| K | VS | PCLK | DVDD_IO | DVDD_IO | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | DDC1_SCL | GND | TX1_0+ | TX1_0- | K | |
| L | P[32] | P[33] | P[34] | P[35] | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | HPD_TX1 | GND | TX1_C+ | TX1_C- | L | |
| M | P[28] | P[29] | P[30] | P[31] | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | R_TX1 | PVDD5 | HEAC_1+ | HEAC_1- | M | |
| N | P[24] | P[25] | P[26] | P[27] | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | CEC2 | PVDD5 | AVDD3 | NC | N | |
| P | P[20] | P[21] | P[22] | P[23] | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | DDC2_SCL | GND | TX2_2+ | TX2_2- | P | |
| R | P[16] | P[17] | P[18] | P[19] | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | DDC2_SDA | GND | TX2_1+ | TX2_1- | R | |
| T | P[14] | P[15] | GND | GND | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | HPD_TX2 | GND | TX2_0+ | TX2_0- | T | |
| U | P[10] | P[11] | P[12] | P[13] | | GND | GND | DVDD | GND | GND | DVDD | GND | GND | DVDD | GND | GND | GND | GND | GND | R_TX2 | GND | TX2_C+ | TX2_C- | U | | |
| V | P[6] | P[7] | P[8] | P[9] | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | PVDD6 | HEAC_2+ | HEAC_2- | V | |
| W | P[2] | P[3] | P[4] | P[5] | | | | | | | | | | | | | | | | | TEST3 | PVDD6 | AVDD3 | NC | W | |
| Y | P[0] | P[1] | DDR_DQS[2] | GND | DDR_DQ[23] | DVDD_DDR | DDR_DQS[3] | GND | DDR_A[11] | DVDD_DDR | DDR_A[4] | GND | DDR_CAS | DVDD_DDR | DDR_CK | GND | DDR_DQ[9] | DVDD_DDR | DDR_DQ[14] | GND | DDR_DQ[6] | PVDD_DDR | GND | Y | | |
| AA | DDR_DQ[18] | GND | GND | DDR_DQS[2] | DDR_DQ[26] | DVDD_DDR | DDR_DQS[3] | NC/GND | DDR_A[8] | DVDD_DDR | DDR_A[2] | GND | DDR_CS | DVDD_DDR | DDR_CK | GND | DDR_DQ[11] | DVDD_DDR | DDR_DM[1] | DDR_DM[0] | GND | GND | DDR_DQ[3] | AA | | |
| AB | DDR_DQ[21] | DDR_DQ[19] | DDR_DQ[17] | DDR_DM[2] | DDR_DQ[30] | DDR_DM[3] | DDR_DQ[31] | DDR_DQ[29] | DDR_A[12] | DDR_A[6] | DDR_A[3] | DDR_A[0] | DDR_BA[0] | DDR_RAS | DDR_CKE | DDR_DQ[12] | DDR_DQS[1] | DDR_DQ[8] | DDR_DQ[13] | DDR_DQ[0] | DDR_DQ[5] | DDR_DQS[0] | DDR_DQ[4] | AB | | |
| AC | DDR_DQ[16] | DDR_DQ[20] | DDR_DQ[22] | DDR_DQ[25] | DDR_DQ[28] | DDR_DQ[27] | DDR_DQ[24] | DDR_A[9] | DDR_A[5] | DDR_A[7] | DDR_A[1] | DDR_A[10] | DDR_BA[1] | DDR_BA[2] | DDR_WE | DDR_VREF | DDR_DQ[10] | DDR_DQS[1] | DDR_DQ[15] | DDR_DQ[7] | DDR_DQ[2] | DDR_DQS[0] | DDR_DQ[1] | AC | | |

Figure 29. ADV8003KBCZ-8 and ADV8003KBCZ-7 Pin Configuration

Table 6. ADV8003KBCZ-8 and ADV8003KBCZ-7 Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------|---------------------------|---|--|
| A1 | OSD_IN[23]/EXT_DIN[7] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[23])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[7]). |
| A2 | OSD_DE | OSD video sync | Data Enable for the OSD Input Port. |
| A3 | OSD_CLK/EXT_CLK | OSD video sync | Pixel Clock for the OSD Input Port (OSD_CLK)/Pixel Clock for External Video Data (EXT_CLK). |
| A4 | AUD_IN[1] | Audio input | I ² S0/DSD1 Audio Input. |
| A5 | AUD_IN[2] | Audio input | I ² S1/DSD2 Audio Input. |
| A6 | AUD_IN[5] | Audio input | LRCLK/DSD5 Audio Input. |
| A7 | ARC2_OUT | Audio output | Audio Return Channel for HDMI Tx2. |
| A8 | MOSI1 | Serial port control | Master Out Slave In (Serial Port 1). Serial Port 1 is used for OSD control. |
| A9 | SCK2 | Serial port control | Serial Clock (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A10 | $\overline{\text{CS2}}$ | Serial port control | Chip Select (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A11 | $\overline{\text{RESET}}$ | Miscellaneous digital | Reset Pin. |
| A12 | XTALN | Miscellaneous digital ¹ | Crystal Input. |
| A13 | PVDD2 | Power | PLL Digital Supply Voltage (1.8 V). |
| A14 | NC | N/A | No Connect. Do not connect to this pin. |
| A15 | NC | N/A | No Connect. Do not connect to this pin. |
| A16 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A17 | RX_CN | Rx input | Rx Clock Complement Input. |
| A18 | RX_ON | Rx input | Rx Channel 0 Complement Input. |
| A19 | RX_1N | Rx input | Rx Channel 1 Complement Input. |
| A20 | RX_2N | Rx input | Rx Channel 2 Complement Input. |
| A21 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A22 | RSET1 | Miscellaneous analog ¹ | Resistor Current Setting for Encoder DACs: DAC1, DAC2, and DAC3. Place the RSET1 resistor as close as possible to the ADV8003. |
| A23 | VREF | Miscellaneous analog ¹ | Optional External Voltage Reference Input for DACs or Voltage Reference Output. Place VREF voltage components as close as possible to the ADV8003. |
| B1 | OSD_IN[21]/EXT_DIN[5] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[21])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[5]). |
| B2 | OSD_IN[22]/EXT_DIN[6] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[22])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[6]). |
| B3 | OSD_VS | OSD video sync | Vertical Sync for the OSD Input Port. |
| B4 | AUD_IN[0] | Audio input | S/PDIF/DSD0 Audio Input. |
| B5 | AUD_IN[3] | Audio input | I ² S2/DSD3 Audio Input. |
| B6 | SFL | SFL | Subcarrier Frequency Lock Signal (SFL). |
| B7 | ARC1_OUT | Audio output | Audio Return Channel for HDMI Tx1. |
| B8 | MISO1 | Serial port control | Master In Slave Out (Serial Port 1). Serial Port 1 is used for OSD control. |
| B9 | MOSI2 | Serial port control | Master Out Slave In (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B10 | MISO2 | Serial port control | Master In Slave Out (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B11 | ALSB | I ² C control | Sets LSB of I ² C address. When the ALSB pin is set low, the I ² C address is 0x18; when the ALSB pin is set high, the I ² C address is 0x1A. |
| B12 | XTALP | Miscellaneous digital ¹ | Crystal Input. |
| B13 | PVDD1 | Power | PLL Analog Supply Voltage (1.8 V). |
| B14 | NC | N/A | No Connect. Do not connect to this pin. |
| B15 | NC | N/A | No Connect. Do not connect to this pin. |
| B16 | GND | GND | Ground. |
| B17 | RX_CP | Rx input | Rx Clock True Input. |
| B18 | RX_OP | Rx input | Rx Channel 0 True Input. |
| B19 | RX_1P | Rx input | Rx Channel 1 True Input. |
| B20 | RX_2P | Rx input | Rx Channel 2 True Input. |
| B21 | GND | GND | Ground. |
| B22 | COMP1 | Miscellaneous analog ¹ | Compensation Pin. Connect a 2.2 nF capacitor from COMP1 to AVDD2. |
| B23 | DAC4 | Analog video output | Encoder DAC4 Output. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|--|
| C1 | OSD_IN[19]/EXT_DIN[3] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[19])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[3]). |
| C2 | OSD_IN[20]/EXT_DIN[4] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[20])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[4]). |
| C3 | GND | GND | Ground. |
| C4 | AUD_IN[4] | Audio input | I ² S3/DSD4 Audio Input. |
| C5 | DSD_CLK | Audio input | DSD Audio Clock Input. |
| C6 | SCLK | Audio input | I ² S Bit Clock Input. |
| C7 | SCL | I ² C control | I ² C Clock Input. SCL is open drain; use a 4.7 k Ω resistor to connect this pin to a 3.3 V supply. |
| C8 | SCK1 | Serial port control | Serial Clock (Serial Port 1). Serial Port 1 is used for OSD control. |
| C9 | GND | GND | Ground. |
| C10 | INT0 | Miscellaneous digital | Interrupt Pin 0. When status bits change, this pin is triggered. |
| C11 | PDN | Miscellaneous digital | Power-Down. This pin controls the power state of the ADV8003. |
| C12 | GND | GND | Ground. |
| C13 | GND | GND | Ground. |
| C14 | NC | N/A | No Connect. Do not connect to this pin. |
| C15 | NC | N/A | No Connect. Do not connect to this pin. |
| C16 | RX_HPD | Rx input | Hot Plug Assert Signal Output for the Rx Input. |
| C17 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C18 | GND | GND | Ground. |
| C19 | GND | GND | Ground. |
| C20 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C21 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C22 | DAC5 | Analog video output | Encoder DAC5 Output. |
| C23 | DAC6 | Analog video output | Encoder DAC6 Output. |
| D1 | OSD_IN[16]/EXT_DIN[0] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[16])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[0]). |
| D2 | OSD_IN[17]/EXT_DIN[1] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[17])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[1]). |
| D3 | OSD_IN[18]/EXT_DIN[2] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[18])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[2]). |
| D4 | GND | GND | Ground. |
| D5 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D6 | MCLK | Audio input | MCLK for S/PDIF Input Audio. |
| D7 | SDA | I ² C control | I ² C Data Input. SDA is open drain; use a 4.7 k Ω resistor to connect this pin to a 3.3 V supply. |
| D8 | $\overline{CS1}$ | Serial port control | Chip Select (Serial Port 1). Serial Port 1 is used for OSD control. |
| D9 | GND | GND | Ground. |
| D10 | INT1 | Miscellaneous digital | Interrupt Pin for HDMI Transmitter Outputs. When status bits change, an interrupt is generated on this pin. |
| D11 | INT2 | Miscellaneous digital | Interrupt Pin for HDMI Receiver Input Lines. When status bits change, an interrupt is generated on this pin. |
| D12 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D13 | TEST1 | Miscellaneous digital | Test Pin. Float this pin. |
| D14 | NC | N/A | No Connect. Do not connect to this pin. |
| D15 | NC | N/A | No Connect. Do not connect to this pin. |
| D16 | RX_5V | Rx input | 5 V Detect Pin for the Rx Input. |
| D17 | NC | N/A | No Connect. Do not connect to this pin. |
| D18 | NC | N/A | No Connect. Do not connect to this pin. |
| D19 | RTERM | HDMI Rx input | This pin sets internal termination resistance. Use a 500 Ω resistor between this pin and GND. Place the RTERM resistor as close as possible to the ADV8003. |
| D20 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D21 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D22 | DAC1 | Analog video output | Encoder DAC1 Output. |
| D23 | DAC2 | Analog video output | Encoder DAC2 Output. |

| Pin No. | Mnemonic | Type | Description |
|---------|---------------------|---|--|
| E1 | OSD_IN[13]/VBI_SCK | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[13])/Serial Clock for VBI Data Serial Port (VBI_SCK). |
| E2 | OSD_IN[14]/VBI_MOSI | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[14])/Master Out Slave In for VBI Data Serial Port (VBI_MOSI). |
| E3 | OSD_IN[15]/VBI_CS | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[15])/Chip Select for VBI Data Serial Port (VBI_CS). |
| E4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| E20 | TEST2 | Miscellaneous analog | Test Pin. Float this pin. |
| E21 | GND | GND | Ground. |
| E22 | COMP2 | Miscellaneous analog ¹ | Compensation Pin. Connect a 2.2 nF capacitor to AVDD2. |
| E23 | DAC3 | Analog video output | Encoder DAC3 Output. |
| F1 | OSD_IN[9] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[9]). |
| F2 | OSD_IN[10] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[10]). |
| F3 | OSD_IN[11] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[11]). |
| F4 | OSD_IN[12] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[12]). |
| F20 | RSET2 | Miscellaneous analog ¹ | Resistor Current Setting for Encoder DACs: DAC4, DAC5, and DAC6. Place the RSET2 resistor as close as possible to the ADV8003. |
| F21 | PVDD3 | Power | PLL Supply (1.8 V). |
| F22 | GND | GND | Ground. |
| F23 | CEC1 | HDMI Tx1 | HDMI Tx1 Consumer Electronics Control (CEC). |
| G1 | OSD_IN[5] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[5]). |
| G2 | OSD_IN[6] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[6]). |
| G3 | OSD_IN[7] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[7]). |
| G4 | OSD_IN[8] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[8]). |
| G7 | GND | GND | Ground. |
| G8 | GND | GND | Ground. |
| G9 | GND | GND | Ground. |
| G10 | DVDD | Power | Digital Power Supply (1.8 V). |
| G11 | GND | GND | Ground. |
| G12 | GND | GND | Ground. |
| G13 | DVDD | Power | Digital Power Supply (1.8 V). |
| G14 | GND | GND | Ground. |
| G15 | GND | GND | Ground. |
| G16 | GND | GND | Ground. |
| G17 | GND | GND | Ground. |
| G20 | ELPF1 | Miscellaneous analog ¹ | External Loop Filter for PLL 1. Connect to PVDD3. |
| G21 | ELPF2 | Miscellaneous analog ¹ | External Loop Filter for PLL 2. Connect to PVDD3. |
| G22 | GND | GND | Ground. |
| G23 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| H1 | OSD_IN[1] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[1]). |
| H2 | OSD_IN[2] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[2]). |
| H3 | OSD_IN[3] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[3]). |
| H4 | OSD_IN[4] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[4]). |
| H7 | GND | GND | Ground. |
| H8 | GND | GND | Ground. |
| H9 | GND | GND | Ground. |
| H10 | GND | GND | Ground. |
| H11 | GND | GND | Ground. |
| H12 | GND | GND | Ground. |
| H13 | GND | GND | Ground. |
| H14 | GND | GND | Ground. |
| H15 | GND | GND | Ground. |
| H16 | GND | GND | Ground. |
| H17 | GND | GND | Ground. |
| H20 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------|---------------------|--|
| H21 | GND | GND | Ground. |
| H22 | TX1_2+ | HDMI Tx1 | HDMI1 Channel 2 True Output. |
| H23 | TX1_2- | HDMI Tx1 | HDMI1 Channel 2 Complementary Output. |
| J1 | DE | Digital video sync | Data Enable for Digital Input Video. |
| J2 | HS | Digital video sync | Horizontal Sync for Digital Input Video. |
| J3 | OSD_HS | Digital video sync | Horizontal Sync for the OSD Input Port (OSD_HS). |
| J4 | OSD_IN[0] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[0]). |
| J7 | DVDD | Power | Digital Power Supply (1.8 V). |
| J8 | GND | GND | Ground. |
| J9 | GND | GND | Ground. |
| J10 | GND | GND | Ground. |
| J11 | GND | GND | Ground. |
| J12 | GND | GND | Ground. |
| J13 | GND | GND | Ground. |
| J14 | GND | GND | Ground. |
| J15 | GND | GND | Ground. |
| J16 | GND | GND | Ground. |
| J17 | DVDD | Power | Digital Power Supply (1.8 V). |
| J20 | DDC1_SDA | HDMI Tx1 | HDCP Slave Serial Data for HDMI Tx1. This pin is open drain; use a 2 k Ω resistor to connect this pin to the HDMI Tx 5 V supply. |
| J21 | GND | GND | Ground. |
| J22 | TX1_1+ | HDMI Tx1 | HDMI1 Channel 1 True Output. |
| J23 | TX1_1- | HDMI Tx1 | HDMI1 Channel 1 Complementary Output. |
| K1 | VS | Digital video sync | Vertical Sync for Digital Input Video. |
| K2 | PCLK | Digital video sync | Pixel Clock for Digital Input Video. |
| K3 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K7 | GND | GND | Ground. |
| K8 | GND | GND | Ground. |
| K9 | GND | GND | Ground. |
| K10 | GND | GND | Ground. |
| K11 | GND | GND | Ground. |
| K12 | GND | GND | Ground. |
| K13 | GND | GND | Ground. |
| K14 | GND | GND | Ground. |
| K15 | GND | GND | Ground. |
| K16 | GND | GND | Ground. |
| K17 | GND | GND | Ground. |
| K20 | DDC1_SCL | HDMI Tx1 | HDCP Slave Serial Clock for HDMI Tx1. This pin is open drain; use a 2 k Ω resistor to connect this pin to the HDMI Tx 5 V supply. |
| K21 | GND | GND | Ground. |
| K22 | TX1_0+ | HDMI Tx1 | HDMI1 Channel 0 True Output. |
| K23 | TX1_0- | HDMI Tx1 | HDMI1 Channel 0 Complementary Output. |
| L1 | P[32] | Digital video input | Digital Video Input Bus[35:0]. |
| L2 | P[33] | Digital video input | Digital Video Input Bus[35:0]. |
| L3 | P[34] | Digital video input | Digital Video Input Bus[35:0]. |
| L4 | P[35] | Digital video input | Digital Video Input Bus[35:0]. |
| L7 | DVDD | Power | Digital Power Supply (1.8 V). |
| L8 | GND | GND | Ground. |
| L9 | GND | GND | Ground. |
| L10 | GND | GND | Ground. |
| L11 | GND | GND | Ground. |
| L12 | GND | GND | Ground. |
| L13 | GND | GND | Ground. |
| L14 | GND | GND | Ground. |
| L15 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|-----------------------|--|
| L16 | GND | GND | Ground. |
| L17 | GND | GND | Ground. |
| L20 | HPD_TX1 | HDMI Tx1 | Hot Plug Assert Signal Input for HDMI Tx1. |
| L21 | GND | GND | Ground. |
| L22 | TX1_C+ | HDMI Tx1 | HDMI1 Clock True Output. |
| L23 | TX1_C- | HDMI Tx1 | HDMI1 Clock Complementary Output. |
| M1 | P[28] | Digital video input | Digital Video Input Bus[35:0]. |
| M2 | P[29] | Digital video input | Digital Video Input Bus[35:0]. |
| M3 | P[30] | Digital video input | Digital Video Input Bus[35:0]. |
| M4 | P[31] | Digital video input | Digital Video Input Bus[35:0]. |
| M7 | GND | GND | Ground. |
| M8 | GND | GND | Ground. |
| M9 | GND | GND | Ground. |
| M10 | GND | GND | Ground. |
| M11 | GND | GND | Ground. |
| M12 | GND | GND | Ground. |
| M13 | GND | GND | Ground. |
| M14 | GND | GND | Ground. |
| M15 | GND | GND | Ground. |
| M16 | GND | GND | Ground. |
| M17 | GND | GND | Ground. |
| M20 | R_TX1 | HDMI Tx1 ¹ | Sets Internal Reference Currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground, as close as possible to the ADV8003. |
| M21 | PVDD5 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| M22 | HEAC_1+ | HDMI Tx1 | HDMI Tx1 HEAC+ from the HDMI Connector. |
| M23 | HEAC_1- | HDMI Tx1 | HDMI Tx1 HEAC- from the HDMI Connector. |
| N1 | P[24] | Digital video input | Digital Video Input Bus[35:0]. |
| N2 | P[25] | Digital video input | Digital Video Input Bus[35:0]. |
| N3 | P[26] | Digital video input | Digital Video Input Bus[35:0]. |
| N4 | P[27] | Digital video input | Digital Video Input Bus[35:0]. |
| N7 | GND | GND | Ground. |
| N8 | GND | GND | Ground. |
| N9 | GND | GND | Ground. |
| N10 | GND | GND | Ground. |
| N11 | GND | GND | Ground. |
| N12 | GND | GND | Ground. |
| N13 | GND | GND | Ground. |
| N14 | GND | GND | Ground. |
| N15 | GND | GND | Ground. |
| N16 | GND | GND | Ground. |
| N17 | GND | GND | Ground. |
| N20 | CEC2 | HDMI Tx2 | HDMI Tx2 Consumer Electronics Control (CEC). |
| N21 | PVDD5 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| N22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| N23 | NC | N/A | No Connect. Do not connect to this pin. |
| P1 | P[20] | Digital video input | Digital Video Input Bus[35:0]. |
| P2 | P[21] | Digital video input | Digital Video Input Bus[35:0]. |
| P3 | P[22] | Digital video input | Digital Video Input Bus[35:0]. |
| P4 | P[23] | Digital video input | Digital Video Input Bus[35:0]. |
| P7 | DVDD | Power | Digital Power Supply (1.8 V). |
| P8 | GND | GND | Ground. |
| P9 | GND | GND | Ground. |
| P10 | GND | GND | Ground. |
| P11 | GND | GND | Ground. |
| P12 | GND | GND | Ground. |
| P13 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|---------------------|--|
| P14 | GND | GND | Ground. |
| P15 | GND | GND | Ground. |
| P16 | GND | GND | Ground. |
| P17 | DVDD | Power | Digital Power Supply (1.8 V). |
| P20 | DDC2_SCL | HDMI Tx2 | HDCP Slave Serial Clock for HDMI Tx2. This pin is open drain; use a 2 k Ω resistor to connect this pin to the HDMI Tx 5 V supply. |
| P21 | GND | GND | Ground. |
| P22 | TX2_2+ | HDMI Tx2 | HDMI2 Channel 2 True Output. |
| P23 | TX2_2- | HDMI Tx2 | HDMI2 Channel 2 Complementary Output. |
| R1 | P[16] | Digital video input | Digital Video Input Bus[35:0]. |
| R2 | P[17] | Digital video input | Digital Video Input Bus[35:0]. |
| R3 | P[18] | Digital video input | Digital Video Input Bus[35:0]. |
| R4 | P[19] | Digital video input | Digital Video Input Bus[35:0]. |
| R7 | GND | GND | Ground. |
| R8 | GND | GND | Ground. |
| R9 | GND | GND | Ground. |
| R10 | GND | GND | Ground. |
| R11 | GND | GND | Ground. |
| R12 | GND | GND | Ground. |
| R13 | GND | GND | Ground. |
| R14 | GND | GND | Ground. |
| R15 | GND | GND | Ground. |
| R16 | GND | GND | Ground. |
| R17 | GND | GND | Ground. |
| R20 | DDC2_SDA | HDMI Tx2 | HDCP Slave Serial Data for HDMI Tx2. This pin is open drain; use a 2 k Ω resistor to connect this pin to the HDMI Tx 5 V supply. |
| R21 | GND | GND | Ground. |
| R22 | TX2_1+ | HDMI Tx2 | HDMI2 Channel 1 True Output. |
| R23 | TX2_1- | HDMI Tx2 | HDMI2 Channel 1 Complementary Output. |
| T1 | P[14] | Digital video input | Digital Video Input Bus[35:0]. |
| T2 | P[15] | Digital video input | Digital Video Input Bus[35:0]. |
| T3 | GND | GND | Ground. |
| T4 | GND | GND | Ground. |
| T7 | GND | GND | Ground. |
| T8 | GND | GND | Ground. |
| T9 | GND | GND | Ground. |
| T10 | GND | GND | Ground. |
| T11 | GND | GND | Ground. |
| T12 | GND | GND | Ground. |
| T13 | GND | GND | Ground. |
| T14 | GND | GND | Ground. |
| T15 | GND | GND | Ground. |
| T16 | GND | GND | Ground. |
| T17 | GND | GND | Ground. |
| T20 | HPD_TX2 | HDMI Tx2 | Hot Plug Assert Signal Input for HDMI Tx2. |
| T21 | GND | GND | Ground. |
| T22 | TX2_0+ | HDMI Tx2 | HDMI2 Channel 0 True Output. |
| T23 | TX2_0- | HDMI Tx2 | HDMI2 Channel 0 Complementary Output. |
| U1 | P[10] | Digital video input | Digital Video Input Bus[35:0]. |
| U2 | P[11] | Digital video input | Digital Video Input Bus[35:0]. |
| U3 | P[12] | Digital video input | Digital Video Input Bus[35:0]. |
| U4 | P[13] | Digital video input | Digital Video Input Bus[35:0]. |
| U7 | GND | GND | Ground. |
| U8 | GND | GND | Ground. |
| U9 | DVDD | Power | Digital Power Supply (1.8 V). |
| U10 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|-----------------------|---|
| U11 | GND | GND | Ground. |
| U12 | DVDD | Power | Digital Power Supply (1.8 V). |
| U13 | GND | GND | Ground. |
| U14 | GND | GND | Ground. |
| U15 | DVDD | Power | Digital Power Supply (1.8 V). |
| U16 | GND | GND | Ground. |
| U17 | GND | GND | Ground. |
| U20 | R_TX2 | HDMI Tx2 ¹ | Sets internal reference currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground, as close as possible to the ADV8003. |
| U21 | GND | GND | Ground. |
| U22 | TX2_C+ | HDMI Tx2 ¹ | HDMI2 Clock True Output. |
| U23 | TX2_C- | HDMI Tx2 ¹ | HDMI2 Clock Complementary Output. |
| V1 | P[6] | Digital video input | Digital Video Input Bus[35:0]. |
| V2 | P[7] | Digital video input | Digital Video Input Bus[35:0]. |
| V3 | P[8] | Digital video input | Digital Video Input Bus[35:0]. |
| V4 | P[9] | Digital video input | Digital Video Input Bus[35:0]. |
| V20 | GND | GND | Ground. |
| V21 | PVDD6 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| V22 | HEAC_2+ | HDMI Tx2 | HDMI Tx2 HEC+ from HDMI Connector. |
| V23 | HEAC_2- | HDMI Tx2 | HDMI Tx2 HEC- from HDMI Connector. |
| W1 | P[2] | Digital video input | Digital Video Input Bus[35:0]. |
| W2 | P[3] | Digital video input | Digital Video Input Bus[35:0]. |
| W3 | P[4] | Digital video input | Digital Video Input Bus[35:0]. |
| W4 | P[5] | Digital video input | Digital Video Input Bus[35:0]. |
| W20 | TEST3 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 0.1 μF capacitor. |
| W21 | PVDD6 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| W22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| W23 | NC | N/A | No Connect. Do not connect to this pin. |
| Y1 | P[0] | Digital video input | Digital Video Input Bus[35:0]. |
| Y2 | P[1] | Digital video input | Digital Video Input Bus[35:0]. |
| Y3 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| Y4 | GND | GND | Ground. |
| Y5 | DDR_DQ[23] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| Y8 | GND | GND | Ground. |
| Y9 | DDR_A[11] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y11 | DDR_A[4] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y12 | GND | GND | Ground. |
| Y13 | DDR_CAS | DDR interface | Column Address Strobe for DDR Memory. |
| Y14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| Y16 | GND | GND | Ground. |
| Y17 | DDR_DQ[9] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y19 | DDR_DQ[14] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y20 | GND | GND | Ground. |
| Y21 | DDR_DQ[6] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y22 | PVDD_DDR | Power | DDR Interface PLL Supply (1.8 V). |
| Y23 | GND | GND | Ground. |
| AA1 | DDR_DQ[18] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA2 | GND | GND | Ground. |
| AA3 | GND | GND | Ground. |
| AA4 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|----------------|---|
| AA5 | DDR_DQ[26] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| AA8 | NC/GND | No connect/GND | For new ADV8003 designs, do not connect to this pin. For designs that must maintain consistency with the ADV8002, this pin can be grounded. |
| AA9 | DDR_A[8] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA11 | DDR_A[2] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA12 | GND | GND | Ground. |
| AA13 | DDR_CS | DDR interface | DDR Chip Select. Interface to external DDR RAM chip selects. |
| AA14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| AA16 | GND | GND | Ground. |
| AA17 | DDR_DQ[11] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA19 | DDR_DM[1] | DDR interface | Data Mask for Data Lines[15:8]. |
| AA20 | DDR_DM[0] | DDR interface | Data Mask for Data Lines[7:0]. |
| AA21 | GND | GND | Ground. |
| AA22 | GND | GND | Ground. |
| AA23 | DDR_DQ[3] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB1 | DDR_DQ[21] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB2 | DDR_DQ[19] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB3 | DDR_DQ[17] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB4 | DDR_DM[2] | DDR interface | Data Mask for Data Lines[23:16]. |
| AB5 | DDR_DQ[30] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB6 | DDR_DM[3] | DDR interface | Data Mask for Data Lines[31:25]. |
| AB7 | DDR_DQ[31] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB8 | DDR_DQ[29] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB9 | DDR_A[12] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB10 | DDR_A[6] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB11 | DDR_A[3] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB12 | DDR_A[0] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB13 | DDR_BA[0] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AB14 | DDR_RAS | DDR interface | Row Address Strobe for DDR Memory. |
| AB15 | DDR_CKE | DDR interface | Clock Enable for External DDR Memory. |
| AB16 | DDR_DQ[12] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB17 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AB18 | DDR_DQ[8] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB19 | DDR_DQ[13] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB20 | DDR_DQ[0] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB21 | DDR_DQ[5] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AB23 | DDR_DQ[4] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC1 | DDR_DQ[16] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC2 | DDR_DQ[20] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC3 | DDR_DQ[22] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC4 | DDR_DQ[25] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC5 | DDR_DQ[28] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC6 | DDR_DQ[27] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC7 | DDR_DQ[24] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC8 | DDR_A[9] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC9 | DDR_A[5] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC10 | DDR_A[7] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC11 | DDR_A[1] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC12 | DDR_A[10] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC13 | DDR_BA[1] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|----------------------------|--|
| AC14 | DDR_BA[2] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AC15 | DDR_WE | DDR interface | Write Enable Signal for DDR RAM. |
| AC16 | DDR_VREF | DDR interface ¹ | Reference Voltage for DDR RAM. |
| AC17 | DDR_DQ[10] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC18 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AC19 | DDR_DQ[15] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC20 | DDR_DQ[7] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC21 | DDR_DQ[2] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AC23 | DDR_DQ[1] | DDR interface | Data Line. Interface to external RAM data lines. |

¹ Sensitive node. Careful layout is important. Keep the associated circuitry as close as possible to the ADV8003.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | | |
|----|-----------------------|-----------------------|-----------------------|------------|------------|------------|------------|------------|-----------|----------|----------|-----------|-----------|-----------|---------|------------|------------|------------|------------|-----------|-----------|------------|-----------|---------|---|
| A | OSD_IN[23]/EXT_DIN[7] | OSD_DE | OSD_CLK/EXT_CLK | AUD_IN[1] | AUD_IN[2] | AUD_IN[5] | TEST4 | MOSI1 | SCK2 | CS2 | RESET | XTALN | PVDD2 | NC | NC | CVDD1 | RX_CN | RX_ON | RX_1N | RX_2N | CVDD1 | NC | NC | A | |
| B | OSD_IN[21]/EXT_DIN[5] | OSD_IN[22]/EXT_DIN[6] | OSD_VS | AUD_IN[0] | AUD_IN[3] | SFL | ARC1_OUT | MISO1 | MISO2 | MISO2 | ALS_B | XTALP | PVDD1 | NC | NC | GND | RX_CP | RX_OP | RX_1P | RX_2P | GND | NC | NC | B | |
| C | OSD_IN[19]/EXT_DIN[3] | OSD_IN[20]/EXT_DIN[4] | GND | AUD_IN[4] | DSD_CLK | SCLK | SCL | SCK1 | GND | INT0 | PDN | GND | GND | NC | NC | RX_HPD | AVDD1 | GND | GND | AVDD1 | AVDD1 | NC | NC | C | |
| D | OSD_IN[16]/EXT_DIN[0] | OSD_IN[17]/EXT_DIN[1] | OSD_IN[18]/EXT_DIN[2] | GND | DVDD_IO | MCLK | SDA | CS1 | GND | INT1 | INT2 | DVDD_IO | TEST1 | NC | NC | RX_5V | NC | NC | RTERM | AVDD2 | AVDD2 | NC | NC | D | |
| E | OSD_IN[13]/VBI_SCK | OSD_IN[14]/VBI_MOS | OSD_IN[15]/VBI_CS | DVDD_IO | | | | | | | | | | | | | | | | TEST2 | GND | NC | NC | E | |
| F | OSD_IN[9] | OSD_IN[10] | OSD_IN[11] | OSD_IN[12] | | | | | | | | | | | | | | | | | NC | PVDD3 | GND | CEC1 | F |
| G | OSD_IN[5] | OSD_IN[6] | OSD_IN[7] | OSD_IN[8] | | | GND | GND | GND | DVDD | GND | GND | DVDD | GND | GND | GND | GND | | | | ELPF1 | ELPF2 | GND | AVDD3 | G |
| H | OSD_IN[1] | OSD_IN[2] | OSD_IN[3] | OSD_IN[4] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | GND | GND | TX1_2+ | TX1_2- | H |
| J | DE | HS | OSD_HS | OSD_IN[0] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | | | | DDC1_SDA | GND | TX1_1+ | TX1_1- | J |
| K | VS | PCLK | DVDD_IO | DVDD_IO | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | DDC1_SCL | GND | TX1_0+ | TX1_0- | K |
| L | P[32] | P[33] | P[34] | P[35] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | HPD_TX1 | GND | TX1_C+ | TX1_C- | L |
| M | P[28] | P[29] | P[30] | P[31] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | R_TX1 | PVDD5 | HEAC_1+ | HEAC_1- | M |
| N | P[24] | P[25] | P[26] | P[27] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | PVDD5 | AVDD3 | NC | N |
| P | P[20] | P[21] | P[22] | P[23] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | | | | NC | GND | NC | NC | P |
| R | P[16] | P[17] | P[18] | P[19] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | GND | NC | NC | R |
| T | P[14] | P[15] | GND | GND | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | GND | NC | NC | T |
| U | P[10] | P[11] | P[12] | P[13] | | | GND | GND | DVDD | GND | GND | DVDD | GND | GND | DVDD | GND | GND | | | | NC | GND | NC | NC | U |
| V | P[6] | P[7] | P[8] | P[9] | | | | | | | | | | | | | | | | | GND | PVDD6 | NC | NC | V |
| W | P[2] | P[3] | P[4] | P[5] | | | | | | | | | | | | | | | | | TEST3 | PVDD6 | AVDD3 | NC | W |
| Y | P[0] | P[1] | DDR_DQS[2] | GND | DDR_DQ[23] | DVDD_DDR | DDR_DQS[3] | GND | DDR_A[11] | DVDD_DDR | DDR_A[4] | GND | DDR_CAS | DVDD_DDR | DDR_CK | GND | DDR_DQ[9] | DVDD_DDR | DDR_DQ[14] | GND | DDR_DQ[6] | PVDD_DDR | GND | Y | |
| AA | DDR_DQ[18] | GND | GND | DDR_DQS[2] | DDR_DQ[26] | DVDD_DDR | DDR_DQS[3] | NC/GND | DDR_A[8] | DVDD_DDR | DDR_A[2] | GND | DDR_CS | DVDD_DDR | DDR_CK | GND | DDR_DQ[11] | DVDD_DDR | DDR_DM[1] | DDR_DM[0] | GND | GND | DDR_DQ[3] | AA | |
| AB | DDR_DQ[21] | DDR_DQ[19] | DDR_DQ[17] | DDR_DM[2] | DDR_DQ[30] | DDR_DM[3] | DDR_DQ[31] | DDR_DQ[29] | DDR_A[12] | DDR_A[6] | DDR_A[3] | DDR_A[0] | DDR_BA[0] | DDR_RAS | DDR_CKE | DDR_DQ[12] | DDR_DQS[1] | DDR_DQ[8] | DDR_DQ[13] | DDR_DQ[0] | DDR_DQ[5] | DDR_DQS[0] | DDR_DQ[4] | AB | |
| AC | DDR_DQ[16] | DDR_DQ[20] | DDR_DQ[22] | DDR_DQ[25] | DDR_DQ[28] | DDR_DQ[27] | DDR_DQ[24] | DDR_A[9] | DDR_A[5] | DDR_A[7] | DDR_A[1] | DDR_A[10] | DDR_BA[1] | DDR_BA[2] | DDR_WE | DDR_VREF | DDR_DQ[10] | DDR_DQS[1] | DDR_DQ[15] | DDR_DQ[7] | DDR_DQ[2] | DDR_DQS[0] | DDR_DQ[1] | AC | |

Figure 30. ADV8003KBCZ-8B and ADV8003KBCZ-7B Pin Configuration

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Table 7. ADV8003KBCZ-8B and ADV8003KBCZ-7B Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|--|
| A1 | OSD_IN[23]/EXT_DIN[7] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[23])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[7]). |
| A2 | OSD_DE | OSD video sync | Data Enable for the OSD Input Port. |
| A3 | OSD_CLK/EXT_CLK | OSD video sync | Pixel Clock for the OSD Input Port (OSD_CLK)/Pixel Clock for External Video Data (EXT_CLK). |
| A4 | AUD_IN[1] | Audio input | I ² S0/DSD1 Audio Input. |
| A5 | AUD_IN[2] | Audio input | I ² S1/DSD2 Audio Input. |
| A6 | AUD_IN[5] | Audio input | LRCLK/DSD5 Audio Input. |
| A7 | TEST4 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| A8 | MOSI1 | Serial port control | Master Out Slave In (Serial Port 1). Serial Port 1 is used for OSD control. |
| A9 | SCK2 | Serial port control | Serial Clock (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A10 | $\overline{CS2}$ | Serial port control | Chip Select (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A11 | \overline{RESET} | Miscellaneous digital | Reset Pin. |
| A12 | XTALN | Miscellaneous digital ¹ | Crystal Input. |
| A13 | PVDD2 | Power | PLL Digital Supply Voltage (1.8 V). |
| A14 | NC | N/A | No Connect. Do not connect to this pin. |
| A15 | NC | N/A | No Connect. Do not connect to this pin. |
| A16 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A17 | RX_CN | Rx input | Rx Clock Complement Input. |
| A18 | RX_ON | Rx input | Rx Channel 0 Complement Input. |
| A19 | RX_1N | Rx input | Rx Channel 1 Complement Input. |
| A20 | RX_2N | Rx input | Rx Channel 2 Complement Input. |
| A21 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A22 | NC | N/A | No Connect. Do not connect to this pin. |
| A23 | NC | N/A | No Connect. Do not connect to this pin. |
| B1 | OSD_IN[21]/EXT_DIN[5] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[21])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[5]). |
| B2 | OSD_IN[22]/EXT_DIN[6] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[22])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[6]). |
| B3 | OSD_VS | OSD video sync | Vertical Sync for the OSD Input Port. |
| B4 | AUD_IN[0] | Audio input | S/PDIF or DSD0 Audio Input. |
| B5 | AUD_IN[3] | Audio input | I ² S2/DSD3 Audio Input. |
| B6 | SFL | SFL | Subcarrier Frequency Lock Signal (SFL). |
| B7 | ARC1_OUT | Audio output | Audio Return Channel for HDMI Tx1. |
| B8 | MISO1 | Serial port control | Master In Slave Out (Serial Port 1). Serial Port 1 is used for OSD control. |
| B9 | MOSI2 | Serial port control | Master Out Slave In (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B10 | MISO2 | Serial port control | Master In Slave Out (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B11 | ALSB | I ² C control | Sets LSB of I ² C address. When the ALSB pin is set low, the I ² C address is 0x18; when the ALSB pin is set high, the I ² C address is 0x1A. |
| B12 | XTALP | Miscellaneous digital ¹ | Crystal Input. |
| B13 | PVDD1 | Power | PLL Analog Supply Voltage (1.8 V). |
| B14 | NC | N/A | No Connect. Do not connect to this pin. |
| B15 | NC | N/A | No Connect. Do not connect to this pin. |
| B16 | GND | GND | Ground. |
| B17 | RX_CP | Rx input | Rx Clock True Input. |
| B18 | RX_OP | Rx input | Rx Channel 0 True Input. |
| B19 | RX_1P | Rx input | Rx Channel 1 True Input. |
| B20 | RX_2P | Rx input | Rx Channel 2 True Input. |
| B21 | GND | GND | Ground. |
| B22 | NC | N/A | No Connect. Do not connect to this pin. |
| B23 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|--|
| C1 | OSD_IN[19]/EXT_DIN[3] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[19])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[3]). |
| C2 | OSD_IN[20]/EXT_DIN[4] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[20])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[4]). |
| C3 | GND | GND | Ground. |
| C4 | AUD_IN[4] | Audio input | I ² S3/DSD4 Audio Input. |
| C5 | DSD_CLK | Audio input | DSD Audio Clock Input. |
| C6 | SCLK | Audio input | I ² S Bit Clock Input. |
| C7 | SCL | I ² C control | I ² C Clock Input. This pin is open drain; use a 4.7 k Ω resistor to connect this pin to a 3.3 V supply. |
| C8 | SCK1 | Serial port control | Serial Clock (Serial Port 1). Serial Port 1 is used for OSD control. |
| C9 | GND | GND | Ground. |
| C10 | INT0 | Miscellaneous digital | Interrupt Pin 0. When status bits change, this pin is triggered. |
| C11 | PDN | Miscellaneous digital | Power-Down. This pin controls the power state of the ADV8003. |
| C12 | GND | GND | Ground. |
| C13 | GND | GND | Ground. |
| C14 | NC | N/A | No Connect. Do not connect to this pin. |
| C15 | NC | N/A | No Connect. Do not connect to this pin. |
| C16 | RX_HPD | Rx input | Hot Plug Assert Signal Output for the Rx Input. |
| C17 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C18 | GND | GND | Ground. |
| C19 | GND | GND | Ground. |
| C20 | AVDD1 | Power | HDMI Rx Inputs, Analog Supply (3.3 V). |
| C21 | AVDD1 | Power | HDMI Rx Inputs, Analog Supply (3.3 V). |
| C22 | NC | N/A | No Connect. Do not connect to this pin. |
| C23 | NC | N/A | No Connect. Do not connect to this pin. |
| D1 | OSD_IN[16]/EXT_DIN[0] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[16])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[0]). |
| D2 | OSD_IN[17]/EXT_DIN[1] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[17])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[1]). |
| D3 | OSD_IN[18]/EXT_DIN[2] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[18])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[2]). |
| D4 | GND | GND | Ground. |
| D5 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D6 | MCLK | Audio input | MCLK for S/PDIF Input Audio. |
| D7 | SDA | I ² C control | I ² C Data Input. This pin is open drain; use a 4.7 k Ω resistor to connect this pin to a 3.3 V supply. |
| D8 | $\overline{CS1}$ | Serial port control | Chip Select (Serial Port 1). Serial Port 1 is used for OSD control. |
| D9 | GND | GND | Ground. |
| D10 | INT1 | Miscellaneous digital | Interrupt Pin for HDMI Transmitter Outputs. When status bits change, an interrupt is generated on this pin. |
| D11 | INT2 | Miscellaneous digital | Interrupt Pin for HDMI Receiver Input Lines. When status bits change, an interrupt is generated on this pin. |
| D12 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D13 | TEST1 | Miscellaneous digital | Test Pin. Float this pin. |
| D14 | NC | N/A | No Connect. Do not connect to this pin. |
| D15 | NC | N/A | No Connect. Do not connect to this pin. |
| D16 | RX_5V | Rx input | 5 V Detect Pin for the Rx Input. |
| D17 | NC | N/A | No Connect. Do not connect to this pin. |
| D18 | NC | N/A | No Connect. Do not connect to this pin. |
| D19 | RTERM | HDMI Rx input | This pin sets internal termination resistance. Use a 500 Ω resistor between this pin and GND. Place the RTERM resistor as close as possible to the ADV8003. |
| D20 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D21 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D22 | NC | N/A | No Connect. Do not connect to this pin. |
| D23 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|---------------------|---|---|
| E1 | OSD_IN[13]/VBI_SCK | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[13])/Serial Clock for VBI Data Serial Port (VBI_SCK). |
| E2 | OSD_IN[14]/VBI_MOSI | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[14])/Master Out Slave In for VBI Data Serial Port (VBI_MOSI). |
| E3 | OSD_IN[15]/VBI_CS | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[15])/Chip Select for VBI Data Serial Port (VBI_CS). |
| E4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| E20 | TEST2 | Miscellaneous analog | Test Pin. Float this pin. |
| E21 | GND | GND | Ground. |
| E22 | NC | N/A | No Connect. Do not connect to this pin. |
| E23 | NC | N/A | No Connect. Do not connect to this pin. |
| F1 | OSD_IN[9] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[9]). |
| F2 | OSD_IN[10] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[10]). |
| F3 | OSD_IN[11] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[11]). |
| F4 | OSD_IN[12] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[12]). |
| F20 | NC | N/A | No Connect. Do not connect to this pin. |
| F21 | PVDD3 | Power | PLL Supply (1.8 V). |
| F22 | GND | GND | Ground. |
| F23 | CEC1 | HDMI Tx1 | HDMI Tx1 Consumer Electronics Control (CEC). |
| G1 | OSD_IN[5] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[5]). |
| G2 | OSD_IN[6] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[6]). |
| G3 | OSD_IN[7] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[7]). |
| G4 | OSD_IN[8] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[8]). |
| G7 | GND | GND | Ground. |
| G8 | GND | GND | Ground. |
| G9 | GND | GND | Ground. |
| G10 | DVDD | Power | Digital Power Supply (1.8 V). |
| G11 | GND | GND | Ground. |
| G12 | GND | GND | Ground. |
| G13 | DVDD | Power | Digital Power Supply (1.8 V). |
| G14 | GND | GND | Ground. |
| G15 | GND | GND | Ground. |
| G16 | GND | GND | Ground. |
| G17 | GND | GND | Ground. |
| G20 | ELPF1 | Miscellaneous analog ¹ | External Loop Filter for PLL 1. Connect to PVDD3. |
| G21 | ELPF2 | Miscellaneous analog ¹ | External Loop Filter for PLL 2. Connect to PVDD3. |
| G22 | GND | GND | Ground. |
| G23 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| H1 | OSD_IN[1] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[1]). |
| H2 | OSD_IN[2] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[2]). |
| H3 | OSD_IN[3] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[3]). |
| H4 | OSD_IN[4] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[4]). |
| H7 | GND | GND | Ground. |
| H8 | GND | GND | Ground. |
| H9 | GND | GND | Ground. |
| H10 | GND | GND | Ground. |
| H11 | GND | GND | Ground. |
| H12 | GND | GND | Ground. |
| H13 | GND | GND | Ground. |
| H14 | GND | GND | Ground. |
| H15 | GND | GND | Ground. |
| H16 | GND | GND | Ground. |
| H17 | GND | GND | Ground. |
| H20 | GND | GND | Ground. |
| H21 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------|---------------------|--|
| H22 | TX1_2+ | HDMI Tx1 | HDMI1 Channel 2 True Output. |
| H23 | TX1_2- | HDMI Tx1 | HDMI1 Channel 2 Complementary Output. |
| J1 | DE | Digital video sync | Data Enable for Digital Input Video. |
| J2 | HS | Digital video sync | Horizontal Sync for Digital Input Video. |
| J3 | OSD_HS | Digital video sync | Horizontal Sync for the OSD Input Port (OSD_HS). |
| J4 | OSD_IN[0] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[0]). |
| J7 | DVDD | Power | Digital Power Supply (1.8 V). |
| J8 | GND | GND | Ground. |
| J9 | GND | GND | Ground. |
| J10 | GND | GND | Ground. |
| J11 | GND | GND | Ground. |
| J12 | GND | GND | Ground. |
| J13 | GND | GND | Ground. |
| J14 | GND | GND | Ground. |
| J15 | GND | GND | Ground. |
| J16 | GND | GND | Ground. |
| J17 | DVDD | Power | Digital Power Supply (1.8 V). |
| J20 | DDC1_SDA | HDMI Tx1 | HDCP Slave Serial Data for HDMI Tx1. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI Tx 5 V supply. |
| J21 | GND | GND | Ground. |
| J22 | TX1_1+ | HDMI Tx1 | HDMI1 Channel 1 True Output. |
| J23 | TX1_1- | HDMI Tx1 | HDMI1 Channel 1 Complementary Output. |
| K1 | VS | Digital video sync | Vertical Sync for Digital Input Video. |
| K2 | PCLK | Digital video sync | Pixel Clock for Digital Input Video. |
| K3 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K7 | GND | GND | Ground. |
| K8 | GND | GND | Ground. |
| K9 | GND | GND | Ground. |
| K10 | GND | GND | Ground. |
| K11 | GND | GND | Ground. |
| K12 | GND | GND | Ground. |
| K13 | GND | GND | Ground. |
| K14 | GND | GND | Ground. |
| K15 | GND | GND | Ground. |
| K16 | GND | GND | Ground. |
| K17 | GND | GND | Ground. |
| K20 | DDC1_SCL | HDMI Tx1 | HDCP Slave Serial Clock for HDMI Tx1. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI Tx 5 V supply. |
| K21 | GND | GND | Ground. |
| K22 | TX1_0+ | HDMI Tx1 | HDMI1 Channel 0 True Output. |
| K23 | TX1_0- | HDMI Tx1 | HDMI1 Channel 0 Complementary Output. |
| L1 | P[32] | Digital video input | Digital Video Input Bus[35:0]. |
| L2 | P[33] | Digital video input | Digital Video Input Bus[35:0]. |
| L3 | P[34] | Digital video input | Digital Video Input Bus[35:0]. |
| L4 | P[35] | Digital video input | Digital Video Input Bus[35:0]. |
| L7 | DVDD | Power | Digital Power Supply (1.8 V). |
| L8 | GND | GND | Ground. |
| L9 | GND | GND | Ground. |
| L10 | GND | GND | Ground. |
| L11 | GND | GND | Ground. |
| L12 | GND | GND | Ground. |
| L13 | GND | GND | Ground. |
| L14 | GND | GND | Ground. |
| L15 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|-----------------------|--|
| L16 | GND | GND | Ground. |
| L17 | GND | GND | Ground. |
| L20 | HPD_TX1 | HDMI Tx1 | Hot Plug Assert Signal Input for HDMI Tx1. |
| L21 | GND | GND | Ground. |
| L22 | TX1_C+ | HDMI Tx1 | HDMI1 Clock True Output. |
| L23 | TX1_C- | HDMI Tx1 | HDMI1 Clock Complementary Output. |
| M1 | P[28] | Digital video input | Digital Video Input Bus[35:0]. |
| M2 | P[29] | Digital video input | Digital Video Input Bus[35:0]. |
| M3 | P[30] | Digital video input | Digital Video Input Bus[35:0]. |
| M4 | P[31] | Digital video input | Digital Video Input Bus[35:0]. |
| M7 | GND | GND | Ground. |
| M8 | GND | GND | Ground. |
| M9 | GND | GND | Ground. |
| M10 | GND | GND | Ground. |
| M11 | GND | GND | Ground. |
| M12 | GND | GND | Ground. |
| M13 | GND | GND | Ground. |
| M14 | GND | GND | Ground. |
| M15 | GND | GND | Ground. |
| M16 | GND | GND | Ground. |
| M17 | GND | GND | Ground. |
| M20 | R_TX1 | HDMI Tx1 ¹ | Sets internal reference currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground, as close as possible to the ADV8003. |
| M21 | PVDD5 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| M22 | HEAC_1+ | HDMI Tx1 | HDMI Tx1 HEAC+ from HDMI Connector. |
| M23 | HEAC_1- | HDMI Tx1 | HDMI Tx1 HEAC- from HDMI Connector. |
| N1 | P[24] | Digital video input | Digital Video Input Bus[35:0]. |
| N2 | P[25] | Digital video input | Digital Video Input Bus[35:0]. |
| N3 | P[26] | Digital video input | Digital Video Input Bus[35:0]. |
| N4 | P[27] | Digital video input | Digital Video Input Bus[35:0]. |
| N7 | GND | GND | Ground. |
| N8 | GND | GND | Ground. |
| N9 | GND | GND | Ground. |
| N10 | GND | GND | Ground. |
| N11 | GND | GND | Ground. |
| N12 | GND | GND | Ground. |
| N13 | GND | GND | Ground. |
| N14 | GND | GND | Ground. |
| N15 | GND | GND | Ground. |
| N16 | GND | GND | Ground. |
| N17 | GND | GND | Ground. |
| N20 | NC | N/A | No Connect. Do not connect to this pin. |
| N21 | PVDD5 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| N22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| N23 | NC | N/A | No Connect. Do not connect to this pin. |
| P1 | P[20] | Digital video input | Digital Video Input Bus[35:0]. |
| P2 | P[21] | Digital video input | Digital Video Input Bus[35:0]. |
| P3 | P[22] | Digital video input | Digital Video Input Bus[35:0]. |
| P4 | P[23] | Digital video input | Digital Video Input Bus[35:0]. |
| P7 | DVDD | Power | Digital Power Supply (1.8 V). |
| P8 | GND | GND | Ground. |
| P9 | GND | GND | Ground. |
| P10 | GND | GND | Ground. |
| P11 | GND | GND | Ground. |
| P12 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|---------------------|---|
| P13 | GND | GND | Ground. |
| P14 | GND | GND | Ground. |
| P15 | GND | GND | Ground. |
| P16 | GND | GND | Ground. |
| P17 | DVDD | Power | Digital Power Supply (1.8 V). |
| P20 | NC | N/A | No Connect. Do not connect to this pin. |
| P21 | GND | GND | Ground. |
| P22 | NC | N/A | No Connect. Do not connect to this pin. |
| P23 | NC | N/A | No Connect. Do not connect to this pin. |
| R1 | P[16] | Digital video input | Digital Video Input Bus[35:0]. |
| R2 | P[17] | Digital video input | Digital Video Input Bus[35:0]. |
| R3 | P[18] | Digital video input | Digital Video Input Bus[35:0]. |
| R4 | P[19] | Digital video input | Digital Video Input Bus[35:0]. |
| R7 | GND | GND | Ground. |
| R8 | GND | GND | Ground. |
| R9 | GND | GND | Ground. |
| R10 | GND | GND | Ground. |
| R11 | GND | GND | Ground. |
| R12 | GND | GND | Ground. |
| R13 | GND | GND | Ground. |
| R14 | GND | GND | Ground. |
| R15 | GND | GND | Ground. |
| R16 | GND | GND | Ground. |
| R17 | GND | GND | Ground. |
| R20 | NC | N/A | No Connect. Do not connect to this pin. |
| R21 | GND | GND | Ground. |
| R22 | NC | N/A | No Connect. Do not connect to this pin. |
| R23 | NC | N/A | No Connect. Do not connect to this pin. |
| T1 | P[14] | Digital video input | Digital Video Input Bus[35:0]. |
| T2 | P[15] | Digital video input | Digital Video Input Bus[35:0]. |
| T3 | GND | GND | Ground. |
| T4 | GND | GND | Ground. |
| T7 | GND | GND | Ground. |
| T8 | GND | GND | Ground. |
| T9 | GND | GND | Ground. |
| T10 | GND | GND | Ground. |
| T11 | GND | GND | Ground. |
| T12 | GND | GND | Ground. |
| T13 | GND | GND | Ground. |
| T14 | GND | GND | Ground. |
| T15 | GND | GND | Ground. |
| T16 | GND | GND | Ground. |
| T17 | GND | GND | Ground. |
| T20 | NC | N/A | No Connect. Do not connect to this pin. |
| T21 | GND | GND | Ground. |
| T22 | NC | N/A | No Connect. Do not connect to this pin. |
| T23 | NC | N/A | No Connect. Do not connect to this pin. |
| U1 | P[10] | Digital video input | Digital Video Input Bus[35:0]. |
| U2 | P[11] | Digital video input | Digital Video Input Bus[35:0]. |
| U3 | P[12] | Digital video input | Digital Video Input Bus[35:0]. |
| U4 | P[13] | Digital video input | Digital Video Input Bus[35:0]. |
| U7 | GND | GND | Ground. |
| U8 | GND | GND | Ground. |
| U9 | DVDD | Power | Digital Power Supply (1.8 V). |
| U10 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|-----------------------|---|
| U11 | GND | GND | Ground. |
| U12 | DVDD | Power | Digital Power Supply (1.8 V). |
| U13 | GND | GND | Ground. |
| U14 | GND | GND | Ground. |
| U15 | DVDD | Power | Digital Power Supply (1.8 V). |
| U16 | GND | GND | Ground. |
| U17 | GND | GND | Ground. |
| U20 | NC | N/A | No Connect. Do not connect to this pin. |
| U21 | GND | GND | Ground. |
| U22 | NC | N/A | No Connect. Do not connect to this pin. |
| U23 | NC | N/A | No Connect. Do not connect to this pin. |
| V1 | P[6] | Digital video input | Digital Video Input Bus[35:0]. |
| V2 | P[7] | Digital video input | Digital Video Input Bus[35:0]. |
| V3 | P[8] | Digital video input | Digital Video Input Bus[35:0]. |
| V4 | P[9] | Digital video input | Digital Video Input Bus[35:0]. |
| V20 | GND | GND | Ground. |
| V21 | PVDD6 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| V22 | NC | N/A | No Connect. Do not connect to this pin. |
| V23 | NC | N/A | No Connect. Do not connect to this pin. |
| W1 | P[2] | Digital video input | Digital Video Input Bus[35:0]. |
| W2 | P[3] | Digital video input | Digital Video Input Bus[35:0]. |
| W3 | P[4] | Digital video input | Digital Video Input Bus[35:0]. |
| W4 | P[5] | Digital video input | Digital Video Input Bus[35:0]. |
| W20 | TEST3 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 0.1 μ F capacitor. |
| W21 | PVDD6 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| W22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| W23 | NC | N/A | No Connect. Do not connect to this pin. |
| Y1 | P[0] | Digital video input | Digital Video Input Bus[35:0]. |
| Y2 | P[1] | Digital video input | Digital Video Input Bus[35:0]. |
| Y3 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| Y4 | GND | GND | Ground. |
| Y5 | DDR_DQ[23] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| Y8 | GND | GND | Ground. |
| Y9 | DDR_A[11] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y11 | DDR_A[4] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y12 | GND | GND | Ground. |
| Y13 | DDR_CAS | DDR interface | Column Address Strobe for DDR Memory. |
| Y14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| Y16 | GND | GND | Ground. |
| Y17 | DDR_DQ[9] | DDR Interface | Data Line. Interface to external RAM data lines. |
| Y18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y19 | DDR_DQ[14] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y20 | GND | GND | Ground. |
| Y21 | DDR_DQ[6] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y22 | PVDD_DDR | Power | DDR Interface PLL Supply (1.8 V). |
| Y23 | GND | GND | Ground. |
| AA1 | DDR_DQ[18] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA2 | GND | GND | Ground. |
| AA3 | GND | GND | Ground. |
| AA4 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| AA5 | DDR_DQ[26] | DDR interface | Data Line. Interface to external RAM data lines. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|----------------|---|
| AA6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| AA8 | NC/GND | No connect/GND | For new ADV8003 designs, do not connect to this pin. For designs that must maintain consistency with the ADV8002, this pin can be grounded. |
| AA9 | DDR_A[8] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA11 | DDR_A[2] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA12 | GND | GND | Ground. |
| AA13 | DDR_CS | DDR interface | DDR Chip Select. Interface to external DDR RAM chip selects. |
| AA14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| AA16 | GND | GND | Ground. |
| AA17 | DDR_DQ[11] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA19 | DDR_DM[1] | DDR interface | Data Mask for Data Lines[15:8]. |
| AA20 | DDR_DM[0] | DDR interface | Data Mask for Data Lines[7:0]. |
| AA21 | GND | GND | Ground. |
| AA22 | GND | GND | Ground. |
| AA23 | DDR_DQ[3] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB1 | DDR_DQ[21] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB2 | DDR_DQ[19] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB3 | DDR_DQ[17] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB4 | DDR_DM[2] | DDR interface | Data Mask for Data Lines[23:16]. |
| AB5 | DDR_DQ[30] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB6 | DDR_DM[3] | DDR interface | Data Mask for Data Lines[31:25]. |
| AB7 | DDR_DQ[31] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB8 | DDR_DQ[29] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB9 | DDR_A[12] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB10 | DDR_A[6] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB11 | DDR_A[3] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB12 | DDR_A[0] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB13 | DDR_BA[0] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AB14 | DDR_RAS | DDR interface | Row Address Strobe for DDR Memory. |
| AB15 | DDR_CKE | DDR interface | Clock Enable for External DDR Memory. |
| AB16 | DDR_DQ[12] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB17 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AB18 | DDR_DQ[8] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB19 | DDR_DQ[13] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB20 | DDR_DQ[0] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB21 | DDR_DQ[5] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AB23 | DDR_DQ[4] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC1 | DDR_DQ[16] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC2 | DDR_DQ[20] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC3 | DDR_DQ[22] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC4 | DDR_DQ[25] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC5 | DDR_DQ[28] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC6 | DDR_DQ[27] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC7 | DDR_DQ[24] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC8 | DDR_A[9] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC9 | DDR_A[5] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC10 | DDR_A[7] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC11 | DDR_A[1] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC12 | DDR_A[10] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC13 | DDR_BA[1] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|----------------------------|--|
| AC14 | DDR_BA[2] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AC15 | DDR_WE | DDR interface | Write Enable Signal for DDR RAM. |
| AC16 | DDR_VREF | DDR interface ¹ | Reference Voltage for DDR RAM. |
| AC17 | DDR_DQ[10] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC18 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AC19 | DDR_DQ[15] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC20 | DDR_DQ[7] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC21 | DDR_DQ[2] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AC23 | DDR_DQ[1] | DDR interface | Data Line. Interface to external RAM data lines. |

¹ Sensitive node. Careful layout is important. Keep the associated circuitry as close as possible to the [ADV8003](#).

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | | |
|----|-----------------------|-----------------------|-----------------------|------------|------------|------------|------------|------------|-----------|----------|----------|-----------|-----------|-----------|---------|------------|------------|------------|------------|-----------|-----------|------------|-----------|---------|---|
| A | OSD_IN[23]/EXT_DIN[7] | OSD_DE- | OSD_CLK/EXT_CLK | AUD_IN[1] | AUD_IN[2] | AUD_IN[5] | ARC2_OUT | MOSI1 | SCK2 | CS2 | RESET | XTALN | PVDD2 | NC | NC | CVDD1 | RX_CN | RX_ON | RX_1N | RX_2N | CVDD1 | NC | NC | A | |
| B | OSD_IN[21]/EXT_DIN[5] | OSD_IN[22]/EXT_DIN[6] | OSD_VS | AUD_IN[0] | AUD_IN[3] | SFL | ARC1_OUT | MISO1 | MISO2 | MISO2 | ALS_B | XTALP | PVDD1 | NC | NC | GND | RX_CP | RX_OP | RX_1P | RX_2P | GND | NC | NC | B | |
| C | OSD_IN[19]/EXT_DIN[3] | OSD_IN[20]/EXT_DIN[4] | GND | AUD_IN[4] | DSD_CLK | SCLK | SCL | SCK1 | GND | INT0 | PDN | GND | GND | NC | NC | RX_HPD | AVDD1 | GND | GND | AVDD1 | AVDD1 | NC | NC | C | |
| D | OSD_IN[16]/EXT_DIN[0] | OSD_IN[17]/EXT_DIN[1] | OSD_IN[18]/EXT_DIN[2] | GND | DVDD_IO | MCLK | SDA | CS1 | GND | INT1 | INT2 | DVDD_IO | TEST1 | NC | NC | RX_5V | NC | NC | RTERM | AVDD2 | AVDD2 | NC | NC | D | |
| E | OSD_IN[13]/VBI_SCK | OSD_IN[14]/VBI_MOS | OSD_IN[15]/VBI_CS | DVDD_IO | | | | | | | | | | | | | | | | | TEST2 | GND | NC | NC | E |
| F | OSD_IN[9] | OSD_IN[10] | OSD_IN[11] | OSD_IN[12] | | | | | | | | | | | | | | | | | NC | PVDD3 | GND | CEC1 | F |
| G | OSD_IN[5] | OSD_IN[6] | OSD_IN[7] | OSD_IN[8] | | | GND | GND | GND | DVDD | GND | GND | DVDD | GND | GND | GND | GND | | | | ELPF1 | ELPF2 | GND | AVDD3 | G |
| H | OSD_IN[1] | OSD_IN[2] | OSD_IN[3] | OSD_IN[4] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | GND | GND | TX1_2+ | TX1_2- | H |
| J | DE | HS | OSD_HS | OSD_IN[0] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | | | | DDC1_SDA | GND | TX1_1+ | TX1_1- | J |
| K | VS | PCLK | DVDD_IO | DVDD_IO | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | DDC1_SCL | GND | TX1_0+ | TX1_0- | K |
| L | P[32] | P[33] | P[34] | P[35] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | HPD_TX1 | GND | TX1_C+ | TX1_C- | L |
| M | P[28] | P[29] | P[30] | P[31] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | R_TX1 | PVDD5 | HEAC_1+ | HEAC_1- | M |
| N | P[24] | P[25] | P[26] | P[27] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | CEC2 | PVDD5 | AVDD3 | NC | N |
| P | P[20] | P[21] | P[22] | P[23] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | | | | DDC2_SCL | GND | TX2_2+ | TX2_2- | P |
| R | P[16] | P[17] | P[18] | P[19] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | DDC2_SDA | GND | TX2_1+ | TX2_1- | R |
| T | P[14] | P[15] | GND | GND | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | HPD_TX2 | GND | TX2_0+ | TX2_0- | T |
| U | P[10] | P[11] | P[12] | P[13] | | | GND | GND | DVDD | GND | GND | DVDD | GND | GND | DVDD | GND | GND | | | | R_TX2 | GND | TX2_C+ | TX2_C- | U |
| V | P[6] | P[7] | P[8] | P[9] | | | | | | | | | | | | | | | | | GND | PVDD6 | HEAC_2+ | HEAC_2- | V |
| W | P[2] | P[3] | P[4] | P[5] | | | | | | | | | | | | | | | | | TEST3 | PVDD6 | AVDD3 | NC | W |
| Y | P[0] | P[1] | DDR_DQS[2] | GND | DDR_DQ[23] | DVDD_DDR | DDR_DQS[3] | GND | DDR_A[11] | DVDD_DDR | DDR_A[4] | GND | DDR_CAS | DVDD_DDR | DDR_CK | GND | DDR_DQ[9] | DVDD_DDR | DDR_DQ[14] | GND | DDR_DQ[6] | PVDD_DDR | GND | Y | |
| AA | DDR_DQ[18] | GND | GND | DDR_DQS[2] | DDR_DQ[26] | DVDD_DDR | DDR_DQS[3] | NC/GND | DDR_A[8] | DVDD_DDR | DDR_A[2] | GND | DDR_CS | DVDD_DDR | DDR_CK | GND | DDR_DQ[11] | DVDD_DDR | DDR_DM[1] | DDR_DM[0] | GND | GND | DDR_DQ[3] | AA | |
| AB | DDR_DQ[21] | DDR_DQ[19] | DDR_DM[17] | DDR_DM[2] | DDR_DQ[30] | DDR_DM[3] | DDR_DQ[31] | DDR_DQ[29] | DDR_A[12] | DDR_A[6] | DDR_A[3] | DDR_A[0] | DDR_BA[0] | DDR_RAS | DDR_CKE | DDR_DQ[12] | DDR_DQS[1] | DDR_DQ[8] | DDR_DQ[13] | DDR_DQ[0] | DDR_DQ[5] | DDR_DQS[0] | DDR_DQ[4] | AB | |
| AC | DDR_DQ[16] | DDR_DQ[20] | DDR_DQ[22] | DDR_DQ[25] | DDR_DQ[28] | DDR_DQ[27] | DDR_DQ[24] | DDR_A[9] | DDR_A[5] | DDR_A[7] | DDR_A[1] | DDR_A[10] | DDR_BA[1] | DDR_BA[2] | DDR_WE | DDR_VREF | DDR_DQ[10] | DDR_DQS[1] | DDR_DQ[15] | DDR_DQ[7] | DDR_DQ[2] | DDR_DQS[0] | DDR_DQ[1] | AC | |

Figure 31. ADV8003KBCZ-8C and ADV8003KBCZ-7C Pin Configuration

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Table 8. ADV8003KBCZ-8C and ADV8003KBCZ-7C Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|--|
| A1 | OSD_IN[23]/EXT_DIN[7] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[23])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[7]). |
| A2 | OSD_DE | OSD video sync | Data Enable for the OSD Input Port. |
| A3 | OSD_CLK/EXT_CLK | OSD video sync | Pixel Clock for the OSD Input Port (OSD_CLK)/Pixel Clock for External Video Data (EXT_CLK). |
| A4 | AUD_IN[1] | Audio input | I ² S0/DSD1 Audio Input. |
| A5 | AUD_IN[2] | Audio input | I ² S1/DSD2 Audio Input. |
| A6 | AUD_IN[5] | Audio input | LRCLK/DSD5 Audio Input. |
| A7 | ARC2_OUT | Audio output | Audio Return Channel for HDMI Tx2. |
| A8 | MOSI1 | Serial port control | Master Out Slave In (Serial Port 1). Serial Port 1 is used for OSD control. |
| A9 | SCK2 | Serial port control | Serial Clock (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A10 | CS2 | Serial port control | Chip Select (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A11 | RESET | Miscellaneous digital | Reset Pin. |
| A12 | XTALN | Miscellaneous digital ¹ | Crystal Input. |
| A13 | PVDD2 | Power | PLL Digital Supply Voltage (1.8 V). |
| A14 | NC | N/A | No Connect. Do not connect to this pin. |
| A15 | NC | N/A | No Connect. Do not connect to this pin. |
| A16 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A17 | RX_CN | Rx input | Rx Clock Complement Input. |
| A18 | RX_ON | Rx input | Rx Channel 0 Complement Input. |
| A19 | RX_1N | Rx input | Rx Channel 1 Complement Input. |
| A20 | RX_2N | Rx input | Rx Channel 2 Complement Input. |
| A21 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A22 | NC | N/A | No Connect. Do not connect to this pin. |
| A23 | NC | N/A | No Connect. Do not connect to this pin. |
| B1 | OSD_IN[21]/EXT_DIN[5] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[21])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[5]). |
| B2 | OSD_IN[22]/EXT_DIN[6] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[22])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[6]). |
| B3 | OSD_VS | OSD video sync | Vertical Sync for the OSD Input Port. |
| B4 | AUD_IN[0] | Audio input | S/PDIF/DSD0 Audio Input. |
| B5 | AUD_IN[3] | Audio input | I ² S2/DSD3 Audio Input. |
| B6 | SFL | SFL | Subcarrier Frequency Lock Signal (SFL). |
| B7 | ARC1_OUT | Audio output | Audio Return Channel for HDMI Tx1. |
| B8 | MISO1 | Serial port control | Master In Slave Out (Serial Port 1). Serial Port 1 is used for OSD control. |
| B9 | MOSI2 | Serial port control | Master Out Slave In (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B10 | MISO2 | Serial port control | Master In Slave Out (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B11 | ALSB | I ² C control | Sets LSB of I ² C address. When the ALSB pin is set low, the I ² C address is 0x18; when the ALSB pin is set high, the I ² C address is 0x1A. |
| B12 | XTALP | Miscellaneous digital ¹ | Crystal Input. |
| B13 | PVDD1 | Power | PLL Analog Supply Voltage (1.8 V). |
| B14 | NC | N/A | No Connect. Do not connect to this pin. |
| B15 | NC | N/A | No Connect. Do not connect to this pin. |
| B16 | GND | GND | Ground. |
| B17 | RX_CP | Rx input | Rx Clock True Input. |
| B18 | RX_OP | Rx input | Rx Channel 0 True Input. |
| B19 | RX_1P | Rx input | Rx Channel 1 True Input. |
| B20 | RX_2P | Rx input | Rx Channel 2 True Input. |
| B21 | GND | GND | Ground. |
| B22 | NC | N/A | No Connect. Do not connect to this pin. |
| B23 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|--|
| C1 | OSD_IN[19]/EXT_DIN[3] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[19])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[3]). |
| C2 | OSD_IN[20]/EXT_DIN[4] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[20])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[4]). |
| C3 | GND | GND | Ground. |
| C4 | AUD_IN[4] | Audio input | I ² S3/DSD4 Audio Input. |
| C5 | DSD_CLK | Audio input | DSD Audio Clock Input. |
| C6 | SCLK | Audio input | I ² S Bit Clock Input. |
| C7 | SCL | I ² C control | I ² C Clock Input. SCL is open drain; use a 4.7 k Ω resistor to connect this pin to a 3.3 V supply. |
| C8 | SCK1 | Serial port control | Serial Clock (Serial Port 1). Serial Port 1 is used for OSD control. |
| C9 | GND | GND | Ground. |
| C10 | INT0 | Miscellaneous digital | Interrupt Pin 0. When status bits change, this pin is triggered. |
| C11 | PDN | Miscellaneous digital | Power-Down. This pin controls the power state of the ADV8003. |
| C12 | GND | GND | Ground. |
| C13 | GND | GND | Ground. |
| C14 | NC | N/A | No Connect. Do not connect to this pin. |
| C15 | NC | N/A | No Connect. Do not connect to this pin. |
| C16 | RX_HPD | Rx input | Hot Plug Assert Signal Output for the Rx Input. |
| C17 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C18 | GND | GND | Ground. |
| C19 | GND | GND | Ground. |
| C20 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C21 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C22 | NC | N/A | No Connect. Do not connect to this pin. |
| C23 | NC | N/A | No Connect. Do not connect to this pin. |
| D1 | OSD_IN[16]/EXT_DIN[0] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[16])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[0]). |
| D2 | OSD_IN[17]/EXT_DIN[1] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[17])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[1]). |
| D3 | OSD_IN[18]/EXT_DIN[2] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[18])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[2]). |
| D4 | GND | GND | Ground. |
| D5 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D6 | MCLK | Audio input | MCLK for S/PDIF Input Audio. |
| D7 | SDA | I ² C control | I ² C Data Input. SDA is open drain; use a 4.7 k Ω resistor to connect this pin to a 3.3 V supply. |
| D8 | CS1 | Serial port control | Chip Select (Serial Port 1). Serial Port 1 is used for OSD control. |
| D9 | GND | GND | Ground. |
| D10 | INT1 | Miscellaneous digital | Interrupt Pin for HDMI Transmitter Outputs. When status bits change, an interrupt is generated on this pin. |
| D11 | INT2 | Miscellaneous digital | Interrupt Pin for HDMI Receiver Input Lines. When status bits change, an interrupt is generated on this pin. |
| D12 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D13 | TEST1 | Miscellaneous digital | Test Pin. Float this pin. |
| D14 | NC | N/A | No Connect. Do not connect to this pin. |
| D15 | NC | N/A | No Connect. Do not connect to this pin. |
| D16 | RX_5V | Rx input | 5 V Detect Pin for the Rx Input. |
| D17 | NC | N/A | No Connect. Do not connect to this pin. |
| D18 | NC | N/A | No Connect. Do not connect to this pin. |
| D19 | RTERM | HDMI Rx input | This pin sets internal termination resistance. Use a 500 Ω resistor between this pin and GND. Place the RTERM resistor as close as possible to the ADV8003. |
| D20 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D21 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D22 | NC | N/A | No Connect. Do not connect to this pin. |
| D23 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|---------------------|---|---|
| E1 | OSD_IN[13]/VBI_SCK | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[13])/Serial Clock for VBI Data Serial Port (VBI_SCK). |
| E2 | OSD_IN[14]/VBI_MOSI | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[14])/Master Out Slave In for VBI Data Serial Port (VBI_MOSI). |
| E3 | OSD_IN[15]/VBI_CS | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[15])/Chip Select for VBI Data Serial Port (VBI_CS). |
| E4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| E20 | TEST2 | Miscellaneous analog | Test Pin. Float this pin. |
| E21 | GND | GND | Ground. |
| E22 | NC | N/A | No Connect. Do not connect to this pin. |
| E23 | NC | N/A | No Connect. Do not connect to this pin. |
| F1 | OSD_IN[9] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[9]). |
| F2 | OSD_IN[10] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[10]). |
| F3 | OSD_IN[11] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[11]). |
| F4 | OSD_IN[12] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[12]). |
| F20 | NC | N/A | No Connect. Do not connect to this pin. |
| F21 | PVDD3 | Power | PLL Supply (1.8 V). |
| F22 | GND | GND | Ground. |
| F23 | CEC1 | HDMI Tx1 | HDMI Tx1 Consumer Electronics Control (CEC). |
| G1 | OSD_IN[5] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[5]). |
| G2 | OSD_IN[6] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[6]). |
| G3 | OSD_IN[7] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[7]). |
| G4 | OSD_IN[8] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[8]). |
| G7 | GND | GND | Ground. |
| G8 | GND | GND | Ground. |
| G9 | GND | GND | Ground. |
| G10 | DVDD | Power | Digital Power Supply (1.8 V). |
| G11 | GND | GND | Ground. |
| G12 | GND | GND | Ground. |
| G13 | DVDD | Power | Digital Power Supply (1.8 V). |
| G14 | GND | GND | Ground. |
| G15 | GND | GND | Ground. |
| G16 | GND | GND | Ground. |
| G17 | GND | GND | Ground. |
| G20 | ELPF1 | Miscellaneous analog ¹ | External Loop Filter for PLL 1. Connect to PVDD3. |
| G21 | ELPF2 | Miscellaneous analog ¹ | External Loop Filter for PLL 2. Connect to PVDD3. |
| G22 | GND | GND | Ground. |
| G23 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| H1 | OSD_IN[1] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[1]). |
| H2 | OSD_IN[2] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[2]). |
| H3 | OSD_IN[3] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[3]). |
| H4 | OSD_IN[4] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[4]). |
| H7 | GND | GND | Ground. |
| H8 | GND | GND | Ground. |
| H9 | GND | GND | Ground. |
| H10 | GND | GND | Ground. |
| H11 | GND | GND | Ground. |
| H12 | GND | GND | Ground. |
| H13 | GND | GND | Ground. |
| H14 | GND | GND | Ground. |
| H15 | GND | GND | Ground. |
| H16 | GND | GND | Ground. |
| H17 | GND | GND | Ground. |
| H20 | GND | GND | Ground. |
| H21 | GND | GND | Ground. |
| H22 | TX1_2+ | HDMI Tx1 | HDMI1 Channel 2 True Output. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------|---------------------|--|
| H23 | TX1_2- | HDMI Tx1 | HDMI1 Channel 2 Complementary Output. |
| J1 | DE | Digital video sync | Data Enable for Digital Input Video. |
| J2 | HS | Digital video sync | Horizontal Sync for Digital Input Video. |
| J3 | OSD_HS | Digital video sync | Horizontal Sync for the OSD Input Port (OSD_HS). |
| J4 | OSD_IN[0] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[0]). |
| J7 | DVDD | Power | Digital Power Supply (1.8 V). |
| J8 | GND | GND | Ground. |
| J9 | GND | GND | Ground. |
| J10 | GND | GND | Ground. |
| J11 | GND | GND | Ground. |
| J12 | GND | GND | Ground. |
| J13 | GND | GND | Ground. |
| J14 | GND | GND | Ground. |
| J15 | GND | GND | Ground. |
| J16 | GND | GND | Ground. |
| J17 | DVDD | Power | Digital Power Supply (1.8 V). |
| J20 | DDC1_SDA | HDMI Tx1 | HDCP Slave Serial Data for HDMI Tx1. This pin is open drain; use a 2 k Ω resistor to connect this pin to the HDMI Tx 5 V supply. |
| J21 | GND | GND | Ground. |
| J22 | TX1_1+ | HDMI Tx1 | HDMI1 Channel 1 True Output. |
| J23 | TX1_1- | HDMI Tx1 | HDMI1 Channel 1 Complementary Output. |
| K1 | VS | Digital video sync | Vertical Sync for Digital Input Video. |
| K2 | PCLK | Digital video sync | Pixel Clock for Digital Input Video. |
| K3 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K7 | GND | GND | Ground. |
| K8 | GND | GND | Ground. |
| K9 | GND | GND | Ground. |
| K10 | GND | GND | Ground. |
| K11 | GND | GND | Ground. |
| K12 | GND | GND | Ground. |
| K13 | GND | GND | Ground. |
| K14 | GND | GND | Ground. |
| K15 | GND | GND | Ground. |
| K16 | GND | GND | Ground. |
| K17 | GND | GND | Ground. |
| K20 | DDC1_SCL | HDMI Tx1 | HDCP Slave Serial Clock for HDMI Tx1. This pin is open drain; use a 2 k Ω resistor to connect this pin to the HDMI Tx 5 V supply. |
| K21 | GND | GND | Ground. |
| K22 | TX1_0+ | HDMI Tx1 | HDMI1 Channel 0 True Output. |
| K23 | TX1_0- | HDMI Tx1 | HDMI1 Channel 0 Complementary Output. |
| L1 | P[32] | Digital video input | Digital Video Input Bus[35:0]. |
| L2 | P[33] | Digital video input | Digital Video Input Bus[35:0]. |
| L3 | P[34] | Digital video input | Digital Video Input Bus[35:0]. |
| L4 | P[35] | Digital video input | Digital Video Input Bus[35:0]. |
| L7 | DVDD | Power | Digital Power Supply (1.8 V). |
| L8 | GND | GND | Ground. |
| L9 | GND | GND | Ground. |
| L10 | GND | GND | Ground. |
| L11 | GND | GND | Ground. |
| L12 | GND | GND | Ground. |
| L13 | GND | GND | Ground. |
| L14 | GND | GND | Ground. |
| L15 | GND | GND | Ground. |
| L16 | GND | GND | Ground. |
| L17 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|-----------------------|---|
| L20 | HPD_TX1 | HDMI Tx1 | Hot Plug Assert Signal Input for HDMI Tx1. |
| L21 | GND | GND | Ground. |
| L22 | TX1_C+ | HDMI Tx1 | HDMI1 Clock True Output. |
| L23 | TX1_C- | HDMI Tx1 | HDMI1 Clock Complementary Output. |
| M1 | P[28] | Digital video input | Digital Video Input Bus[35:0]. |
| M2 | P[29] | Digital video input | Digital Video Input Bus[35:0]. |
| M3 | P[30] | Digital video input | Digital Video Input Bus[35:0]. |
| M4 | P[31] | Digital video input | Digital Video Input Bus[35:0]. |
| M7 | GND | GND | Ground. |
| M8 | GND | GND | Ground. |
| M9 | GND | GND | Ground. |
| M10 | GND | GND | Ground. |
| M11 | GND | GND | Ground. |
| M12 | GND | GND | Ground. |
| M13 | GND | GND | Ground. |
| M14 | GND | GND | Ground. |
| M15 | GND | GND | Ground. |
| M16 | GND | GND | Ground. |
| M17 | GND | GND | Ground. |
| M20 | R_TX1 | HDMI Tx1 ¹ | Sets Internal Reference Currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground. The external resistor should be placed as close as possible to the ADV8003. |
| M21 | PVDD5 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| M22 | HEAC_1+ | HDMI Tx1 | HDMI Tx1 HEAC+ from HDMI Connector. |
| M23 | HEAC_1- | HDMI Tx1 | HDMI Tx1 HEAC- from HDMI Connector. |
| N1 | P[24] | Digital video input | Digital Video Input Bus[35:0]. |
| N2 | P[25] | Digital video input | Digital Video Input Bus[35:0]. |
| N3 | P[26] | Digital video input | Digital Video Input Bus[35:0]. |
| N4 | P[27] | Digital video input | Digital Video Input Bus[35:0]. |
| N7 | GND | GND | Ground. |
| N8 | GND | GND | Ground. |
| N9 | GND | GND | Ground. |
| N10 | GND | GND | Ground. |
| N11 | GND | GND | Ground. |
| N12 | GND | GND | Ground. |
| N13 | GND | GND | Ground. |
| N14 | GND | GND | Ground. |
| N15 | GND | GND | Ground. |
| N16 | GND | GND | Ground. |
| N17 | GND | GND | Ground. |
| N20 | CEC2 | HDMI Tx2 | HDMI Tx2 Consumer Electronics Control (CEC). |
| N21 | PVDD5 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| N22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| N23 | NC | N/A | No Connect. Do not connect to this pin. |
| P1 | P[20] | Digital video input | Digital Video Input Bus[35:0]. |
| P2 | P[21] | Digital video input | Digital Video Input Bus[35:0]. |
| P3 | P[22] | Digital video input | Digital Video Input Bus[35:0]. |
| P4 | P[23] | Digital video input | Digital Video Input Bus[35:0]. |
| P7 | DVDD | Power | Digital Power Supply (1.8 V). |
| P8 | GND | GND | Ground. |
| P9 | GND | GND | Ground. |
| P10 | GND | GND | Ground. |
| P11 | GND | GND | Ground. |
| P12 | GND | GND | Ground. |
| P13 | GND | GND | Ground. |
| P14 | GND | GND | Ground. |
| P15 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|---------------------|--|
| P16 | GND | GND | Ground. |
| P17 | DVDD | Power | Digital Power Supply (1.8 V). |
| P20 | DDC2_SCL | HDMI Tx2 | HDCP Slave Serial Clock for HDMI Tx2. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI Tx 5 V supply. |
| P21 | GND | GND | Ground. |
| P22 | TX2_2+ | HDMI Tx2 | HDMI2 Channel 2 True Output. |
| P23 | TX2_2- | HDMI Tx2 | HDMI2 Channel 2 Complementary Output. |
| R1 | P[16] | Digital video input | Digital Video Input Bus[35:0]. |
| R2 | P[17] | Digital video input | Digital Video Input Bus[35:0]. |
| R3 | P[18] | Digital video input | Digital Video Input Bus[35:0]. |
| R4 | P[19] | Digital video input | Digital Video Input Bus[35:0]. |
| R7 | GND | GND | Ground. |
| R8 | GND | GND | Ground. |
| R9 | GND | GND | Ground. |
| R10 | GND | GND | Ground. |
| R11 | GND | GND | Ground. |
| R12 | GND | GND | Ground. |
| R13 | GND | GND | Ground. |
| R14 | GND | GND | Ground. |
| R15 | GND | GND | Ground. |
| R16 | GND | GND | Ground. |
| R17 | GND | GND | Ground. |
| R20 | DDC2_SDA | HDMI Tx2 | HDCP Slave Serial Data for HDMI Tx2. This pin is open drain; use a 2 kΩ resistor to connect this pin to the HDMI Tx 5 V supply. |
| R21 | GND | GND | Ground. |
| R22 | TX2_1+ | HDMI Tx2 | HDMI2 Channel 1 True Output. |
| R23 | TX2_1- | HDMI Tx2 | HDMI2 Channel 1 Complementary Output. |
| T1 | P[14] | Digital video input | Digital Video Input Bus[35:0]. |
| T2 | P[15] | Digital video input | Digital Video Input Bus[35:0]. |
| T3 | GND | GND | Ground. |
| T4 | GND | GND | Ground. |
| T7 | GND | GND | Ground. |
| T8 | GND | GND | Ground. |
| T9 | GND | GND | Ground. |
| T10 | GND | GND | Ground. |
| T11 | GND | GND | Ground. |
| T12 | GND | GND | Ground. |
| T13 | GND | GND | Ground. |
| T14 | GND | GND | Ground. |
| T15 | GND | GND | Ground. |
| T16 | GND | GND | Ground. |
| T17 | GND | GND | Ground. |
| T20 | HPD_TX2 | HDMI Tx2 | Hot Plug Assert Signal Input for HDMI Tx2. |
| T21 | GND | GND | Ground. |
| T22 | TX2_0+ | HDMI Tx2 | HDMI2 Channel 0 True Output. |
| T23 | TX2_0- | HDMI Tx2 | HDMI2 Channel 0 Complementary Output. |
| U1 | P[10] | Digital video input | Digital Video Input Bus[35:0]. |
| U2 | P[11] | Digital video input | Digital Video Input Bus[35:0]. |
| U3 | P[12] | Digital video input | Digital Video Input Bus[35:0]. |
| U4 | P[13] | Digital video input | Digital Video Input Bus[35:0]. |
| U7 | GND | GND | Ground. |
| U8 | GND | GND | Ground. |
| U9 | DVDD | Power | Digital Power Supply (1.8 V). |
| U10 | GND | GND | Ground. |
| U11 | GND | GND | Ground. |
| U12 | DVDD | Power | Digital Power Supply (1.8 V). |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|-----------------------|--|
| U13 | GND | GND | Ground. |
| U14 | GND | GND | Ground. |
| U15 | DVDD | Power | Digital Power Supply (1.8 V). |
| U16 | GND | GND | Ground. |
| U17 | GND | GND | Ground. |
| U20 | R_TX2 | HDMI Tx2 ¹ | Sets internal reference currents. Place a 470 Ω resistor (1% tolerance) between this pin and ground, as close as possible to the ADV8003. |
| U21 | GND | GND | Ground. |
| U22 | TX2_C+ | HDMI Tx2 | HDMI2 Clock True Output. |
| U23 | TX2_C- | HDMI Tx2 | HDMI2 Clock Complementary Output. |
| V1 | P[6] | Digital video input | Digital Video Input Bus[35:0]. |
| V2 | P[7] | Digital video input | Digital Video Input Bus[35:0]. |
| V3 | P[8] | Digital video input | Digital Video Input Bus[35:0]. |
| V4 | P[9] | Digital video input | Digital Video Input Bus[35:0]. |
| V20 | GND | GND | Ground. |
| V21 | PVDD6 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| V22 | HEAC_2+ | HDMI Tx2 | HDMI Tx2 HEC+ from the HDMI Connector. |
| V23 | HEAC_2- | HDMI Tx2 | HDMI Tx2 HEC- from the HDMI Connector. |
| W1 | P[2] | Digital video input | Digital Video Input Bus[35:0]. |
| W2 | P[3] | Digital video input | Digital Video Input Bus[35:0]. |
| W3 | P[4] | Digital video input | Digital Video Input Bus[35:0]. |
| W4 | P[5] | Digital video input | Digital Video Input Bus[35:0]. |
| W20 | TEST3 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 0.1 μ F capacitor. |
| W21 | PVDD6 | Power ¹ | HDMI Tx PLL Power Supply (1.8 V). |
| W22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| W23 | NC | N/A | No Connect. Do not connect to this pin. |
| Y1 | P[0] | Digital video input | Digital Video Input Bus[35:0]. |
| Y2 | P[1] | Digital video input | Digital Video Input Bus[35:0]. |
| Y3 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| Y4 | GND | GND | Ground. |
| Y5 | DDR_DQ[23] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| Y8 | GND | GND | Ground. |
| Y9 | DDR_A[11] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y11 | DDR_A[4] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y12 | GND | GND | Ground. |
| Y13 | DDR_CAS | DDR interface | Column Address Strobe for DDR Memory. |
| Y14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| Y16 | GND | GND | Ground. |
| Y17 | DDR_DQ[9] | DDR Interface | Data Line. Interface to external RAM data lines. |
| Y18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y19 | DDR_DQ[14] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y20 | GND | GND | Ground. |
| Y21 | DDR_DQ[6] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y22 | PVDD_DDR | Power | DDR Interface PLL Supply (1.8 V). |
| Y23 | GND | GND | Ground. |
| AA1 | DDR_DQ[18] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA2 | GND | GND | Ground. |
| AA3 | GND | GND | Ground. |
| AA4 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| AA5 | DDR_DQ[26] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|----------------------------|---|
| AA8 | NC/GND | No connect/GND | For new ADV8003 designs, do not connect to this pin. For designs that must maintain consistency with the ADV8002, this pin can be grounded. |
| AA9 | DDR_A[8] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA11 | DDR_A[2] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA12 | GND | GND | Ground. |
| AA13 | DDR_ \overline{CS} | DDR interface | DDR Chip Select. Interface to external DDR RAM chip selects. |
| AA14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| AA16 | GND | GND | Ground. |
| AA17 | DDR_DQ[11] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA19 | DDR_DM[1] | DDR interface | Data Mask for Data Lines[15:8]. |
| AA20 | DDR_DM[0] | DDR interface | Data Mask for Data Lines[7:0]. |
| AA21 | GND | GND | Ground. |
| AA22 | GND | GND | Ground. |
| AA23 | DDR_DQ[3] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB1 | DDR_DQ[21] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB2 | DDR_DQ[19] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB3 | DDR_DQ[17] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB4 | DDR_DM[2] | DDR interface | Data Mask for Data Lines[23:16]. |
| AB5 | DDR_DQ[30] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB6 | DDR_DM[3] | DDR interface | Data Mask for Data Lines[31:25]. |
| AB7 | DDR_DQ[31] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB8 | DDR_DQ[29] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB9 | DDR_A[12] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB10 | DDR_A[6] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB11 | DDR_A[3] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB12 | DDR_A[0] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB13 | DDR_BA[0] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AB14 | DDR_ \overline{RAS} | DDR interface | Row Address Strobe for DDR Memory. |
| AB15 | DDR_CKE | DDR interface | Clock Enable for External DDR Memory. |
| AB16 | DDR_DQ[12] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB17 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AB18 | DDR_DQ[8] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB19 | DDR_DQ[13] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB20 | DDR_DQ[0] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB21 | DDR_DQ[5] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AB23 | DDR_DQ[4] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC1 | DDR_DQ[16] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC2 | DDR_DQ[20] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC3 | DDR_DQ[22] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC4 | DDR_DQ[25] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC5 | DDR_DQ[28] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC6 | DDR_DQ[27] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC7 | DDR_DQ[24] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC8 | DDR_A[9] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC9 | DDR_A[5] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC10 | DDR_A[7] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC11 | DDR_A[1] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC12 | DDR_A[10] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC13 | DDR_BA[1] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AC14 | DDR_BA[2] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AC15 | DDR_ \overline{WE} | DDR interface | Write Enable Signal for DDR RAM. |
| AC16 | DDR_VREF | DDR interface ¹ | Reference Voltage for DDR RAM. |

| Pin No. | Mnemonic | Type | Description |
|---------|------------|---------------|--|
| AC17 | DDR_DQ[10] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC18 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AC19 | DDR_DQ[15] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC20 | DDR_DQ[7] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC21 | DDR_DQ[2] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AC23 | DDR_DQ[1] | DDR interface | Data Line. Interface to external RAM data lines. |

¹ Sensitive node. Careful layout is important. Keep the associated circuitry as close as possible to the [ADV8003](#).

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | | |
|----|-----------------------|-----------------------|-----------------------|------------|------------|------------|------------|------------|-----------|----------|----------|-----------|-----------|-----------|---------|------------|------------|------------|------------|-----------|-----------|------------|-----------|-------|---|
| A | OSD_IN[23]/EXT_DIN[7] | OSD_DE | OSD_CLK/EXT_CLK | TEST4 | TEST5 | TEST6 | TEST7 | MOSI1 | SCK2 | CS2 | RESET | XTALN | PVDD2 | NC | NC | CVDD1 | RX_CN | RX_ON | RX_1N | RX_2N | CVDD1 | NC | NC | A | |
| B | OSD_IN[21]/EXT_DIN[5] | OSD_IN[22]/EXT_DIN[6] | OSD_VS | TEST8 | TEST9 | TEST10 | TEST11 | MISO1 | MISO2 | MISO2 | ALS_B | XTALP | PVDD1 | NC | NC | GND | RX_CP | RX_OP | RX_1P | RX_2P | GND | NC | NC | B | |
| C | OSD_IN[19]/EXT_DIN[3] | OSD_IN[20]/EXT_DIN[4] | GND | TEST12 | TEST13 | TEST14 | SCL | SCK1 | GND | INT0 | PDN | GND | GND | NC | NC | RX_HPD | AVDD1 | GND | GND | AVDD1 | AVDD1 | NC | NC | C | |
| D | OSD_IN[16]/EXT_DIN[0] | OSD_IN[17]/EXT_DIN[1] | OSD_IN[18]/EXT_DIN[2] | GND | DVDD_IO | TEST15 | SDA | CS1 | GND | TEST16 | INT2 | DVDD_IO | TEST1 | NC | NC | RX_5V | NC | NC | RTERM | AVDD2 | AVDD2 | NC | NC | D | |
| E | OSD_IN[13]/VBI_SCK | OSD_IN[14]/VBI_MOS | OSD_IN[15]/VBI_CS | DVDD_IO | | | | | | | | | | | | | | | | TEST2 | GND | NC | NC | E | |
| F | OSD_IN[9] | OSD_IN[10] | OSD_IN[11] | OSD_IN[12] | | | | | | | | | | | | | | | | | NC | PVDD3 | GND | NC | F |
| G | OSD_IN[5] | OSD_IN[6] | OSD_IN[7] | OSD_IN[8] | | | GND | GND | GND | DVDD | GND | GND | DVDD | GND | GND | GND | GND | | | | ELPF1 | ELPF2 | GND | AVDD3 | G |
| H | OSD_IN[1] | OSD_IN[2] | OSD_IN[3] | OSD_IN[4] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | GND | GND | NC | NC | H |
| J | DE | HS | OSD_HS | OSD_IN[0] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | | | | NC | GND | NC | NC | J |
| K | VS | PCLK | DVDD_IO | DVDD_IO | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | GND | NC | NC | K |
| L | P[32] | P[33] | P[34] | P[35] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | GND | NC | NC | L |
| M | P[28] | P[29] | P[30] | P[31] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | PVDD5 | NC | NC | M |
| N | P[24] | P[25] | P[26] | P[27] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | PVDD5 | AVDD3 | NC | N |
| P | P[20] | P[21] | P[22] | P[23] | | | DVDD | GND | GND | GND | GND | GND | GND | GND | GND | GND | DVDD | | | | NC | GND | NC | NC | P |
| R | P[16] | P[17] | P[18] | P[19] | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | GND | NC | NC | R |
| T | P[14] | P[15] | GND | GND | | | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | GND | | | | NC | GND | NC | NC | T |
| U | P[10] | P[11] | P[12] | P[13] | | | GND | GND | DVDD | GND | GND | DVDD | GND | GND | DVDD | GND | GND | | | | NC | GND | NC | NC | U |
| V | P[6] | P[7] | P[8] | P[9] | | | | | | | | | | | | | | | | | GND | PVDD6 | NC | NC | V |
| W | P[2] | P[3] | P[4] | P[5] | | | | | | | | | | | | | | | | | TEST3 | PVDD6 | AVDD3 | NC | W |
| Y | P[0] | P[1] | DDR_DQS[2] | GND | DDR_DQ[23] | DVDD_DDR | DDR_DQS[3] | GND | DDR_A[11] | DVDD_DDR | DDR_A[4] | GND | DDR_CAS | DVDD_DDR | DDR_CK | GND | DDR_DQ[9] | DVDD_DDR | DDR_DQ[14] | GND | DDR_DQ[6] | PVDD_DDR | GND | Y | |
| AA | DDR_DQ[18] | GND | GND | DDR_DQS[2] | DDR_DQ[26] | DVDD_DDR | DDR_DQS[3] | NC/GND | DDR_A[8] | DVDD_DDR | DDR_A[2] | GND | DDR_CS | DVDD_DDR | DDR_CK | GND | DDR_DQ[11] | DVDD_DDR | DDR_DM[1] | DDR_DM[0] | GND | GND | DDR_DQ[3] | AA | |
| AB | DDR_DQ[21] | DDR_DQ[19] | DDR_DQ[17] | DDR_DM[2] | DDR_DQ[30] | DDR_DM[3] | DDR_DQ[31] | DDR_DQ[29] | DDR_A[12] | DDR_A[6] | DDR_A[3] | DDR_A[0] | DDR_BA[0] | DDR_RAS | DDR_CKE | DDR_DQ[12] | DDR_DQS[1] | DDR_DQ[8] | DDR_DQ[13] | DDR_DQ[0] | DDR_DQ[5] | DDR_DQS[0] | DDR_DQ[4] | AB | |
| AC | DDR_DQ[16] | DDR_DQ[20] | DDR_DQ[22] | DDR_DQ[25] | DDR_DQ[28] | DDR_DQ[27] | DDR_DQ[24] | DDR_A[9] | DDR_A[5] | DDR_A[7] | DDR_A[1] | DDR_A[10] | DDR_BA[1] | DDR_BA[2] | DDR_WE | DDR_VREF | DDR_DQ[10] | DDR_DQS[1] | DDR_DQ[15] | DDR_DQ[7] | DDR_DQ[2] | DDR_DQS[0] | DDR_DQ[1] | AC | |

Figure 32. ADV8003KBCZ-7T Pin Configuration

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Table 9. ADV8003KBCZ-7T Pin Function Descriptions

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|--|
| A1 | OSD_IN[23]/EXT_DIN[7] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[23])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[7]). |
| A2 | OSD_DE | OSD video sync | Data Enable for the OSD Input Port. |
| A3 | OSD_CLK/EXT_CLK | OSD video sync | Pixel Clock for the OSD Input Port (OSD_CLK)/Pixel Clock for External Video Data (EXT_CLK). |
| A4 | TEST4 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| A5 | TEST5 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| A6 | TEST6 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| A7 | TEST7 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| A8 | MOSI1 | Serial port control | Master Out Slave In (Serial Port 1). Serial Port 1 is used for OSD control. |
| A9 | SCK2 | Serial port control | Serial Clock (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A10 | CS2 | Serial port control | Chip Select (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| A11 | RESET | Miscellaneous digital | Reset Pin. |
| A12 | XTALN | Miscellaneous digital ¹ | Crystal Input. |
| A13 | PVDD2 | Power | PLL Digital Supply Voltage (1.8 V). |
| A14 | NC | N/A | No Connect. Do not connect to this pin. |
| A15 | NC | N/A | No Connect. Do not connect to this pin. |
| A16 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A17 | RX_CN | Rx input | Rx Clock Complement Input. |
| A18 | RX_0N | Rx input | Rx Channel 0 Complement Input. |
| A19 | RX_1N | Rx input | Rx Channel 1 Complement Input. |
| A20 | RX_2N | Rx input | Rx Channel 2 Complement Input. |
| A21 | CVDD1 | Power | Comparator Supply Voltage (1.8 V). |
| A22 | NC | N/A | No Connect. Do not connect to this pin. |
| A23 | NC | N/A | No Connect. Do not connect to this pin. |
| B1 | OSD_IN[21]/EXT_DIN[5] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[21])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[5]). |
| B2 | OSD_IN[22]/EXT_DIN[6] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[22])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[6]). |
| B3 | OSD_VS | OSD video sync | Vertical Sync for the OSD Input Port. |
| B4 | TEST8 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| B5 | TEST9 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| B6 | TEST10 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| B7 | TEST11 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| B8 | MISO1 | Serial port control | Master In Slave Out (Serial Port 1). Serial Port 1 is used for OSD control. |
| B9 | MOSI2 | Serial port control | Master Out Slave In (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B10 | MISO2 | Serial port control | Master In Slave Out (Serial Port 2). Serial Port 2 is used for the external flash ROM. |
| B11 | ALSB | I ² C control | Sets LSB of I ² C address. When the ALSB pin is set low, the I ² C address is 0x18; when the ALSB pin is set high, the I ² C address is 0x1A. |
| B12 | XTALP | Miscellaneous digital ¹ | Crystal Input. |
| B13 | PVDD1 | Power | PLL Analog Supply Voltage (1.8 V). |
| B14 | NC | N/A | No Connect. Do not connect to this pin. |
| B15 | NC | N/A | No Connect. Do not connect to this pin. |
| B16 | GND | GND | Ground. |
| B17 | RX_CP | Rx input | Rx Clock True Input. |
| B18 | RX_OP | Rx input | Rx Channel 0 True Input. |
| B19 | RX_1P | Rx input | Rx Channel 1 True Input. |
| B20 | RX_2P | Rx input | Rx Channel 2 True Input. |
| B21 | GND | GND | Ground. |
| B22 | NC | N/A | No Connect. Do not connect to this pin. |
| B23 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------|---|---|
| C1 | OSD_IN[19]/EXT_DIN[3] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[19])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[3]). |
| C2 | OSD_IN[20]/EXT_DIN[4] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[20])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[4]). |
| C3 | GND | GND | Ground. |
| C4 | TEST12 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| C5 | TEST13 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| C6 | TEST14 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| C7 | SCL | I ² C control | I ² C Clock Input. This pin is open drain; use a 4.7 kΩ resistor to connect this pin to a 3.3 V supply. |
| C8 | SCK1 | Serial port control | Serial Clock (Serial Port 1). Serial Port 1 is used for OSD control. |
| C9 | GND | GND | Ground. |
| C10 | INT0 | Miscellaneous digital | Interrupt Pin 0. When status bits change, this pin is triggered. |
| C11 | PDN | Miscellaneous digital | Power-Down. This pin controls the power state of the ADV8003. |
| C12 | GND | GND | Ground. |
| C13 | GND | GND | Ground. |
| C14 | NC | N/A | No Connect. Do not connect to this pin. |
| C15 | NC | N/A | No Connect. Do not connect to this pin. |
| C16 | RX_HPD | Rx input | Hot Plug Assert Signal Output for the Rx Input. |
| C17 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C18 | GND | GND | Ground. |
| C19 | GND | GND | Ground. |
| C20 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C21 | AVDD1 | Power | HDMI Rx Inputs Analog Supply (3.3 V). |
| C22 | NC | N/A | No Connect. Do not connect to this pin. |
| C23 | NC | N/A | No Connect. Do not connect to this pin. |
| D1 | OSD_IN[16]/EXT_DIN[0] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[16])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[0]). |
| D2 | OSD_IN[17]/EXT_DIN[1] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[17])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[1]). |
| D3 | OSD_IN[18]/EXT_DIN[2] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[18])/Additional TTL Input for External CCIR 656 Video Data (EXT_DIN[2]). |
| D4 | GND | GND | Ground. |
| D5 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D6 | TEST15 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| D7 | SDA | I ² C control | I ² C Data Input. This pin is open drain; use a 4.7 kΩ resistor to connect this pin to a 3.3 V supply. |
| D8 | $\overline{CS1}$ | Serial port control | Chip Select (Serial Port 1). Serial Port 1 is used for OSD control. |
| D9 | GND | GND | Ground. |
| D10 | TEST16 | Miscellaneous digital | Test Pin. Connect this pin to ground through a 4.7 kΩ resistor. |
| D11 | INT2 | Miscellaneous digital | Interrupt Pin for HDMI Receiver Input Lines. When status bits change, an interrupt is generated on this pin. |
| D12 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| D13 | TEST1 | Miscellaneous digital | Test Pin. Float this pin. |
| D14 | NC | N/A | No Connect. Do not connect to this pin. |
| D15 | NC | N/A | No Connect. Do not connect to this pin. |
| D16 | RX_5V | Rx input | 5 V Detect Pin for the Rx Input. |
| D17 | NC | N/A | No Connect. Do not connect to this pin. |
| D18 | NC | N/A | No Connect. Do not connect to this pin. |
| D19 | RTERM | HDMI Rx input | This pin sets internal termination resistance. Use a 500 Ω resistor between this pin and GND. Place the RTERM resistor as close as possible to the ADV8003. |
| D20 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D21 | AVDD2 | Power | Analog Power Supply (3.3 V). |
| D22 | NC | N/A | No Connect. Do not connect to this pin. |
| D23 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|---------------------|---|---|
| E1 | OSD_IN[13]/VBI_SCK | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[13])/Serial Clock for VBI Data Serial Port (VBI_SCK). |
| E2 | OSD_IN[14]/VBI_MOSI | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[14])/Master Out Slave In for VBI Data Serial Port (VBI_MOSI). |
| E3 | OSD_IN[15]/VBI_CS | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[15])/Chip Select for VBI Data Serial Port (VBI_CS). |
| E4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| E20 | TEST2 | Miscellaneous analog | Test Pin. Float this pin. |
| E21 | GND | GND | Ground. |
| E22 | NC | N/A | No Connect. Do not connect to this pin. |
| E23 | NC | N/A | No Connect. Do not connect to this pin. |
| F1 | OSD_IN[9] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[9]). |
| F2 | OSD_IN[10] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[10]). |
| F3 | OSD_IN[11] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[11]). |
| F4 | OSD_IN[12] | OSD video input/ miscellaneous digital | External OSD Video Pixel Input Port (OSD_IN[11]). |
| F20 | NC | N/A | No Connect. Do not connect to this pin. |
| F21 | PVDD3 | Power | PLL Supply (1.8 V). |
| F22 | GND | GND | Ground. |
| F23 | NC | N/A | No Connect. Do not connect to this pin. |
| G1 | OSD_IN[5] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[5]). |
| G2 | OSD_IN[6] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[6]). |
| G3 | OSD_IN[7] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[7]). |
| G4 | OSD_IN[8] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[8]). |
| G7 | GND | GND | Ground. |
| G8 | GND | GND | Ground. |
| G9 | GND | GND | Ground. |
| G10 | DVDD | Power | Digital Power Supply (1.8 V). |
| G11 | GND | GND | Ground. |
| G12 | GND | GND | Ground. |
| G13 | DVDD | Power | Digital Power Supply (1.8 V). |
| G14 | GND | GND | Ground. |
| G15 | GND | GND | Ground. |
| G16 | GND | GND | Ground. |
| G17 | GND | GND | Ground. |
| G20 | ELPF1 | Miscellaneous analog ¹ | External Loop Filter for PLL 1. Connect to PVDD3. |
| G21 | ELPF2 | Miscellaneous analog ¹ | External Loop Filter for PLL 2. Connect to PVDD3. |
| G22 | GND | GND | Ground. |
| G23 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| H1 | OSD_IN[1] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[1]). |
| H2 | OSD_IN[2] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[2]). |
| H3 | OSD_IN[3] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[3]). |
| H4 | OSD_IN[4] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[4]). |
| H7 | GND | GND | Ground. |
| H8 | GND | GND | Ground. |
| H9 | GND | GND | Ground. |
| H10 | GND | GND | Ground. |
| H11 | GND | GND | Ground. |
| H12 | GND | GND | Ground. |
| H13 | GND | GND | Ground. |
| H14 | GND | GND | Ground. |
| H15 | GND | GND | Ground. |
| H16 | GND | GND | Ground. |
| H17 | GND | GND | Ground. |
| H20 | GND | GND | Ground. |
| H21 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------|---------------------|--|
| H22 | NC | N/A | No Connect. Do not connect to this pin. |
| H23 | NC | N/A | No Connect. Do not connect to this pin. |
| J1 | DE | Digital video sync | Data Enable for Digital Input Video. |
| J2 | HS | Digital video sync | Horizontal Sync for Digital Input Video. |
| J3 | OSD_HS | Digital video sync | Horizontal Sync for the OSD Input Port (OSD_HS). |
| J4 | OSD_IN[0] | OSD video input | External OSD Video Pixel Input Port (OSD_IN[0]). |
| J7 | DVDD | Power | Digital Power Supply (1.8 V). |
| J8 | GND | GND | Ground. |
| J9 | GND | GND | Ground. |
| J10 | GND | GND | Ground. |
| J11 | GND | GND | Ground. |
| J12 | GND | GND | Ground. |
| J13 | GND | GND | Ground. |
| J14 | GND | GND | Ground. |
| J15 | GND | GND | Ground. |
| J16 | GND | GND | Ground. |
| J17 | DVDD | Power | Digital Power Supply (1.8 V). |
| J20 | NC | N/A | No Connect. Do not connect to this pin. |
| J21 | GND | GND | Ground. |
| J22 | NC | N/A | No Connect. Do not connect to this pin. |
| J23 | NC | N/A | No Connect. Do not connect to this pin. |
| K1 | VS | Digital video sync | Vertical Sync for Digital Input Video. |
| K2 | PCLK | Digital video sync | Pixel Clock for Digital Input Video. |
| K3 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K4 | DVDD_IO | Power | Digital Interface Supply (3.3 V). |
| K7 | GND | GND | Ground. |
| K8 | GND | GND | Ground. |
| K9 | GND | GND | Ground. |
| K10 | GND | GND | Ground. |
| K11 | GND | GND | Ground. |
| K12 | GND | GND | Ground. |
| K13 | GND | GND | Ground. |
| K14 | GND | GND | Ground. |
| K15 | GND | GND | Ground. |
| K16 | GND | GND | Ground. |
| K17 | GND | GND | Ground. |
| K20 | NC | N/A | No Connect. Do not connect to this pin. |
| K21 | GND | GND | Ground. |
| K22 | NC | N/A | No Connect. Do not connect to this pin. |
| K23 | NC | N/A | No Connect. Do not connect to this pin. |
| L1 | P[32] | Digital video input | Digital Video Input Bus[35:0]. |
| L2 | P[33] | Digital video input | Digital Video Input Bus[35:0]. |
| L3 | P[34] | Digital video input | Digital Video Input Bus[35:0]. |
| L4 | P[35] | Digital video input | Digital Video Input Bus[35:0]. |
| L7 | DVDD | Power | Digital Power Supply (1.8 V). |
| L8 | GND | GND | Ground. |
| L9 | GND | GND | Ground. |
| L10 | GND | GND | Ground. |
| L11 | GND | GND | Ground. |
| L12 | GND | GND | Ground. |
| L13 | GND | GND | Ground. |
| L14 | GND | GND | Ground. |
| L15 | GND | GND | Ground. |
| L16 | GND | GND | Ground. |
| L17 | GND | GND | Ground. |
| L20 | NC | N/A | No Connect. Do not connect to this pin. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|---------------------|---|
| L21 | GND | GND | Ground. |
| L22 | NC | N/A | No Connect. Do not connect to this pin. |
| L23 | NC | N/A | No Connect. Do not connect to this pin. |
| M1 | P[28] | Digital video input | Digital Video Input Bus[35:0]. |
| M2 | P[29] | Digital video input | Digital Video Input Bus[35:0]. |
| M3 | P[30] | Digital video input | Digital Video Input Bus[35:0]. |
| M4 | P[31] | Digital video input | Digital Video Input Bus[35:0]. |
| M7 | GND | GND | Ground. |
| M8 | GND | GND | Ground. |
| M9 | GND | GND | Ground. |
| M10 | GND | GND | Ground. |
| M11 | GND | GND | Ground. |
| M12 | GND | GND | Ground. |
| M13 | GND | GND | Ground. |
| M14 | GND | GND | Ground. |
| M15 | GND | GND | Ground. |
| M16 | GND | GND | Ground. |
| M17 | GND | GND | Ground. |
| M20 | NC | N/A | No Connect. Do not connect to this pin. |
| M21 | PVDD5 | Power ¹ | PLL Power Supply (1.8 V). |
| M22 | NC | N/A | No Connect. Do not connect to this pin. |
| M23 | NC | N/A | No Connect. Do not connect to this pin. |
| N1 | P[24] | Digital video input | Digital Video Input Bus[35:0]. |
| N2 | P[25] | Digital video input | Digital Video Input Bus[35:0]. |
| N3 | P[26] | Digital video input | Digital Video Input Bus[35:0]. |
| N4 | P[27] | Digital video input | Digital Video Input Bus[35:0]. |
| N7 | GND | GND | Ground. |
| N8 | GND | GND | Ground. |
| N9 | GND | GND | Ground. |
| N10 | GND | GND | Ground. |
| N11 | GND | GND | Ground. |
| N12 | GND | GND | Ground. |
| N13 | GND | GND | Ground. |
| N14 | GND | GND | Ground. |
| N15 | GND | GND | Ground. |
| N16 | GND | GND | Ground. |
| N17 | GND | GND | Ground. |
| N20 | NC | N/A | No Connect. Do not connect to this pin. |
| N21 | PVDD5 | Power ¹ | PLL Power Supply (1.8 V). |
| N22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| N23 | NC | N/A | No Connect. Do not connect to this pin. |
| P1 | P[20] | Digital video input | Digital Video Input Bus[35:0]. |
| P2 | P[21] | Digital video input | Digital Video Input Bus[35:0]. |
| P3 | P[22] | Digital video input | Digital Video Input Bus[35:0]. |
| P4 | P[23] | Digital video input | Digital Video Input Bus[35:0]. |
| P7 | DVDD | Power | Digital Power Supply (1.8 V). |
| P8 | GND | GND | Ground. |
| P9 | GND | GND | Ground. |
| P10 | GND | GND | Ground. |
| P11 | GND | GND | Ground. |
| P12 | GND | GND | Ground. |
| P13 | GND | GND | Ground. |
| P14 | GND | GND | Ground. |
| P15 | GND | GND | Ground. |
| P16 | GND | GND | Ground. |
| P17 | DVDD | Power | Digital Power Supply (1.8 V). |

| Pin No. | Mnemonic | Type | Description |
|---------|----------|---------------------|---|
| P20 | NC | N/A | No Connect. Do not connect to this pin. |
| P21 | GND | GND | Ground. |
| P22 | NC | N/A | No Connect. Do not connect to this pin. |
| P23 | NC | N/A | No Connect. Do not connect to this pin. |
| R1 | P[16] | Digital video input | Digital Video Input Bus[35:0]. |
| R2 | P[17] | Digital video input | Digital Video Input Bus[35:0]. |
| R3 | P[18] | Digital video input | Digital Video Input Bus[35:0]. |
| R4 | P[19] | Digital video input | Digital Video Input Bus[35:0]. |
| R7 | GND | GND | Ground. |
| R8 | GND | GND | Ground. |
| R9 | GND | GND | Ground. |
| R10 | GND | GND | Ground. |
| R11 | GND | GND | Ground. |
| R12 | GND | GND | Ground. |
| R13 | GND | GND | Ground. |
| R14 | GND | GND | Ground. |
| R15 | GND | GND | Ground. |
| R16 | GND | GND | Ground. |
| R17 | GND | GND | Ground. |
| R20 | NC | N/A | No Connect. Do not connect to this pin. |
| R21 | GND | GND | Ground. |
| R22 | NC | N/A | No Connect. Do not connect to this pin. |
| R23 | NC | N/A | No Connect. Do not connect to this pin. |
| T1 | P[14] | Digital video input | Digital Video Input Bus[35:0]. |
| T2 | P[15] | Digital video input | Digital Video Input Bus[35:0]. |
| T3 | GND | GND | Ground. |
| T4 | GND | GND | Ground. |
| T7 | GND | GND | Ground. |
| T8 | GND | GND | Ground. |
| T9 | GND | GND | Ground. |
| T10 | GND | GND | Ground. |
| T11 | GND | GND | Ground. |
| T12 | GND | GND | Ground. |
| T13 | GND | GND | Ground. |
| T14 | GND | GND | Ground. |
| T15 | GND | GND | Ground. |
| T16 | GND | GND | Ground. |
| T17 | GND | GND | Ground. |
| T20 | NC | N/A | No Connect. Do not connect to this pin. |
| T21 | GND | GND | Ground. |
| T22 | NC | N/A | No Connect. Do not connect to this pin. |
| T23 | NC | N/A | No Connect. Do not connect to this pin. |
| U1 | P[10] | Digital video input | Digital Video Input Bus[35:0]. |
| U2 | P[11] | Digital video input | Digital Video Input Bus[35:0]. |
| U3 | P[12] | Digital video input | Digital Video Input Bus[35:0]. |
| U4 | P[13] | Digital video input | Digital Video Input Bus[35:0]. |
| U7 | GND | GND | Ground. |
| U8 | GND | GND | Ground. |
| U9 | DVDD | Power | Digital Power Supply (1.8 V). |
| U10 | GND | GND | Ground. |
| U11 | GND | GND | Ground. |
| U12 | DVDD | Power | Digital Power Supply (1.8 V). |
| U13 | GND | GND | Ground. |
| U14 | GND | GND | Ground. |
| U15 | DVDD | Power | Digital Power Supply (1.8 V). |
| U16 | GND | GND | Ground. |

| Pin No. | Mnemonic | Type | Description |
|---------|----------------------------------|-----------------------|---|
| U17 | GND | GND | Ground. |
| U20 | NC | N/A | No Connect. Do not connect to this pin. |
| U21 | GND | GND | Ground. |
| U22 | NC | N/A | No Connect. Do not connect to this pin. |
| U23 | NC | N/A | No Connect. Do not connect to this pin. |
| V1 | P[6] | Digital video input | Digital Video Input Bus[35:0]. |
| V2 | P[7] | Digital video input | Digital Video Input Bus[35:0]. |
| V3 | P[8] | Digital video input | Digital Video Input Bus[35:0]. |
| V4 | P[9] | Digital video input | Digital Video Input Bus[35:0]. |
| V20 | GND | GND | Ground. |
| V21 | PVDD6 | Power ¹ | PLL Power Supply (1.8 V). |
| V22 | NC | N/A | No Connect. Do not connect to this pin. |
| V23 | NC | N/A | No Connect. Do not connect to this pin. |
| W1 | P[2] | Digital video input | Digital Video Input Bus[35:0]. |
| W2 | P[3] | Digital video input | Digital Video Input Bus[35:0]. |
| W3 | P[4] | Digital video input | Digital Video Input Bus[35:0]. |
| W4 | P[5] | Digital video input | Digital Video Input Bus[35:0]. |
| W20 | TEST3 | Miscellaneous digital | Test Pin. Connect this pin to Ground through a 0.1 μ F capacitor. |
| W21 | PVDD6 | Power ¹ | PLL Power Supply (1.8 V). |
| W22 | AVDD3 | Power | HDMI Analog Power Supply (1.8 V). |
| W23 | NC | N/A | No Connect. Do not connect to this pin. |
| Y1 | P[0] | Digital video input | Digital Video Input Bus[35:0]. |
| Y2 | P[1] | Digital video input | Digital Video Input Bus[35:0]. |
| Y3 | DDR_DQS[2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| Y4 | GND | GND | Ground. |
| Y5 | DDR_DQ[23] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y7 | DDR_DQS[3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| Y8 | GND | GND | Ground. |
| Y9 | DDR_A[11] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y11 | DDR_A[4] | DDR interface | Address Line. Interface to external RAM address lines. |
| Y12 | GND | GND | Ground. |
| Y13 | $\overline{\text{DDR_CAS}}$ | DDR interface | Column Address Strobe for DDR Memory. |
| Y14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y15 | DDR_ $\overline{\text{CK}}$ | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| Y16 | GND | GND | Ground. |
| Y17 | DDR_DQ[9] | DDR Interface | Data Line. Interface to external RAM data lines. |
| Y18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| Y19 | DDR_DQ[14] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y20 | GND | GND | Ground. |
| Y21 | DDR_DQ[6] | DDR interface | Data Line. Interface to external RAM data lines. |
| Y22 | PVDD_DDR | Power | DDR Interface PLL Supply (1.8 V). |
| Y23 | GND | GND | Ground. |
| AA1 | DDR_DQ[18] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA2 | GND | GND | Ground. |
| AA3 | GND | GND | Ground. |
| AA4 | $\overline{\text{DDR_DQS}}$ [2] | DDR interface | Data Strobe for DDR Data Bytes[23:16]. |
| AA5 | DDR_DQ[26] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA6 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA7 | $\overline{\text{DDR_DQS}}$ [3] | DDR interface | Data Strobe for DDR Data Bytes[31:24]. |
| AA8 | NC/GND | No connect/GND | For new ADV8003 designs, do not connect to this pin. For designs that must maintain consistency with the ADV8002, this pin can be grounded. |
| AA9 | DDR_A[8] | DDR interface | Address Line. Interface to external RAM address lines. |
| AA10 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA11 | DDR_A[2] | DDR interface | Address Line. Interface to external RAM address lines. |

| Pin No. | Mnemonic | Type | Description |
|---------|-----------------------------|----------------------------|--|
| AA12 | GND | GND | Ground. |
| AA13 | DDR_ $\overline{\text{CS}}$ | DDR interface | DDR Chip Select. Interface to external DDR RAM chip selects. |
| AA14 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA15 | DDR_CK | DDR interface | DDR Memory Clock. Interface to external DDR RAM clock lines. |
| AA16 | GND | GND | Ground. |
| AA17 | DDR_DQ[11] | DDR interface | Data Line. Interface to external RAM data lines. |
| AA18 | DVDD_DDR | Power | DDR Interface Supply (1.8 V). |
| AA19 | DDR_DM[1] | DDR interface | Data Mask for Data Lines[15:8]. |
| AA20 | DDR_DM[0] | DDR interface | Data Mask for Data Lines[7:0]. |
| AA21 | GND | GND | Ground. |
| AA22 | GND | GND | Ground. |
| AA23 | DDR_DQ[3] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB1 | DDR_DQ[21] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB2 | DDR_DQ[19] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB3 | DDR_DQ[17] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB4 | DDR_DM[2] | DDR interface | Data Mask for Data Lines[23:16]. |
| AB5 | DDR_DQ[30] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB6 | DDR_DM[3] | DDR interface | Data Mask for Data Lines[31:25]. |
| AB7 | DDR_DQ[31] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB8 | DDR_DQ[29] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB9 | DDR_A[12] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB10 | DDR_A[6] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB11 | DDR_A[3] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB12 | DDR_A[0] | DDR interface | Address Line. Interface to external RAM address lines. |
| AB13 | DDR_BA[0] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AB14 | DDR_RAS | DDR interface | Row Address Strobe for DDR Memory. |
| AB15 | DDR_CKE | DDR interface | Clock Enable for External DDR Memory. |
| AB16 | DDR_DQ[12] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB17 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AB18 | DDR_DQ[8] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB19 | DDR_DQ[13] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB20 | DDR_DQ[0] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB21 | DDR_DQ[5] | DDR interface | Data Line. Interface to external RAM data lines. |
| AB22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AB23 | DDR_DQ[4] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC1 | DDR_DQ[16] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC2 | DDR_DQ[20] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC3 | DDR_DQ[22] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC4 | DDR_DQ[25] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC5 | DDR_DQ[28] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC6 | DDR_DQ[27] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC7 | DDR_DQ[24] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC8 | DDR_A[9] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC9 | DDR_A[5] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC10 | DDR_A[7] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC11 | DDR_A[1] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC12 | DDR_A[10] | DDR interface | Address Line. Interface to external RAM address lines. |
| AC13 | DDR_BA[1] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AC14 | DDR_BA[2] | DDR interface | Bank Address Line. Indicates which data bank to write/read from. |
| AC15 | DDR_ $\overline{\text{WE}}$ | DDR interface | Write Enable Signal for DDR RAM. |
| AC16 | DDR_VREF | DDR interface ¹ | Reference Voltage for DDR RAM. |
| AC17 | DDR_DQ[10] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC18 | DDR_DQS[1] | DDR interface | Data Strobe for DDR Data Bytes[15:8]. |
| AC19 | DDR_DQ[15] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC20 | DDR_DQ[7] | DDR interface | Data Line. Interface to external RAM data lines. |

| Pin No. | Mnemonic | Type | Description |
|----------------|-----------------|---------------|--|
| AC21 | DDR_DQ[2] | DDR interface | Data Line. Interface to external RAM data lines. |
| AC22 | DDR_DQS[0] | DDR interface | Data Strobe for DDR Data Bytes[7:0]. |
| AC23 | DDR_DQ[1] | DDR interface | Data Line. Interface to external RAM data lines. |

¹ Sensitive node. Careful layout is important. The associated circuitry should be kept as close as possible to the [ADV8003](#).

DESIGN CONSIDERATIONS

POWER-UP SEQUENCE

The power-up sequence of the [ADV8003](#) is as follows:

1. Hold the RESET and PDN pins low.
2. Bring up the 3.3 V supplies (DVDD_IO, AVDD1, AVDD2).
3. A minimum delay of 20 ms is required from the point at which the 3.3 V reaches its minimum recommended value (that is, 3.14 V) before powering up the 1.8 V supplies.
4. Bring up the 1.8 V supplies (DVDD, PVDD1, PVDD2, PVDD3, PVDD5, PVDD6, CVDD1, AVDD3, DVDD_DDR, PVDD_DDR). These should be powered up together. That is, there should be a difference of less than 0.3 V between them.
5. RESET can be pulled high after supplies have been powered up.
6. A complete reset is recommended after power-up. This can be performed by the system microcontroller.

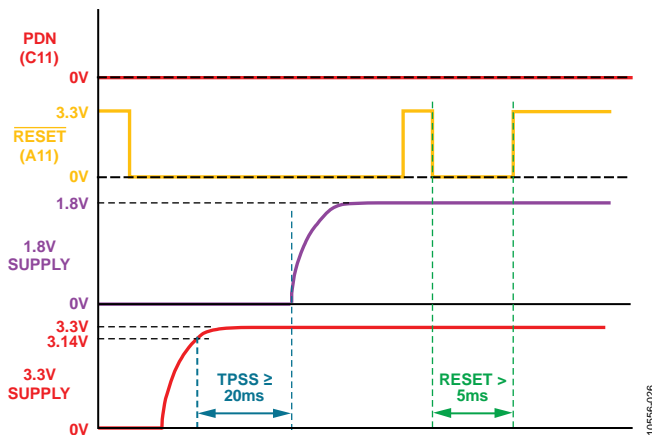


Figure 33. Supply Power-Up Sequence

THERMAL CONSIDERATIONS

The thermal performance of the [ADV8003](#) is influenced by a number of factors, for example, power dissipation of the [ADV8003](#), PCB design, and ambient temperature.

These factors, allied to any other application-specific factors that may affect the thermal performance of [ADV8003](#), must be considered to ensure that the junction temperature of the [ADV8003](#) does not exceed 125°C.

The flexibility of the [ADV8003](#) can, in theory, result in the part being configured in modes where the junction temperature exceeds the maximum rated specification. To ensure that this does not happen, the [ADV8003](#) must be characterized on the final customer PCB to ensure that maximum rated specifications are not exceeded in the planned modes of operation. Using fewer internal layers on a PCB reduces the amount of thermal conductivity between the [ADV8003](#) and the PCB itself. This may necessitate some thermal management effort or affect the modes in which the [ADV8003](#) can be configured.

Calculate thermal conductivity as follows:

1. Configure the [ADV8003](#) in the highest required power mode of operation.
2. Measure the ambient temperature of the enclosure.
3. Measure the case temperature at the top of the [ADV8003](#).

$$T_J = T_C + 5^\circ\text{C}$$

$$T_{J\text{MAX}} = T_{A\text{MAX}} - T_A (\text{actual}) + T_C (\text{actual}) + 5^\circ\text{C}$$

where:

T_J is the junction temperature (inside the [ADV8003](#)).

T_C is the case temperature (top surface of the [ADV8003](#)).

T_A is the ambient temperature (in the locality of the [ADV8003](#)).

Maximum specified $T_{A\text{MAX}}$ for the [ADV8003](#) is 70°C. Depending on the result of the previous calculations/ measurement for the specific system, a lower $T_{A\text{MAX}}$ limit may need to be specified for that system to ensure that $T_{J\text{MAX}}$ remains safely below 125°C.

FUNCTIONAL OVERVIEW

VIDEO INPUT

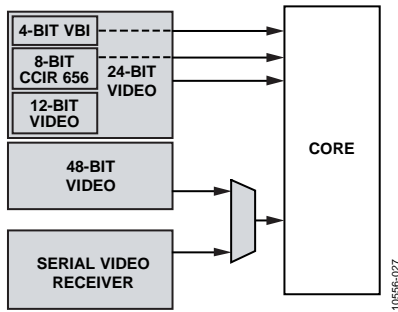


Figure 34. Digital Video Interface

The [ADV8003](#) can receive data via the 48-bit input pixel port, the 24-bit OSD input port, or from the output of an HDMI transmitter.

The 48-bit input pixel port can receive data from an upstream analog/HDMI front-end device such as the [ADV7619](#). This bus can accept multiple input formats in both RGB and YPrPb color spaces. Double data rate (DDR) input formats are also supported.

The 24-bit input pixel port can also receive video data from an upstream analog/HDMI front-end device such as the [ADV7844](#) or OSD data from an external OSD generator. This bus can accept multiple input formats up to UXGA. DDR input formats are also supported. The video input on the 24-bit pixel port can be scaled and overlaid onto the main video path.

The serial video receiver can accept the output of an HDMI transmitter such as the [ADV7511](#), [ADV7623](#) or [ADV7850](#). Using this configuration, the transceiver can extract HDMI audio for processing before reinsertion the audio into the [ADV8003](#) via the audio pins, for output through the HDMI transmitters. This input does not support EDID or HDCP operations.

Picture-in-picture (PiP) support is possible when receiving video data on more than one of the video inputs, such as the 48-bit pixel port and the serial video receiver.

Flexible digital interface features include the following:

- (Up to) 48-bit pixel port for general video data
- (Up to) 24-bit pixel port for external OSD, if the [ADV8003](#) internal OSD is not used
- Option to connect the output of HDMI transmitter

FLEXIBLE DIGITAL CORE

The [ADV8003](#) has a flexible digital core that enables many different configurations of single, dual and triple video processing paths. Video processing can be placed first in the signal chain to ensure that all outputs are processed to the highest quality.

OSD can be placed at numerous locations within the signal chain to vary the number of outputs on which the OSD is displayed. PiP can also be supported via the OSD block, using a pixel port input that is connected to the OSD block. Several modes of operation are defined to help the user quickly integrate the [ADV8003](#) into a system.

VIDEO SIGNAL PROCESSOR (VSP)

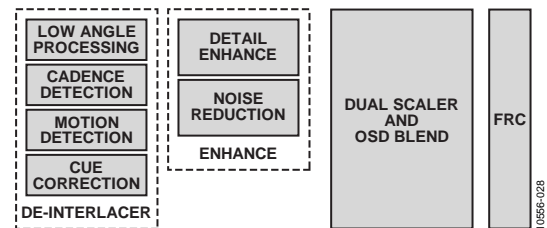


Figure 35. Video Processing

The [ADV8003](#) offers video de-interlacing and scaling. The de-interlacer, located in the primary VSP, is motion adaptive and offers high performance on low angle edges. It can support input video resolutions of 480i, 576i, and 1080i.

The dual scalers in the [ADV8003](#) support the Analog Devices proprietary scaling algorithm, which provides very high quality video upscaling and downscaling. This scaling algorithm helps eradicate many of the common problems that are encountered when scaling video data, such as saw tooth, edge blurring, and ringing.

The primary and secondary scalers are capable of up- and down-scaling between a range of SD and HD video resolutions (for example, 480p, 576p, 720p, and 1080p). The primary scaler in the [ADV8003KBCZ-8/ADV8003KBCZ-8B/ADV8003KBCZ-8C](#) models is capable of upscaling to 4k × 2k video resolutions.

Cadence detection and frame rate conversion are also supported in the [ADV8003](#), which allows film formats to be displayed at their native frame rate, as well as being converted to the native refresh rate of the TV. Additional video processing in the [ADV8003](#) helps with reduction of common video artifacts such as mosquito, random, and block noise. The [ADV8003](#) also includes an aspect ratio converter, as well as a panorama mode feature.

The following VSP features are included:

- High performance motion adaptive SD/HD de-interlacer and scaler
- Two scalers, allowing independent scaling on [ADV8003](#) outputs
- Frame rate converter, supporting conversion between multiple frame rates (23.976 Hz, 24 Hz, 25 Hz, 29.97 Hz, 30 Hz, 50 Hz, 59.94 Hz, and 60 Hz)
- Noise reduction, which helps with the reduction of random, block, and mosquito noise
- Five manually programmable color space converters that are distributed between inputs and outputs

ON-SCREEN DISPLAY (OSD)

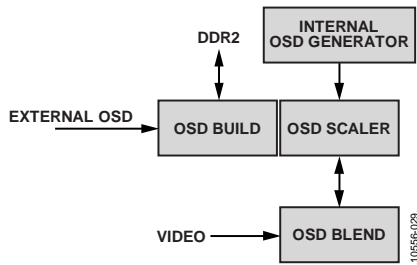


Figure 36. Bitmap OSD

The **ADV8003** incorporates a bitmap-based OSD block that allows users to create impressive OSD designs that can include bitmap images, as well as motion and animation. Individual regions of the OSD can be alpha blended and prioritized over other regions.

An OSD development tool, Blimp, is provided to assist in the design and development of custom OSDs and to abstract the OSD hardware from the user. This tool automatically generates two design elements: a design resource containing character sets and images that must be downloaded to an external SPI flash on the board; and code that must be integrated with system APIs to link the functionality of the OSD with the functionality of the system.

The OSD design resource is loaded into external DDR2 memories on power-up by the OSD coprocessor of the **ADV8003**. This coprocessor is responsible for handling upper level commands from the user and translating them into lower level operations for the OSD and DMA.

OSD features include the following:

- Pixel-by-pixel alpha blending and priority levels assigned to the different OSD components
- A high performance OSD scaler allows the rendering of OSDs at a single resolution, as well as blending at different resolutions

EXTERNAL DDR2 MEMORY

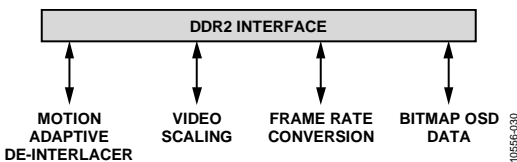


Figure 37. External DDR2 Memory Interface

External DDR2 memory is required for motion adaptive de-interlacing, scaling, frame rate conversion, and bitmap OSD overlay. The bandwidth of external memory required is determined by the input video formats that the **ADV8003** must support, as well as the level of video processing required (scaling, conversion, and OSD). Depending on the input video resolution and video processing options, one or two DDR2 memories may be required.

HDMI TRANSMITTERS

The **ADV8003** features dual HDMI transmitters. The transmitters provided on the **ADV8003KBCZ-8/ADV8003KBCZ-8B/ADV8003KBCZ-8C** support all HDTV formats up to 4k x 2k; the transmitters on the **ADV8003KBCZ-7/ADV8003KBCZ-7B/ADV8003KBCZ-7C/ADV8003KBCZ-7T** support all HDTV formats up to 1080p. All parts support all of the mandatory and many of the optional 3D formats, and audio return channel (ARC), which allows an S/PDIF audio connection between the source and sink. Each HDMI transmitter features a full function CEC master and on-chip MPUs with DDC I²C masters to perform HDCP operations and EDID operations.

HDMI Tx features include the following:

- Audio return channel (ARC) support
- Mandatory 3D formats and many optional 3D formats
- Content type bits
- CEC controller
- HDMI audio interface and support for multiple audio formats (S/PDIF, I²S, DSD)

VIDEO ENCODER

The **ADV8003** features a high speed digital-to-analog video encoder. Six 12-bit NSV, 3.3 V video DACs provide support for worldwide composite (CVBS), S-Video (Y-C), and component (YPrPb/RGB) analog outputs in standard definition (SD), enhanced definition (ED), or high definition (HD) video formats. It is also possible to enable the video encoder of the **ADV8003** to work in simultaneous modes where both an SD and ED/HD formats are output.

Encoder features include the following:

- Six 12-bit NSV video DACs capable of outputting video standards of up to 1080p with additional oversampling
- Multiformat video output support; composite (CVBS), S-Video (Y-C), component YPrPb (SD, ED and HD), and component RGB (SD, ED and HD)
- Simultaneous SD and ED/HD operation
- Copy generation management system (CGMS)
- Closed captioning and widescreen signaling (WSS)
- Rovi® Rev. 7.1.L1 (SD) and Rev. 1.4 (ED) compliant

PROFESSIONAL CONFIGURATION

To accommodate professional applications where HDMI and analog video output are not desired, the **ADV8003** offers a 30-bit TTL input, 30-bit TTL output mode. This mode suits applications where a video signal processor is required between two TTL interfaces (for example, an HDMI receiver and an FPGA).

REGISTER MAP ARCHITECTURE

The registers of the **ADV8003** are controlled via a 2-wire serial (I²C-compatible) interface. Addressing in the **ADV8003** is 16-bit with 8-bit data. This means that I²C writes to the part are in the following form: <I²C Address>, <Address MSBs>, <Address LSBs>, <Data>.

For example, to write 0xFF to the encoder register map, which is Register 0xE4AF, the bytes sent over the I²C interface are: 0x1A, 0xE4, 0xAF, 0xFF. The addresses are outlined in Table 10. Figure 38 shows the register map architecture for the **ADV8003**.

The **ADV8003** also has a number of SPI register maps used for OSD functions. These are accessed through the APIs defined in the Blimp software tool.

Table 10. ADV8003 I²C Address and Register Address Range for the Different HW Blocks

| Register Map Name | I ² C Address | Register Address |
|-------------------|---|------------------|
| IO Map | 0x1A (when the ALSB pin is set high) or 0x18 (when the ALSB pin is set low) | 0x1A00 to 0x1BFF |
| Primary VSP Map 1 | | 0xE800 to 0xE8FF |
| Primary VSP Map 2 | | 0xE900 to 0xE9FF |
| Secondary VSP Map | | 0xE600 to 0xE6FF |
| DPLL Map | | 0xE000 to 0xE0FF |
| Rx Main Map | | 0xE200 to 0xE2FF |
| Rx InfoFrame Map | | 0xE300 to 0xE3FF |
| Encoder Map | | 0xE400 to 0xE4FF |
| Tx1 Main Map | | 0xEC00 to 0xECFF |
| Tx1 EDID Map | | 0xEE00 to 0xEEFF |
| Tx1 CEC Map | | 0xF000 to 0xF0FF |
| Tx1 UDP Map | | 0xF200 to 0xF2FF |
| Tx1 Test Map | | 0xF300 to 0xF3FF |
| Tx2 Main Map | | 0xF400 to 0xF4FF |
| Tx2 EDID Map | | 0xF600 to 0xF6FF |
| Tx2 CEC Map | | 0xF800 to 0xF8FF |
| Tx2 UDP Map | | 0xFA00 to 0xFAFF |
| Tx2 Test Map | | 0xFB00 to 0xFBFF |

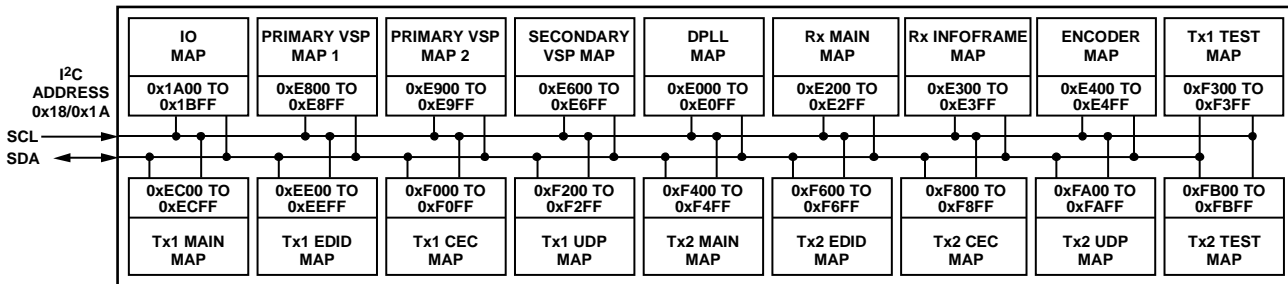


Figure 38. Register Map Architecture

10256-031

TYPICAL APPLICATIONS DIAGRAM

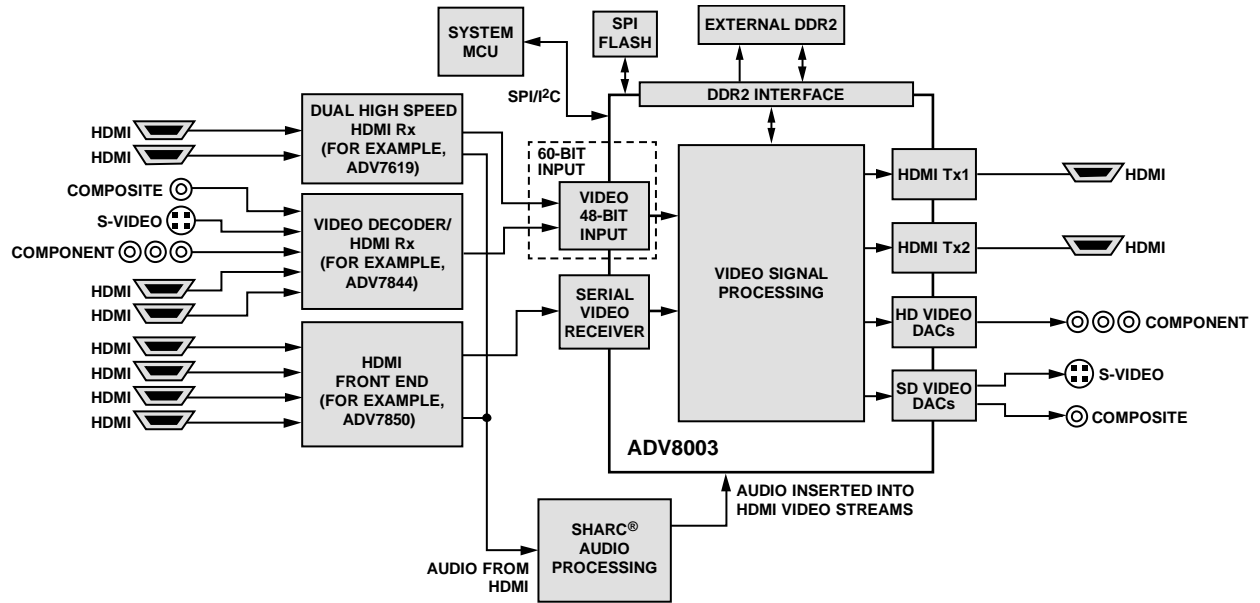
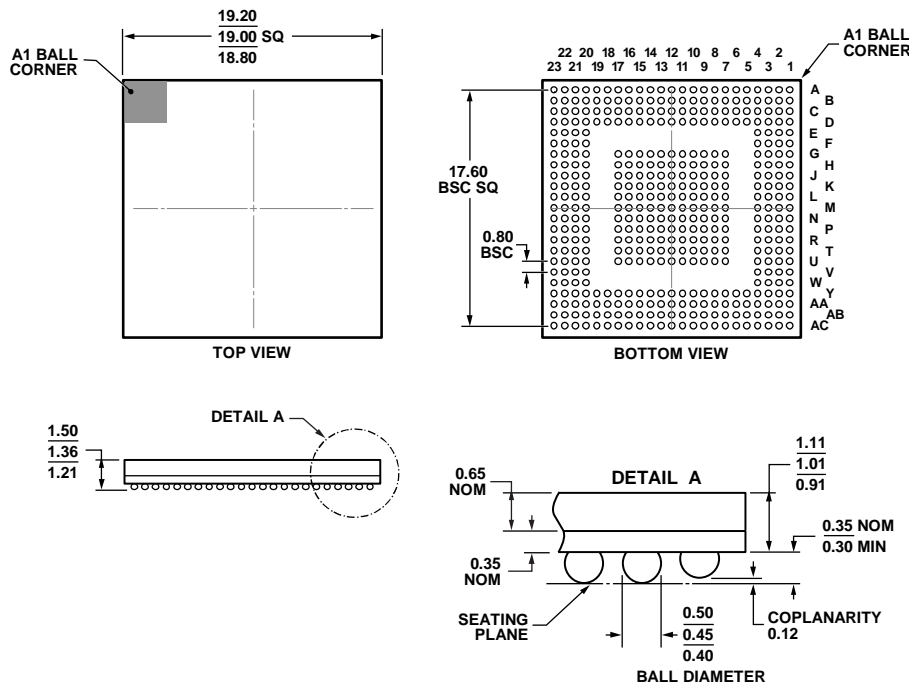


Figure 39. System Block Diagram

10556-032

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-275-PPAB-2.
 Figure 40. 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
 (BC-425-1)
 Dimensions shown in millimeters

11-22-2011-A

ORDERING GUIDE

| Model ^{1, 2} | Temperature Range | Package Description | Package Option |
|-----------------------|-------------------|---|----------------|
| ADV8003KBCZ-8 | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| ADV8003KBCZ-8B | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| ADV8003KBCZ-8C | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| ADV8003KBCZ-7 | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| ADV8003KBCZ-7B | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| ADV8003KBCZ-7C | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| ADV8003KBCZ-7T | 0°C to 70°C | 425-Ball Chip Scale Package Ball Grid Array [CSP_BGA] | BC-425-1 |
| EVAL-ADV8003-SMZ-P | | ADV8003KBCZ-7C Evaluation Board | |

¹ Z = RoHS Compliant Part.

² The evaluation board does not require HDCP or Rovi licensing.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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