Low-Power, 2-Channel, 24-Bit, Simultaneous Sampling Analog-to-Digital Converter with PGA Built-In

1. FEATURES

- AEC-Q100
- Operating temperature range: –40°C to 125°C
- Two high-resolution ADCs with onboard PGA
- Data rate: 125SPS to 16kSPS
- Programmable gain: 1, 2, 3, 4, 6, 8, or 12
- Input bias current: 100pA (max)
- Supplies: unipolar or bipolar
  - Analog: 2.7V to 5.5V
  - Digital: 1.65V to 3.6V
- Internal bias amplifier
- Burnout current for sensor detect
- Flexible power mode
  - High-Resolution mode
  - High-Speed mode
- Built-in oscillator and reference
- Supply monitor, internal temp sensor, OSC fault detection, overrange detection
- Flexible power-down, standby mode
- SPI™-compatible serial interface, timeout reset
- Cyclic redundancy check (CRC) on communications, checksum
- Support ADC data FIFO for reducing polling time of the external device to save power
- Functional safety
- QFN-32 package

2. APPLICATIONS

- Battery management systems
- Data Acquisition systems
- Battery test equipment
- Electricity meters: commercial and residential
- Circuit breaker
- Energy storage systems
- Temperature measurements

3. DESCRIPTION

ADX320Q/ADX3202Q is a one/two-channel, simultaneous sampling, 24-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) that offers wide dynamic range, low power, and buffered analog inputs, making the device an excellent fit for automotive battery management systems (BMS). The ADC inputs can be directly interfaced to shunt resistors for bidirectional battery current measurements, to resistor-divider networks for high-voltage measurements, or to temperature sensors (such as thermistors or analog output temperature sensors). The individual ADC channels can be independently configured depending on the sensor input. A low-noise, programmable gain amplifier (PGA) provides gains ranging from 1 to 12 to amplify low-level signals. The device features a global-chop mode to remove offset drift over temperature and time. Additionally, this device integrates offset and gain calibration registers to help remove signal-chain errors. A low-drift, 2.4V or 4.2V reference and precision oscillator is integrated into the device, reducing printed circuit board (PCB) area. Optional cyclic redundancy checks (CRCs) on the data input, data output, and register map maintain communication integrity.

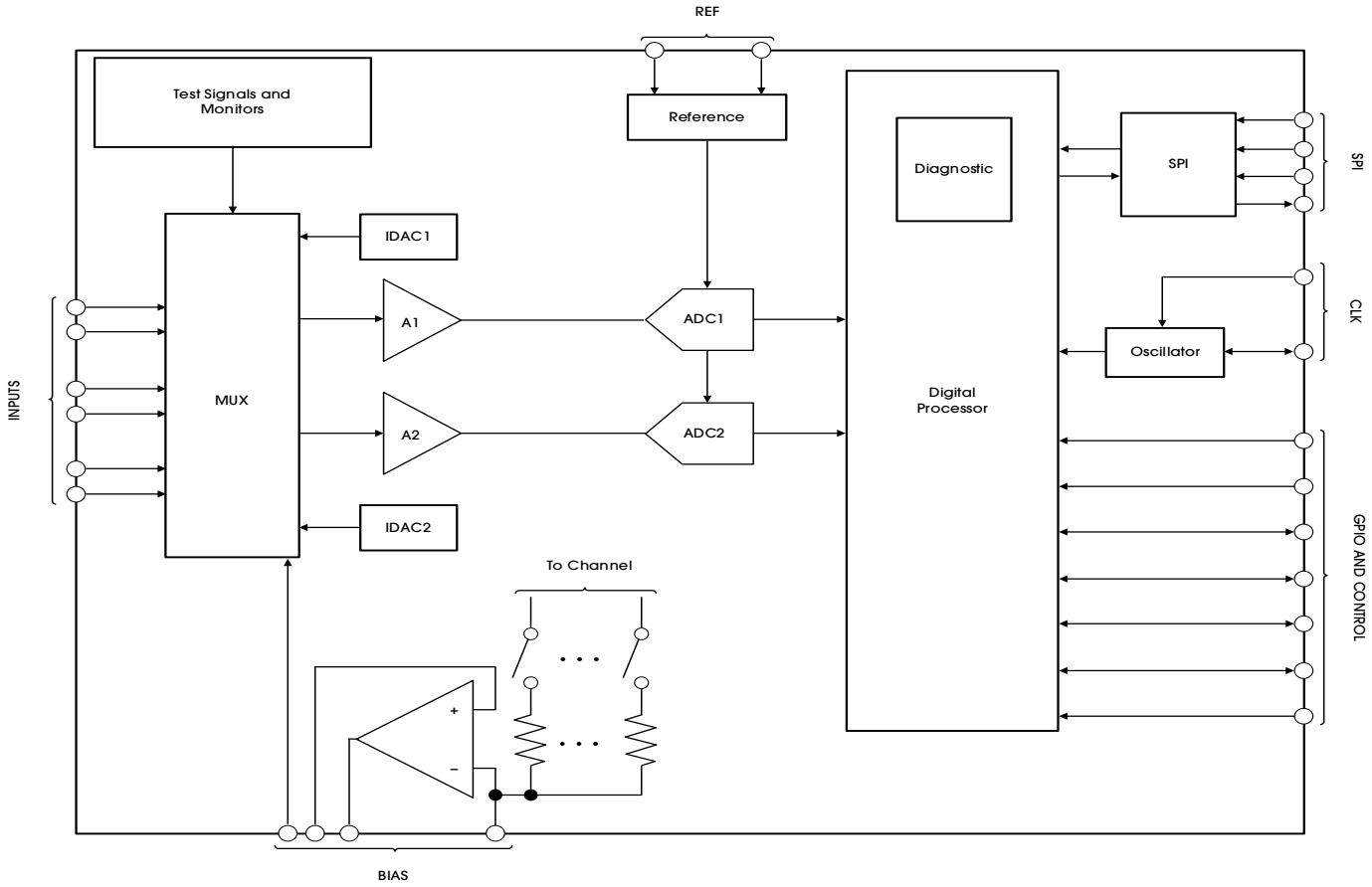


Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER[1]	CH (#)	MARK	PACKAGE	RESOLUTION (BIT)	FUNCTIONAL SAFETY	CRC/ECC	FIFO	OP. TEMP. (°C)	RATING	PKG. OPTION
ADX320AQFN32	1	ADX320	QFN-32	24			Y	–40-85	Industrial	T/R-1500
ADX320QAQFN32	1	ADX320Q	QFN-32	24	Y	Y	Y	–40-125	Auto	T/R-1500
ADX3202AQFN32	2	ADX3202	QFN-32	24			Y	–40-85	Industrial	T/R-1500
ADX3202QAQFN32	2	ADX3202Q	QFN-32	24	Y	Y	Y	–40-125	Auto	T/R-1500

Table 2. Family Selection Guide

ORDER NUMBER[1]	CH (#)	MARK	PACKAGE	RESOLUTION (BIT)	FUNCTIONAL SAFETY	CRC/ECC	FIFO	OP. TEMP. (°C)	RATING	PKG. OPTION
ADX310AQFN32	1	ADX310	QFN-32	16				–40-85	Industrial	T/R-1500
ADX310QAQFN32	1	ADX310Q	QFN-32	16	Y	Y		–40-125	Auto	T/R-1500
ADX3102AQFN32	2	ADX3102	QFN-32	16				–40-85	Industrial	T/R-1500
ADX3102QAQFN32	2	ADX3102Q	QFN-32	16	Y	Y		–40-125	Auto	T/R-1500

Devices can be ordered via the following two ways:
1. Place orders directly on our website (www.analogysemi.com), or,
2. Contact our sales team by mailing to sales@analogysemi.com.

4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration (ADX320Q).

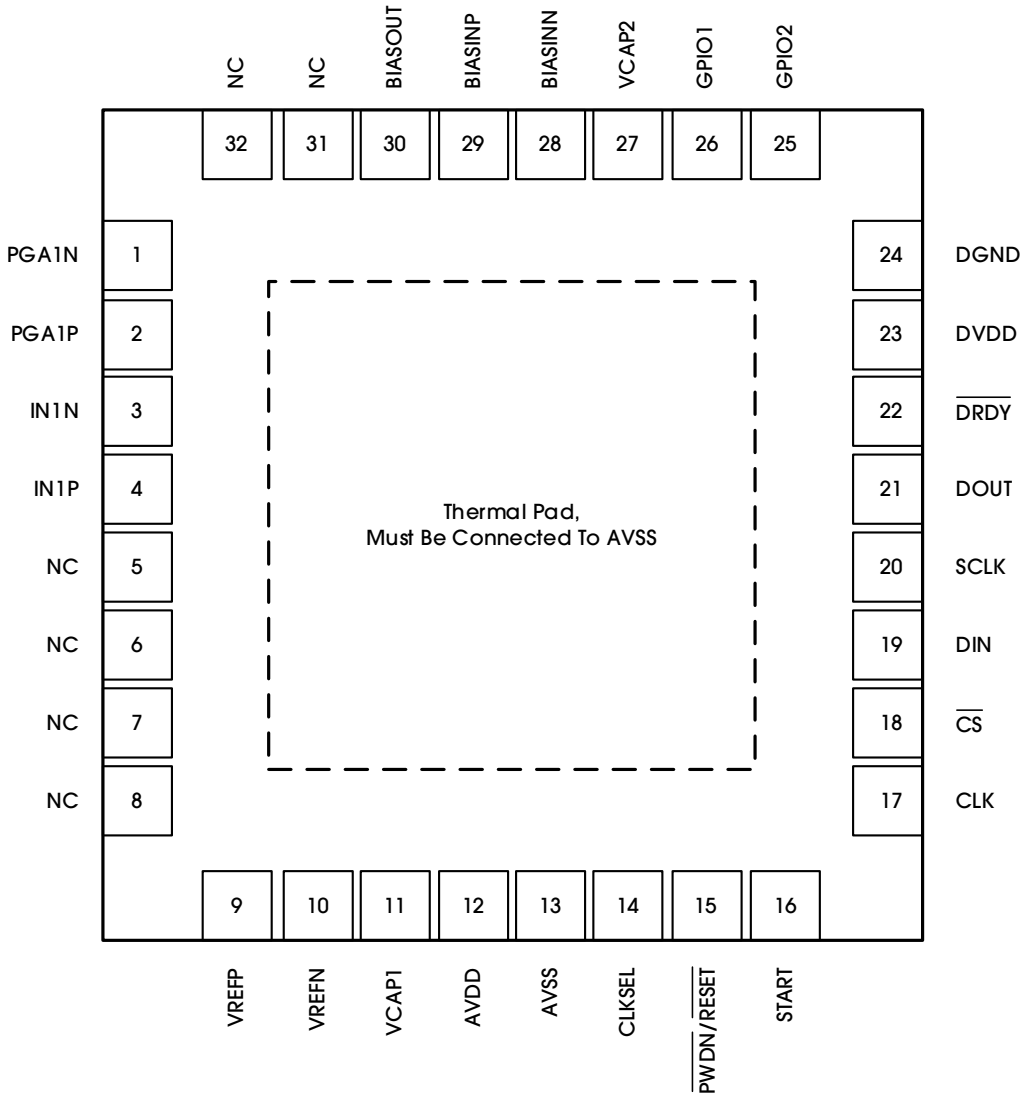


Figure 1. Pin Configuration (ADX320Q)

Table 3 lists the pin functions (ADX320Q).

Table 3. Pin Functions (ADX320Q)

POSITION	PIN	TYPE	DESCRIPTION
1	PGA1N	Analog output	PGA1 inverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1P.
2	PGA1P	Analog output	PGA1 noninverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1N.
3	IN1N(1)	Analog input	Differential analog negative input 1
4	IN1P(1)	Analog input	Differential analog positive input 1
5, 6, 7, 8, 31, 32	NC	—	Do not connect
9	VREFP	Analog input/output	Positive reference voltage
10	VREFN	Supply	Negative reference voltage, must be connected to AVSS
11	VCAP1	—	Analog bypass capacitor, bandgap output
12	AVDD	Supply	Analog supply
13	AVSS	Supply	Analog ground
14	CLKSEL	Digital input	Master clock select
15	$\overline{\text{PWDN}}/\overline{\text{RESET}}$	Digital input	Power-down or system reset, active low
16	START	Digital input	Start conversion
17	CLK	Digital input	Master clock input
18	$\overline{\text{CS}}$	Digital input	Chip select
19	DIN	Digital input	SPI data input
20	SCLK	Digital input	SPI clock
21	DOUT	Digital output	SPI data output
22	$\overline{\text{DRDY}}$	Digital output	Data ready, active low
23	DVDD	Supply	Digital power supply
24	DGND	Supply	Digital ground
25	GPIO2	Digital input/output	General-purpose I/O 2
26	GPIO1	Digital input/output	General-purpose I/O 1
27	VCAP2	Supply	Analog bypass capacitor, AVDD + 2V
28	BIASINN	Analog input	Bias amplifier inverting input. Connect to AVDD if not used.
29	BIASINP	Analog input/output	Bias amplifier noninverting input or bias input to MUX, configured by register. Connect to AVDD if not used.
30	BIASOUT	Analog output	Bias amplifier output
Power Pad	Pad	—	Thermal pad, must be connected to AVSS

Note: Connect unused analog pins to AVDD.

Figure 2 illustrates the pin configuration (ADX3202Q).

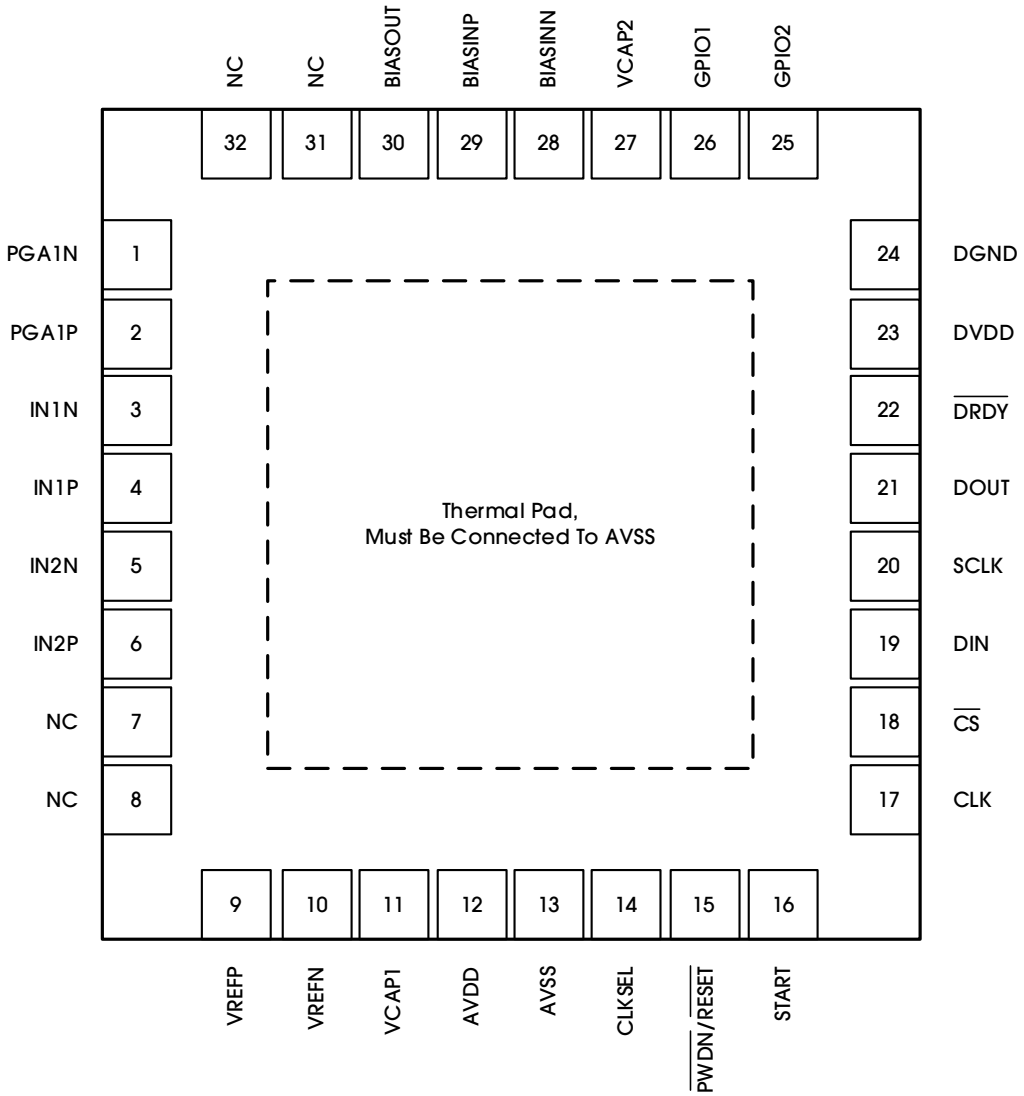


Figure 2. Pin Configuration (ADX3202Q)

Table 4 lists the pin functions (ADX3202Q).

Table 4. Pin Functions (ADX3202Q)

POSITION	PIN	TYPE	DESCRIPTION
1	PGA1N	Analog output	PGA1 inverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1P.
2	PGA1P	Analog output	PGA1 noninverting output, connecting 220pF to AVSS and connecting 4.7nF to PGA1N.
3	IN1N(1)	Analog input	Differential analog negative input 1
4	IN1P(1)	Analog input	Differential analog positive input 1
5	IN2N(1)	Analog input	Differential analog negative input 2
6	IN2P(1)	Analog input	Differential analog positive input 2,
7	NC	—	Do not connect
8	NC	—	Do not connect
9	VREFP	Analog input/output	Positive reference voltage
10	VREFN	Supply	Negative reference voltage, must be connected to AVSS
11	VCAP1	—	Analog bypass capacitor, bandgap output
12	AVDD	Supply	Analog supply
13	AVSS	Supply	Analog ground
14	CLKSEL	Digital input	Master clock select
15	$\overline{\text{PWDN}}/\overline{\text{RESET}}$	Digital input	Power-down or system reset, active low
16	START	Digital input	Start conversion
17	CLK	Digital input	Master clock input
18	$\overline{\text{CS}}$	Digital input	Chip select
19	DIN	Digital input	SPI data in
20	SCLK	Digital input	SPI clock
21	DOUT	Digital output	SPI data out
22	$\overline{\text{DRDY}}$	Digital output	Data ready, active low
23	DVDD	Supply	Digital power supply
24	DGND	Supply	Digital ground
25	GPIO2	Digital input/output	General-purpose I/O 2
26	GPIO1	Digital input/output	General-purpose I/O 1
27	VCAP2	Supply	Analog bypass capacitor, AVDD + 2V
28	BIASINN	Analog input	Bias amplifier inverting input. Connect to AVDD if not used.
29	BIASINP	Analog input/output	Bias amplifier noninverting input or bias input to MUX, configured by register. Connect to AVDD if not used.
30	BIASOUT	Analog output	Bias amplifier output
31	NC	—	Do not connect
32	NC	—	Do not connect
Power Pad	Pad	—	Thermal pad, must be connected to AVSS

Note: Connect unused analog pins to AVDD.

5. SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 5 lists the absolute maximum ratings of the ADX320Q/ADX3202Q.

Table 5. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Power-Supply Voltage	AVDD to AVSS	–0.3	7.0	V
	AVSS to DGND	–3	0.2	
	DVDD to DGND	–0.3	5.0	
	Analog input to AVSS	AVSS – 0.3	AVDD + 0.3	
	Digital input to DVDD	DVSS – 0.3	DVDD + 0.3	
Input Current	To any pin except supply pins	–10	10	mA
	Momentary	–100	100	
	Continuous	–10	10	
Temperature	Operating, T_A	–40	125	°C
	Junction, T_J	–40	125	
	Storage, T_{stg}	–60	150	

Note: Stresses beyond those listed under Table 5 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 7. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD RATINGS

Table 6 lists the ESD ratings of the ADX320Q/ADX3202Q.

Table 6. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per AEC Q100-002(1)	±3500	V
		Charged device model (CDM), per AEC Q100-011	±2000	

Note: AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 RECOMMENDED OPERATING CONDITIONS

Table 7 lists the recommended operating conditions for the ADX320Q/ADX3202Q.

Table 7. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
POWER SUPPLY					
Analog Power Supply, AVDD to AVSS	AVDD	2.7	3	5.5	V
Digital Power Supply, DVDD to DGND	DVDD	1.65	1.8	3.6	V
ANALOG INPUTS					
Voltage		AVSS		AVDD	V
DIGITAL INPUTS					
Voltage		DVSS		DVDD	V
TEMPERATURE RANGE					
Operating Ambient Temperature	T_A	–40		125	°C

5.4 THERMAL INFORMATION

Table 8 lists the thermal information for the ADX320Q/ADX3202Q.

Table 8. Thermal Information

PARAMETER	SYMBOL	QFN-32	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	42.2	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	14.9	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	0.3	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	14.2	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	16.7	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	8.2	°C/W

5.5 ELECTRICAL CHARACTERISTICS

Table 9 lists the electrical characteristics of ADX320Q/ADX3202Q. Minimum and maximum specifications apply from –40°C to 125°C, typical specifications are at 25°C, all specifications are at DVDD = 1.8V, AVDD – AVSS = 3V(1), V_{REF} = 2.4V, external f_{CLK} = 512kHz, data rate = 500SPS, C_{FILTER} = 4.7nF || 220pF(2), and gain = 6, unless otherwise noted.

Table 9. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Full-Scale Differential Input Voltage (AINP – AINN)			±V_{REF} / gain			V
Input Common-Mode Range			See the INPUT COMMON-MODE RANGE section			
Input Capacitance to GND				15		pF
Input Capacitance Differential Input Pair				1		pF
Input Bias Current (PGA Chop = 8kHz)		T_A = 25°C, input = 1.5V			±100	pA
		T_A = –40°C to 125°C, input = 1.5V		±11		pA
DC Input Impedance		No pull-up or pull-down current source	20			GΩ
		Current source sensor burn-out (nA), AVSS + 0.3V < AIN < AVDD – 0.3V		> 10		GΩ
PGA PERFORMANCE						
Gain Settings			1, 2, 3, 4, 6, 8, 12			
Bandwidth (Channel 1)		With a 4.7nF capacitor on PGA output (see the PGA SETTINGS AND INPUT RANGE section for details)		6.8		kHz
ADC PERFORMANCE						
Resolution			24			Bits
Data Rate		f_{CLK} = 512kHz	125		16000	SPS
CHANNEL PERFORMANCE (DC PERFORMANCE)						
Input-Referred Noise			See the NOISE PERFORMANCE section			
Integral Nonlinearity		Full-scale with gain = 6, best fit		2		ppm
Offset Error		CH1		±27		µV
		CH2		±58		µV
Offset Error Drift		CH1		0.016		µV/°C
		CH2		0.4		µV/°C
Offset Error with Calibration		CH1		±1		µV
		CH2		±11		µV
Gain Error		Excluding voltage reference error, CH1		±0.06	±0.23	% of FS
		Excluding voltage reference error, CH2		±0.22	±0.9	% of FS
Gain Error with Calibration				At noise level		
Gain Drift		Excluding voltage reference drift, CH1		3.7		ppm/°C
		Excluding voltage reference drift, CH2		8.4		
Gain Match Between Channels				0.12		% of FS
Common-Mode Rejection Ratio	CMRR	f_{CM} = 50Hz and 60Hz(4)	103	117		dB

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio	PSRR	f_{PS} = 50Hz and 60Hz		95		dB
Crosstalk		f_{IN} = 50Hz and 60Hz		–118		dB
Signal-to-Noise Ratio	SNR	f_{IN} = 10Hz input, gain = 6, CH1		106		dB
Total Harmonic Distortion	THD	10Hz, –0.5dBFs, C_{FILTER} = 4.7nF		–109		dB
		100Hz, –0.5dBFs, C_{FILTER} = 4.7nF		–98		dB
DIGITAL FILTER						
SINC3 Digital Filter		–3dB bandwidth		0.262 f_{DR}		Hz
		Full digital filter setting timing		4		Conversions
AMPLIFIER						
Bias Integrated Noise		BW = 150Hz		1		μV_{RMS}
Gain Bandwidth Product	GBP	50kΩ || 10pF load, gain = 1		150		kHz
Slew Rate	SR	50kΩ || 10pF load, gain = 1		0.1		V/μs
Common-Mode Input Range	CMIR		AVSS + 0.3		AVDD – 0.3	V
Common-Mode Resistor Matching		Internal 200kΩ resistor matching		0.02		%
Short-Circuit Current	I_{SC}			2		mA
Quiescent Power Consumption				3.5		μA
BURN-OUT CURRENT						
Frequency		See the REGISTER MAPS section for settings		(0, 8)		kHz
Current		IBURN-OUT(5:0) = 000000		0.02		nA
		Step size		2.75		nA
Current Accuracy				±20		%
Comparator Threshold Accuracy				±20		mV
EXTERNAL REFERENCE						
Reference Input Voltage		3V supply V_{REF} = (VREFP – VREFN)	2	2.5	VDD – 0.3	V
		5V supply V_{REF} = (VREFP – VREFN)	2	4	VDD – 0.3	V
Negative Input	VREFN			AVSS		V
Positive Input	VREFP			AVSS + 2.5		V
Input Impedance				107		kΩ
INTERNAL REFERENCE						
Output Voltage		Register bit CONFIG2.VREF_4V = 0		2.43		V
		Register bit CONFIG2.VREF_4V = 1		4.043		V
Output Current Drive		Available for external use		100		μA
V_{REF} Accuracy				±0.3		%
V_{REF} Drift		–40°C ≤ T_A ≤ 125°C		10		ppm/°C
Start-Up Time		Settled to 0.2% with 10μF capacitor on VREFP pin		62.4		ms
Quiescent Current Consumption		Register bit CONFIG2.VREF_4V = 0		25		μA
		Register bit CONFIG2.VREF_4V = 1		37		μA
SYSTEM MONITORS						
Analog Supply Reading Error				0.25		%
Digital Supply Reading Error				0.03		%

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Device Wakeup			From power-supply ramp after power-on reset (POR) to $\overline{DRDY}$ low		27		ms
			From power-down mode to $\overline{DRDY}$ low		26		ms
			From STANDBY mode to $\overline{DRDY}$ low		10		ms
VCAP1 Settling Time			1% accuracy		0.4		s
Temp. Sensor Reading	Voltage		T_A = 25°C		143		mV
	Coefficient				377		µV/°C
TEST SIGNAL							
Signal Frequency			See the REGISTER MAPS section for settings		At DC and 1Hz		Hz
Signal Voltage			See the REGISTER MAPS section for settings		±1		mV
Accuracy					±2		%

CLOCK							
Internal Oscillator Clock Frequency			Nominal frequency		512		kHz
Internal Clock Accuracy			T_A = 25°C			±1	%
			–40°C ≤ T_A ≤ 125°C			±2.5	%
Internal Oscillator Start-Up Time					31		µs
Internal Oscillator Power Consumption					35		µW
External Clock Input Frequency			CLKSEL pin = 0, CLK_DIV = 0	485	512	562.5	kHz
			CLKSEL pin = 0, CLK_DIV = 1	1.94	2.048	2.25	MHz
DIGITAL INPUT/OUTPUT							
Logic Level	DVDD = 1.8V to 3.6V	V_{IH}		0.8 DVDD		DVDD + 0.1	V
	DVDD = 1.8V to 3.6V	V_{IL}		–0.1		0.2 DVDD	V
	DVDD = 1.65V to 1.8V	V_{IH}		DVDD – 0.2			V
	DVDD = 1.65V to 1.8V	V_{IL}				0.2	V
	DVDD = 1.65V to 3.6V	V_{OH}	I_{OH} = –500µA	0.8 DVDD			V
	DVDD = 1.65V to 3.6V	V_{OL}	I_{OL} = +500µA			0.2 DVDD	V
	Input current	I_{IN}	0V < $V_{DigitalInput}$ < DVDD	–10		+10	µA
POWER SUPPLY REQUIREMENTS							
Analog Supply	AVDD – AVSS	AVDD		2.7	3	5.5	V
Digital Supply	DVDD – DGND	DVDD		1.65	1.8	3.6	V
AVDD – DVDD				–2.1		3.6	V
SUPPLY CURRENT (AMPLIFIER TURNED OFF)							
I_{AVDD}	ADX3202Q		AVDD – AVSS = 3V		312		µA
			AVDD – AVSS = 5V		350		µA

I_{DVDD}	ADX3202Q		DVDD = 3.3V		51		µA
			DVDD = 1.8V		26		µA
POWER DISSIPATION (ANALOG SUPPLY = 3V, AMPLIFIER TURNED OFF)							
Quiescent Power Dissipation	ADX320Q		Normal mode		601	685	µW
			Standby mode		213		µW
	ADX3202Q		Normal mode		985	1108	µW
			Standby mode		213		µW
Quiescent Power Dissipation, per Channel	ADX320Q		Normal mode		601		µW
	ADX3202Q		Normal mode		493		µW
POWER DISSIPATION (ANALOG SUPPLY = 5V, BIAS AMPLIFIER TURNED OFF)							
Quiescent Power Dissipation	ADX320Q		Normal mode		1120		µW
			Standby mode		378		µW
	ADX3202Q		Normal mode		1800		µW
			Standby mode		378		µW
Quiescent Power Dissipation, per Channel	ADX320Q		Normal mode		1120		µW
	ADX3202Q		Normal mode		900		µW
POWER DISSIPATION IN POWER-DOWN MODE							
Analog Supply = 3V	DVDD = 1.8V				1800		µW
	DVDD = 3.3V				378		µW
Analog Supply = 5V	DVDD = 1.8V				1120		µW
	DVDD = 3.3V				378		µW
TEMPERATURE							
Specified Temperature Range				–40		125	°C
Operating Temperature Range				–40		125	°C
Storage Temperature Range				–60		150	°C

Note 1: Performance is applicable for 5V operation as well. Production testing for limits is performed at 3V.
Note 2: C_{FILTER} is the capacitor across the PGA outputs, see the PGA SETTINGS AND INPUT RANGE section for details.
Note 3: Noise data measured in a 10-second interval. Test not performed in production. Input-referred noise is calculated with input shorted over a 10-second interval.
Note 4: CMRR is measured with a common-mode signal of AVSS + 0.3V to AVDD – 0.3V. The values indicated are the minimum of the two channels.

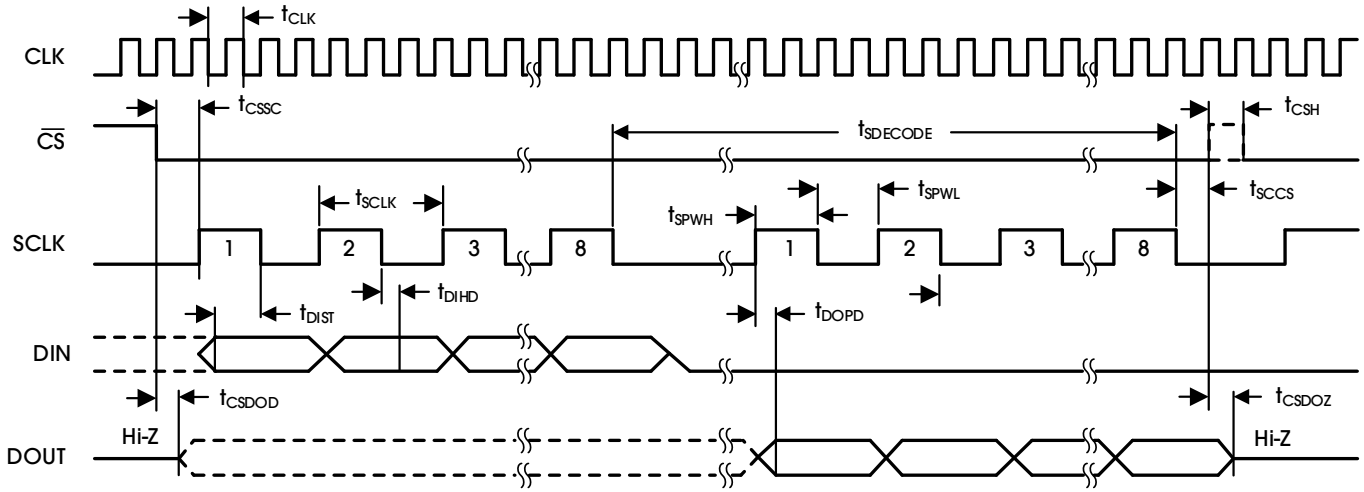
5.6 TIMING REQUIREMENTS

Table 10 lists the timing requirements. Specifications apply from –40°C to 125°C, load on DOUT = 20pF || 100kΩ.

Table 10. Timing Requirements

PARAMETER	SYMBOL	2.7V ≤ DVDD ≤ 3.6V			1.65V ≤ DVDD < 2.7V			UNITS
		MIN	NOM	MAX	MIN	NOM	MAX	
Master Clock Period (CLK_DIV Bit of BO_STAT Register = 0)	t_{CLK}	1775		2170	1775		2170	ns
Master Clock Period (CLK_DIV Bit of BO_STAT Register = 1)		444		542	444		542	ns
$\overline{CS}$ Low to First SCLK, Setup Time	t_{CSSC}	6			17			ns
SCLK Period	t_{SCLK}	50			66.6			ns
SCLK Pulse Width, High and Low	$t_{SPWH, L}$	15			25			ns
DIN Valid to SCLK Falling Edge: Setup Time	t_{DIST}	10			10			ns
Valid DIN after SCLK Falling Edge: Hold Time	t_{DIHD}	10			11			ns
SCLK Rising Edge to DOUT Valid	t_{DOPD}			12			22	ns
$\overline{CS}$ High Pulse	t_{CSH}	2			2			t_{CLK}s
$\overline{CS}$ Low to DOUT Driven	t_{CSDOD}	10			20			ns
Eighth SCLK Falling Edge to $\overline{CS}$ High	t_{SCCS}	3			3			t_{CLK}s
Command Decode Time	$t_{SDECODE}$	4			4			t_{CLK}s
$\overline{CS}$ High to DOUT Hi-Z	t_{CSDOZ}			10			20	ns

Figure 3 shows the serial interface timing.



NOTE: SPI settings are CPOL = 0 and CPHA = 1.

Figure 3. Serial Interface Timing

6. TYPICAL OPERATING CHARACTERISTICS

T_A = 25°C, DVDD = 1.8V, AVDD – AVSS = 3V, V_{REF} = 2.42V, external f_{CLK} = 512kHz, data rate = 500SPS, C_{FILTER} = 4.7nF, and gain = 6, unless otherwise noted.

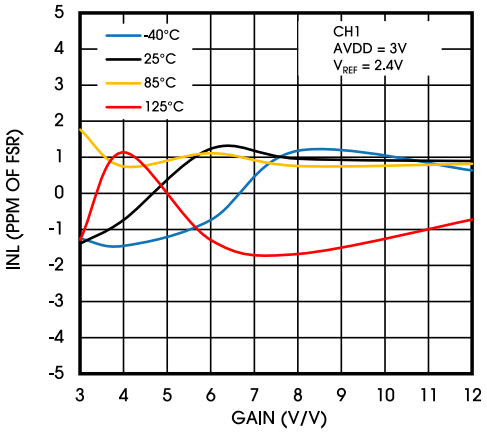


Figure 4. INL vs. Gain

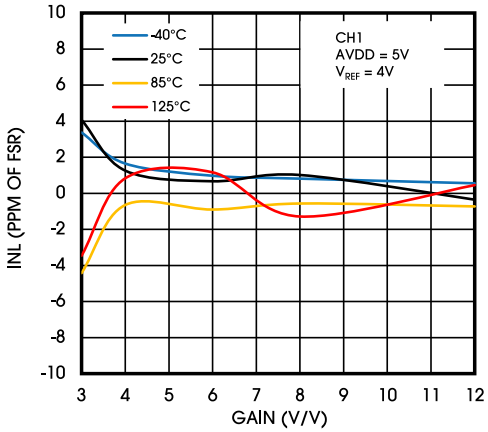


Figure 5. INL vs. Gain

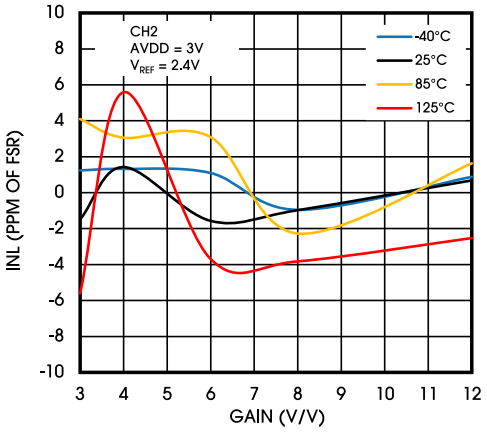


Figure 6. INL vs. Gain

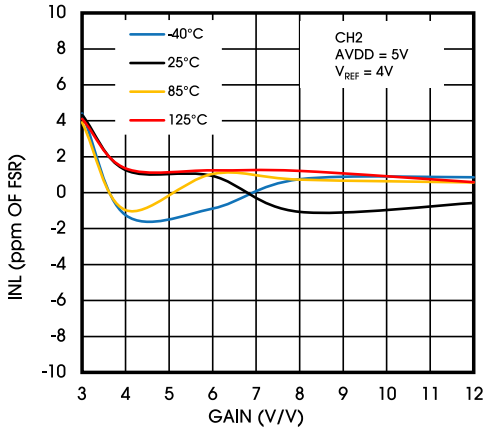


Figure 7. INL vs. Gain

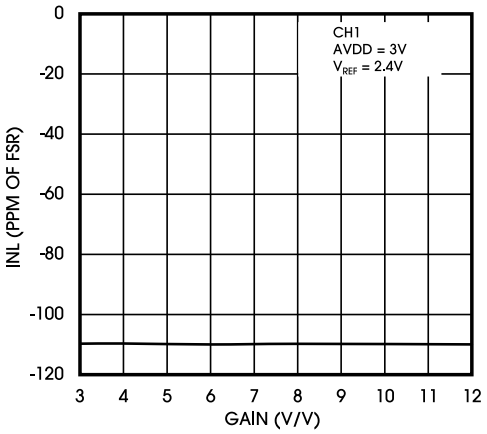


Figure 8. INL vs. Gain

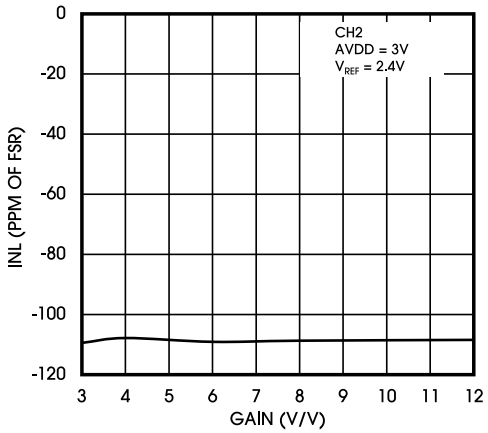


Figure 9. INL vs. Gain

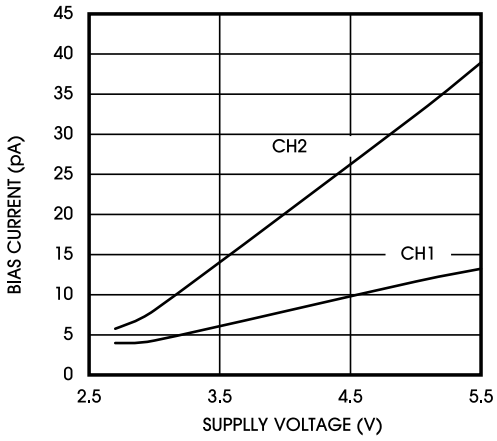


Figure 10. Bias Current vs. Supply Voltage

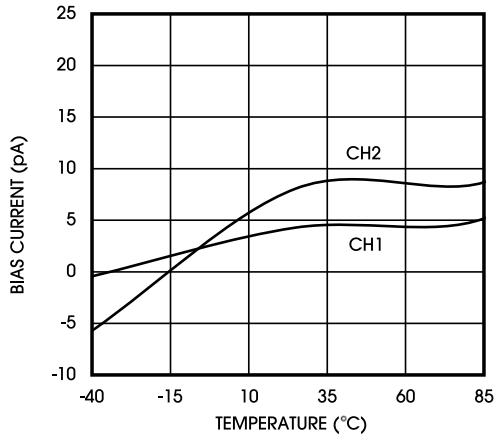


Figure 11. Bias Current vs. Temperature

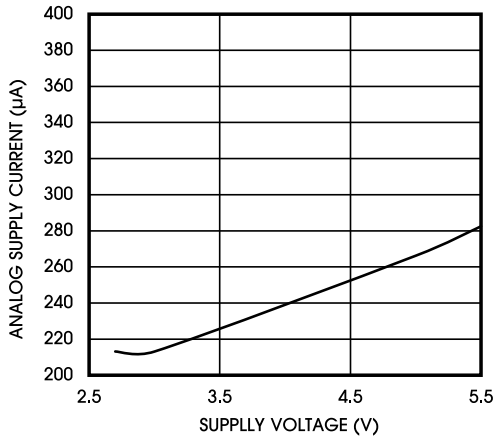


Figure 12. Analog Supply Current vs. Supply Voltage

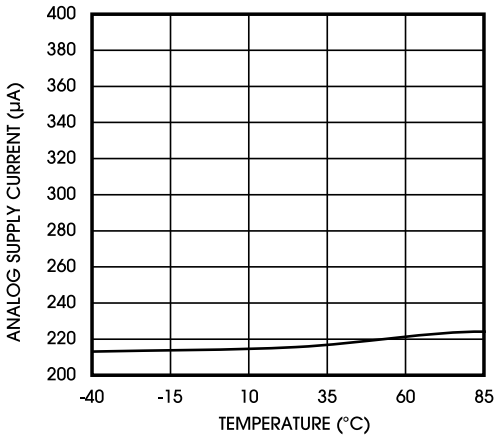


Figure 13. Analog Supply Current vs. Temperature

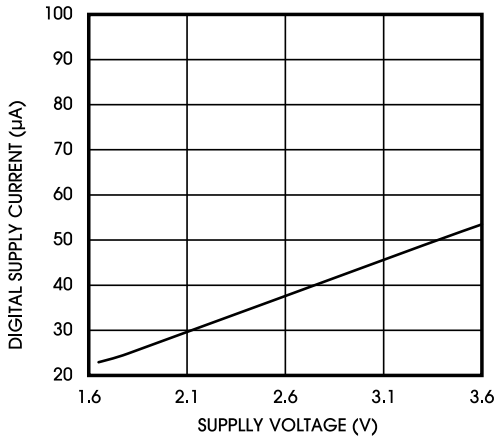


Figure 14. Digital Supply Current vs. Supply Voltage

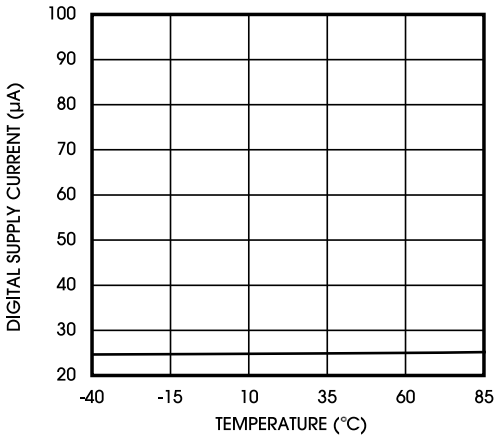


Figure 15. Digital Supply Current vs. Temperature

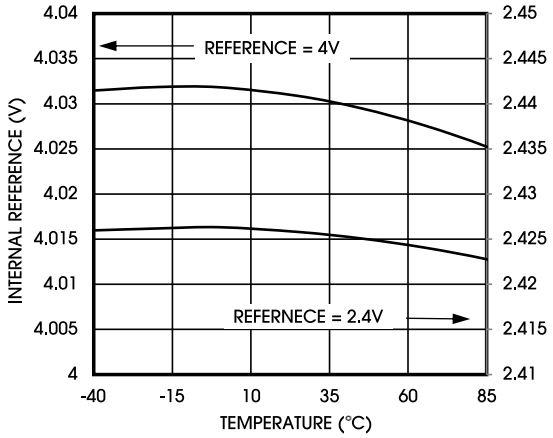


Figure 16. Internal Reference vs. Temperature

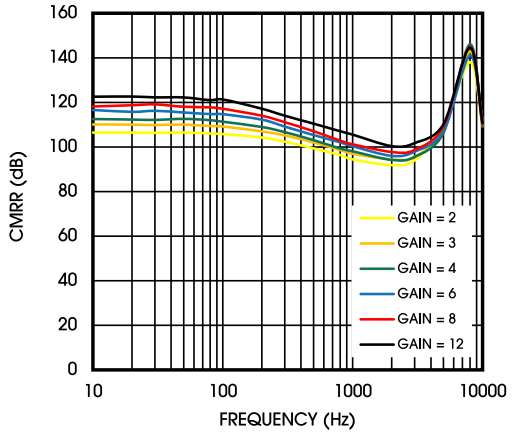


Figure 17. CMRR

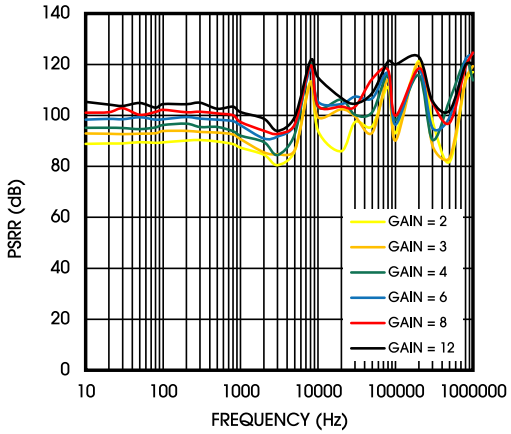


Figure 18. PSRR

7. PARAMETER MEASUREMENT INFORMATION

7.1 NOISE PERFORMANCE

The ADX320Q/ADX3202Q noise performance can be optimized by adjusting the data rate and PGA setting. As the averaging is increased by reducing the data rate, the noise drops correspondingly. Increasing the programmable gain amplifier (PGA) value reduces the input-referred noise, which is particularly useful when measuring low-level biopotential signals. Table 11 through Table 21 summarize the ADX320Q/ADX3202Q noise performance. The data are representative of typical noise performance at T_A = 25°C. The data shown are the result of averaging the readings from multiple devices and are measured with the inputs shorted together. For the shown data rates, the ratio is approximately 6.6.

The data are also representative of the ADX320Q/ADX3202Q noise performance when using a low-noise external reference. In Table 11 through Table 21, μV_{RMS} and μV_{PP} are measured values. Effective resolution (EFF RESOL) and dynamic range (DYN RANGE) are calculated with Equation 1 and Equation 2.

$$\text{Effective Resolution} = \log_2\left(\frac{2 \times V_{REF}}{\text{Gain} \times V_{RMS}}\right) \quad (1)$$

$$\text{Dynamic Range} = 20 \times \log_{10}\left|\frac{V_{REF}}{\sqrt{2} \times V_{RMS\_Noise} \times \text{Gain}}\right| \quad (2)$$

Table 11 through Table 18 show measurements taken with an internal reference on channel 1 in high-resolution mode.

Table 11. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.42V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1				PGA GAIN = 2			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	2.4	15.6	117.0	20.9	1.0	7.4	118.8	21.2
001	250	65.5	3.2	21.3	114.6	20.5	1.4	10.2	116.0	20.8
010	500	131	4.1	32.0	112.4	20.2	1.9	14.4	113.0	20.3
011	1000	262	5.9	46.4	109.2	19.6	2.8	26.3	109.8	19.7
100	2000	524	10.6	107.6	104.2	18.8	5.4	97.7	104.0	18.8
101	4000	1048	42.8	598.0	92.0	16.8	21.2	393.4	92.1	16.8
110	8000	2096	237	3860	77.2	14.3	118.5	1342.8	77.2	14.3

Table 12. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.42V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 3				PGA GAIN = 4			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.8	6.3	117.4	21.0	0.7	5.2	116.0	20.8
001	250	65.5	1.1	8.1	114.6	20.5	0.9	7.3	113.5	20.4
010	500	131	1.5	12.0	111.7	20.1	1.3	9.7	110.6	19.9
011	1000	262	2.1	20.7	108.7	19.6	1.8	15.3	107.6	19.4
100	2000	524	3.8	63.4	103.6	18.7	3.1	50.4	102.9	18.6
101	4000	1048	14.5	251.8	91.9	16.8	10.9	183.5	91.9	16.8
110	8000	2096	78.9	895.2	77.2	14.3	58.8	671.4	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 13. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.42V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 6				PGA GAIN = 8			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.6	4.8	113.3	20.3	0.5	3.9	112.1	20.1
001	250	65.5	0.8	6.8	111.0	19.9	0.7	5.9	109.2	19.6
010	500	131	1.1	9.3	108.4	19.5	1.0	8.8	106.6	19.2
011	1000	262	1.5	12.0	105.5	19.0	1.4	12.2	103.6	18.7
100	2000	524	2.4	33.0	101.3	18.3	2.2	23.8	99.9	18.1
101	4000	1048	7.5	108.4	91.6	16.7	5.8	74.8	91.3	16.7
110	8000	2096	39.3	447.6	77.2	14.3	29.7	335.7	77.1	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 14. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.42V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 12			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.5	4.0	108.4	19.5
001	250	65.5	0.7	5.0	106.4	19.2
010	500	131	1.0	8.8	103.4	18.7
011	1000	262	1.3	11.2	100.6	18.2
100	2000	524	1.9	18.7	97.3	17.7
101	4000	1048	4.4	48.9	90.2	16.5
110	8000	2096	18.6	202.8	77.7	14.4

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 15. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 1				PGA GAIN = 2			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	2.0	14.9	123.1	22.0	1.0	7.0	123.3	22.0
001	250	65.5	2.6	18.8	120.8	21.6	1.3	9.9	120.6	21.5
010	500	131	3.5	27.9	118.3	21.2	1.9	14.9	117.7	21.1
011	1000	262	5.3	51.0	114.7	20.5	2.8	29.1	114.2	20.5
100	2000	524	14.0	253.4	106.2	19.1	7.3	137.5	105.9	19.1
101	4000	1048	69.4	1520.7	92.3	16.8	35.8	716.8	92.0	16.8
110	8000	2096	396.6	5175.0	77.1	14.3	197.2	2237.7	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 16. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 3				PGA GAIN = 4			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.8	5.3	121.7	21.7	0.7	4.7	120.4	21.5
001	250	65.5	1.0	7.9	119.6	21.4	0.9	6.7	118.2	21.1
010	500	131	1.4	10.6	116.7	20.9	1.2	8.8	115.6	20.7
011	1000	262	2.1	21.2	113.3	20.3	1.7	17.3	112.3	20.1
100	2000	524	4.9	93.9	105.8	19.1	3.8	69.4	105.4	19.0
101	4000	1048	23.3	466.2	92.2	16.8	17.6	319.0	92.2	16.8
110	8000	2096	132.3	1491.8	77.1	14.3	98.1	1118.9	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 17. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 6				PGA GAIN = 8			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.6	3.8	118.5	21.2	0.5	3.7	116.9	20.9
001	250	65.5	0.7	5.6	116.4	20.8	0.7	5.6	114.7	20.5
010	500	131	1.0	8.6	113.5	20.4	0.9	7.7	111.8	20.1
011	1000	262	1.4	11.1	110.4	19.8	1.3	11.5	108.8	19.6
100	2000	524	2.8	44.8	104.6	18.9	2.3	33.8	103.7	18.7
101	4000	1048	12.0	203.9	92.0	16.8	9.0	144.2	92.0	16.8
110	8000	2096	66.0	745.9	77.2	14.3	48.9	559.4	77.2	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 18. Input-Referred Noise (μV_{RMS} / μV_{PP}) 5V Analog Supply and 4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 12			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	125	32.75	0.5	3.6	113.7	20.4
001	250	65.5	0.6	4.9	111.3	20.0
010	500	131	0.8	7.9	108.9	19.6
011	1000	262	1.2	10.3	106.0	19.1
100	2000	524	1.9	24.2	101.7	18.4
101	4000	1048	6.2	85.9	91.7	16.7
110	8000	2096	32.6	373.0	77.3	14.3

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 19 through Table 21 show measurements taken with an internal reference on channel 2 in high-speed mode.

Table 19. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 3				PGA GAIN = 4			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	250	65.5	2.7	19.2	106.6	19.2	2.1	15.8	106.3	19.2
001	500	131	3.6	27.6	103.9	18.8	2.9	22.8	103.3	18.7
010	1000	262	5.2	39.4	100.9	18.3	4.2	35.0	100.1	18.1
011	2000	524	7.4	60.6	97.8	17.7	5.9	50.4	97.2	17.6
100	4000	1048	10.6	103.6	94.6	17.2	8.5	78.6	94.0	17.1
101	8000	2096	20.4	293.7	88.9	16.3	15.7	204.5	88.7	16.2
110	16000	4192	82.3	1007.1	76.8	14.3	62.1	671.4	76.8	14.2

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 20. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 6				PGA GAIN = 8			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)	μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	250	65.5	1.6	11.3	105.1	19.0	1.3	8.9	104.1	18.8
001	500	131	2.3	15.9	101.9	18.4	1.9	13.6	101.2	18.3
010	1000	262	3.1	24.2	99.1	18.0	2.7	22.4	98.1	17.8
011	2000	524	4.5	32.0	96.1	17.5	3.8	33.0	95.1	17.3
100	4000	1048	6.4	55.1	93.0	16.9	5.4	45.7	92.0	16.8
101	8000	2096	11.4	124.1	88.0	16.1	9.1	90.4	87.4	16.0
110	16000	4192	41.6	475.6	76.7	14.2	31.7	367.2	76.6	14.2

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

Table 21. Input-Referred Noise (μV_{RMS} / μV_{PP}) 3V Analog Supply and 2.4V Reference(1)

DR BITS OF CONFIG1 REGISTER	OUTPUT DATA RATE (SPS)	–3dB BANDWIDTH (Hz)	PGA GAIN = 12			
			μV_{RMS} (μV)	μV_{PP} (μV)	DYN RANGE (dB)	EFF RESOL (BIT)
000	250	65.5	1.1	7.7	102.5	18.5
001	500	131	1.5	12.5	99.6	18.0
010	1000	262	2.1	17.1	96.5	17.5
011	2000	524	3.0	23.7	93.6	17.0
100	4000	1048	4.3	36.7	90.5	16.5
101	8000	2096	6.9	69.9	86.3	15.8
110	16000	4192	21.5	202.8	76.4	14.2

Note: At least 15s of consecutive sampling readings were used to calculate noise values in this table.

8. DETAILED DESCRIPTION

8.1 OVERVIEW

The ADX320Q/ADX3202Q devices are low-power, multichannel, simultaneously-sampling, 24-bit delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with integrated programmable gain amplifiers (PGAs). These devices integrate various capacitive sensor functions that make them well-suited for multichannel data acquisition systems.

The ADX320Q/ADX3202Q devices have a highly programmable multiplexer that allows for temperature, supply, input short. The PGA gain can be chosen from one of seven settings (1, 2, 3, 4, 6, 8, and 12). The ADCs in the device offer data rates from 125SPS to 16kSPS. Communication to the device is accomplished using an SPI-compatible interface. The device provides two general-purpose I/O (GPIO) pins for general use. Multiple devices can be synchronized using the START pin. The internal reference can be programmed to either 2.4V or 4V. The internal oscillator generates a 512kHz clock.

8.2 FUNCTIONAL BLOCK DIAGRAM

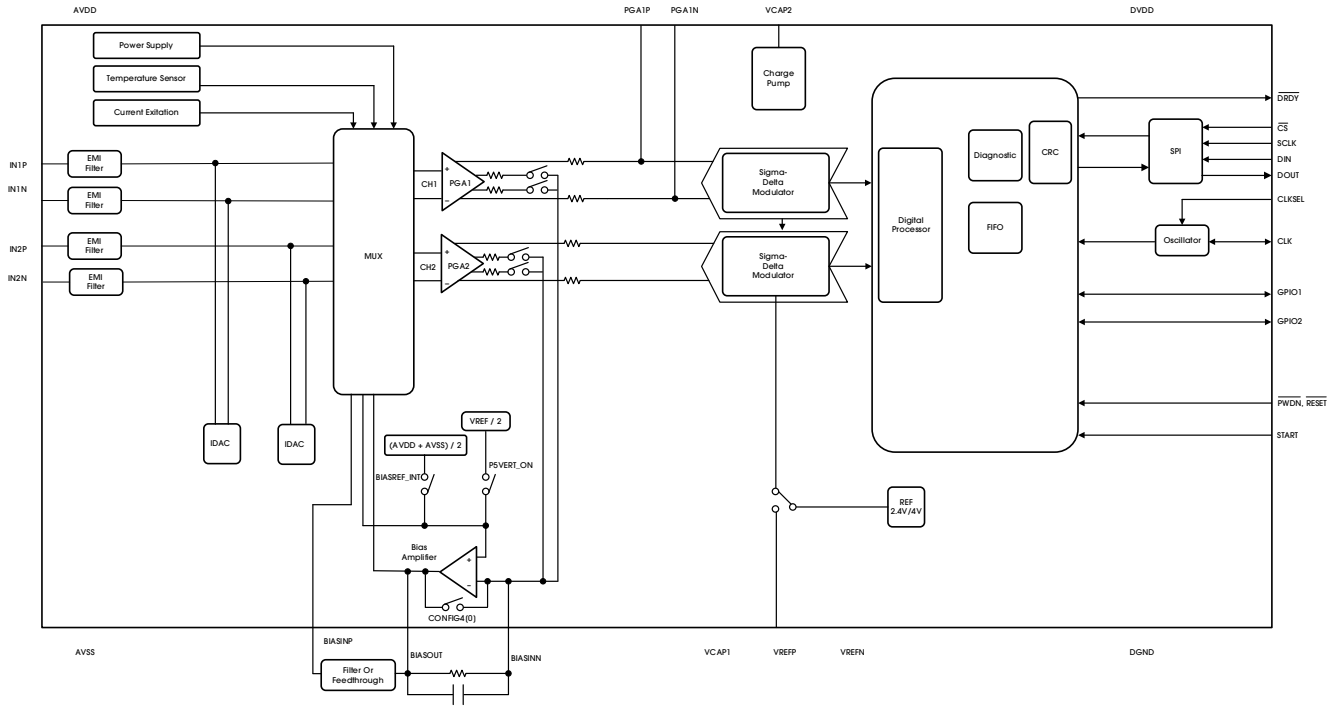


Figure 19. Functional Block Diagram

8.3 FEATURE DESCRIPTION

This section contains details of the ADX320Q/ADX3202Q internal functional elements. The analog blocks are discussed first followed by the digital interface. Blocks implementing specific functions are covered in the end.

Throughout this document, f_{CLK} denotes the signal frequency at the CLK pin, t_{CLK} denotes the signal period of the CLK pin, f_{DR} denotes the output data rate, t_{DR} denotes the output data time period, and f_{MOD} denotes the frequency at which the modulator samples the input.

8.3.1 EMI FILTER

An RC filter at the input acts as an electromagnetic interference (EMI) filter on channels 1 and 2. The –3dB filter bandwidth is approximately 6MHz.

8.3.2 INPUT MULTIPLEXER

The ADX320Q/ADX3202Q input multiplexers are very flexible and provide many configurable signal-switching options. Figure 20 shows the multiplexer for the ADX320Q/ADX3202Q. Note that TESTP, TESTM, and BIASINP/BIASREF are common to both channels. INP and INN are separate for each of the three pins. This flexibility allows for significant device and sub-system diagnostics, calibration, and configuration. Switch settings for each channel are selected by writing the appropriate values to the CH1SET or CH2SET register (see the CH1SET and CH2SET registers for details). More details of the features of the multiplexer are discussed in the INPUT MULTIPLEXER section.

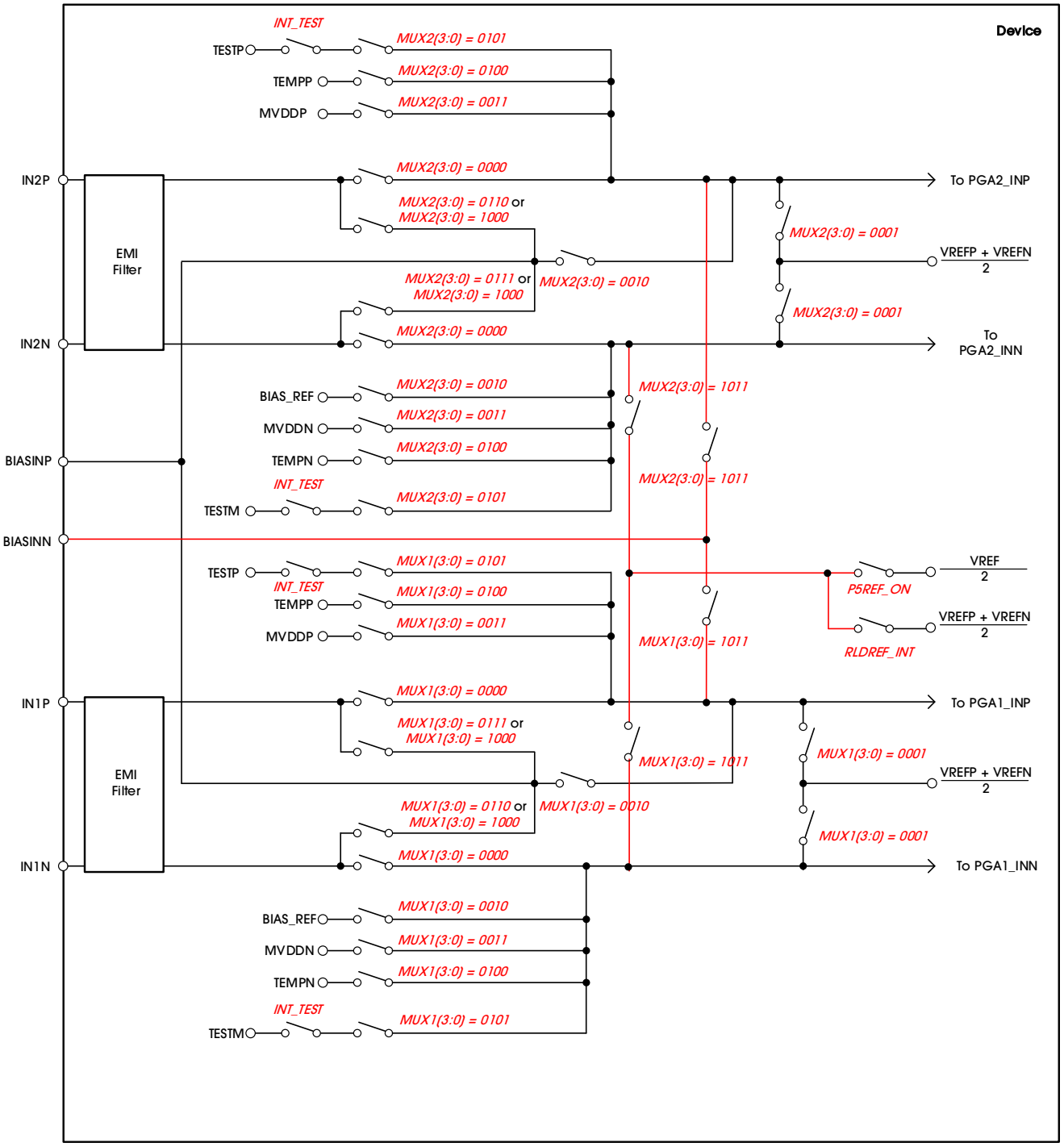
8.3.3 DEVICE NOISE MEASUREMENTS

Setting CHnSET(3:0) = 0001 sets the common-mode voltage of (VREFP + VREFN) / 2 to both inputs of the channel. This setting can be used to test the inherent noise of the device in the user system.

8.3.4 TEST SIGNALS (TESTP AND TESTN)

Setting CHnSET(3:0) = 0101 provides internally-generated test signals for use in sub-system verification at power-up. This functionality allows the entire signal chain to be tested out.

Test signals are controlled through register settings (see the CONFIG2 register for details). INT_TEST enables the test signal and TEST_FREQ controls switching at the required frequency.



NOTE: MVDD monitor voltage supply depends on channel number; see the Supply Measurements (MVDDP, MVDDN) section.

Figure 20. Input Multiplexer Block for Both Channels

8.3.5 TEMPERATURE SENSOR (TEMPP, TEMPN)

The ADX320Q/ADX3202Q contain an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density 16x that of the other, as shown in Figure 21. The difference in diode current densities yields a difference in voltage that is proportional to absolute temperature.

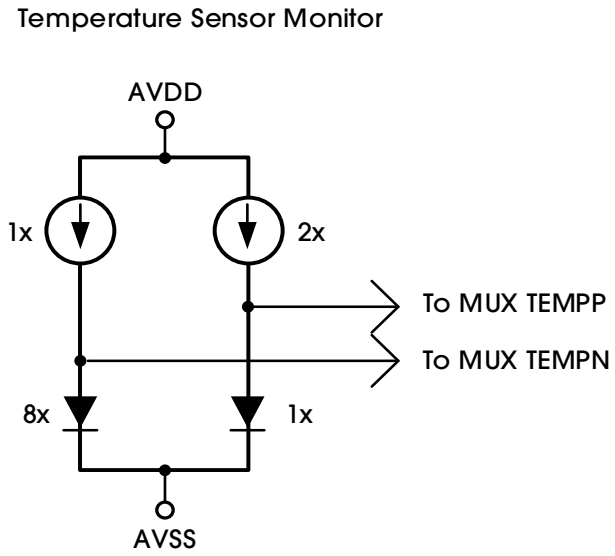


Figure 21. Temperature Sensor Measurement in the Input

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note that self-heating of the ADX320Q/ADX3202Q causes a higher reading than the temperature of the surrounding PCB.

The scale factor of Equation 3 converts the temperature reading to °C. Before using this equation, the temperature reading code must first be scaled to µV.

$$\text{Temperature (°C)} = \left[\frac{\text{Temperature Reading (µV) - 143000µV}}{337\text{µV/°C}}\right] + 25\text{°C} \quad (3)$$

8.3.6 SUPPLY MEASUREMENTS (MVDDP, MVDDN)

Setting CHnSET(3:0) = 0011 sets the channel inputs to different supply voltages of the device. For channel 1, (MVDDP – MVDDN) is (0.5 (AVDD + AVSS)), for channel 2, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

8.3.7 EXCITATION CURRENT SIGNALS

The excitation current signals are fed into the multiplexer before the switches. The comparators that detect the voltage are also connected to the multiplexer block before the switches. For a detailed description of the excitation current block, refer to the SENSOR BURN-OUT section.

8.3.8 AUXILIARY SINGLE-ENDED INPUT

The AMPINP pin is primarily used for routing the bias amplifier voltage to any of inputs. This pin can also be used as a multiple single-ended input channel. The signal at the AMPINP pin can be measured with respect to the midsupply ((AVDD + AVSS) / 2). This measurement is done by configuring the channel multiplexer setting MUXn(3:0) to '0010' in the CH1SET and CH2SET registers.

8.3.9 ANALOG INPUT

The ADX320Q/ADX3202Q analog inputs are fully differential. Assuming PGA = 1, the differential input (INP – INN) can span between $-V_{REF}$ to $+V_{REF}$. Note that the absolute range for INP and INN must be between AVSS – 0.3V and AVDD + 0.3V. Refer to Table 25 for an explanation of the correlation between the analog input and the digital codes. There are two general methods of driving the ADX320Q/ADX3202Q analog input: single-ended or differential, as shown in Figure 22 and Figure 23. Note that INP and INN are 180°C out-of-phase in the differential input method. When the input is single-ended, the INN input is held at the common-mode voltage, preferably at mid-supply. The INP input swings around the same common voltage and the peak-to-peak amplitude is (common-mode + 1/2 V_{REF}) and (common-mode – 1/2 V_{REF}). When the input is differential, the common-mode is given by (INP + INN) / 2. Both INP and INN inputs swing from (common-mode + 1/2 V_{REF} to common-mode – 1/2 V_{REF}). For optimal performance, it is recommended that the ADX320Q/ADX3202Q be used in a differential configuration.

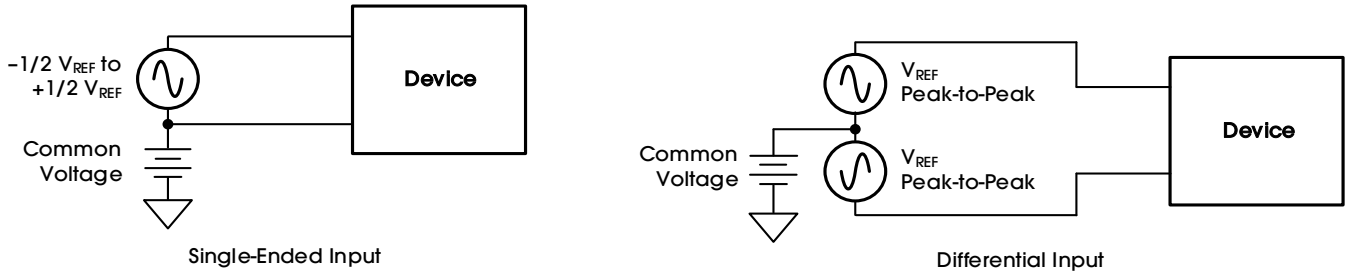
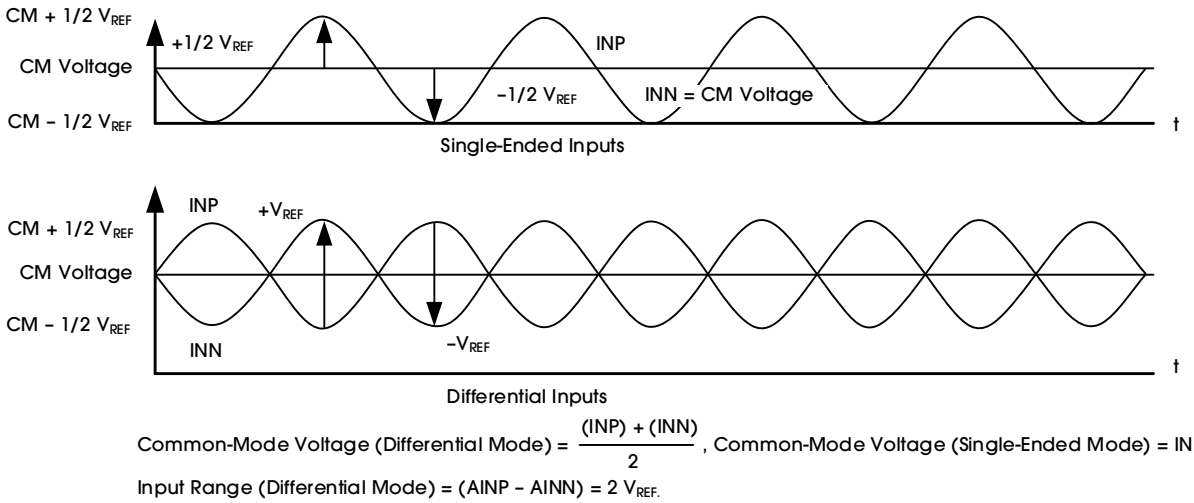


Figure 22. Methods of Driving the ADX320Q/ADX3202Q: Single-Ended or Differential



Common-Mode Voltage (Differential Mode) = $\frac{(INP) + (INN)}{2}$, Common-Mode Voltage (Single-Ended Mode) = INN.

Input Range (Differential Mode) = (AINP – AINN) = 2 V_{REF}.

Figure 23. Using the ADX320Q/ADX3202Q in Single-Ended and Differential Input Modes

8.3.10 PGA SETTINGS AND INPUT RANGE

The PGA is a differential input or differential output amplifier. It has seven gain settings (1, 2, 3, 4, 6, 8, and 12) that can be set by writing to the CHnSET register (see the CH1SET and CH2SET Registers in the REGISTER MAPS section for details). The ADX320Q/ADX3202Q devices have CMOS inputs and hence have negligible current noise.

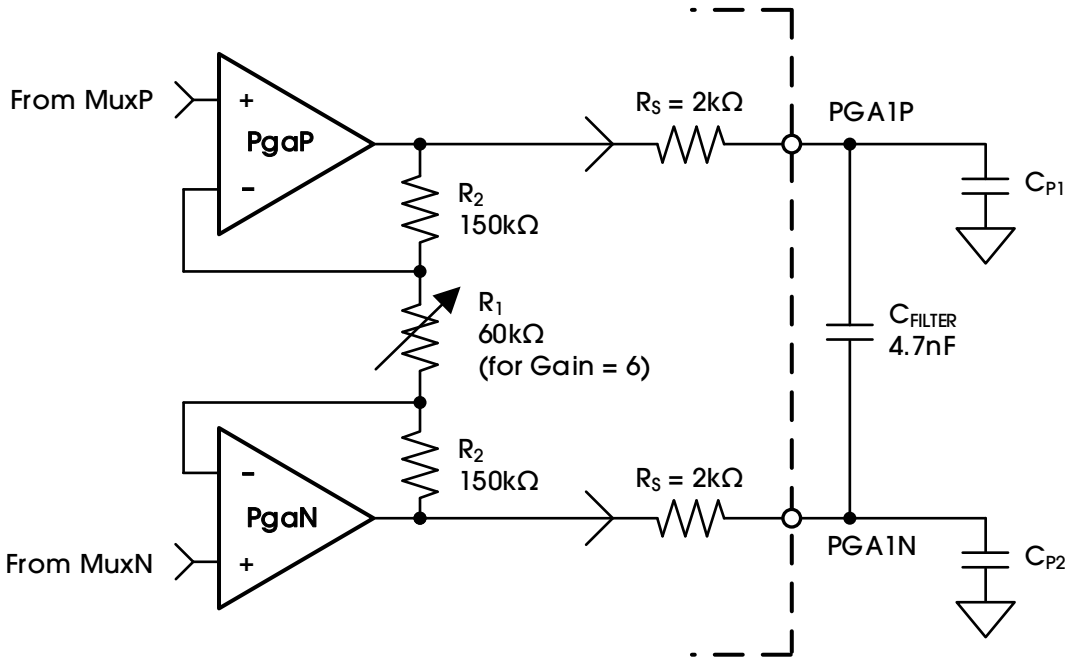


Figure 24. PGA Implementation

The PGA resistor string that implements the gain has 360kΩ of resistance for a gain of 6. This resistance provides a current path across the outputs of the PGA in the presence of a differential input signal. This current is in addition to the quiescent current specified for the device in the presence of a differential signal at the input. The PGA output is filtered by an RC filter before it goes to the ADC. The filter is formed by an internal resistor R_S = 2kΩ and an external capacitor C_{FILTER} (4.7nF, typical). This filter acts as an anti-aliasing filter with the –3dB bandwidth of 8.4kHz. The internal R_S resistor is accurate to 15%, so actual bandwidth will vary. This RC filter also suppresses the glitch at the PGA output caused by ADC sampling. The minimum value of C_{FILTER} that can be used is 4nF. A larger value C_{FILTER} capacitor can be used for increased attenuation at higher frequencies for anti-aliasing purposes. If channel 1 of the ADX320Q/ADX3202Q is used for capacitive measurement, then a 4.7nF external capacitor is recommended. The tradeoff is that a larger capacitor value gives degraded THD performance. See Figure 25 for a diagram explaining the THD versus C_{FILTER} value for a 10Hz input signal. Capacitor 1 and capacitor 2 can be 220pF ± 5% for typical application.

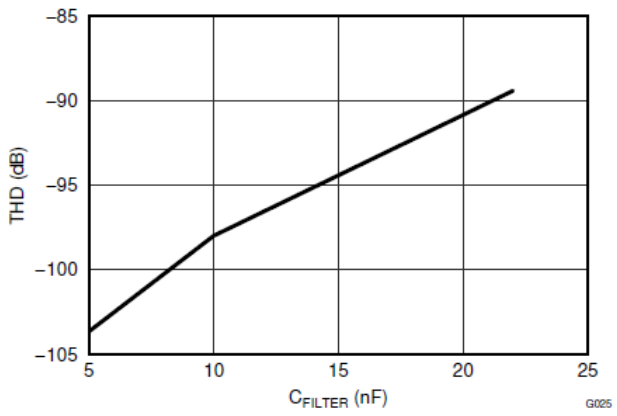


Figure 25. THD vs. C_{FILTER} Value

Special care must be taken in PCB layout to minimize the parasitic capacitance C_{P1} / C_{P2}. The absolute value of these capacitances must be less than 20pF. Ideally, C_{FILTER} should be placed right at the pins to minimize these capacitors. Mismatch between these capacitors will lead to CMRR degradation. Assuming everything else is perfectly matched, the 60Hz CMRR as a function of this mismatch is given by Equation 4.

$$CMRR = 20\log \frac{Gain}{2\pi \times 2e3 \times \Delta C_P \times 60} \quad (4)$$

Where:

- $\Delta C_P = C_{P1} - C_{P2}$.

For example, a mismatch of 20pF with a gain of 6 limits the CMRR to 112dB. If ΔCP is small, then the CMRR is limited by the PGA itself and is as specified in the ELECTRICAL CHARACTERISTICS table. The PGA are chopped internally at either 8, 32, or 64kSPS, as determined by the CHOP bits (see the BIAS_SENS register, bits(7:6)). The digital decimation filter filters out the chopping ripple in the normal path, so the chopping ripple is not a concern. First-order filtering is provided by the RC filter at the PGA output. Additional filtering may be needed to suppress the chopping ripple. If the PGA output is routed to other circuitry, a 20kΩ series resistance must be added in the path near the CFILTER capacitor. The routing should be matched to maintain the CMRR performance.

8.3.10.1 INPUT COMMON-MODE RANGE

The usable input common-mode range of the front end depends on various parameters, including the maximum differential input signal, supply voltage, and PGA gain. Equation 5 describes this range.

$$AVDD - 0.2V - \left(\frac{Gain \times V_{MAX\_DIFF}}{2}\right) > CM > AVSS + 0.2V + \left(\frac{Gain \times V_{MAX\_DIFF}}{2}\right) \quad (5)$$

Where:

- V_{MAX_DIFF} = maximum differential signal at the input of the PGA.

CM = common-mode range.

For example:

If VDD = 3V, gain = 6, and VMAX_DIFF = 350mV, then 1.25V < CM < 1.75V.

8.3.10.2 INPUT DIFFERENTIAL DYNAMIC RANGE

The differential (INP – INN) signal range depends on the analog supply and reference used in the system. Equation 6 shows this range.

$$Max\ (INP - INN) < \frac{V_{REF}}{Gain}, \text{Full-Scale Range} = \frac{\pm V_{REF}}{Gain} = \frac{2V_{REF}}{Gain} \quad (6)$$

The 3V supply, with a reference of 2.4V and a gain of 6, is optimized for power with a differential input signal of approximately 300mV. For higher dynamic range, a 5V supply with a reference of 4V (set by the VREF_4V bit of the CONFIG2 register) can be used to increase the differential dynamic range.

8.3.10.3 ADC ΔΣ MODULATOR

Each channel of the ADX320Q/ADX3202Q has a 24-bit ΔΣ ADC. This converter uses a second-order modulator optimized for low-power applications. The modulator samples the input signal at the rate of $f_{MOD} = f_{CLK} / 4$ or $f_{CLK} / 16$, as determined by the CLK_DIV bit. In both cases, the sampling clock has a typical value of 128kHz. As in the case of any ΔΣ modulator, the ADX320Q/ADX3202Q noise is shaped until $f_{MOD} / 2$, as shown in Figure 26. The on-chip digital decimation filters explained in the DIGITAL DECIMATION FILTER section can be used to filter out the noise at higher frequencies. These on-chip decimation filters also provide antialias filtering. This feature of the ΔΣ converters drastically reduces the complexity of analog antialiasing filters that are typically needed with nyquist ADCs.

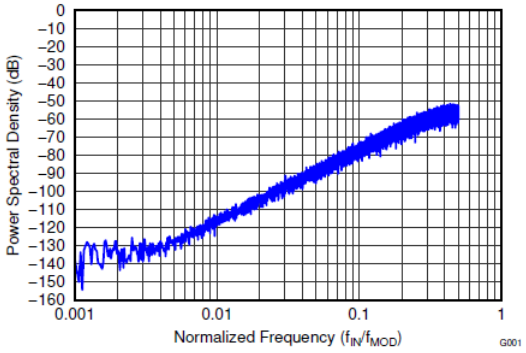


Figure 26. Power Spectral Density (PSD) of a ΔΣ Modulator

8.3.11 DIGITAL DECIMATION FILTER

The digital filter receives the modulator output and decimates the data stream. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rates.

8.3.12 SINC FILTER STAGE (SINX / X)

The sinc filter is a variable decimation rate, third-order, low-pass filter. Data are supplied to this section of the filter from the modulator at the rate of f_{MOD}. The sinc filter attenuates the high-frequency noise of the modulator, then decimates the data stream into parallel data. The decimation rate affects the overall data rate of the converter.

Equation 7 shows the scaled Z-domain transfer function of the sinc filter.

$$|H(z)| = \left| \frac{1 - Z^{-N}}{1 - Z^{-1}} \right|^3 \tag{7}$$

The frequency-domain transfer function of the sinc filter is shown in Equation 8.

$$|H(f)| = \left| \frac{\sin\left[\frac{N\pi f}{f_{MOD}}\right]}{N \times \sin\left[\frac{\pi f}{f_{MOD}}\right]} \right|^3 \tag{8}$$

Where:

- N = decimation ratio

The sinc filter has notches (or zeroes) that occur at the output data rate and multiples thereof. At these frequencies, the filter has infinite attenuation. Figure 27 shows the sinc filter frequency response and Figure 28 shows the sinc filter roll-off. With a step change at input, the filter takes 3 t_{DR} to settle. After a START signal rising edge, the filter takes t_{SETTLE} time to give the first data output. The filter settling times at various data rates are discussed in the START section. Figure 29 and Figure 30 show the filter transfer function until f_{MOD} / 2 and f_{MOD} / 16, respectively, at different data rates. Figure 31 shows the transfer function extended until 4 f_{MOD}. It can be seen that the ADX320Q/ADX3202Q passband repeats itself at every f_{MOD}. The input R-C anti-aliasing filters in the system should be chosen such that any interference in frequencies around multiples of f_{MOD} are attenuated sufficiently.

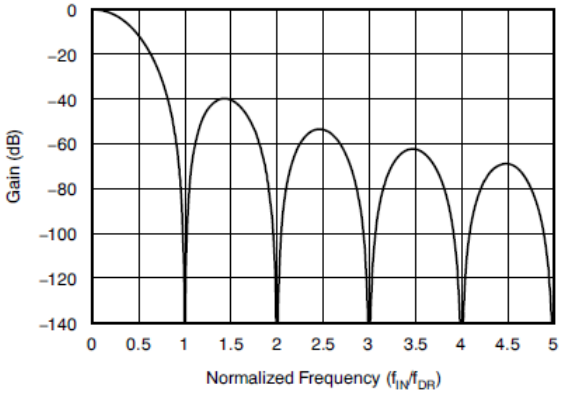


Figure 27. Sinc Filter Frequency Response

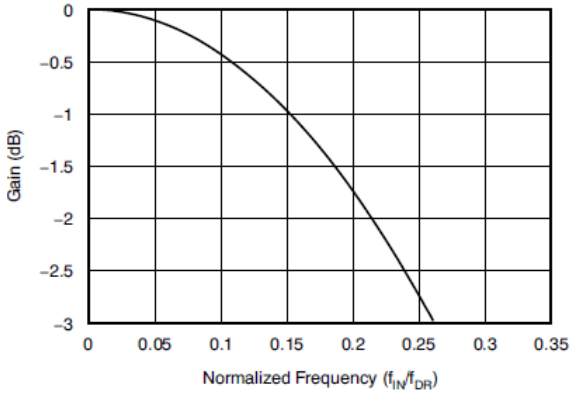


Figure 28. Sinc Filter Roll-Off

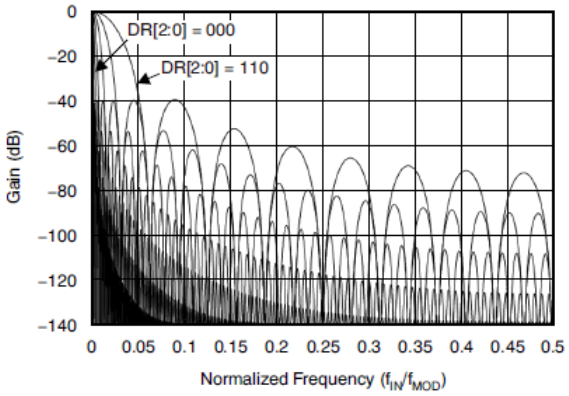


Figure 29. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 2

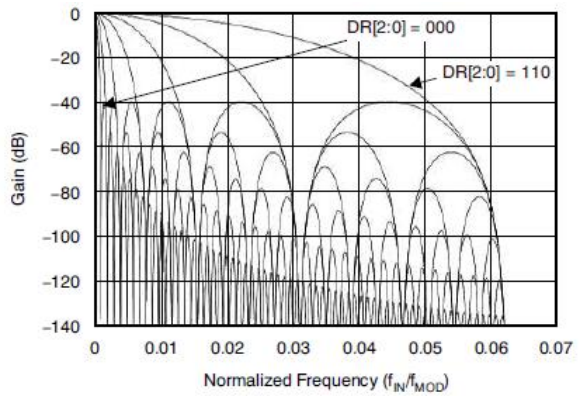


Figure 30. Transfer Function of On-Chip Decimation Filters Until f_{MOD} / 16

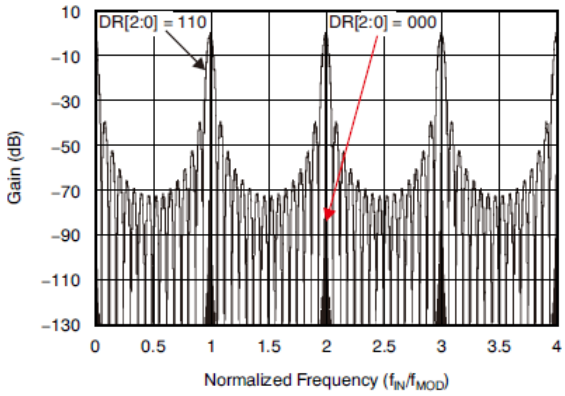
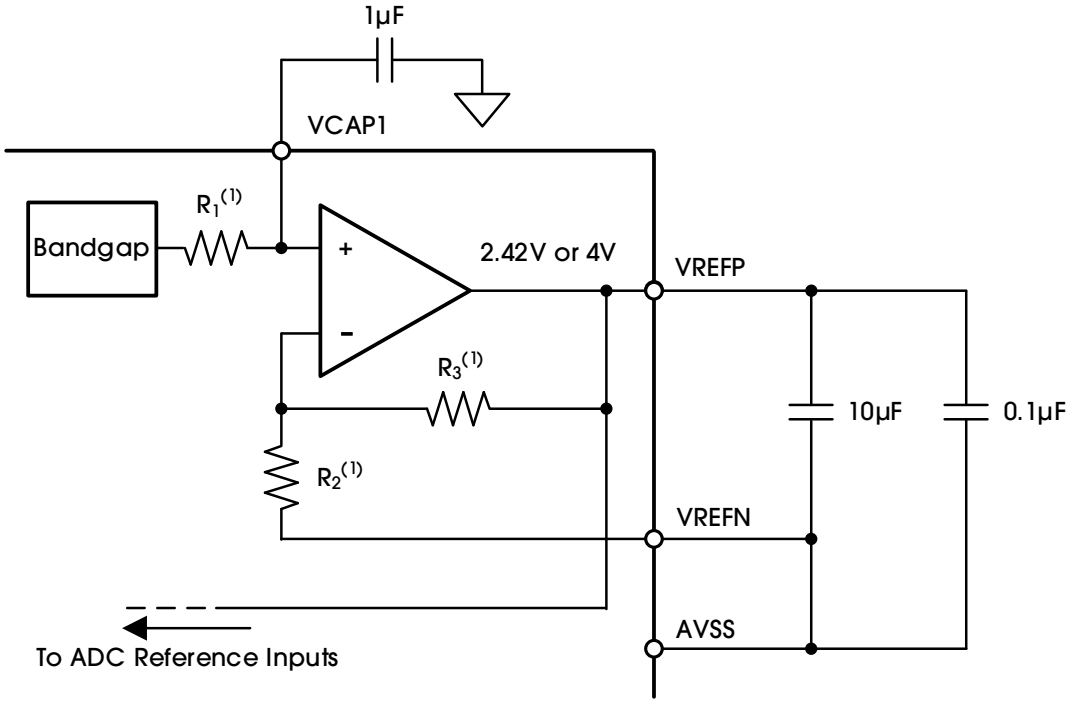


Figure 31. Transfer Function of On-Chip Decimation Filters Until 4 f_{MOD} for DR(2:0) = 000 and DR(2:0) = 110

8.3.13 REFERENCE

Figure 32 shows a simplified block diagram of the ADX320Q/ADX3202Q internal reference. The reference voltage is generated with respect to AVSS. The VREFN pin must always be connected to AVSS.



(1) For V_{REF} = 2.42V: R_1 = 100kΩ, R_2 = 200kΩ, and R_3 = 200kΩ. For V_{REF} = 4V: R_1 = 84kΩ, R_2 = 120kΩ, and R_3 = 280kΩ.

Figure 32. Internal Reference

The external band-limiting capacitors determine the amount of reference noise contribution. For high-end capacitive sensing systems, the capacitor values should be chosen such that the bandwidth is limited to less than 10Hz so that the reference noise does not dominate the system noise. When using a 3V analog supply, the internal reference must be set to 2.4V. In case of a 5V analog supply, the internal reference can be set to 4V by setting the VREF_4V bit in the CONFIG2 register.

Alternatively, the internal reference buffer can be powered down and VREFP can be applied externally. Figure 33 shows a typical external reference drive circuitry. Power-down is controlled by the PDB_REFBUF bit in the CONFIG2 register. This power-down is also used to share internal references when two devices are cascaded. By default, the device wakes up in external reference mode.

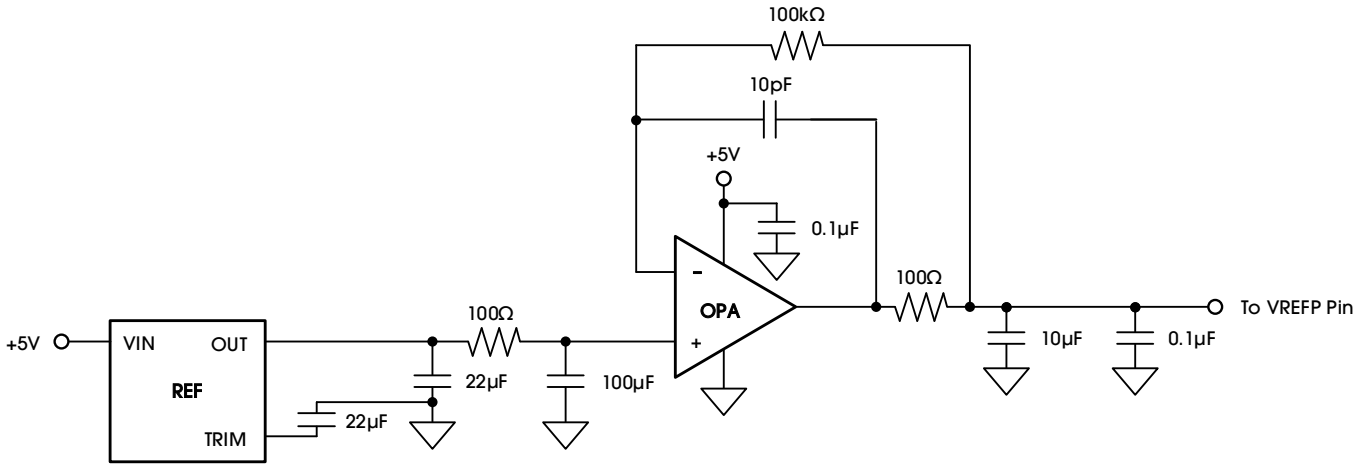


Figure 33. External Reference Driver

8.3.14 CLOCK

The ADX320Q/ADX3202Q devices provide two different methods for device clocking: internal and external. Internal clocking is ideally suited for low-power, battery-powered systems. The internal oscillator is trimmed for accuracy at room temperature. Over the specified temperature range the accuracy varies, see the ELECTRICAL CHARACTERISTICS. Clock selection is controlled by the CLKSEL pin and the CLK_EN register bit.

The CLKSEL pin selects either the internal or external clock. The CLK_EN bit in the CONFIG2 register enables and disables the oscillator clock to be output in the CLK pin. A truth table for these two pins is shown in Table 22. The CLK_EN bit is useful when multiple devices are used in a daisy-chain configuration. It is recommended that during power-down the external clock be shut down to save power.

Table 22. CLKSEL Pin and CLK_EN Bit

CLKSEL PIN	CONFIG2.CLK_EN BIT	CLOCK SOURCE	CLK PIN STATUS
0	X	External clock	Input: external clock
1	0	Internal clock oscillator	3-state
1	1	Internal clock oscillator	Output: internal clock oscillator

The ADX320Q/ADX3202Q devices have the option to choose between two different external clock frequencies (512kHz or 2.048MHz). This frequency is selected by setting the CLK_DIV bit (bit 6) in the BO_STAT register. The modulator must be clocked at 128kHz, regardless of the external clock frequency. Figure 34 shows the relationship between the external clock (f_{CLK}) and the modulator clock (f_{MOD}). The default mode of operation is f_{CLK} = 512kHz. The higher frequency option has been provided to allow the SPI to run at a higher speed. SCLK can be only twice the speed of f_{CLK} during a register read or write, see section on sending multi-byte commands. Having the 2.048MHz option allows for register read and writes to be performed at SCLK speeds up to 4.096MHz.

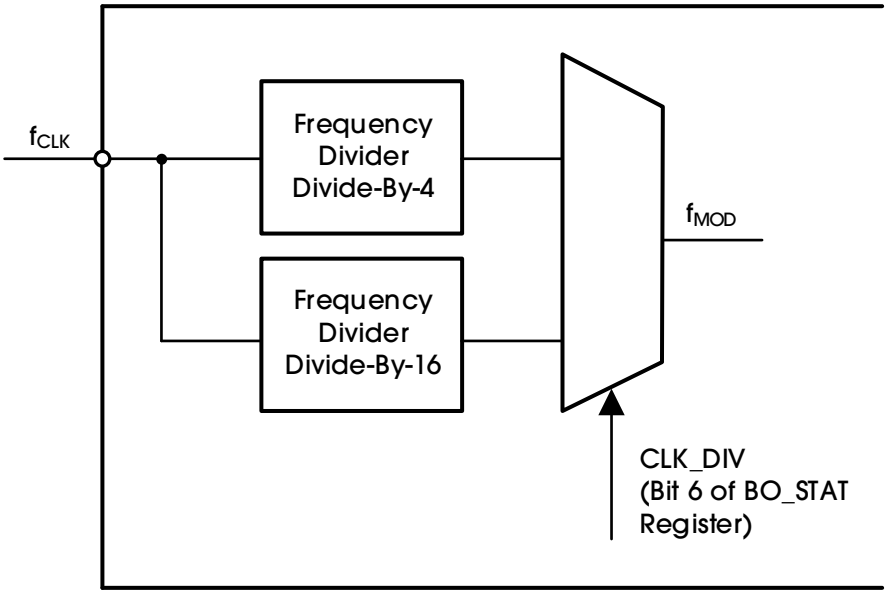


Figure 34. Relationship Between External Clock (f_{CLK}) and Modulator Clock (f_{MOD})

The ADX320Q/ADX3202Q can set internal oscillator clock to detect external clock when the CLKSEL pin is 0. If the external clock missing extends 255 internal oscillator cycles, the device clock source will be switched to internal oscillator clock and the CLK_MISS field of MOD_STAT1 will be set. After CLK_MISS is set a chip level, reset is needed.

8.3.15 POWER MODE

The device has four working modes to balance the performance and power for dedicated application usage. Table 23 shows the configuration for different modes. High-Speed has better performance and the higher power consumption, while High-Resolution has the better power consumption compared with the High-Speed mode on the same data rate setting. Follow Table 23 to configure the power mode.

Table 23. WMODE Setting

WMODE	CLOCK FREQUENCY	BO_STAT(6:5)	PWR(6)	BO_SENS(6)	DR(2:0) and ODR
High-Speed	1.024MHz /2.048MHz	2'b00 / 2'b10'	0: f_{MOD} = 256kHz	0	DR = 0, ODR = 250SPS
High-Resolution	512kHz / 2.048MHz	2'b00 /2'b01	0: f_{MOD} = 128kHz	0	DR = 0, ODR = 125SPS

With different working mode, the data rate can be configured to meet application requirements. The f_{MOD} is decided by WMODE, clock frequency, and clock divider.

Table 24. Data Rate Configuration

BIT	OVERSAMPLING RATIO	f_{MOD} = 256kHz	f_{MOD} = 128kHz
000	f_{MOD} / 1024	250SPS	125SPS
001	f_{MOD} / 512	500SPS	250SPS
010	f_{MOD} / 256	1kSPS (default)	500SPS (default)
011	f_{MOD} / 128	2kSPS	1kSPS
100	f_{MOD} / 64	4kSPS	2kSPS
101	f_{MOD} / 32	8kSPS	4kSPS
110	f_{MOD} / 16	16kSPS	8kSPS
111	Do not use	Do not use	Do not use

8.3.16 DATA FORMAT

The ADX320Q/ADX3202Q devices output 24 bits of data per channel in binary two's complement format, MSB first. The LSB has a weight of V_{REF} / (2^{23} – 1). A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 25 summarizes ideal output codes for different input signals. All 24 bits toggle when the analog input is at positive or negative full-scale.

Table 25. Ideal Output Code versus Input Signal

INPUT SIGNAL, V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
≥ V_{REF}	7FFFFFh
+V_{REF} / (2^{23} – 1)	000001h
0	000000h
–V_{REF} / (2^{23} – 1)	FFFFFFh
≤ –V_{REF} (2^{23} / 2^{23} – 1)	800000h

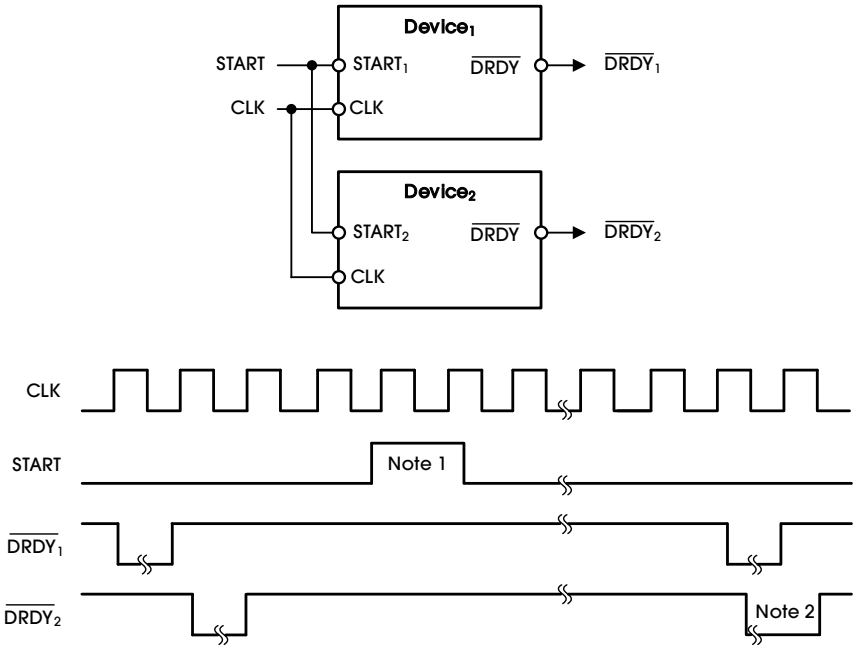
Note: Excludes effects of noise, linearity, offset, and gain error.

8.3.17 MULTIPLE DEVICE CONFIGURATION

The ADX320Q/ADX3202Q devices are designed to provide configuration flexibility when multiple devices are used in a system. The serial interface typically needs four signals: DIN, DOUT, SCLK, and $\overline{CS}$. With one additional chip select signal per device, multiple devices can be connected together. The number of signals needed to interface n devices is 3 + n.

The bias amplifiers can be daisy-chained as explained in the BIAS CONFIGURATION WITH MULTIPLE DEVICES section. To use the internal oscillator in a daisy-chain configuration, one of the devices must be set as the master for the clock source with the internal oscillator enabled (CLKSEL pin = 1) and the internal oscillator clock brought out of the device by setting the CLK_EN register bit to '1'. This master device clock is used as the external clock source for the other devices.

When using multiple devices, the devices can be synchronized with the START signal. The delay from START to the $\overline{DRDY}$ signal is fixed for a fixed data rate (see the START section for more details on the settling times). Figure 35 shows the behavior of two devices when synchronized with the START signal.



(1) Start pulse must be at least one t_{MOD} cycle wide.
(2) Settling time number uncertainty is one t_{MOD} cycle.

Figure 35. Synchronizing Multiple Converters

8.3.18 STANDARD MODE

Figure 36 shows a configuration with two devices cascaded together. 2. Together, they create a system with four channels. DOUT, SCLK, and DIN are shared. Each device has its own chip select. When a device is not selected by the corresponding $\overline{CS}$ being driven to logic 1, the DOUT of this device is high-impedance. This structure allows the other device to take control of the DOUT bus.

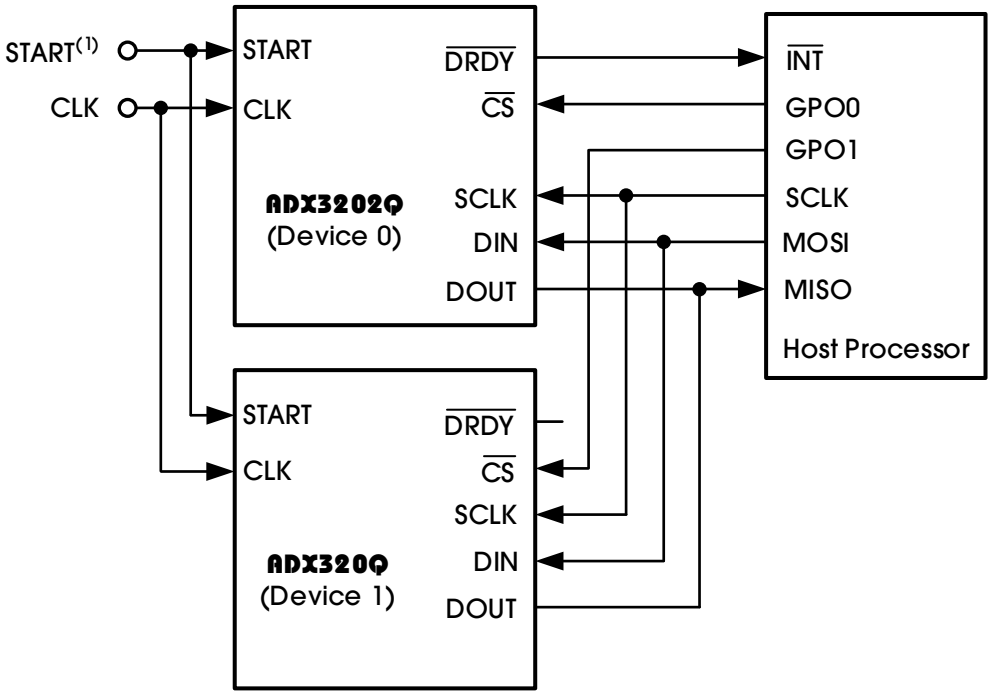
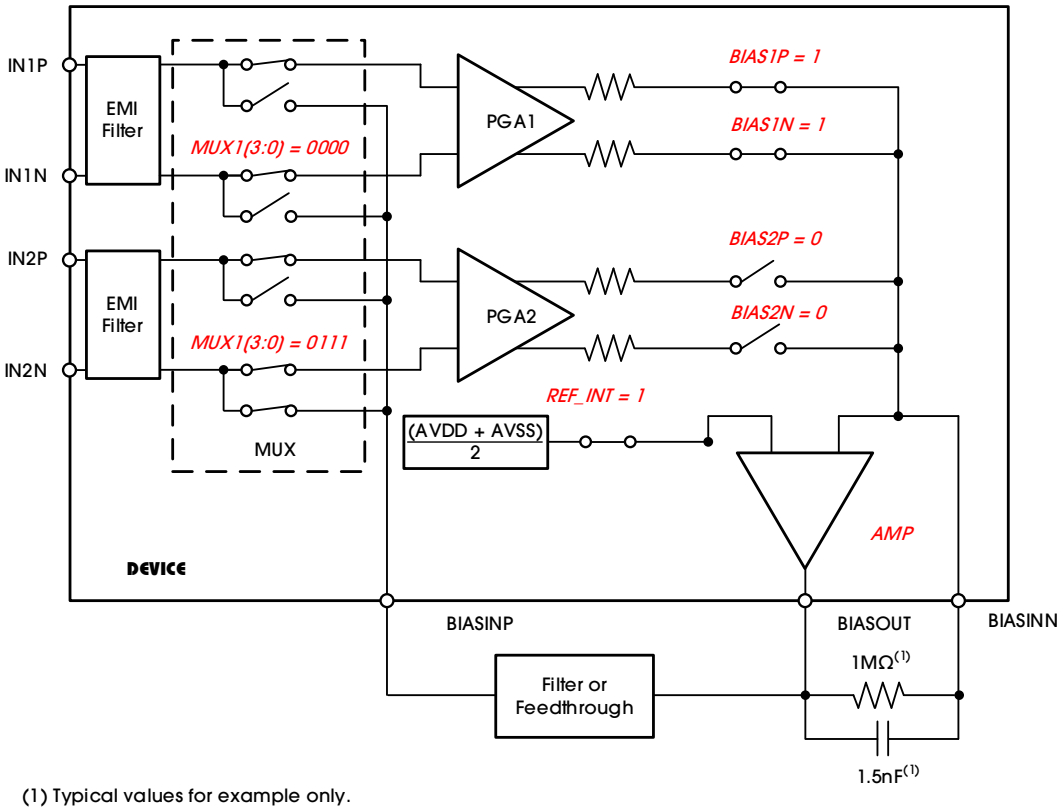


Figure 36. Multiple Device Configurations

8.3.19 INPUT MULTIPLEXER

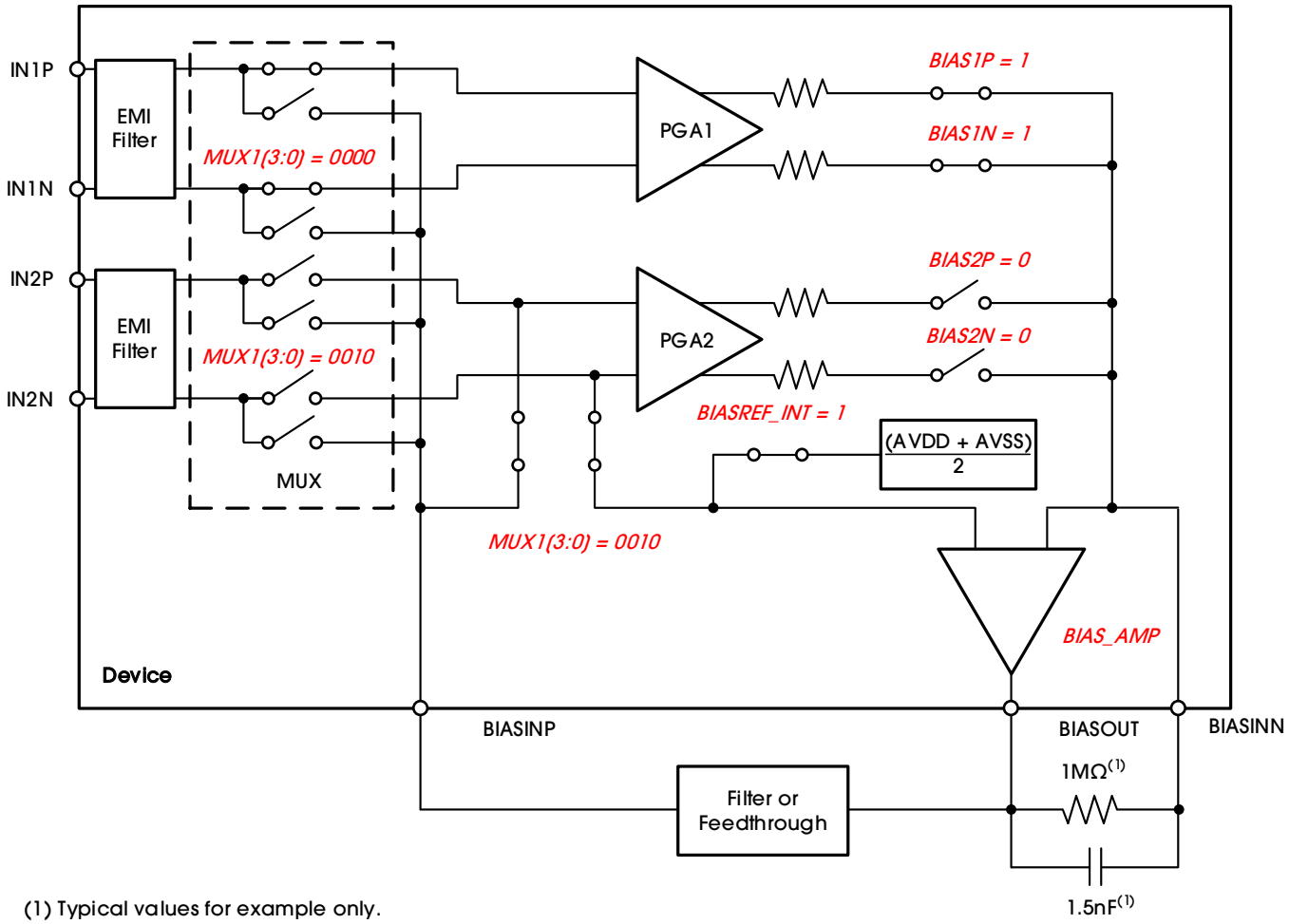
The input multiplexer has special functions for the bias drive signal. The BIAS signal is available at the BIASOUT pin once the appropriate channels are selected for BIAS derivation, feedback elements are installed external to the chip, and the loop is closed. This signal can be fed after filtering or fed directly into the BIASINP pin, as shown in Figure 37. This BIASINP signal can be multiplexed into any one of the input by setting the MUX bits of the appropriate channel set registers to '0110' for P-side or '0111' for N-side. Figure 37 shows the BIAS signal generated from channel 1 and routed to the N-side of channel 2. This feature can be used as the reference signal to drive the common-mode voltage. Note that the corresponding channel cannot be used and can be powered down.



(1) Typical values for example only.

Figure 37. Example BIAS Signal Configured to be Routed to IN2N

The BIASOUT signal can also be routed to a channel (that is not used for the calculation of BIAS) for measurement. Figure 38 shows the register settings to route the BIASINP signal to channel 2. The measurement is done with respect to the voltage (AVDD + AVSS) / 2. This feature is useful for debugging purposes during product development.



(1) Typical values for example only.

Figure 38. BIASOUT Signal Configured to be Read Back by Channel 2

8.3.20 SENSOR BURN-OUT

The ADX320Q/ADX3202Q sensor burn-out functional blocks provide significant flexibility to the user to choose from various sensor burn-out strategies. Though called sensor burn-out, this is in fact an sensor detection.

The basic principle is to inject an excitation signal and measure the response to find out if the sensor is off. As shown in the sensor burn-out functional block diagram in Figure 39, this circuit provides two different methods of determining the state of the sensor. The methods differ in the frequency content of the excitation signal. BURN-OUT can be selectively done on a per channel basis using the BO_SENS register. Also, the internal excitation circuitry can be disabled and just the sensing circuitry can be enabled.

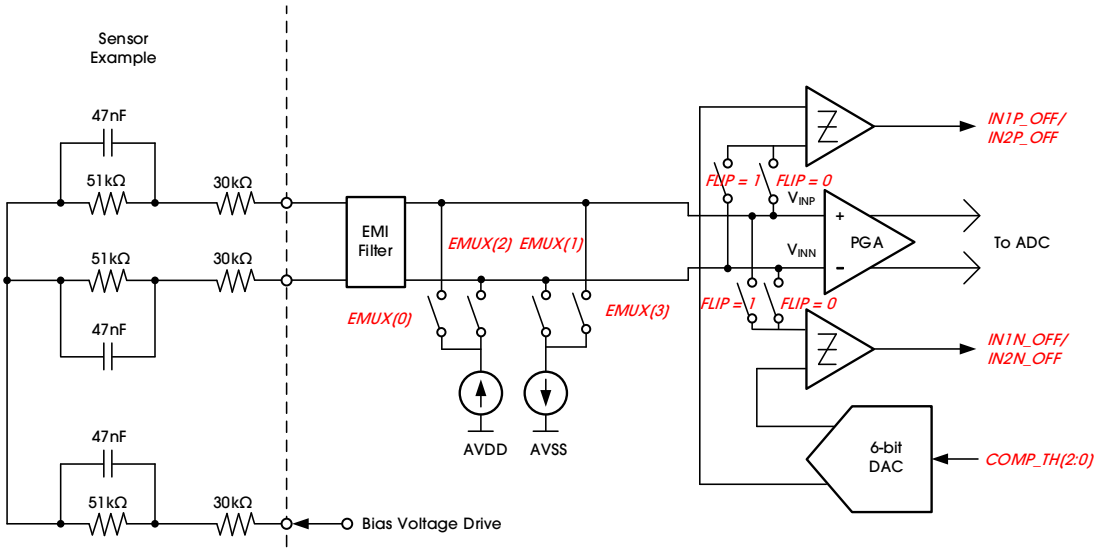
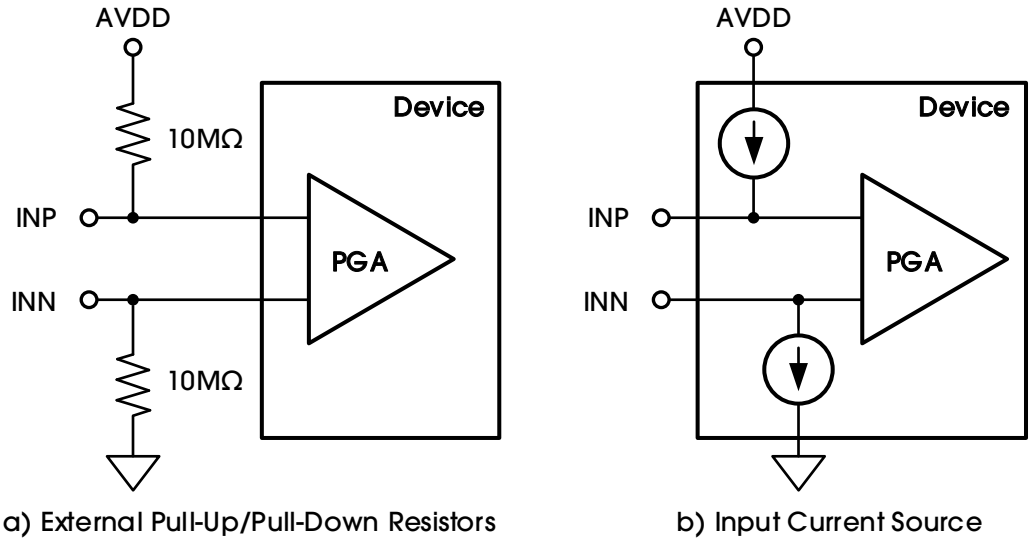


Figure 39. Sensor Burn-Out

The block shows DAC provides a programmable reference current and programmable DAC output voltage for comparators. Burn-out has the debounce filter to remove the 50Hz/60Hz power frequency interference by enabling debounce (1:0) of BO_CFG register. The debounce time is the setting time for the first valid data.

In this method, the burn-out excitation is with a DC signal. The DC excitation signal can be chosen from either an external pull-up or pull-down resistor or a current source or sink, as shown in Figure 40. One side of the channel is pulled to supply and the other side is pulled to ground. The internal current source and current sink can be swapped by setting the FLIP1 and FLIP2 bits in the BO_SENS register. In case of current source or sink, the magnitude of the current can be set by using the IBURN-OUT(1:0) bits in the BO register. The current source or sink gives larger input impedance compared to the 10MΩ pull-up or pull-down resistor.



a) External Pull-Up/Pull-Down Resistors b) Input Current Source

Figure 40. DC Burn-Out Excitation Options

Sensing of the response can be done either by looking at the digital output code from the device or by monitoring the input voltages with an on-chip comparator. If either of the sensors is off, the pull-up resistors and the pull-down resistors saturate the channel. By looking at the output code, it can be determined that either the P-side or the N-side is off. To pinpoint which one is off, the comparators must be used. The input voltage is also monitored using a comparator and a 6-bit digital-to-analog converter (DAC) whose levels are set by the COMP_TH(2:0) bits in the BO register. The output of the comparators are stored in the BO_STAT register. These two registers are available as a part of the output data stream. (See the DATA OUTPUT (DOUT) section.) If DC burn-out is not used, the burn-out comparators can be powered down by setting the PDB_BO_COMP bit in the CONFIG2 register.

BO_ISTEP can be used to adjust the current value and comparator voltage for sensor burn-out. If CUR_LEVEL of BO_ISTEP is 0, the amplitude of the excitation current used for sensor burn-out can be programmed in the ISTEP field, where codes 0 to 63 result in currents ranging from 0nA to 174nA in steps of 2.75nA. An example procedure to turn on DC burn-out is given in the BURN-OUT section.

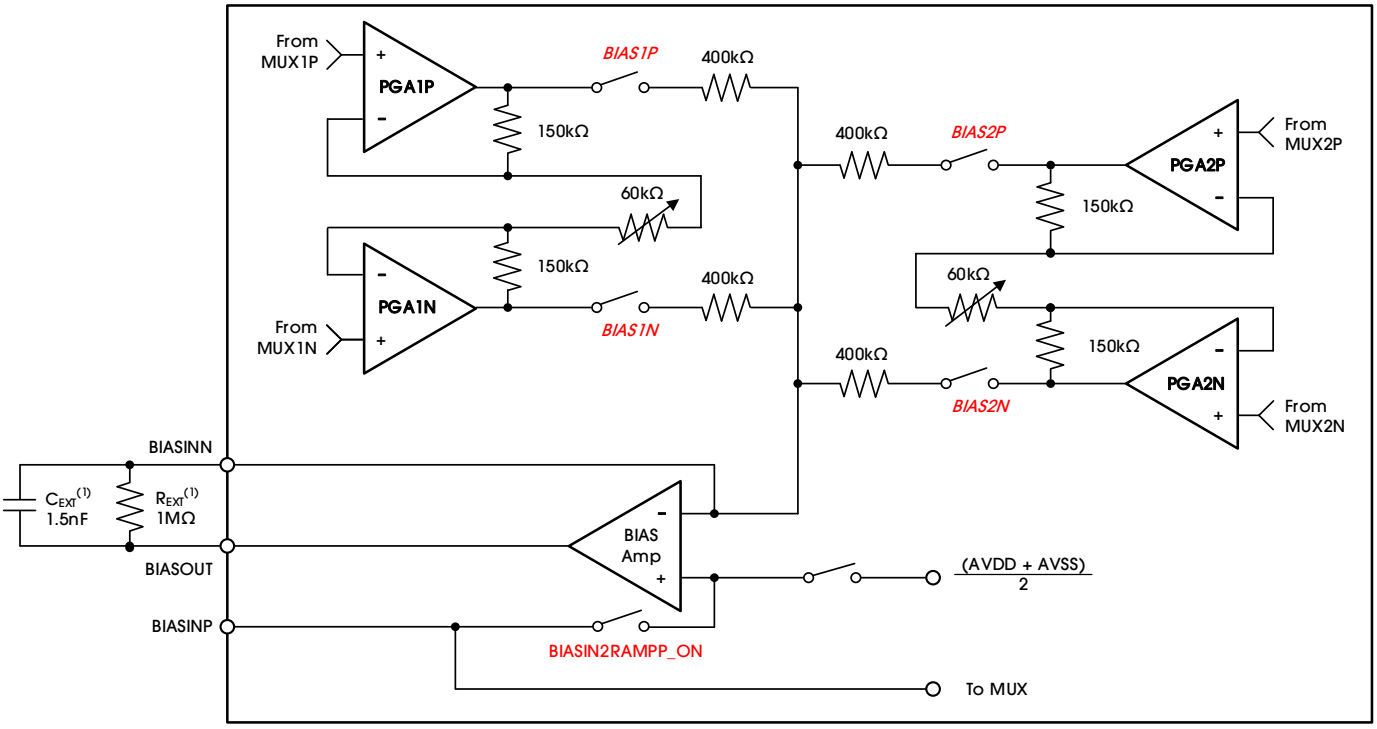
When the BIAS amplifier is powered on, the current source has no function. Only the comparator can be used to sense the voltage at the output of the BIAS amplifier. The comparator thresholds are set by the same BO(7:5) bits used to set the thresholds for other negative inputs. It is optional to use BO_BIAS to set the threshold of positive and negative rails via the BIAS_DEC_EN and the RCOMP_TH(2:0) bits to control the voltage value.

BIAS_BO_P and BIAS_BO_N in the MOD_STAT2 register show the status of BIAS burn-out.

8.3.21 BIAS AMPLIFIER

The bias amplifier circuitry is used as a means to counter the common-mode interference in a system as a result of power lines and other sources. The BIAS circuit senses the common-mode of a selected set of sensors and creates a negative feedback loop by driving a inverted common-mode signal. The negative feedback loop restricts the common-mode movement to a narrow range, depending on the loop gain. Stabilizing the entire loop is specific to the individual user system based on the various poles in the loop. The ADX320Q/ADX3202Q devices integrate the MUXes to select the channel and an operational amplifier. All the amplifier terminals are available at the pins, allowing the user to choose the components for the feedback loop. The circuit shown in Figure 41 shows the overall functional connectivity for the BIAS circuit.

The reference voltage for the bias amplifier can be chosen to be internally generated (AVDD + AVSS) / 2 or it can be provided externally with a resistive divider. The selection of an internal versus external reference voltage for the BIAS loop is defined by writing the appropriate value to the BIASREF_INT bit in the PWR register.



(1) Typical values.

Figure 41. BIAS Channel Selection

If the BIAS function is not used, the amplifier can be powered down using the PDB_BIAS bit. This bit is also used in daisy-chain mode to power down all but one of the BIAS amplifiers.

The functionality of the BIASINP pin is explained in the INPUT MULTIPLEXER section.

8.3.22 BIAS CONFIGURATION WITH MULTIPLE DEVICES

Figure 42 shows multiple devices connected to a BIAS.

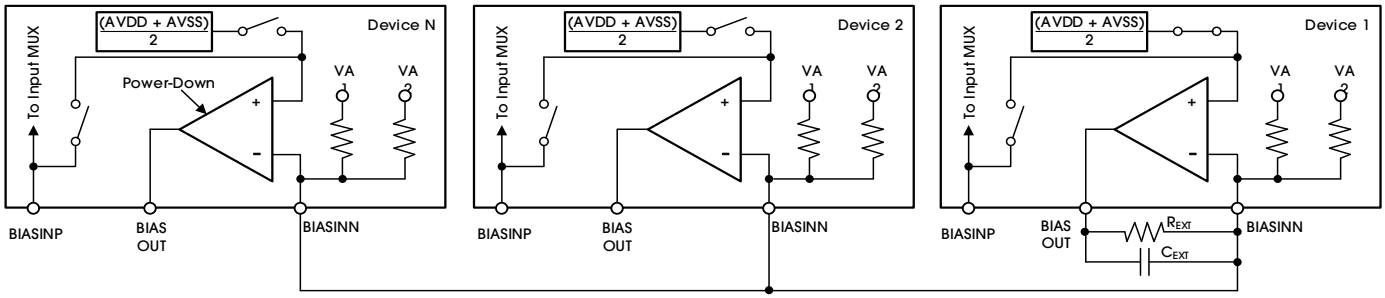


Figure 42. BIAS Connection for Multiple Devices

8.3.23 FIFO

The ADX320Q/ADX3202Q devices have 12 depth sample FIFO inside. The width of every sample is 56 bits. The software uses the FIFO_CFG2 depth field to set the FIFO content numbers for triggering MCU to read FIFO data, and GPIO_SEL(1:0) are used to select the output GPIO status. Figure 43 shows the FIFO sample frame format for FRAME_CFG(2:0) of the FIFO_CFG1 register.

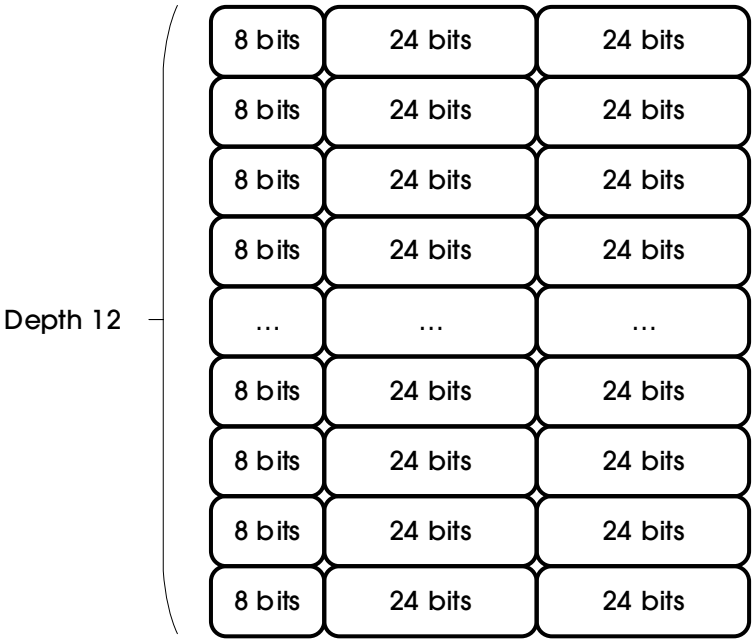


Figure 43. FIFO Frame Format

There are two formats for FIFO usage application. In both occasions, the FIFO data will not enable the CRC.

- If the application only activates one ADC channel to sample data, it is better to configure FRAME_CFG = 000. The frame format is as below: Two continuous ADC data (first conversion data and second conversion data) make one FIFO sample item. The active channel is decided by the PD fields of CH1SET and CH2SET.

  ```
  {3-bit burn-out (1st), 3-bit burn-out (2nd), 1-bit GPIO (1st), 1-bit GPIO (2nd), 24-bit conversion data (1st), 24-bit conversion data (2nd)}
  ```

  Note that the 3-bit burn-out is the active channel to sample data sensor burn-out status based on the register configuration.

- If the application activates two ADC channels, it is better to configure FRAME_CFG = 001. The active channel is decided by the PD fields of CH1SET and CH2SET. The frame format is as below:

  ```
  {5-bit burn-out, 1b0, 2-bit GPIO data, 24-bit CH1 conversion data,24-bit CH2 conversion data}
  ```

  Note that the 5-bit burn-out is the active channel to sample conversion data sensor burn-out status based on the register configuration.

8.3.23.1 FIFO USAGE SEQUENCE

The software needs to stop the RDATAC mode before enabling FIFO. The RFIFO command will be dropped if CRC check fails and there is no data output. If FIFO is disabled, the system will always read wrong FIFO entry data, but it will not disturb the FIFO data. FIFO will output a $\overline{DRDY}$ or a GPIO interrupt to external MCU, and then wait the external MCU to send the RFIFO command to read FIFO data. The external MCU is able to read more data items than threshold value based on the DLVL(4:0) fields of FIFO_STAT register status, however, the RFIFO number cannot exceed the maximum FIFO depth.

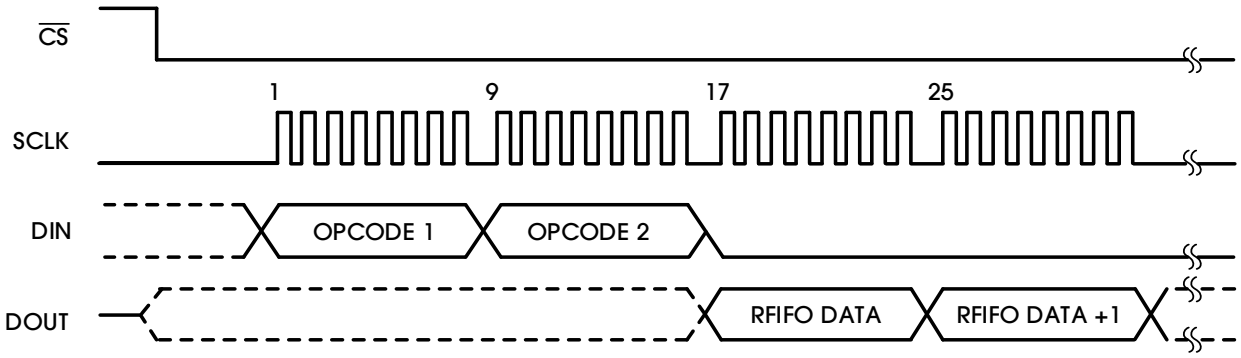


Figure 44. RFIFO Sequence

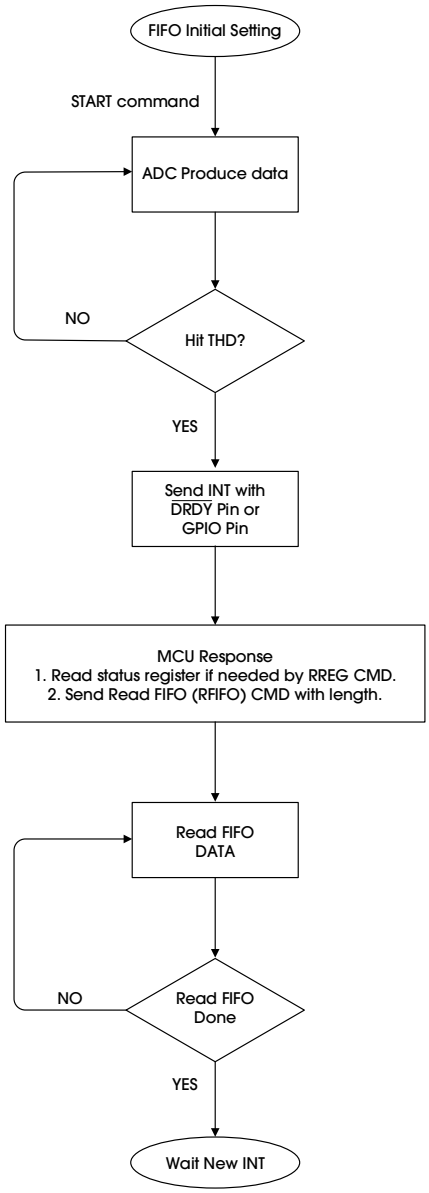


Figure 45. FIFO Read Usage Sequence

8.3.24 SHORT PROTECTION

The device is enabled to detect the output pin short ground or short power status when IO_3MA field of CONIFG5 is configured to IO High Drive mode, and it will reduce the current to 500μA automatically when short condition is met. The DOUT, $\overline{\text{DRDY}}$, GPIO1, GPIO2, and CLK pin has this capability when they are configured as output. The first short status will be captured into MOD_STAT1 register with the SHORT_GND and SHORT_PWD fields. The software needs to clear the fields before capturing the new short status. When any of the output pin is shorted to ground, the SHORT_GND will be set. When any of the output pin is shorted to power, SHORT_PWD will be set.

8.3.25 I/O TIMING CAPABILITY

For digital I/O output function, the IO_3MA and IO_SRM fields of the CONFIG5 register is used to control the I/O power consumption, maximum frequency, and anti-EMI interference capability except the DOUT pin. The DOUT pin has a dedicated DOUT_DO3MA controller bit in the EPMIX_CFG register, All I/O share one IO_SRM configuration value. Follow the settings listed in Table 26 to configurate a reasonable value based on application requirement.

Table 26. Recommended I/O Configuration

I/O FREQUENCY MAX. OUT	IO_SRM VALUE	IO_3MA	DOUT_DO3MA	ANTI-EMI	POWER
3MHz	0	0	1	Best	Lower
4MHz	0	1	0	Middle	Low
10MHz	1	0	1	Middle	High
20MHz	1	1	0	Wort	Higher

8.3.26 INTERRUPT

The device has five interrupt sources and the interrupt is output to GPIO by configuring the INTGPIO field of COFNG5 and enabling the GPIO register output function. The five interrupts are BO interrupt INT1, ADC data out of range interrupt INT2, FIFO interrupt INT3, CLK missing interrupt INT4, and invalid SPI CMD interrupt INT5. All Interrupts will drive GPIO to high when the interrupt is triggered.

- For INT1, the minimum interrupt pulse is different. It is about 15.6ms when the DEBOUCE field of BO_CFG is configured to 2'b10, and it is about 7.8ms when the DEBOUCE field is configured to 2'b01. Before using INT1, enable the BO_ISTEP.BO_INT_EN field.
- For INT2, the minimum interrupt pulse is one FDR cycle. Before using INT2, enable the CONFIG4.DR_INT_EN field.
- For INT3, the minimum interrupt pulse is about 4μs. Before using INT3, enable the FIFO_CFG1.FIFO_INT_EN field.
- For INT4, the CLK missing is a long pulse until the software clears it or there is a system reset. Before using INT4, enable the CONFIG4.CLK_MISS_INT_EN field.
- For INT5, the first invalid command is reported, and the interrupt is a long pulse until the software clears the invalid command status. Before using INT5, enable the CONFIG5.INV_CMD_INT_EN field.

8.3.27 SETTING THE DEVICE FOR BASIC DATA CAPTURE

This section outlines the procedure to configure the device in a basic state and capture data. The procedure is intended to put the device in a datasheet condition to check if the device is working properly in the user's system. It is recommended that this procedure be followed initially to get familiar with the device settings. Once this procedure has been verified, the device can be configured as needed. For details on the timings for commands, refer to the appropriate sections in the datasheet. Figure 46 details a flowchart of the configuration procedure.

8.3.27.1 BURN-OUT

Sample code to set DC burn-out with current source or sink resistors on all channels:

```
WREG BO 10h // Comparator threshold at 95% and 5%, current source or sink resistor // DC burn-out
WREG CONFIG2 E0h // Turn on DC burn-out comparators
WREG BO_SENS 0Fh // Turn on both P- and N-side of all channels for burn-out sensing
```

Observe the status bits of the output data stream to monitor burn-out status.

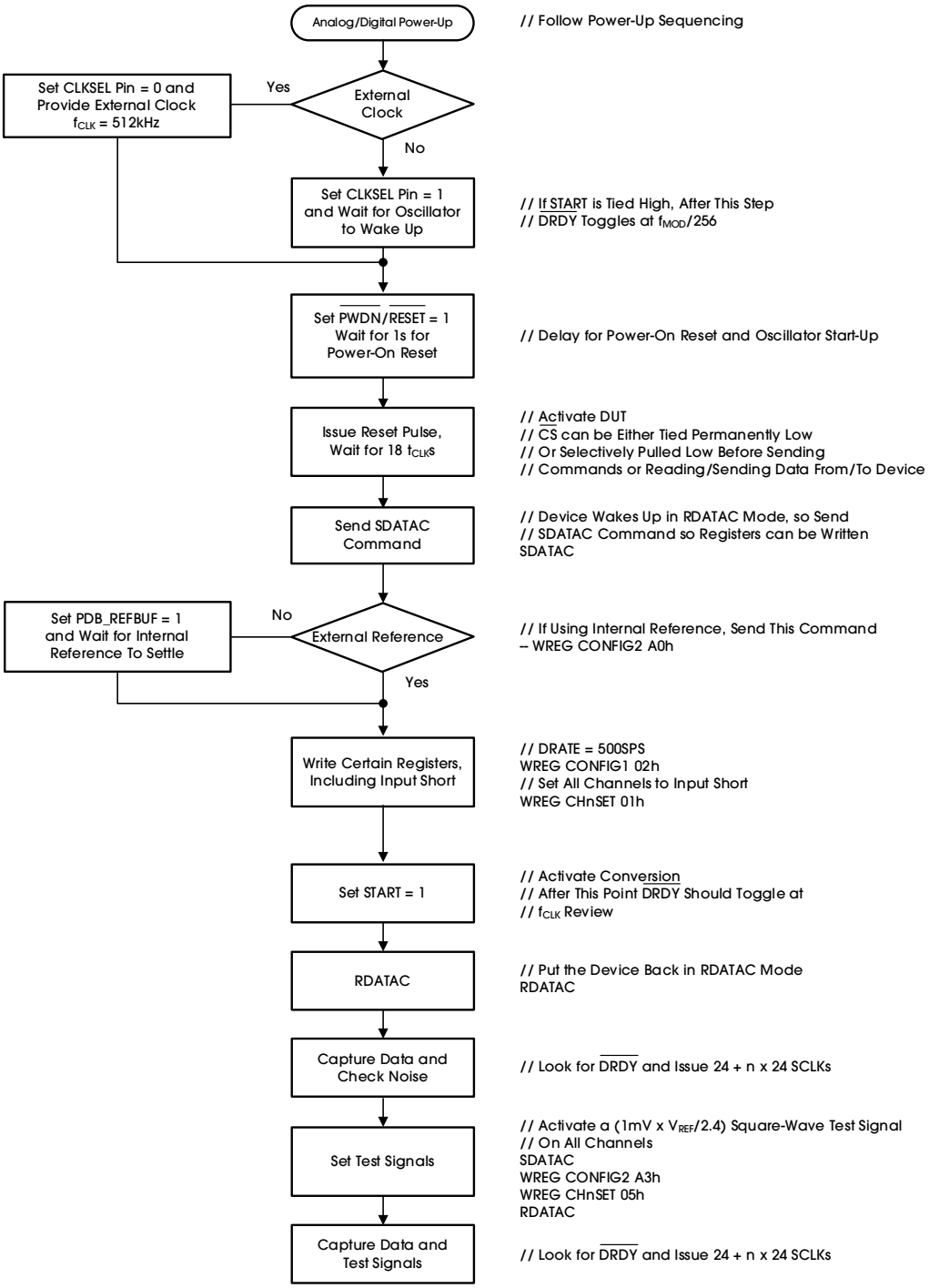


Figure 46. Initial Flow at Power-Up

8.3.28 DEVICE FUNCTIONAL MODES

The ADX320Q/ADX3202Q can be used in different functional modes, as a single device in a system, or as multiple devices in a system. The ADX320Q/ADX3202Q devices are designed to provide configuration flexibility when multiple devices are used in a system, as explained in the MULTIPLE DEVICE CONFIGURATION section.

In terms of data conversion, the device can operate in continuous mode as explained in the CONTINUOUS MODE section, or in the Single-Shot mode as explained in the SINGLE-SHOT MODE section.

8.3.29 FUNCTION SAFETY MANUAL

Table 27 provides an overview of safety mechanism. The functional safety feature is useful for auto-application, please take care the safety mechanism and user registers content to use this features.

Table 27. Safety Mechanism Overview

SM	DIAGNOSTIC NAME	DESCRIPTION/SAFETY STATE	STATUS FLAG
1	Device Error	Device initial setting error	EF_UERR
2	CLK Miss or Invalid	External clock is missing or invalid.	CLK_MISS
3	PGA1 Out of Range	PGA1 P side or N side out of range	PGA1P_OOR PGA1N_OOR
4	PGA2 Out of Range	PGA2 P side or N side out of range	PGA2P_OOR PGA2N_OOR
5	BIAS Burn-Out	BIAS burn-out for P side or N side	BIAS_BO_P BIAS_BO_N
6	Channel 1 Burn-Out	Channel 1 P or N side burn-out	IN1N_OFF IN1P_OFF
7	Channel 2 Burn-Out	Channel 2 P or N side burn-out	IN2N_OFF IN2P_OFF
8	Output Pin Short	Output pin is shorted to power or ground.	SHOT_PWR SHOT_GND
9	Invalid Command	Invalid command is detected.	INVALID_CMD_ERR
10	CRC Error	Command CRC or data CRC error	DAT_CRC_ERR CMD_CRC_ERR
11	FRAME Miss	Frame is missing or overlapped by new data.	FRAME_MISS
12	FIFO Error	FIFO read pointer is not equal to write pointer when FIFO is disabled.	FIFO_ERR

8.3.30 OFFSET CALIBRATION

The ADX320Q/ADX3202Q devices provide offset calibration to reduce the offset error. After reset or power-on, perform an offset calibration to cancel most offset. The offset calibration can also offset temperature drift. It is recommended to perform an offset calibration when environment temperature changes significantly.

To perform an offset calibration, send an OFFSETCAL command. After the command is completed, offset adjustment value is written into the OFC_CH00 to OFC_CH22 registers. The conversion data is automatically compensated before it is read out. No more calculation is needed for offset calibration.

See Table 9 for the performance of offset after calibration. OFC_CH*xx* can be read and written. It is also supported to write a specific value in the OFC_CH*xx* register.

8.4 PROGRAMMING

8.4.1 SPI INTERFACE

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT. The interface reads conversion data, reads and writes registers, and controls the ADX320Q/ADX3202Q operation. The $\overline{DRDY}$ output is used as a status signal to indicate when data are ready. $\overline{DRDY}$ goes low when new data are available.

8.4.1.1 CHIP SELECT ($\overline{CS}$)

$\overline{CS}$ selects the ADX320Q/ADX3202Q for SPI communication. $\overline{CS}$ must remain low for the entire duration of the serial communication. After the serial communication is finished, always wait four or more t_{CLK} cycles before taking $\overline{CS}$ high. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK and DIN are ignored, and DOUT enters a high-impedance state. $\overline{DRDY}$ asserts when data conversion is complete, regardless of whether $\overline{CS}$ is high or low.

8.4.1.2 SERIAL CLOCK (SCLK)

SCLK is the serial peripheral interface (SPI) serial clock. SCLK is used to shift commands in and shift data out from the device. The serial clock features a Schmitt-triggered input and clocks data on the DIN and DOUT pins into and out of the ADX320Q/ADX3202Q. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally forcing a clock event. The absolute maximum SCLK limit is specified in the Table 10. When shifting in commands with SCLK, make sure that the entire set of SCLKs is issued to the device. Failure to do so could result in the device serial interface being placed into an unknown state, requiring $\overline{CS}$ to be taken high to recover.

For a single device, the minimum speed needed for the SCLK depends on the number of channels, number of bits of resolution, and output data rate. (For multiple cascaded devices, see the MULTIPLE DEVICE CONFIGURATION section.) The minimum speed can be calculated with Equation 9.

$$t_{SCLK} < \frac{t_{DR} - 4\,t_{CLK}}{72\ (2 \times 24\ \text{bits} + \text{STATUS})} \tag{9}$$

For example, if the ADX3202Q is used in a 500SPS mode (2 channels, 24-bit resolution), the minimum SCLK speed is approximately 36kHz.

Data retrieval can be done either by putting the device in RDATAC mode or by issuing a RDATA command for data on demand. The above SCLK rate limitation applies to RDATAC. For the RDATA command, the limitation applies if data must be read in between two consecutive $\overline{DRDY}$ signals. Equation 9 assumes that no other commands are issued in between data captures. SCLK can only be twice the speed of f_{CLK} during register reads and writes. For faster SPI interface, use f_{CLK} = 2.048MHz and set the CLK_DIV register bit (in the BO_STAT register) to '1'.

8.4.1.3 DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to communicate with the ADX320Q/ADX3202Q (opcode commands and register data). The device latches data on DIN on the SCLK falling edge.

8.4.1.4 DATA OUTPUT (DOUT)

The data output pin (DOUT) is used with SCLK to read conversion and register data from the ADX320Q/ADX3202Q. The START pin must transition from low to high before the data output pin can generate any data. Data on DOUT are shifted out on the SCLK rising edge. DOUT goes to a high-impedance state when $\overline{CS}$ is high.

Figure 47 shows the data output protocol for the ADX3202Q.

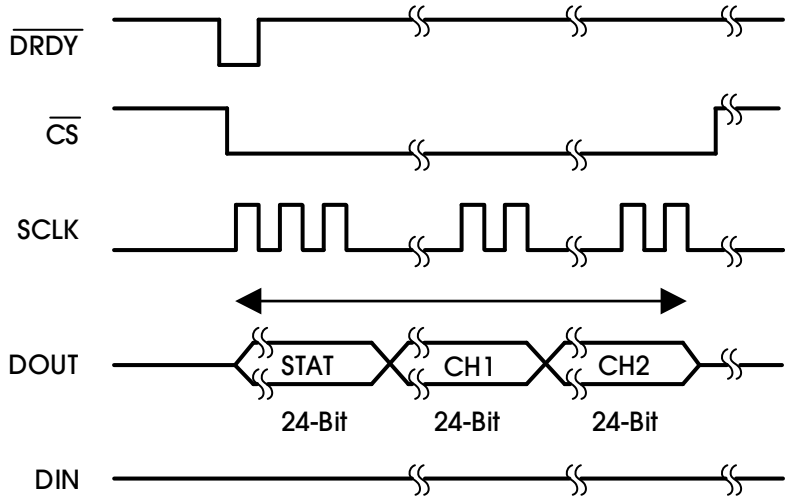


Figure 47. SPI Bus Data Output for the ADX3202Q (Two Channels)

8.4.1.5 DATA RETRIEVAL

Data retrieval can be accomplished in one of two methods. The read data continuous command (see the RDATAC: READ DATA CONTINUOUS section) can be used to set the device in a mode to read the data continuously without sending opcodes. The read data command (see the RDATA: READ DATA section) can be used to read just one data output from the device (see the SPI COMMAND DEFINITIONS section for more details). The conversion data are read by shifting data out on DOUT. The MSB of the data on DOUT is clocked out on the first SCLK rising edge. $\overline{DRDY}$ returns to high on the first SCLK falling edge. DIN should remain low for the entire read operation.

The number of bits in the data output depends on the number of channels and the number of bits per channel. For the ADX320Q/ADX3202Q, the number of data outputs is (24 status bits + 24 bits × 2 channels) = 72 bits. The format of the 24 status bits is:

(1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 8 '0's + 24 bits × 2 channels) when CONFG1.DOUT_CRC_EN is disabled, or

(1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD + 24 bits × 2 channels) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 24 bits × 2 channels) data field.

The data format for each channel data is two's complement, MSB first. When channels are powered down using user register settings, the corresponding channel output is set to '0'. However, the sequence of channel outputs remains the same. Table 28 lists the data formats.

Table 28. Data Format

PRODUCT	DATA FORMAT
24-bit ADC, 1-channel	The data format is 48 bits with the same 24 bits status and CRC rule for 2-channel product. (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 8 '0's + 24 bits) when CONFG1.DOUT_CRC_EN is disabled, or (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD + 24 bits) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 24 bits) data field,
16-bit ADC, 2-channel	The data format is 48 bits without CRC and data format is 56 bits with CRC. (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits × 2 channels) when CONFG1.DOUT_CRC_EN is disabled, or (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD +16 bits × 2 channels) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits × 2 channels) data field,
16-bit ADC, 1-channel	The data format is 32 bits without CRC and data format is 40 bits with CRC. (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits) when CONFG1.DOUT_CRC_EN is disabled, or (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 8-bit CRC STATUS WORD +16 bits) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (1100 + BO_STAT(4:0) + GPIO(1:0) + 5 '0's + 16 bits) data field,
Any product with FIFO	The data format is 56 bits without CRC, and data format is 72 bits with CRC. (FIFO_ITEMB0 + FIFO_ITEMB1 + FIFO_ITEMB2 + FIFO_ITEMB3 + FIFO_ITEMB4 + FIFO_ITEMB5 + FIFO_ITEMB6) when CONFG1.DOUT_CRC_EN is disabled, or (FIFO_ITEMB0 + 8'b0 + 8-bit CRC STATUS WORD + FIFO_ITEMB1 + FIFO_ITEMB2 + FIFO_ITEMB3 + FIFO_ITEMB4 + FIFO_ITEMB5 + FIFO_ITEMB6) when CONFG1.DOUT_CRC_EN is enabled and CRC data is for (FIFO_ITEMB0 + 8'b0 + FIFO_ITEMB1 + FIFO_ITEMB2 + FIFO_ITEMB3 + FIFO_ITEMB4 + FIFO_ITEMB5 + FIFO_ITEMB6) data field,

The ADX320Q/ADX3202Q devices also provide a multiple readback feature. Data can be read out multiple times by simply giving more SCLKs, in which case the MSB data byte repeats after reading the last byte. In RDATAC mode, hardware is able to check FRAME overwrite for SPI slow read reason or SPI interface hang by setting CONFIG5.FRAM_CHK_EN to 1. When the FRAME overwrite detection feature is enabled, the data cannot be read out multiple times by simply giving more SCLKs. In RFIFO mode, when FIFO_CFG1(0) is enabled, the RDATA and RDATAC commands are not allowed to be sent.

8.4.1.6 DATA READY ($\overline{DRDY}$)

$\overline{DRDY}$ is an output. When it transitions low, new conversion data are ready. The $\overline{CS}$ signal has no effect on the data ready signal. The behavior of $\overline{DRDY}$ is determined by whether the device is in RDATAC mode or the RDATA command is being used to read data on demand. (See the RDATAC: READ DATA CONTINUOUS and RDATA: READ DATAs sections for further details).

When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption.

The START pin or the START command is used to place the device either in normal data capture mode or pulse data capture mode.

Figure 48 shows the relationship between $\overline{DRDY}$, DOUT, and SCLK during data retrieval (in case of an ADX320Q/ADX3202Q with a selected data rate that gives 24-bit resolution). DOUT is latched out at the SCLK rising edge. $\overline{DRDY}$ is a fixed 4-6 µs low level when ADC data is ready for being read.

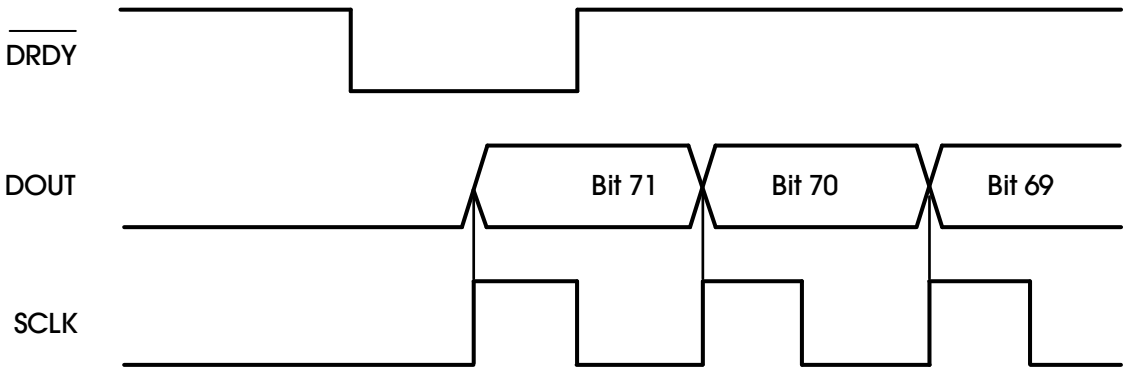


Figure 48. $\overline{DRDY}$ with Data Retrieval ($\overline{CS}$ = 0)

8.4.1.7 GPIO

The ADX320Q/ADX3202Q devices have a total of two general-purpose digital input/output (GPIO) pins available in the normal mode of operation. The digital I/O pins are individually configurable as either inputs or as outputs through the GPIOC bits register. The GPIOD bits in the GPIO register control the level of the pins. When reading the GPIOD bits, the data returned are the logic level of the pins, whether they are programmed as inputs or outputs. When the GPIO pin is configured as an input, a write to the corresponding GPIOD bit has no effect. When configured as an output, a write to the GPIOD bit sets the output value.

If configured as inputs, these pins must be driven (do not float) and valid GPIO data can be read after 4 t_{CLK} with CLKDIV = 0 or 16 t_{CLK} with CLKDIV = 1 once input pins are driven. The GPIO pins are set as inputs after power-on or after a reset. Figure 49 shows the GPIO port structure. The pins should be shorted to DGND with a series resistor if not used.

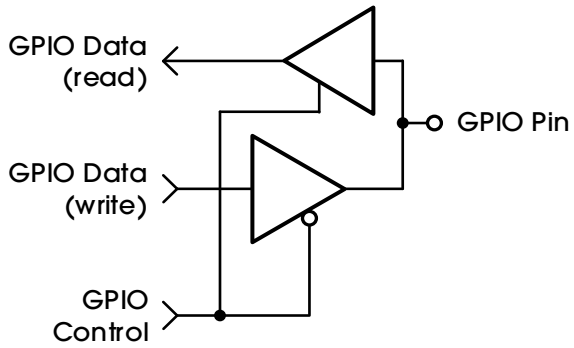


Figure 49. GPIO Port Pin

8.4.1.8 POWER-DOWN AND RESET (PWDN/RESET)

The PWDN/RESET pins are shared. If PWDN/RESET is held low for longer than 2^9 f_{MOD} clock cycles, the device is powered down. The implementation is such that the device is always reset when PWDN/RESET makes a transition from high to low. If the device is powered down, it is reset first and then if 2^{10} clock elapses it is powered down. Hence, all registers must be rewritten after power-up.

There are two methods to reset the ADX320Q/ADX3202Q: pull the PWDN/RESET pin low, or send the RESET opcode command. When using the PWDN/RESET pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the PWDN / RESET pin back high. The RESET command takes effect on the eighth SCLK falling edge of the opcode command. On reset, it takes 18 t_{CLK} cycles to complete initialization of the configuration registers to the default states and start the conversion cycle. Note that an internal RESET is automatically issued to the digital filter whenever the CONFIG1, RESP1, PWR, and ERM_CFG(2:0) are set to a new value with a WREG command.

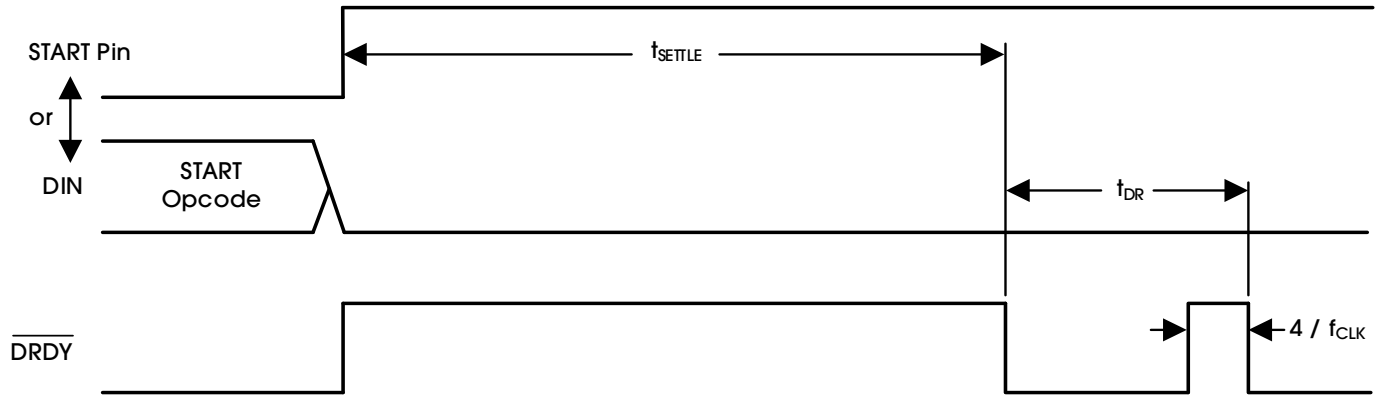
8.4.1.9 START

The START pin must be set high or the START command sent to begin conversions. When START is low or if the START command has not been sent, the device does not issue a DRDY signal (conversions are halted).

When using the START opcode to control conversion, hold the START pin low. The ADX320Q/ADX3202Q devices feature two modes to control conversion: continuous mode and single-shot mode. The mode is selected by SINGLE_SHOT (bit 7 of the CONFIG1 register). In multiple device configurations, the START pin is used to synchronize devices (see the MULTIPLE DEVICE CONFIGURATION section for more details).

8.4.1.10 SETTLING TIME

The settling time (t_{SETTLE}) is the time it takes for the converter to output fully settled data when the START signal is pulled high. Once START is pulled high, DRDY is also pulled high. The next DRDY falling edge indicates that data are ready. Figure 50 shows the timing diagram and Table 29 shows the settling time for different data rates. The settling time depends on f_{CLK} and the decimation ratio (controlled by the DR(2:0) bits in the CONFIG1 register). Refer to Table 29 for the settling time as a function of t_{MOD}. Note that when START is held high and there is a step change in the input signal, it takes 3 t_{DR} for the filter to settle to the new value. Settled data are available on the fourth DRDY pulse. Settling time number uncertainty is one t_{MOD} cycle. Therefore, it is recommended to add one t_{MOD} cycle delay before issuing SCLK to retrieve data.



(1) Settling time uncertainty is one t_{MOD} cycle.

Figure 50. Settling Time

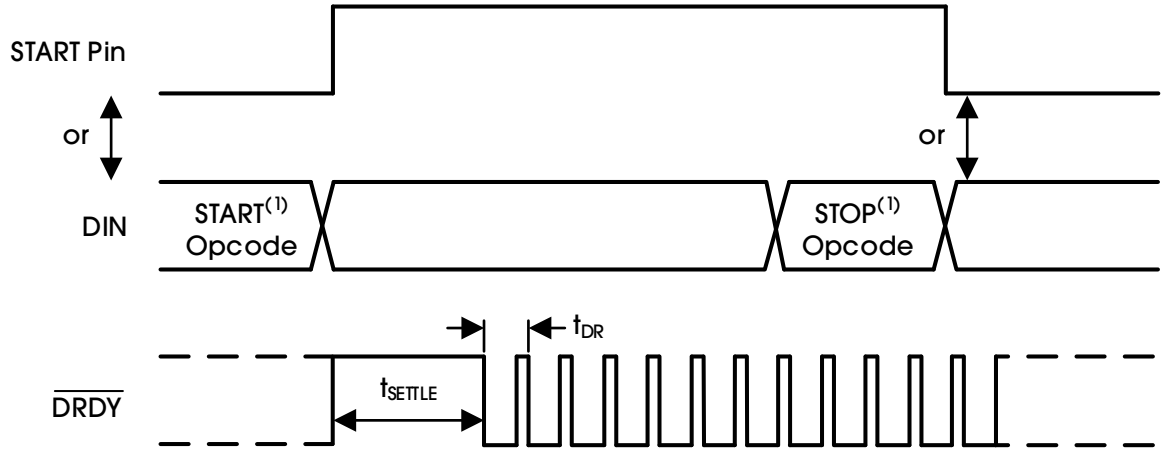
Table 29. Settling Time for Different Data Rates

DR(2:0)	SETTLING TIME(1)	UNITS(2)
000	4100	t_{MOD}
001	2052	t_{MOD}
010	1028	t_{MOD}
011	516	t_{MOD}
100	260	t_{MOD}
101	132	t_{MOD}
110	68	t_{MOD}
111	—	—

Note 1: Settling time uncertainty is one t_{MOD} cycle.
Note 2: t_{MOD} = 4 t_{CLK} for CLK_DIV = 0 and t_{MOD} = 16 t_{CLK} for CLK_DIV = 1.

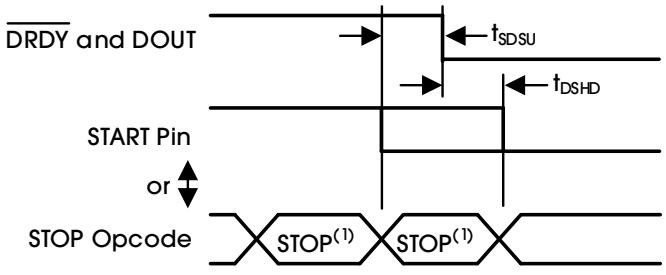
8.4.1.11 CONTINUOUS MODE

Conversions begin when the START pin is taken high or when the START opcode command is sent. As seen in Figure 51, the $\overline{DRDY}$ output goes high when conversions start and trigger a 4µs negative pulse when data are ready. Conversions continue indefinitely until the START pin is taken low or the STOP opcode command is transmitted. When the START pin is pulled low or the stop command is issued, the conversion in progress is allowed to complete. Figure 51 and Table 30 show the required $\overline{DRDY}$ timing to the START pin and the START and STOP opcode commands when controlling conversions in this mode. To keep the converter running continuously, the START pin can be permanently tied high. Note that when switching from pulse mode to continuous mode, the START signal is pulsed or a STOP command must be issued, followed by a START command. This conversion mode is ideal for applications that require a fixed continuous stream of conversions results.



(1) START and STOP opcode commands take effect on the seventh SCLK falling edge.

Figure 51. Continuous Conversion Mode



(1) START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

Figure 52. START to $\overline{DRDY}$ Timing

Table 30. Timing Characteristics for Figure 51

PARAMETER	SYMBOL	MIN	UNITS
START Pin Low or STOP Opcode to $\overline{DRDY}$ Setup Time to Halt Further Conversions	t_{SDSU}	8	t_{MOD}
START Pin Low or STOP Opcode to Complete Current Conversion	t_{DSHD}	8	t_{MOD}

Note: START and STOP commands take effect on the seventh SCLK falling edge at the end of the opcode transmission.

8.4.1.12 SINGLE-SHOT MODE

The single-shot mode is enabled by setting the SINGLE_SHOT bit in the CONFIG1 register to '1'. In single-shot mode, the ADX320Q/ADX3202Q devices perform a single conversion when the START pin is taken high or when the START opcode command is sent. As seen in Figure 53, when a conversion is complete, $\overline{DRDY}$ goes low and further conversions are stopped. Regardless of whether the conversion data are read or not, $\overline{DRDY}$ remains low. To begin a new conversion, take the START pin low and then back high, or transmit the START opcode again. When switching from continuous mode to pulse mode, make sure the START signal is pulsed or issue a STOP command followed by a START command.

This conversion mode is provided for applications that require non-standard or non-continuous data rates. Issuing a START command or toggling the START pin high resets the digital filter, effectively dropping the data rate by a factor of four. Note that this mode leaves the system more susceptible to aliasing effects, requiring more complex analog anti-aliasing filters at the inputs. Loading on the host processor increases because it must toggle the START pin or send a START command to initiate a new conversion cycle.

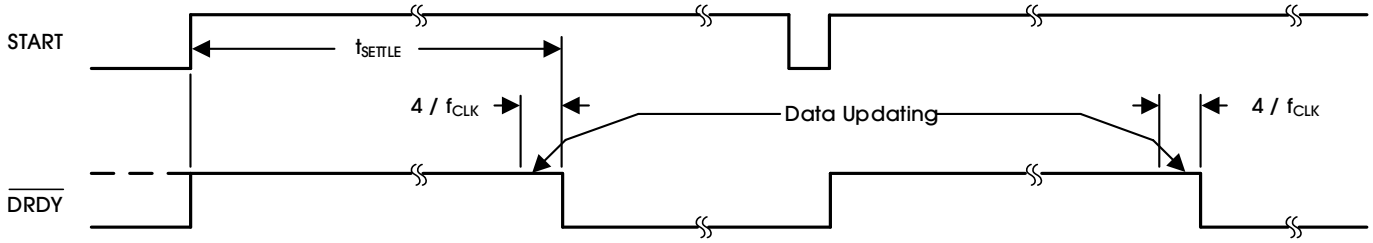


Figure 53. $\overline{DRDY}$ with No Data Retrieval in Single-Shot Mode

8.4.2 SPI COMMAND DEFINITIONS

The ADX320Q/ADX3202Q devices provide flexible configuration control. The opcode commands summarized in Table 31 control and configure the ADX320Q/ADX3202Q operation. The opcode commands are stand-alone, except for the register read and register write operations that require a second command byte plus data. $\overline{CS}$ can be taken high or held low between opcode commands but must stay low for the entire command operation (especially for multi-byte commands). System opcode commands and the RDATA command are decoded by the ADX320Q/ADX3202Q on the seventh SCLK falling edge. The register read and write opcodes are decoded on the eighth SCLK falling edge. Be sure to follow SPI timing requirements when pulling $\overline{CS}$ high after issuing a command.

Table 31. Command Definitions

COMMAND	DESCRIPTION	FIRST BYTE	SECOND BYTE
SYSTEM COMMANDS			
WAKEUP	Wake up from standby mode	0000 0010 (02h)	0x0E (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
STANDBY	Enter standby mode	0000 0100 (04h)	0x1C (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
RESET	Reset the device	0000 0110 (06h)	0x12/0x13 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
START	Start or restart (synchronize) conversions	0000 1000 (08h)	0x38 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
STOP	Stop conversion	0000 1010 (0Ah)	0x36 (CRC byte when CONFIG3.DIN_CRC_EN) is enabled.
LOCK	Lock SPI interface	0001 0101 (15h)	0x6b (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
UNLOCK	Unlock SPI interface	0001 0110 (16h)	0x62 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
OFFSETCAL	Channel offset calibration	0001 1010 (1Ah)	0x46 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
DATA READ COMMANDS			
RDATAC	Enable Read Data Continuous mode. This mode is the default mode at power-up.(1)	0001 0000 (10h)	0x70 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
SDATAC	Stop Read Data Continuously mode	0001 0001 (11h)	0x77 (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
RDATA	Read data by command, supports multiple read back.	0001 0010 (12h)	0x7e (CRC byte when CONFIG3.DIN_CRC_EN is enabled.)
REGISTER READ COMMANDS			
RREG	Read n nnnn registers starting at address r rrrr	001r rrrr (2xh)(2)(4)	000n nnnn(2)
RFIFO	Read FIFO data command with read number	011 0000(60h)	000n nnnn(2)
WREG	Write n nnnn registers starting at address r rrrr	010r rrrr (4xh)(3)(4)	000n nnnn(2)

Note 1: When in RDATAC mode, the RREG command is ignored.
Note 2: n nnnn = number of registers to be read or written – 1. For example, to read or write three registers, set n nnnn = 0 (0010). r rrrr = starting register address for read and write opcodes.
Note 3: When CONFIG3.DIN_CRC_EN is enabled, the Command in the following sections includes both COMMAND byte and CRC status byte.
Note 4: Registers with address >1Fh can only be accessed through burst mode. They cannot be read or written directly.

8.4.2.1 WAKEUP: EXIT STANDBY MODE

This opcode exits the low-power standby mode, see the STANDBY: ENTER STANDBY MODE section. Time is required when exiting standby mode (see the ELECTRICAL CHARACTERISTICS for details). There are no restrictions on the SCLK rate for this command and it can be issued any time. Any following command must be sent after 4 t_{CLK} cycles.

8.4.2.2 STANDBY: ENTER STANDBY MODE

This opcode command enters the low-power standby mode. All parts of the circuit are shut down except for the reference section. The standby mode power consumption is specified in the ELECTRICAL CHARACTERISTICS table. There are no restrictions on the SCLK rate for this command and it can be issued any time. Do not send any other command other than the wakeup command after the device enters the standby mode.

8.4.2.3 RESET: RESET REGISTERS TO DEFAULT VALUES

This command resets the digital filter cycle and returns all register settings to the default values. See the POWER-DOWN AND RESET (PWDN/RESET) section for more details. There are no restrictions on the SCLK rate for this command and it can be issued any time. It takes 9 f_{MOD} cycles to execute the RESET command. Avoid sending any commands during this time.

8.4.2.4 START: START CONVERSIONS

This opcode starts data conversions. Tie the START pin low to control conversions by command. If conversions are in progress, this command has no effect. The STOP opcode command is used to stop conversions. If the START command is immediately followed by a STOP command, then have a gap of 4 t_{CLK} cycles between them. When the START opcode is sent to the device, keep the START pin low until the STOP command is issued. (See the START section for more details.) There are no restrictions on the SCLK rate for this command and it can be issued any time.

8.4.2.5 STOP: STOP CONVERSIONS

This opcode stops conversions. Tie the START pin low to control conversions by command. When the STOP command is sent, the conversion in progress completes and further conversions are stopped. If conversions are already stopped, this command has no effect. There are no restrictions on the SCLK rate for this command and it can be issued any time.

8.4.2.6 OFFSETCAL: CHANNEL OFFSET CALIBRATION

This command is used to cancel the channel offset. The CALIB_ON bit in the PWR register must be set to '1' before issuing this command. OFFSETCAL must be executed every time there is a change in the PGA gain settings.

8.4.2.7 LOCK: LOCK SPI INTERFACE

This command is used to lock the SPI interface, preventing the device from accidentally latching unwanted commands that can change the state of the device. When the interface is locked, the device only responds to the RREG, RDATA, and UNLOCK commands and continues to output conversion data even when locked. The LOCK status will be cleared when there is an internal reset event or SPI reset, for example, reset by pulling the $\overline{CS}$ pin low to high. For the WREG command operation under the LOCK status, if the WREG number and data contain the RREG, RDATA, and UNLOCK decoding, it may disturb the LOCK command function, and the device status and command status registers can be read to check the exception status.

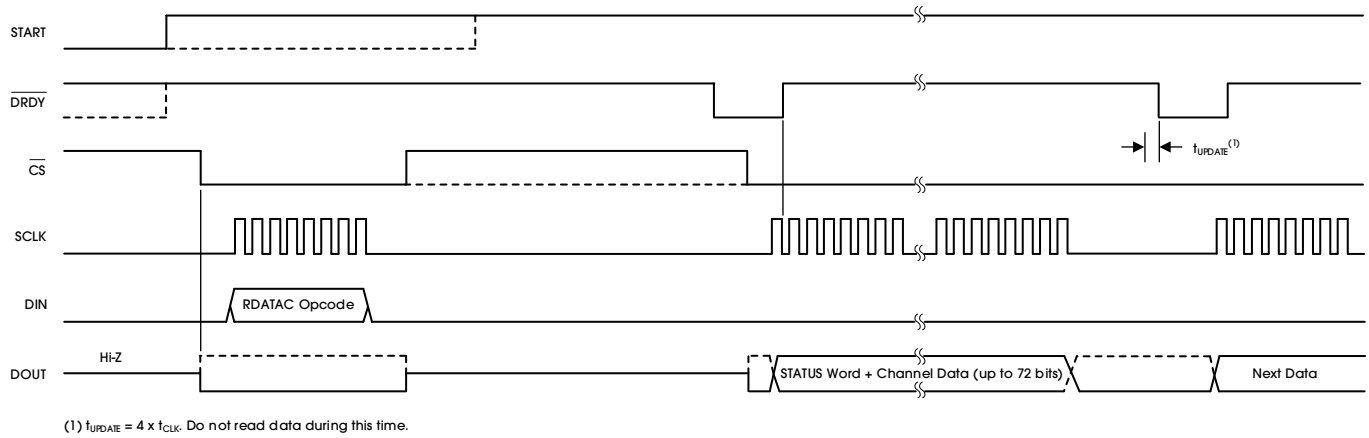
8.4.2.8 UNLOCK: UNLOCK SPI INTERFACE

This command is used to unlock the SPI interface if previously locked by the LOCK command.

8.4.2.9 RDATAC: READ DATA CONTINUOUS

This opcode enables the output of conversion data on each $\overline{DRDY}$ without the need to issue subsequent read data opcodes. This mode places the conversion data in the output register and may be shifted out directly. The read data continuous mode is the device default mode, the device defaults to this mode on power-up.

RDATAC mode is cancelled by the Stop Read Data Continuous command. If the device is in RDATAC mode, a SDATAC command must be issued before any other commands (except LOCK and UNLOCK commands) can be sent to the device. There is no restriction on the SCLK rate for this command. However, the subsequent data retrieval SCLKs or the SDATAC opcode command should wait at least 4 t_{CLK} cycles. RDATAC timing is shown in Figure 54. As Figure 54 shows, there is a keep-out zone of 4 t_{CLK} cycles around the $\overline{DRDY}$ pulse where this command cannot be issued in. To retrieve data from the device after the RDATAC command is issued, make sure either the START pin is high or the START command is issued. Figure 54 shows the recommended way to use the RDATAC command. RDATAC is ideally-suited for applications such as data loggers or recorders where registers are set once and do not need to be re-configured. $\overline{DRDY}$ is fixed 4-6 μs low level when ADC data is ready for being read.



(1) t_{UPDATE} = 4 x t_{CLK}. Do not read data during this time.

Figure 54. RDATAC Usage

8.4.2.10 SDATAC: STOP READ DATA CONTINUOUS

This opcode cancels the Read Data Continuous mode. There is no restriction on the SCLK rate for this command, but the following command must wait for 4 t_{CLK} cycles.

8.4.2.11 RDATA: READ DATA

Issue this command after $\overline{DRDY}$ goes low to read the conversion result (in Stop Read Data Continuous mode). There is no restriction on the SCLK rate for this command, and no wait time is needed for the subsequent commands or data retrieval SCLKs. To retrieve data from the device after RDATA command is issued, make sure either the START pin is high or the START command is issued. When reading data with the RDATA command, the read operation can overlap the occurrence of the next $\overline{DRDY}$ without data corruption. Figure 55 shows the recommended way to use the RDATA command. RDATA is best suited for the systems where register setting must be read or changed often between conversion cycles. $\overline{DRDY}$ is fixed 4-6μs low level when ADC data is ready for being read.

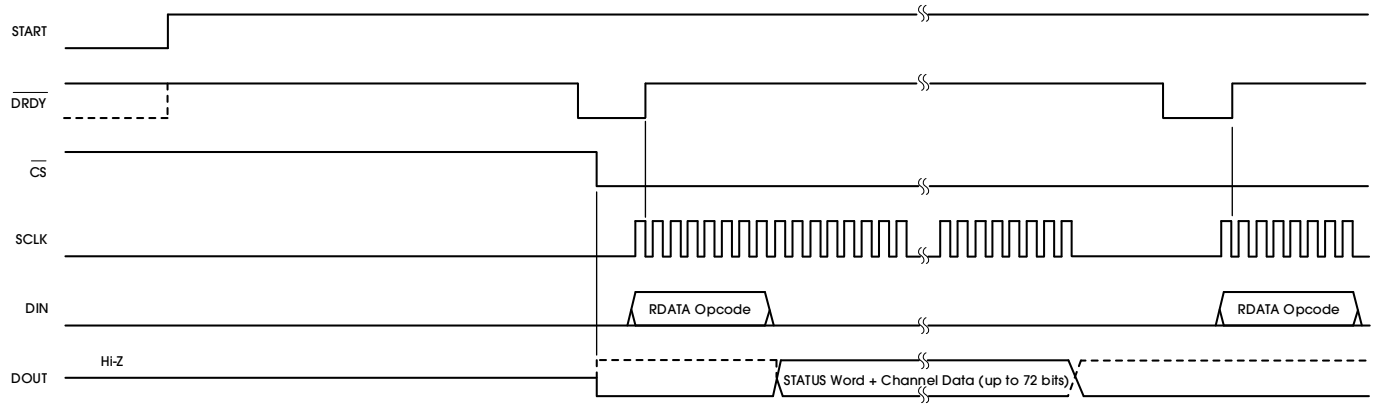


Figure 55. RDATA Usage

8.4.2.12 SENDING MULTI-BYTE COMMANDS

The ADX320Q/ADX3202Q serial interfaces decode commands in bytes and require 4 t_{CLK} cycles to decode and execute. Therefore, when sending multi-byte commands, a 4 t_{CLK} period must separate the end of one byte (or opcode) and the next.

Assume CLK is 512kHz, then $t_{SDECODE}$ (4 t_{CLK}) is 7.8125μs. When SCLK is 16MHz, one byte can be transferred in 500ns. This byte-transfer time does not meet the $t_{SDECODE}$ specification, therefore, a delay must be inserted so the end of the second byte arrives 7.3125μs later. If SCLK is 1MHz, one byte is transferred in 8μs. Because this transfer time exceeds the $t_{SDECODE}$ specification, the processor can send subsequent bytes without delay. In this later scenario, the serial port can be programmed to move from single-byte transfer per cycle to multiple bytes.

8.4.2.13 RREG: READ FROM REGISTER

This opcode reads register data. The Register Read command is a two-byte opcode followed by the output of the register data. The first byte contains the command opcode and the register address. The second byte of the opcode specifies the number of registers to read – 1.

1. First opcode byte: 001r rrrr, where r rrrr is the starting register address.
2. Second opcode byte: 000n nnnn, where n nnnn is the number of registers to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first register, as shown in Figure 56. When the device is in read data continuous mode, it is necessary to issue a SDATAC command before the RREG command can be issued. The RREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the SERIAL CLOCK (SCLK) section for more details. Note that $\overline{CS}$ must be low for the entire command.

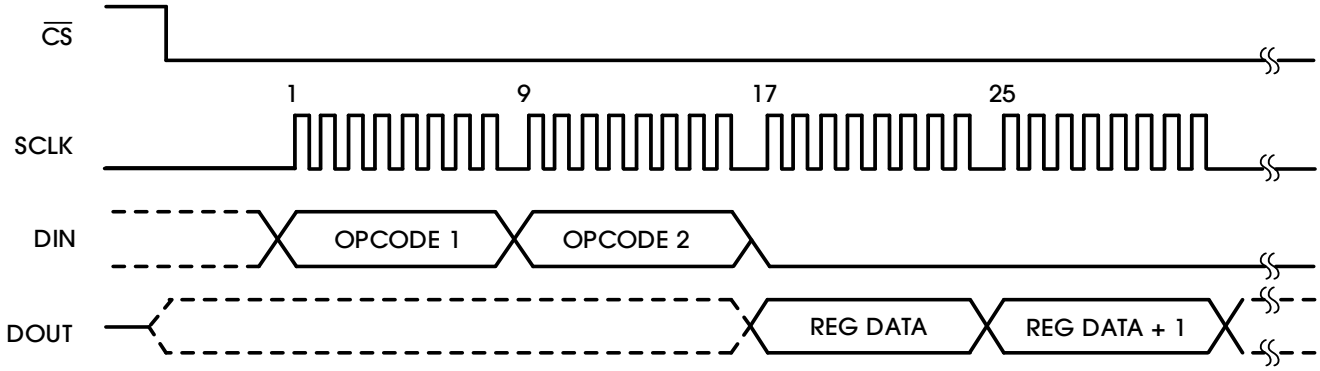


Figure 56. RREG Command Example: Read Two Registers Starting from Register 00h (ID Register) (OPCODE 1 = 0010 0000, OPCODE 2 = 0000 0001)

8.4.2.14 RFIFO: READ FIFO DATA

This opcode reads internal FIFO data. The FIFO Read command is a two-byte opcode followed by the output of the FIFO data. The first byte contains the command opcode. The second byte of the opcode specifies the number of FIFO items to read –1.

1. First opcode byte: 0110 0000.
2. Second opcode byte: 000n nnnn, where n nnnn is the number of FIFO items to read – 1.

The 17th SCLK rising edge of the operation clocks out the MSB of the first FIFO item data, as shown in Figure 57. When the device is in read data continuous mode, it is necessary to issue a SDATAC command before the RFIFO command can be issued. The RFIFO command can be issued when FIFO threshold is hit and the FIFO will set $\overline{DRDY}$ and interrupt to external MCU if the FIFO interrupt is enabled. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the SERIAL CLOCK (SCLK) section for more details. Note that $\overline{CS}$ must be low for the entire command.

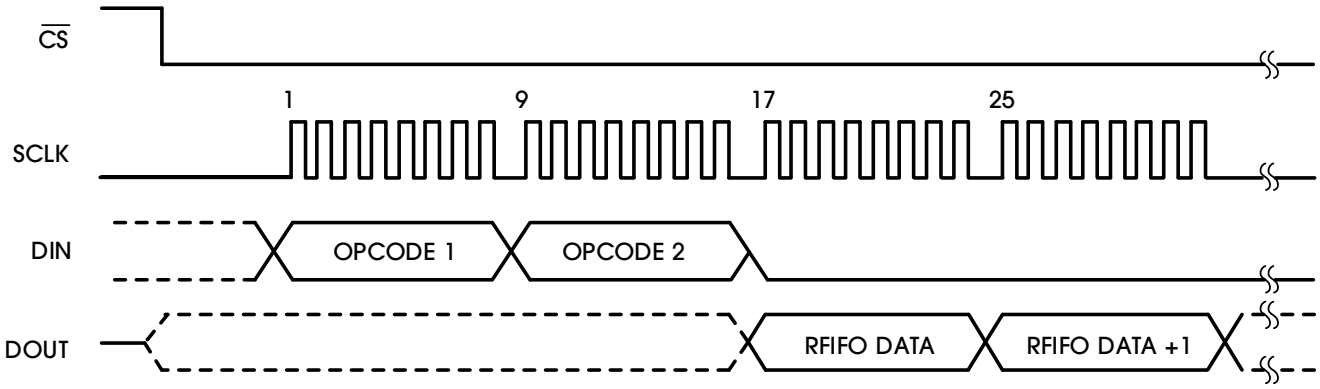


Figure 57. RFIFO Command Example: Read Two Registers Starting from FIFO

8.4.2.15 WREG: WRITE TO REGISTER

This opcode writes register data. The Register Write command is a two-byte opcode followed by the input of the register data. The first byte contains the command opcode and the register address.

The second byte of the opcode specifies the number of registers to write – 1.

1. First opcode byte: 010r rrrr, where r rrrr is the starting register address.
2. Second opcode byte: 000n nnnn, where n nnnn is the number of registers to write – 1.

After the opcode bytes, the register data follows (in MSB-first format), as shown in Figure 58. The WREG command can be issued at any time. However, because this command is a multi-byte command, there are restrictions on the SCLK rate depending on the way the SCLKs are issued. See the SERIAL CLOCK (SCLK) section for more details. Note that $\overline{CS}$ must be low for the entire command.

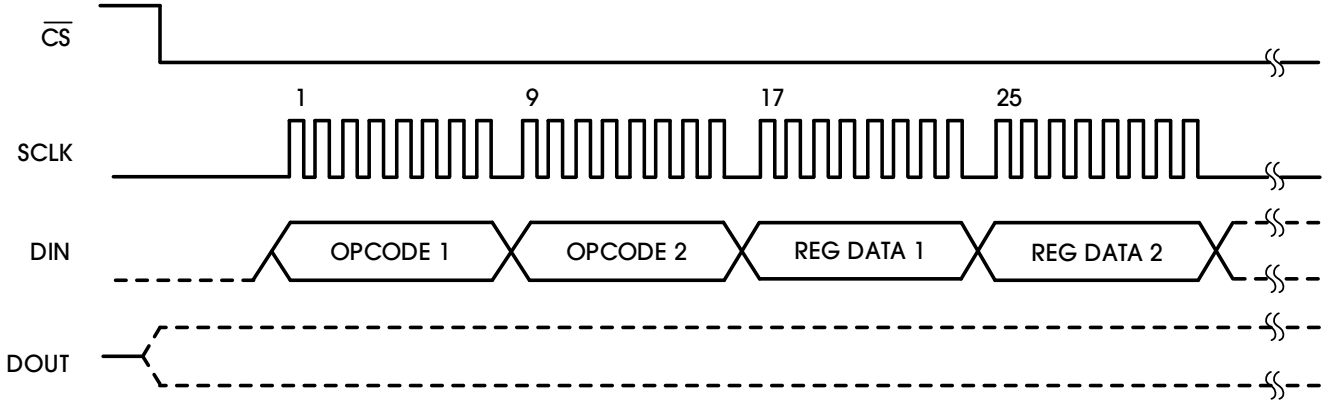


Figure 58. WREG Command Example: Write Two Registers Starting from 00h (ID Register) (OPCODE 1 = 0100 0000, OPCODE 2 = 0000 0001)

8.4.3 SPI CRC FEATURE

For all SPI commands, the 8-bit CRC status word follows the end of the whole command when CONFIG3.DIN_CRC_EN is enabled. The device will also check the CRC status word. Execution will not be performed for the WAKEUP, STANDBY, RESET, START, STOP, OFFSETCAL, LOCK, UNLOCK, RDATAC, SDATAC, RDATA, and RREG commands if the CRC status word is mismatched, and the MOD_STAT.CMD_CRC_ERR will be set. In other words, a CRC error occurs if the CRC words do not match. When the input CRC check fails, the device will not execute any commands, except for the WREG and RFIFO commands.

1. A WREG command always executes even when the CRC check fails. It will set MOD_STAT.DAT_CRC_ERR.
2. An RFIFO command executes one FIFO entry reading even when the CRC check fails. Only the first FIFO entry will be read, and the reading will repeat if RFIFO length is set in the command to inform user that CRC check of RFIFO fails. It will set MOD_STAT.DAT_CRC_ERR.

For burst register reading operation with RREG, the device will output a CRC status word at last when CONFIG3.DOUT_CRC_EN is enabled. The CRC status word will not be included in the count number in RREG.

For burst register writing operation with WREG, the host must provide a CRC status word at last when CONFIG3.DIN_CRC_EN is enabled. The CRC status word will not be included in the count number in WREG. To enable and disable CRC with CONFIG3.DIN_CRC_EN, the CRC check follows rules below:

1. If CRC is disabled, to enable the SPI CRC check, write CONFIG3.DIN_CRC_EN to one, and this whole write command does NOT have the CRC check.
2. If CRC is enabled, to disable the SPI CRC check, write CONFIG3.DIN_CRC_EN to zero, and this whole write command has the CRC check.

In CRC8 mode, it uses the CRC-8-CCITT formula as below:

$$P(x) = x^8 + x^2 + x + 1$$

9. REGISTER MAPS

Table 32 describes the various ADX320Q/ADX3202Q registers.

Table 32. Register Assignments

ADDRESS	REGISTER	RESET VALUE (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE SETTINGS (READ-ONLY REGISTERS)										
00h	ID	XX	REV_ID2	REV_ID1	REV_ID0	1	0	0	1	REV_ID
GLOBAL SETTINGS ACROSS CHANNELS (READ AND WRITE REGISTERS)										
01h	CONFIG1	02	SINGLE_SHOT	0	0	0	0	DR2	DR1	DR0
02h	CONFIG2	80	1	PDB_BO_COMP	PDB_REFBUF	VREF_4V	CLK_EN	0	INT_TEST	TEST_FREQ
03h	BO	10	COMP_TH2	COMP_TH1	COMP_TH0	1	IBURN-OUT1	IBURN-OUT0	0	0
CHANNEL-SPECIFIC SETTINGS (READ AND WRITE REGISTERS)										
04h	CH1SET	00	PD1	GAIN1_2	GAIN1_1	GAIN1_0	MUX1_3	MUX1_2	MUX1_1	MUX1_0
05h	CH2SET	00	PD2	GAIN2_2	GAIN2_1	GAIN2_0	MUX2_3	MUX2_2	MUX2_1	MUX2_0
06h	BIAS_SENS	00	CHOP1	CHOP0	PDB_BIAS	BIAS_BO_SENS	BIAS2N	BIAS2P	BIAS1N	BIAS1P
07h	BO_SENS	00	0	CP_FREQ	FLIP2	FLIP1	EMUX_BO3	EMUX_BO2	EMUX_BO1	EMUX_BO0
08h	BO_STAT	00	0	CLK_DIV1	CLK_DIV0	BIAS_STAT	IN2N_OFF	IN2P_OFF	IN1N_OFF	IN1P_OFF
GPIO AND OTHER REGISTERS (READ AND WRITE REGISTERS)										
09h	RSV	00	0	0	0	0	0	0	1	0
0Ah	CAL	02	CALOFF_ON	0	0	0	0	0	0	1
0Bh	GPIO	0C	0	0	0	0	GPIOC2	GPIOC1	GPIOD2	GPIOD1
ENHANCE PERFORMANCE SETTING REGISTERS (READ AND WRITE REGISTERS)										
0Ch	CONFIG3	00	0	P5VREF_ON	0	0	DIN_CRC_EN	DOUT_CRC_EN	SPI_TIMEOUT1	SPI_TIMEOUT0
0Dh	CONFIG4	00	DR_INT_EN	ADC_DAT_THD1	ADC_DAT_THD0	0	CLK_MISS_INT_EN	0	BIASINP2RAMPP_ON	RAMPOUT2RAMPN_ON
0Eh	CONIFG5	71	OSC_2M_EN	INT2GPIO2	INT2GPIO1	INT2GPIO0	INV_CMD_INT_EN	FRAME_CHK_EN	IO_3MA	IO_SRM
0Fh	BO_ISTEP	00	BO_INT_EN	CUR_LEVEL	ISTEP5	ISTEP4	ISTEP_3	ISTEP2	ISTEP1	ISTEP0
10h	BO_BIAS	00	EMUX_BO3	EMUX_BO2	EMUX_BO1	EMUX_BO0	0	0	0	0
12h	BO_CFG	00	0	0	0	DEBOUNCE1	DEBOUNCE0	OFC_EN	0	0
13h	PWR	40	0	WMODE	0	0	0	0	0	0
14h	CLK_CFG	10	0	0	SHORT_PROTECT	FSEL1	FSEL0	DOUT_DO3MA	0	0
16h	FIFO_CFG1	00	FIFO_INT_EN	0	0	FIFO_RST	FRAME_CFG2	FRAME_CFG1	FRAME_CFG0	FIFO_EN
17h	FIFO_CFG2	00	STATUS_SEL2	STATUS_SEL1	STATUS_SEL0	DEPTH4	DEPTH3	DEPTH2	DEPTH1	DEPTH0

ADDRESS	REGISTER	RESET VALUE (HEX)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DEVICE STATUS AND PROPERTY (READ-ONLY REGISTERS)										
18h	FIFO_STAT	40	FIFO_RDY	FIFO_EMPTY	FIFO_FULL	FIFO_ERR	DLVL3	DLVL2	DLVL1	DLVL0
DEVICE STATUS AND PROPERTY (READ AND WRITE REGISTERS)										
19h	MOD_STAT1	00	INVALID_CMD_ERR	SHORT_GND	CLK_MISS	FRAME_MISS	DAT_CRC_ERR	CMD_CRC_ERR	OORNG	SHORT_PWR
1Ah	MOD_STAT2	00	BIAS_BO_P	BIAS_BO_N	0	0	PGA2N_OOR	PGA2P_OOR	PGA1N_OOR	PGA1P_OOR
1Bh	OP_STAT_CMD	00	EFU_UERR	EFU_CERR	RDATAC_DONE	RD_FIFO_DONE	CAL_DONE	RDATA_DONE	REG_WR_DONE	REG_RD_DONE
DEVICE STATUS AND PROPERTY (READ-ONLY REGISTERS)										
1Ch	OP_STAT_SYS	92	SPI_UNLOCK	SPI_LOCK	SDC_MODE	RDC_MODE	STOP	START	WAKEUP	STARNDBY
1Dh	FI	XX	0	0	FS_ID5	FS_ID4	FS_ID3	FS_ID2	FS_ID1	FS_ID0
1Eh	ID_PR	70	PAR_ID3	PAR_ID2	PAR_ID1	PAR_ID0	0	0	0	0
EXTENDED FEATURE CONFIGURATION										
22h(1)	OFC_CH10	00	OFC_B7	OFC_B6	OFC_B5	OFC_B4	OFC_B3	OFC_B2	OFC_B1	OFC_B0
23h(1)	OFC_CH11	00	OFC_B15	OFC_B14	OFC_B13	OFC_B12	OFC_B11	OFC_B10	OFC_B9	OFC_B8
24h(1)	OFC_CH12	00	OFC_B23	OFC_B22	OFC_B21	OFC_B20	OFC_B19	OFC_B18	OFC_B17	OFC_B16
25h(1)	OFC_CH20	00	OFC_B7	OFC_B6	OFC_B5	OFC_B4	OFC_B3	OFC_B2	OFC_B1	OFC_B0
26h(1)	OFC_CH21	00	OFC_B15	OFC_B14	OFC_B13	OFC_B12	OFC_B11	OFC_B10	OFC_B9	OFC_B8
27h(1)	OFC_CH22	00	OFC_B23	OFC_B22	OFC_B21	OFC_B20	OFC_B19	OFC_B18	OFC_B17	OFC_B16
28h(1)	RSV	04	0	0	0	0	0	1	0	0

Note: Registers with address > 1Fh can only be accessed through burst mode. They cannot be read or written directly.

9.1 REGISTER DESCRIPTIONS

9.1.1 ID: ID CONTROL REGISTER (READ-ONLY) (ADDRESS = 00H)

Return to the SUMMARY TABLE. This register is programmed during device manufacturing to indicate device characteristics.

Table 33. ID Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	REV_ID(2:0)	Identification 000 = Reserved 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Reserved 111 = ADX320Q/ADX3202Q
4	1	Reads High
3:2	0	Reads Low
1	1	Reads High
0	REV_ID	Feature set identification 1 = 2-channel product 0 = 1-channel product

9.1.2 CONFIG1: CONFIGURATION REGISTER 1 (ADDRESS = 01H)

Return to the SUMMARY TABLE. This register configures each ADC channel sample rate.

Table 34. CONFIG1 Field Descriptions

BIT	FIELD	DESCRIPTION
7	SINGLE_SHOT	Single-shot conversion This bit sets the conversion mode. 0 = Continuous conversion mode (default) 1 = Single-shot mode
6:3	0	Reserved. Must be set to '0'.
2:0	DR(2:0)	These bits determine the oversampling ratio of both channel 1 and channel 2.

BIT	OVERSAMPLING RATIO	f_{MOD} = 256kHz	f_{MOD} = 128kHz
000	f_{MOD} / 1024	250SPS	125SPS
001	f_{MOD} / 512	500SPS	250SPS
010	f_{MOD} / 256	1kSPS (default)	500SPS (default)
011	f_{MOD} / 128	2kSPS	1kSPS
100	f_{MOD} / 64	4kSPS	2kSPS
101	f_{MOD} / 32	8kSPS	4kSPS
110	f_{MOD} / 16	16kSPS	8kSPS
111	Do not use	Do not use	Do not use

Note: f_{CLK} = 512kHz and CLK_DIV = 0 or f_{CLK} = 2.048MHz and CLK_DIV = 1.

9.1.3 CONFIG2: CONFIGURATION REGISTER 2 (ADDRESS = 02H)

Return to the SUMMARY TABLE. This register configures the test signal, clock, reference, and BO buffer.

Table 35. CONFIG2 Field Descriptions

BIT	FIELD	DESCRIPTION
7	1	Reserved. Must be set to '1'.
6	PDB_BO_COMP	Burn-out comparator power-down This bit powers down the burn-out comparators. 0 = Burn-out comparators disable (default) 1 = Burn-out comparators enable
5	PDB_REFBUF	Reference buffer power-down This bit powers down the internal reference buffer so that the external reference can be used. 0 = Reference buffer is powered down (default). 1 = Reference buffer is enabled.
4	VREF_4V	Enables 4V reference This bit chooses either the 2.4V or 4V reference. 0 = 2.4V reference (default) 1 = 4V reference
3	CLK_EN	CLK connection This bit determines whether the internal oscillator signal is connected to the CLK pin when an internal oscillator is used. 0 = Oscillator clock output disable (default) 1 = Oscillator clock output enable
2	0	Reserved. Must be set to '0'.
1	INT_TEST	Test signal selection This bit determines whether the test signal is turned on. 0 = Off (default) 1 = On, amplitude = ±(VREFP – VREFN) / 2400
0	TEST_FREQ	Test signal frequency This bit determines the test signal frequency. 0 = At DC (default) 1 = Square wave at 1Hz

9.1.4 BO: BURN-OUT CONTROL REGISTER (ADDRESS = 03H)

Return to the SUMMARY TABLE. This register configures the SENSOR BURN-OUT operation.

Table 36. BO Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	COMP_TH(2:0)	Burn-out comparator threshold These bits determine the burn-out comparator threshold. See the SENSOR BURN-OUT section for a detailed description. Comparator positive side 000 = 95% (default) 001 = 92.5% 010 = 90% 011 = 87.5% 100 = 85% 101 = 80% 110 = 75% 111 = 70% Comparator negative side 000 = 5% (default) 001 = 7.5% 010 = 10% 011 = 12.5% 100 = 15% 101 = 20% 110 = 25% 111 = 30%
4	1	Reserved. Must be set to '1'.
3:2	IBURN-OUT(1:0)	Burn-out current magnitude These bits determine the magnitude of current for the current BURN-OUT mode when CUR_LEVEL is zero; otherwise the current magnitude is decided by the ISTEP field. 00 = 6nA (default) 01 = 22nA 10 = Reserved 11 = Reserved
1:0	0	Reserved. Must be set to '0'.

9.1.5 CH1SET: CHANNEL 1 SETTINGS (ADDRESS = 04H)

Return to the SUMMARY TABLE. This register configures the power mode, PGA gain, and multiplexer settings channels. See the INPUT MULTIPLEXER section for details.

Table 37. CH1SET Field Descriptions

BIT	FIELD	DESCRIPTION
7	PD1	Channel 1 power-down 0 = Normal operation (default) 1 = Channel 1 power-down(1)
6:4	GAIN1(2:0)	Channel 1 PGA gain setting These bits determine the PGA gain setting for channel 1. 000 = 6 (default) 001 = 1 010 = 2 011 = 3 100 = 4 101 = 8 110 = 12
3:0	MUX1(3:0)	Channel 1 input selection These bits determine the channel 1 input selection. 0000 = Normal sensor input (default) 0001 = Input shorted (for offset measurements) 0010 = BIAS_MEASURE 0011 = MVDD(2) for supply measurement 0100 = Temperature sensor 0101 = Test signal 0110 = BIAS_DRP (positive input is connected to BIASINP.) 0111 = BIAS_DRM (negative input is connected to BIASINP.) 1000 = BIAS_DRPM (both positive and negative inputs are connected to BIASIN.) 1001 = Route IN3P and IN3N to channel 1 inputs 1010 = Reserved 1011 = BIAS_OUT

Note 1: When powering down channel 1, make sure the input multiplexer is set to input short configuration. Bits(3:0) = 001.

Note 2: For channel 1, (MVDDP – MVDDN) is (0.5(AVDD + AVSS)).
For channel 2, (MVDDP – MVDDN) is DVDD / 4. Note that to avoid saturating the PGA while measuring power supplies, the gain must be set to '1'.

9.1.6 CH2SET: CHANNEL 2 SETTINGS (ADDRESS = 05H)

Return to the SUMMARY TABLE. This register configures the power mode, PGA gain, and multiplexer settings channels. See the INPUT MULTIPLEXER section for details.

Table 38. CH2SET Field Descriptions

BIT	FIELD	DESCRIPTION
7	PD2	Channel 2 power-down 0 = Normal operation (default) 1 = Channel 2 power-down(1)
6:4	GAIN2(2:0)	Channel 2 PGA gain setting These bits determine the PGA gain setting for channel 2. 000 = 6 (default) 011 = 3 100 = 4 101 = 8 110 = 12 Others: Reserved
3:0	MUX2(3:0)	Channel 2 Input Selection These Bits Determine The Channel 2 Input Selection. 0000 = Normal Sensor Input (Default) 0001 = Input Shorted (For Offset Measurements) 0010 = BIAS_MEASURE 0011 = VDD / 2 For Supply Measurement 0100 = Temperature Sensor 0101 = Test Signal 0110 = BIAS_DRP (Positive Input Is Connected To BIASINP.) 0111 = BIAS_DRM (Negative Input Is Connected To BIASINP.) 1000 = BIAS_DRPM (Both Positive And Negative Inputs Are Connected To BIASINP.) 1001 = Route IN3P And IN3N To Channel 2 Inputs 1010 = Reserved 1011 = BIAS_OUT Others: Reserved

Note: When powering down channel 2 and for the ADX320Q, make sure the input multiplexer is set to input short configuration. Bits(3:0) = 001.

9.1.7 BIAS_SENS: BIAS AMPLIFIER SENSE SELECTION (ADDRESS = 06H)

Return to the SUMMARY TABLE. This register controls the selection of the positive and negative signals from each channel for bias amplifier derivation. See the BIAS AMPLIFIER section for details.

Table 39. BIAS_SENS Field Descriptions

BIT	FIELD	DESCRIPTION
7:6	CHOP(1:0)	Chop frequency (NOT USED)
5	PDB_BIAS	BIAS buffer power This bit determines the BIAS buffer power state. 0 = BIAS buffer is powered down (default). 1 = BIAS buffer is enabled.
4	BIAS_BO_SENS	BIAS burn-out sense function This bit enables the BIAS burn-out sense function. 0 = BIAS burn-out sense is disabled (default). 1 = BIAS burn-out sense is enabled.
3	BIAS2N	Channel 2 BIAS negative inputs This bit controls the selection of negative inputs from channel 2 for bias amplifier derivation. 0 = Not connected (default) 1 = BIAS connected to IN2N
2	BIAS2P	Channel 2 BIAS positive inputs This bit controls the selection of positive inputs from channel 2 for bias amplifier derivation. 0 = Not connected (default) 1 = BIAS connected to IN2P
1	BIAS1N	Channel 1 BIAS negative inputs This bit controls the selection of negative inputs from channel 1 for bias amplifier derivation. 0 = Not connected (default) 1 = BIAS connected to IN1N
0	BIAS1P	Channel 1 BIAS positive inputs This bit controls the selection of positive inputs from channel 1 for bias amplifier derivation. 0 = Not connected (default) 1 = BIAS connected to IN1P

9.1.8 BO_SENS: BURN-OUT SENSE SELECTION (ADDRESS = 07H)

Return to the SUMMARY TABLE. This register selects the positive and negative side from each channel for sensor burn-out. See the SENSOR BURN-OUT section for details. Note that the BO_STAT register bits should be ignored if the corresponding BO_SENS bits are set to '1'.

Table 40. BO_SENS Field Descriptions

<table>
<tr><th>BIT</th><th>FIELD</th><th>DESCRIPTION</th></tr>
<tr><td>7</td><td>0</td><td>Reserved. Must be set to ‘0’.</td></tr>
<tr><td>6</td><td>CP_FREQ</td><td>Charge pump frequency selection
This bit sets the charge pump frequency with different WMODE setting. See the POWER MODE section.
<table>
<tr><th>BIT</th><th>HI-SPEED</th><th>HI-RESOLUTION</th></tr>
<tr><td>0</td><td>512kHz</td><td>256kHz</td></tr>
<tr><td>1</td><td>256kHz</td><td>128kHz</td></tr>
</table></td></tr>
<tr><td>5</td><td>FLIP2</td><td>Channel 2 comparator polarity selection
This bit controls the direction of the comparator used for burn-out derivation of channel 2.
0 = IN2P connects to the positive side of comparator, and IN2N connects to the negative side of comparator (default).
1 = IN2N connects to the positive side of comparator, and IN2P connects to the negative side of comparator.</td></tr>
<tr><td>4</td><td>FLIP1</td><td>Channel 1 comparator polarity selection
This bit controls the direction of the comparator used for burn-out derivation of channel 1.
0 = IN1P connects to the positive side of comparator, and IN1N connects to the negative side of comparator (default).
1 = IN1N connects to the positive side of comparator, and IN1P connects to the negative side of comparator.</td></tr>
<tr><td>3:0</td><td>EMUX_BO(3:0)</td><td>Channel 1 burn-out configuration setting
<table>
<tr><th>BIT</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0: The positive side of the input channel is disconnected to AVDD (default).
1: The positive side of the input channel is connected to AVDD.</td></tr>
<tr><td>1</td><td>0: The negative side of the input channel is disconnected to AVSS (default).
1: The negative side of the input channel is connected to AVSS.</td></tr>
<tr><td>2</td><td>0: The negative side of the input channel is disconnected to AVDD (default).
1: The negative side of the input channel is connected to AVDD.</td></tr>
<tr><td>3</td><td>0: The positive side of the input channel is disconnected to AVSS (default).
1: The positive side of the input channel is connected to AVSS.</td></tr>
</table></td></tr>
</table>

9.1.9 BO_STAT: BURN-OUT STATUS (ADDRESS = 08H)

Return to the SUMMARY TABLE. This register stores the status of whether the positive or negative sensor on each channel is on or off. See the SENSOR BURN-OUT section for details. Ignore the BO_STAT values if the corresponding BO_SENS bits are not set to '1'.

'0' is connected (default) and '1' is burn-out. When the BO_SENS bits(3:0) are '0', the BO_STAT bits should be ignored.

Table 41. BO_STAT Field Descriptions

BIT	FIELD	DESCRIPTION
7	0	Reserved. Must be set to '0'.
6:5	CLK_DIV(1:0)	Clock divider selection This bit sets the modular divider ratio between f_{CLK} and f_{MOD}. 00 = f_{MOD} = f_{CLK} / 4 01 = f_{MOD} = f_{CLK} / 8 10 = f_{MOD} = f_{CLK} / 16 11 = Reserved
4	BIAS_STAT	BIAS burn-out status This bit determines the status of BIAS. 0 = BIAS is connected (default). 1 = BIAS is not connected.
3	IN2N_OFF	Channel 2 negative sensor status This bit determines if the channel 2 negative sensor is connected. 0 = Connected (default) 1 = Not connected
2	IN2P_OFF	Channel 2 positive sensor status This bit determines if the channel 2 positive sensor is connected. 0 = Connected (default) 1 = Not connected
1	IN1N_OFF	Channel 1 negative sensor status This bit determines if the channel 1 negative sensor is connected. 0 = Connected (default) 1 = Not connected
0	IN1P_OFF	Channel 1 positive sensor status This bit determines if the channel 1 positive sensor is connected. 0 = Connected (default) 1 = Not connected

9.1.10 RSV: RESERVED REGISTER (ADDRESS = 09H)

Return to the SUMMARY TABLE.

Table 42. RSV Field Descriptions

BIT	FIELD	DESCRIPTION
7:2	0	Reserved. Must be set to '0'.
1	1	Reserved. Must be set to '1'.
0	0	Reserved. Must be set to '0'.

9.1.11 CAL: CALIBRATION REGISTER (ADDRESS = 0AH)

Return to the SUMMARY TABLE. This register controls the calibration functionality.

Table 43. CAL Field Descriptions

BIT	FIELD	DESCRIPTION
7	CALOFF_ON	Calibration on This bit is used to enable offset calibration. 0 = Off (default) 1 = On
6:1	0	Reserved. Must be set to '0'.
0	1	Reserved. Must be set to '1'.

9.1.12 GPIO: GENERAL-PURPOSE I/O REGISTER (ADDRESS = 0BH)

Return to the SUMMARY TABLE. This register controls the GPIO pins.

Table 44. GPIO Field Descriptions

BIT	FIELD	DESCRIPTION
7:4	0	Reserved. Must be set to '0'.
3:2	GPIOC(2:1)	GPIO 1 and 2 control These bits determine if the corresponding GPIOD pin is an input or output. 0 = Output 1 = Input (default)
1:0	GPIOD(2:1)	GPIO 1 and 2 data These bits are used to read and write data to the GPIO ports. When reading the register, the data returned correspond to the state of the GPIO external pins, no matter that they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect.

9.1.13 CONFIG3: FUNCTION CONFIGURATION REGISTER 3 (ADDRESS = 0CH)

Return to the SUMMARY TABLE. This register controls the feature configuration.

Table 45. CONFIG3 Field Descriptions

BIT	FIELD	DESCRIPTION
7	0	Reserved. Must be set to '0'.
6	P5VREF_ON	V_{REF} / 2 switch 0 = 1/2 V_{REF} switch is turned off (default). 1 = 1/2 V_{REF} switch is turned on.
5	0	Reserved. Must be set to '0'.
4	0	Reserved. Must be set to '0'.
3	DIN_CRC_EN	Communication input data CRC check enable 0 = Input data CRC disable (default) 1 = Input data CRC enable
2	DOUT_CRC_EN	Communication output data CRC check enable 0 = Output data CRC disable (default) 1 = Output data CRC enable
1:0	SPI_TIMEOUT(1:0)	SPI interface reset function control to detect idle clock number 00 = Disable (default) 01 = SPI interface will be reset after 255 divider clock cycles with BO_STAT(6).CLK_DIV configuration. 10 = SPI interface will be reset after 1023 divider clock cycles with BO_STAT(6).CLK_DIV configuration. 11 = SPI interface will be reset after 4095 divider clock cycles with BO_STAT(6).CLK_DIV configuration.

9.1.14 CONFIG4: FUNCTION CONFIGURATION REGISTER 4 (ADDRESS = 0DH)

Return to the SUMMARY TABLE. This register controls the feature configuration.

Table 46. CONFIG4 Field Descriptions

BIT	FIELD	DESCRIPTION
7	DR_INT_EN	ADC data out of range interrupt enable 0 = ADC data out of range interrupt disable (default) 1 = ADC data out of range interrupt enable
6:5	ADC_DAT_THD(1:0)	ADC data threshold to set out of range flag 00 = ADC data range exceeds 24-bit data range (default). Others = Reserved
4	0	Reserved. Must be set to '0'.
3	CLK_MISS_INT_EN	External clock miss interrupt enable 0 = Clock Miss Interrupt disable 1 = Clock Miss Interrupt enable
2	0	Reserved. Must be set to '0'.
1	BIASINP2RAMPP_ON	BIASINP input to BIAS AMP input positive switch 0 = Switch is disconnected (default). 1 = Switch is connected.
0	RAMPOUT2RAMPN_ON	BIAS AMP output to BIAS AMP input negative switch 0 = Switch is disconnected (default). 1 = Switch is connected.

9.1.15 CONFIG5: FUNCTION CONFIGURATION REGISTER 5 (ADDRESS = 0EH)

Return to the SUMMARY TABLE. This register controls the feature configuration.

Table 47. CONFIG5 Field Descriptions

BIT	FIELD	DESCRIPTION
7	OSC_2M_EN	2M OSC enable control External clock is selected when the CLKSEL pin is 0. It is used to monitor external CLK missing or invalid issue. 0 = Disable OSC (default). 1 = Enable OSC to check External Clock idle status.
6:4	INTGPIO(2:0)	Interrupt output to GPIO, including BO interrupt INT1, ADC data out of range interrupt INT2, FIFO interrupt INT3, CLK missing interrupt INT4, and invalid SPI command interrupt INT5. 000 = INT1, INT2, INT3, INT4, INT5 output to external with GPIO1. 001 = INT1, INT2, INT3, INT4, INT5 output to external with GPIO2. 010 = INT1, INT2, INT3, INT5 output to external with GPIO1, INT4 output to external with GPIO2. 011 = INT1, INT2, INT4, INT5 output to external with GPIO1, INT3 output to external with GPIO2. 100 = INT1, INT3, INT4, INT5 output to external with GPIO1, INT2 output to external with GPIO2. 101 = INT2, INT3, INT4, INT5 output to external with GPIO1, INT1 output to external with GPIO2. 110 = INT1, INT2, INT3, INT4 output to external with GPIO1, INT5 output to external with GPIO2. 111 = NO interrupt output to GPIO pin. (default) Others = Reserved
3	INV_CMD_INT_EN	Invalid SPI command interrupt enable It generates an interrupt for the invalid command if the command is detected. 0 = Invalid SPI command Interrupt disable 1 = Invalid SPI command Interrupt enable
2	FRAME_CHK_EN	FRAME Overwrite Check enable (it does not check FIFO overwrite) 0 = Disable FRAME miss check for SPI slow read (default) 1 = Enable FRAME miss check for SPI slow read
1	IO_3MA	IO strong (3mA) mode enable 0 = Strong mode disable (default) 1 = Strong mode enable
0	IO_SRM	IO slew read mode enable 1 = IO slew read mode enable (default) 0 = IO slew read mode disable

9.1.16 BO_ISTEP: BURN-OUT CURRENT STEP CONFIGURATION REGISTER (ADDRESS = 0FH)

Return to the SUMMARY TABLE. This register controls the IDAC current step.

Table 48. BO_ISTEP Field Descriptions

BIT	FIELD	DESCRIPTION
7	BO_INT_EN	Burn-out interrupt enable 0 = Burn-out interrupt disable (default) 1 = Burn-out interrupt enable, and the interrupt is output to the GPIO1 or GPIO2 pin.
6	CUR_LEVEL	Burn-out current level selection it this bit is zero, the IDAC current setting comes from the IBURN-OUT(1:0) value. 0 = Disable ISTEP value configuration (default) 1 = Enable ISTEP value configuration
5:0	ISTEP(5:0)	Burn-out current magnitude These bits determine the magnitude of current for the current burn-out mode when CUR_LEVEL is one; otherwise the current magnitude is decided by the IBURN-OUT(1:0) fields. 000000 = 0nA and step = 2.7nA (default) 000001 = 2.7nA ……. 111111 = 173.25nA

9.1.17 BO_BIAS: BURN-OUT STEP CONFIGURATION REGISTER (ADDRESS = 10H)

Return to the SUMMARY TABLE. This register controls the BIAS threshold step.

Table 49. BO_BIAS Field Descriptions

BIT	FIELD	DESCRIPTION
7:4	EMUX_BO(3:0)	Channel 2 burn-out configuration setting
3:0	0	Reserved. Must be set to ‘0’.

BIT	DESCRIPTION
0	0: The positive side of the input channel is disconnected to AVDD (default). 1: The positive side of the input channel is connected to AVDD.
1	0: The negative side of the input channel is disconnected to AVSS (default). 1: The negative side of the input channel is connected to AVSS.
2	0: The negative side of the input channel is disconnected to AVDD (default). 1: The negative side of the input channel is connected to AVDD.
3	0: The positive side of the input channel is disconnected to AVSS (default). 1: The positive side of the input channel is connected to AVSS.

9.1.18 BO_CFG: BURN-OUT CONFIGURATION REGISTER (ADDRESS = 12H)

Return to the SUMMARY TABLE. This register controls the burn-out detection.

Table 50. BO_CFG Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	0	Reserved. Must be set to '0'.
4:3	DEBOUNCE(1:0)	Burn-out output debounce time 00 = Debounce disable (default) 01 = Debounce time 117ms 10 = Debounce time 335ms 11 = Reserved
2	OFC_EN	Function offset calibration enable 0 = User calibration disable 1 = User calibration enable
1:0	0	Reserved. Must be set to '0'.

9.1.19 PWR: POWER MODE REGISTER (ADDRESS = 13H)

Return to the SUMMARY TABLE. This register controls sensor rotation mode.

Table 51. PWR Field Descriptions

BIT	FIELD	DESCRIPTION
7	0	Reserved. Must be set to '0'.
6	WMODE	Device power mode selection 00 = High-Speed mode 01 = High-Resolution mode 10 = Reserved 11 = Reserved
5:0	0	Reserved. Must be set to '0'.

9.1.20 CLK-CFG: CLOCK CONFIGURATION REGISTER (ADDRESS = 14H)

Return to the SUMMARY TABLE. This register controls the configuration.

Table 52. CLK-CFG Field Descriptions

BIT	FIELD	DESCRIPTION
7:6	0	Reserved. Must be set to '0'.
5	SHORT_PROTECT	SHORT_PROTECT enable control 0 = Short protect disable (default) 1 = Short protect enable
4:3	FSEL(1:0)	FSEL to select internal OSC clock frequency 00 = Reserved 01 = 1024kHz 10 = 512kHz (default) 11 = 256kHz
2	DOUT_DO3MA	DOUT pin current strength control 0 = DOUT pin has strong driving strength. 1 = DOUT pin has low driving strength to save power.
1:0	0	Reserved. Must be set to '0'.

9.1.21 FIFO_CFG1: FIFO CONFIGURATION REGISTER 1 (ADDRESS = 16H)

Return to the SUMMARY TABLE. This register controls the FIFO configuration.

Table 53. FIFO_CFG1 Field Descriptions

BIT	FIELD	DESCRIPTION
7	FIFO_INT_EN	FIFO interrupt enable when FIFO data hit threshold. 0: FIFO interrupt disable (default) 1: FIFO interrupt enable
6:5	0	Reserved. Must be set to '0'.
4	FIFO_RST	FIFO reset control 0 = FIFO software reset disable (default). 1 = FIFO software reset enable. Software must write 0 to clear the FIFO_RST bit.
3:1	FRAME_CFG(2:0)	FRAME configuration 5-bit burn-out (BIAS_stat, in2n_off, in2p_off, in1n_off, in1p_off) 3-bit burn-out (BIAS_stat, in2n_off, in2p_off) when channel 2 is active. 3-bit burn-out (BIAS_stat, in1n_off, in1p_off) when channel 1 is active.
0	FIFO_EN	FIFO enable control 0 = FIFO is disabled (default). 1 = FIFO is enabled.

BIT	DESCRIPTION
000	Only one active channel for conversion data The frame format is as below (default): 3-bit burn-out (1st), 3-bit burn-out (2nd), 1-bit DUMMY (1st) or 1-bit GPIO (1st), 1-bit DUMMY (2nd) or 1-bit GPIO (2nd), 24-bit conversion data (1st), 24-bit conversion data (2nd)
001	Two active channels for conversion data The frame format is as below: {5-bit burn-out, 1'b0, 2-bit GPIO or 2-bit DUMMY data, 24-bit CH1 conversion data, 24-bit CH2 conversion data}
Others	Reserved

9.1.22 FIFO_CFG2: FIFO CONFIGURATION REGISTER 2 (ADDRESS = 17H)

Return to the SUMMARY TABLE. This register controls the FIFO configuration.

Table 54. FIFO_CFG2 Field Descriptions

BIT	FIELD	DESCRIPTION
7:5	STATUS_SEL(2:0)	FIFO read pointer overwrite pointer FAULT 000 = No GPIO into FIFO frame (default) 001 = Put GPIO1 data into FIFO frame 010 = Put GPIO2 data into FIFO frame 011 = Put GPIO1 and GPIO2 data into FIFO frame Others = Reserved
4:0	DEPTH(4:0)	FIFO data to trigger MCU read data 00000 = 1-item data to trigger MCU read data (default) 00001 = 2-item data to trigger MCU read data 00010 = 3-item data to trigger MCU read data … 01011 = 12-item data to trigger MCU read data Others = Reserved

9.1.23 FIFO_STAT: FIFO STATUS REGISTER (ADDRESS = 18H)

Return to the SUMMARY TABLE. This register controls the FIFO status.

Table 55. FIFO_STAT Field Descriptions

BIT	FIELD	DESCRIPTION
7	FIFO_RDY	FIFO data is ready for MCU read. 0 = FIFO data does not meet threshold (default). 1 = FIFO data is ready for MCU read.
6	FIFO_EMPTY	FIFO status 0 = FIFO is not empty. 1 = FIFO is empty (default).
5	FIFO_FULL	FIFO status 0 = FIFO is not full (default). 1 = FIFO is full.
4	FIFO_ERROR	FIFO error occurs. Write the FIFO_RST field of FIFO_CFG1 to clear FIFO error. 0 = No FIFO error. 1 = If FIFO is disabled and FIFO read pointer is not equal to write pointer, the FIFO error occurs. FIFO will be disabled when the read/write is triggered unexpectedly, or when FIFO is not empty.
3:0	DLVL(3:0)	FIFO data watermark level for MCU read data 0000 = No-item data in FIFO for MCU read (default) 0001 = 1-item data in FIFO for MCU read data 0010 = 2-item data in FIFO for MCU read data … 1011 = 12-item data in FIFO for MCU read data Others = Reserved

9.1.24 MOD_STAT1: INTERNAL MODULE STATUS REGISTER 1 (ADDRESS = 19H)

Return to the SUMMARY TABLE. This register stores the status of device submodule.

Table 56. MOD_STAT1 Field Descriptions

BIT	FIELD	DESCRIPTION
7	INVALID_CMD_ERR	Invalid SPI command is detected. Only the first invalid command will set this bit, Ignore this bit when DIN_CRC_EN is set. 0 = There is no invalid SPI command error. 1 = There is an invalid SPI command error.
6	SHORT_GND	Digital pin shorted to ground. Software needs to write zero to clear last status before using it again. 0 = No pin shorted to ground (default) 1 = Digital pin shorted to ground
5	CLK_MISS	Input clock missing or invalid issue occurs. This bit will always be set until device reset is triggered. This is a critical fault for application. 0 = No clock missing occurs (default). 1 = Clock missing occurs.
4	FRAME_MISS	Frame buffer overwrite occurs. 0 = No frame buffer overwrite (default). 1 = Frame buffer is overwritten and missing occurs.
3	DAT_CRC_ERR	SPI write command and data CRC error occurs. 0 = SPI write data has no CRC error (default). 1 = SPI write data has CRC error.
2	CMD_CRC_ERR	SPI command CRC error occurs, except WREG command 0 = Input command has no CRC error (default). 1 = Input command has CRC error.
1	OORNG	ADC value out-of-range occurs. The ADC result out of range flag (default) 0 = ADC value not out of range 1 = ADC value out of range
0	SHORT_PWR	Digital pin shorted to power. Software needs to write zero to clear last status before using it again. 0 = No pin shorted to power (default) 1 = Digital pin shorted to power

9.1.25 MOD_STAT2: INTERNAL MODULE REGISTER 2 (ADDRESS = 1AH)

Return to the SUMMARY TABLE. This register stores the status of device submodule.

Table 57. MOD_STAT2 Field Descriptions

BIT	FIELD	DESCRIPTION
7	BIAS_BO_P	BIAS burn-out status Software needs to write zero to clear last status before using it again. 0 = No BIAS positive burn-out occurs (default). 1 = BIAS positive burn-out occurs.
6	BIAS_BO_N	BIAS burn-out status Software needs to write zero to clear last status before using it again. 0 = No BIAS negative burn-out occurs (default). 1 = BIAS negative burn-out occurs.
5	0	Reserved. Must be set to '0'.
4	0	Reserved. Must be set to '0'.
3	PGA2N_OOR	PGA2 negative out of range Software needs to write zero to clear last status before using it again. 0 = No PGA2 negative out of range (default). 1 = PGA2 negative out of range occurs.
2	PGA2P_OOR	PGA2 positive out of range Software needs to write zero to clear last status before using it again. 0 = No PGA2 positive out of range (default). 1 = PGA2 positive out of range occurs.
1	PGA1N_OOR	PGA1 negative out of range Software needs to write zero to clear last status before using it again. 0 = No PGA1 negative out of range (default). 1 = PGA1 negative out of range occurs.
0	PGA1P_OOR	PGA1 positive out of range Software needs to write zero to clear last status before using it again. 0 = No PGA1 positive out of range (default). 1 = PGA1 positive out of range occurs.

9.1.26 OP_STAT_CMD: OPERATION STATUS COMMAND REGISTER (ADDRESS = 1BH)

Return to the SUMMARY TABLE. This register stores the status of user command.

Table 58. OP_STAT_CMD Field Descriptions

BIT	FIELD	DESCRIPTION
7	EFU_UERR	eFuse unacceptable error 0 = No unacceptable error 1 = Unacceptable error
6	EFU_CERR	eFuse Correct error 0 = No correctable error 1 = Correctable error
5	RDATAC_DONE	RDATA Continuously command The bit shows the RDATA command status if device executes the RDATAC command. 0 = NO RDATAC command is executed (default). 1 = RDATAC command is executed.
4	RD_FIFO_DONE	FIFO Read Command execution status when FIFO is enabled. The RFIFO command will be dropped if FIFO is enabled. 0 = Device has NOT executed the RFIFO command (default). 1 = Device has executed the RFIFO command.
3	CAL_DONE	Device Calibration done The bit shows the Channel Offset Calibration status if device executes the OFFSETCAL command. 0 = No device calibration (default) 1 = Device calibration done
2	RDATA_DONE	Read ADC data to shift register status. 0 = Device has NOT executed the RDATA command (default) 1 = Device has executed the RDATA command.
1	REG_WR_DONE	Device has executed a WREG command. 0 = Device has NOT executed the WREG command (default). 1 = Device has executed the WREG command
0	REG_RD_DONE	Device has executed a RREG command. 0 = Device has NOT executed the RREG command (default). 1 = Device has executed the RREG command.

9.1.27 OP_STAT_SYS: SYSTEM OPERATION STATUS REGISTER (ADDRESS = 1CH)

Return to the SUMMARY TABLE. This register stores the status of user operation.

Table 59. OP_STAT_SYS Field Descriptions

BIT	FIELD	DESCRIPTION
7	SPI_UNLOCK	Device is locked for the LOCK command. The device SPI is in locked status if device executes the UNLOCK command, and the status is cleared to zero when device executes the LOCK command. 0 = SPI interface is locked. 1 = SPI interface is unlocked (default).
6	SPI_LOCK	Device is locked for the LOCK command. The device SPI is in locked status if device executes the LOCK command, and the status is cleared to zero when device executes the UNLOCK command. 0 = SPI interface is unlocked (default). 1 = SPI interface is locked.
5	SDC_MODE	Stop Read Data Continuously mode The device is in Stop Read Data Continuously mode if device executes the SDATAC command. The status is cleared to zero when device executes the RDATAC command. 0 = Device in Read Data Continuously mode (default). 1 = Device NOT in Read Data Continuously mode
4	RDC_MODE	Read Data Continuously mode (only indicates device mode) The device is in Read Data Continuously mode if device executes the RDATAC command. The status is cleared to zero when device executes the SDATAC command. 0 = Device NOT in Read Data Continuously mode 1 = Device in Read Data Continuously mode (default)
3	STOP	Stop Conversion status The device is in Stop Conversion state if device executes the STOP command. The status is cleared to ZERO when device executes the START command or sets the START pin. 0 = Device NOT in Stop Conversion status (default). 1 = Device in Stop Conversions status
2	START	Start Conversion status The device has executed the START command or a valid START event from the START pin. 0 = Device has NOT executed the START command or START Pin event (default). 1 = Device executed a START command or START Pin event.
1	WAKEUP	Device in WAKEUP mode The device is in WAKEUP mode if the device executes a wakeup command. The bit is cleared to zero if the device executes a STANDBY command. 0 = Device NOT in WAKEUP mode 1 = Device in WAKEUP mode (default)
0	STANDBY	Device in STANDBY mode The device is in STANDBY mode if the device executes a standby command. The bit is cleared to zero if the device executes a WAKEUP command. 0 = Device NOT in STANDBY mode (default) 1 = Device in STANDBY mode

9.1.28 FI: FUCTION INDICATOR REGISTER (READ-ONLY) (ADDRESS = 1DH)

Return to the SUMMARY TABLE. This register stores the device manufacture information.

Table 60. FI Field Descriptions

BIT	FIELD	DESCRIPTION
7:6	0	Reserved. Must be set to '0'.
5:0	FS_ID(5:0)	Feature set identification Bit 0 = 0: Bit 1 = 0: Bit 2 = 0: Bit 3 = 0: Has FIFO Bit 4 = 0: Has DFS Bit 5 = 0: Has DHP

9.1.29 ID_PR: ID PART INFORMATION REGISTER (READ-ONLY) (ADDRESS = 1EH)

Return to the SUMMARY TABLE. This register indicates the device part information.

Table 61. ID_PR Field Descriptions

BIT	FIELD	DESCRIPTION
7:4	PAR_ID(3:0)	Identification 0x7: ADX320Q/ADX3202Q Others: Reserved
3:0	0	Reserved. Must be set to '0'.

9.1.30 OFC_CH10: CHANNEL 1 OFFSET CALIBRATION REGISTER 0 (ADDRESS = 22H)

Return to the SUMMARY TABLE. This register controls the channel 1 offset calibration.

Table 62. OFC_CH10 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(7:0)	Offset calibration register byte 0 (channel 1)

9.1.31 OFC_CH11: CHANNEL 1 OFFSET CALIBRATION REGISTER 1 (ADDRESS = 23H)

Return to the SUMMARY TABLE. This register controls the channel 1 offset calibration.

Table 63. OFC_CH11 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(15:8)	Offset calibration register byte 1 (channel 1)

9.1.32 OFC_CH12: CHANNEL 1 OFFSET CALIBRATION REGISTFER 2 (ADDRESS = 24H)

Return to the SUMMARY TABLE. This register controls the channel 1 offset calibration.

Table 64. OFC_CH12 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(23:16)	Offset calibration register byte 2 (channel 1)

9.1.33 OFC_CH20: CHANNEL 2 OFFSET CALIBRATION REGISTER 0 (ADDRESS = 25H)

Return to the SUMMARY TABLE. This register controls the channel 2 offset calibration.

Table 65. OFC_CH20 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(7:0)	Offset calibration register byte 0 (channel 2)

9.1.34 OFC_CH21: CHANNEL 2 OFFSET CALIBRATION REGISTER 1 (ADDRESS = 26H)

Return to the SUMMARY TABLE. This register controls the channel 2 offset calibration.

Table 66. OFC_CH21 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(15:8)	Offset calibration register byte 1 (channel 2)

9.1.35 OFC_CH22: CHANNEL 2 OFFSET CALIBRATION REGISTER 2 (ADDRESS = 27H)

Return to the SUMMARY TABLE. This register controls the channel 2 offset calibration.

Table 67. OFC_CH22 Field Descriptions

BIT	FIELD	DESCRIPTION
7:0	OFC_B(23:16)	Offset calibration register byte 2 (channel 2)

9.1.36 RSV: RESERVED REGISTER (ADDRESS = 28H)

Return to the SUMMARY TABLE.

Table 68. RSV Field Descriptions

BIT	FIELD	DESCRIPTION
7:3	0	Reserved. Must be set to '0'.
2	1	Reserved. Must be set to '1'.
1:0	0	Reserved. Must be set to '0'.

10. POWER SUPPLY RECOMMENDATIONS

The nominal performance of the device is specified with an analog supply voltage AVDD of 3V and an internal reference voltage VREFP of 2.4V. The device also operates using power supplies at the AVDD pin from 2.7V to 5.5V with excellent performance.

10.1 POWER-SUPPLY SEQUENCING

Before device power-up, all digital and analog inputs must be low. At the time of power-up, all of these signals should remain low until the power supplies have stabilized, as shown in Figure 59. At this time, begin supplying the master clock signal to the CLK pin. Wait for time t_{POR}, then transmit a RESET pulse. After releasing RESET, the configuration register must be programmed, see the CONFIG1 register for details. The power-up sequence timing is shown in Table 69.

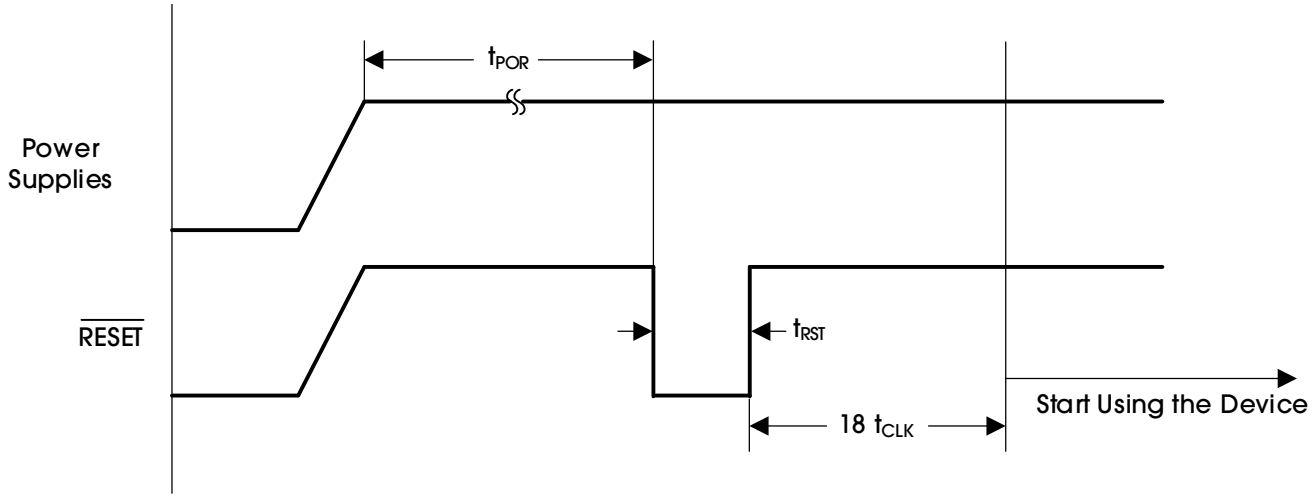


Figure 59. Power-Up Timing Diagram

Table 69. Power-Up Sequence Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Wait after Power-Up until Reset	t_{POR}	2^{12}			t_{MOD}
Reset Low Width	t_{RST}	1			t_{MOD}

11. LAYOUT

11.1 LAYOUT GUIDELINES

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices.

Noise propagates into analog circuitry through the power pins of the circuit as a whole and of the device. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry. Connect low-ESR, 0.1μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.

To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.

Place the external components as close to the device as possible. Keep the traces as short as possible.

11.1.1 PCB LAYOUT

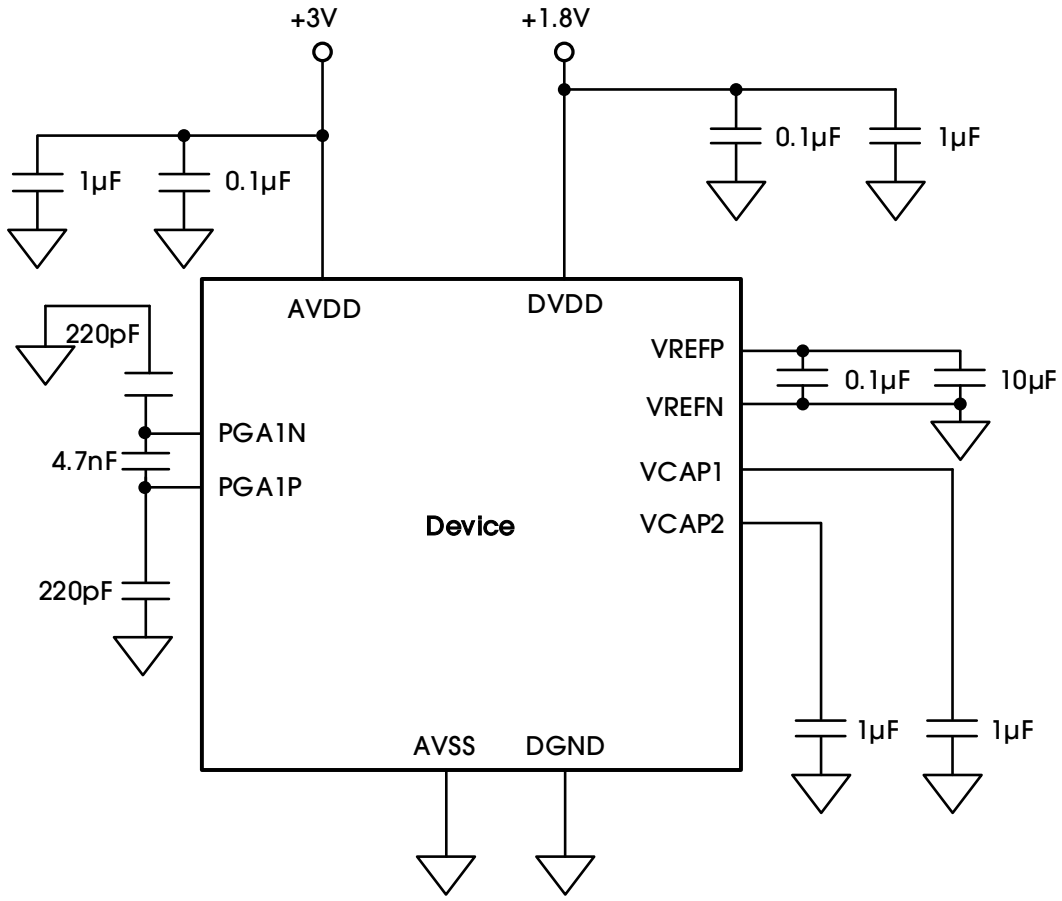
11.1.1.1 POWER SUPPLIES AND GROUNDING

The ADX320Q/ADX3202Q devices have two supplies: AVDD and DVDD. AVDD should be as quiet as possible. AVDD provides the supply to the charge pump block and has transients at f_{CLK}. It is important to eliminate noise from AVDD that is non-synchronous with the ADX320Q/ADX3202Q operation. Each ADX320Q/ADX3202Q supply should be bypassed with 10μF and a 0.1μF solid ceramic capacitors. It is recommended that placement of the digital circuits (such as the DSP, microcontrollers, and FPGAs) in the system is done so that the return currents on those devices do not cross the ADX320Q/ADX3202Q analog return path. The ADX320Q/ADX3202Q can be powered from unipolar or bipolar supplies.

The capacitors used for decoupling can be of the surface-mount, low-cost, low-profile multi-layer ceramic type. In most cases, the VCAP1 capacitor can also be a multi-layer ceramic, but in systems where the board is subjected to high or low frequency vibration, it is recommended that a non-ferroelectric capacitor such as a tantalum or class 1 capacitor (for example, C0G or NPO) be installed. EIA class 2 and class 3 dielectrics (such as X7R, X5R, X8R, and such) are ferroelectric. The piezoelectric property of these capacitors can appear as electrical noise coming from the capacitor. When using internal reference, noise on the VCAP1 node results in performance degradation.

11.1.1.1.1 CONNECTING THE DEVICE TO UNIPOLAR (+3V OR +1.8V) SUPPLIES

Figure 60 shows the ADX320Q/ADX3202Q connected to a unipolar supply. In this example, the analog supply (AVDD) is referenced to analog ground (AVSS) and the digital supply (DVDD) is referenced to digital ground (DGND).

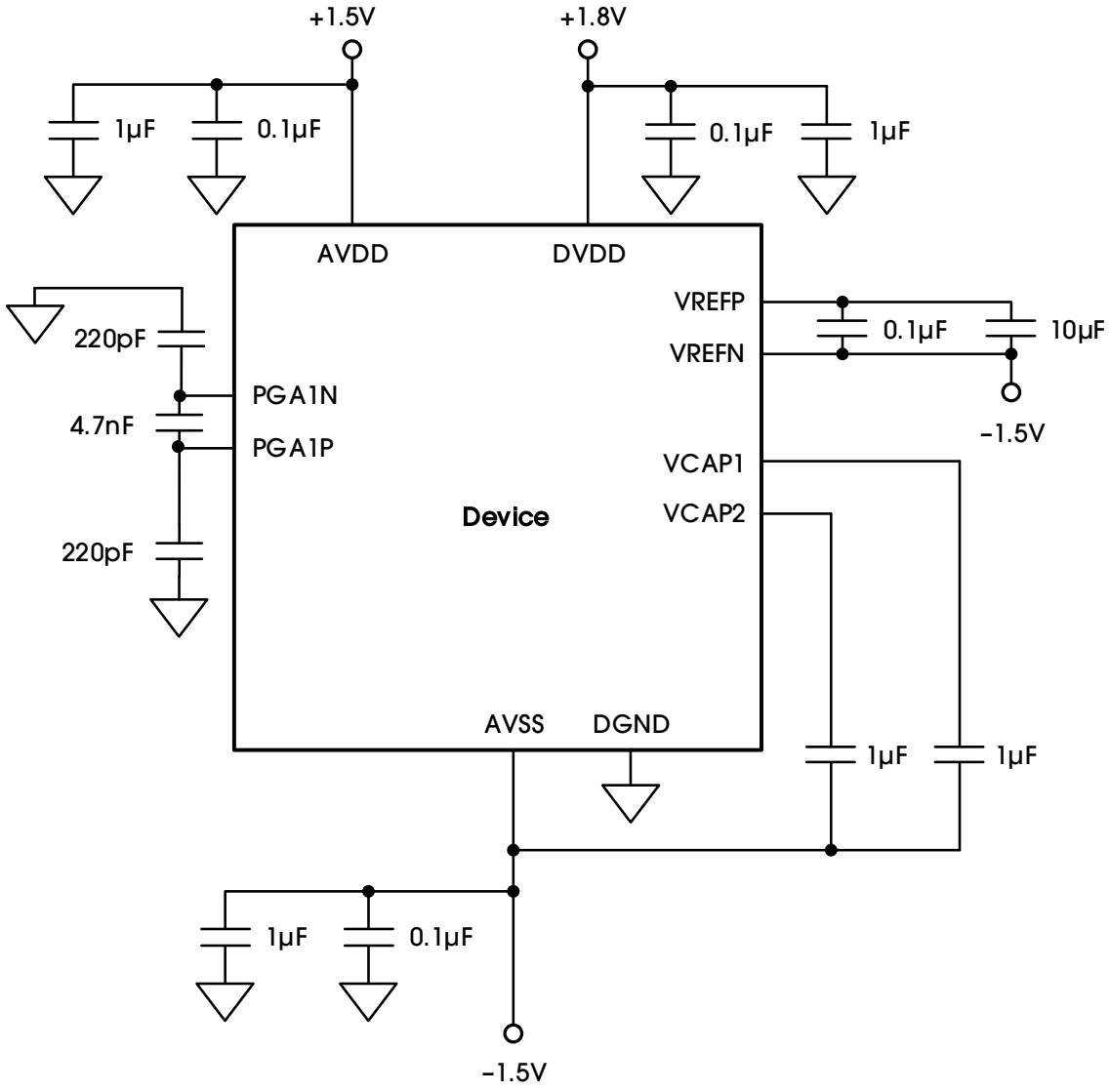


Regarding the capacitors for supply, reference, VCAP1, and VCAP2, place them as close to the package as possible.

Figure 60. Single-Supply Operation

11.1.1.1.2 CONNECTING THE DEVICE TO BIPOLAR (±1.5V OR 1.8V) SUPPLIES

Figure 61 illustrates the ADX320Q/ADX3202Q connected to a bipolar supply. In this example, the analog supplies connect to the device analog supply (AVDD). This supply is referenced to the device analog return (AVSS), and the digital supply (DVDD) is referenced to the device digital ground return (DGND).



Regarding the capacitors for supply, reference, VCAP1, and VCAP2, place them as close to the package as possible.

Figure 61. Bipolar Supply Operation

11.1.1.2 SHIELDING ANALOG SIGNAL PATHS

As with any precision circuit, careful PCB layout ensures the best performance. It is essential to make short, direct interconnections and avoid stray wiring capacitance—particularly at the analog input pins and AVSS. These analog input pins are high-impedance and extremely sensitive to extraneous noise. The AVSS pin should be treated as a sensitive analog signal and connected directly to the supply ground with proper shielding. Leakage currents between the PCB traces can exceed the ADX320Q/ADX3202Q input bias current if shielding is not implemented. Digital signals should be kept as far as possible from the analog input signals on the PCB.

11.2 LAYOUT EXAMPLE

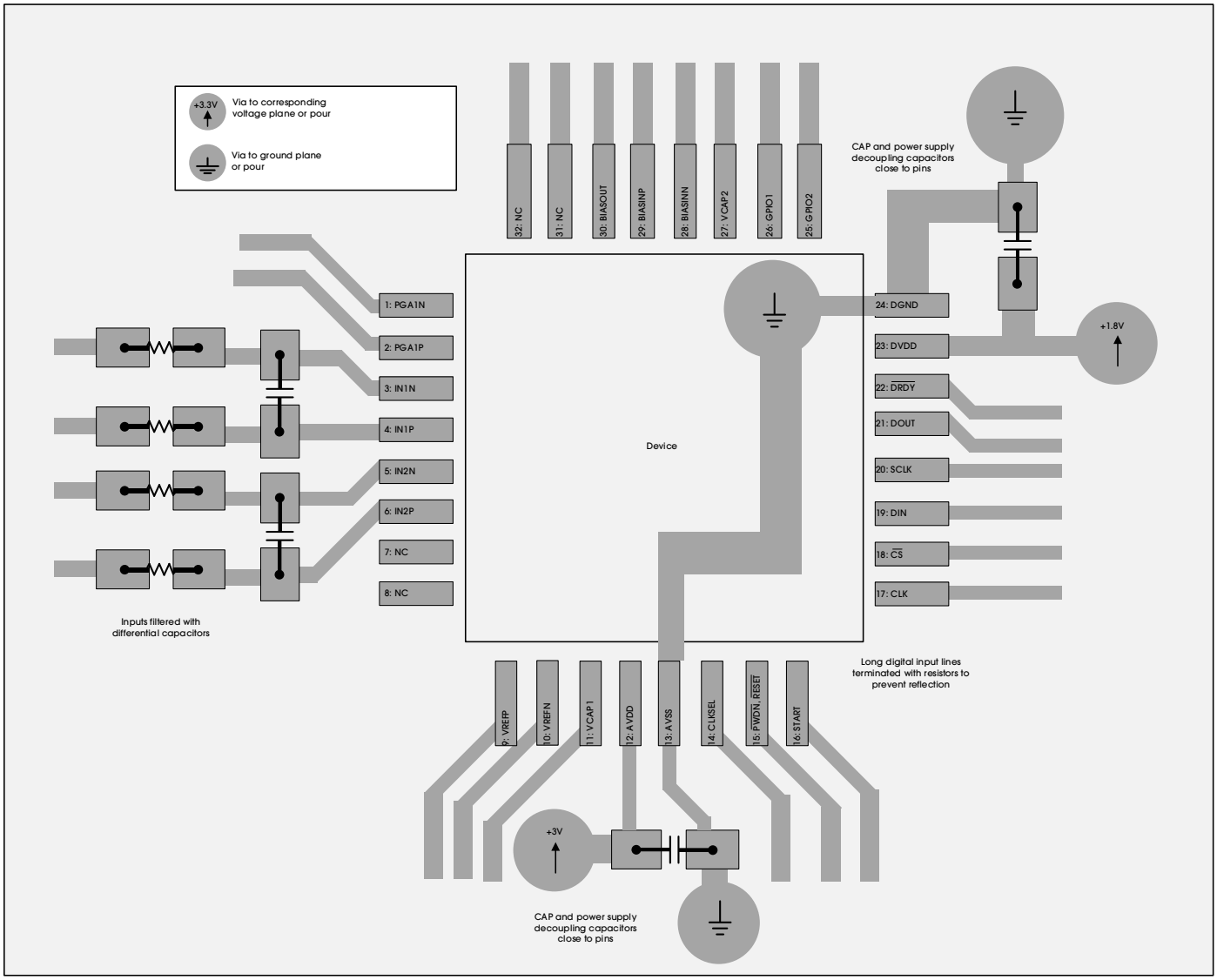


Figure 62. Example PCB Layout for Single-Supply Operation

12. PACKAGE INFORMATION

The ADX320Q/ADX3202Q is available in the QFN-32 packages. Figure 63 shows the package view.

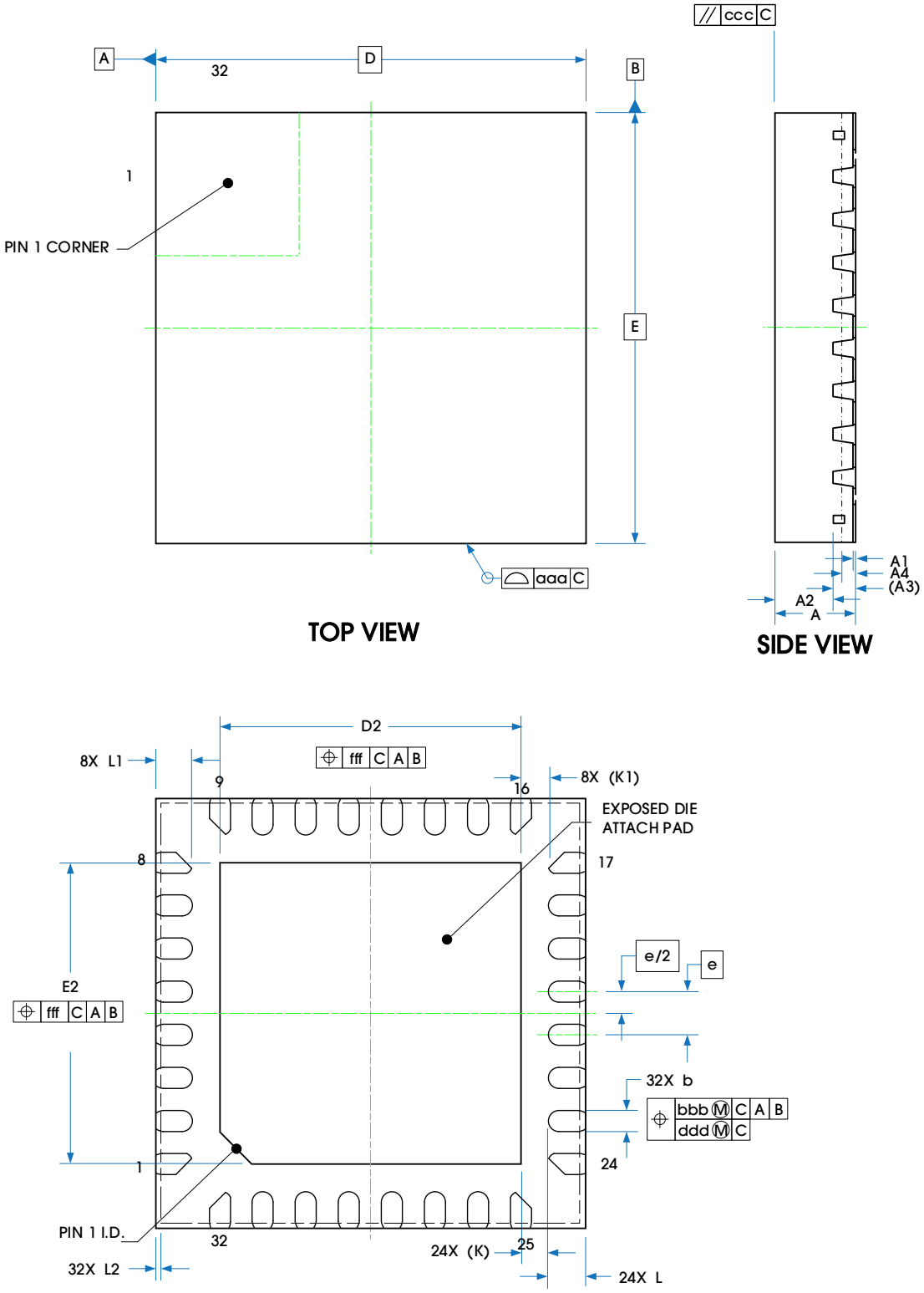


Figure 63. Package View

Table 70 provides detailed information about the dimensions.

Table 70. Dimensions

PARAMETER		SYMBOL	DIMENSIONS IN MILLIMETERS		
			MIN	NOM	MAX
Total Thickness		A	0.7	0.75	0.8
Stand Off		A1	0	0.02	0.05
Mold Thickness		A2	—	0.55	—
L/F Thickness		A3		0.203 REF	
Side Wettable Depth		A4	0.075	—	0.18
Lead Width		b	0.15	0.2	0.25
Body Size	X	D		4 BSC	
	Y	E		4 BSC	
Lead Pitch		e		0.4 BSC	
EP Size	X	D2	2.7	2.8	2.9
	Y	E2	2.7	2.8	2.9
Lead Length		L	0.25	0.35	0.45
		L1	0.235	0.335	0.435
Side Wettable Width		L2	0.01	—	0.09
Lead Tip to Exposed Pad Edge		K		0.25 REF	
		K1		0.265 REF	
Package Edge Tolerance		aaa		0.1	
Mold Flatness		ccc		0.1	
Lead Offset		bbb		0.07	
		ddd		0.05	
Exposed Pad Offset		fff		0.1	

13. TAPE AND REEL INFORMATION

Figure 64 illustrates the carrier tape.

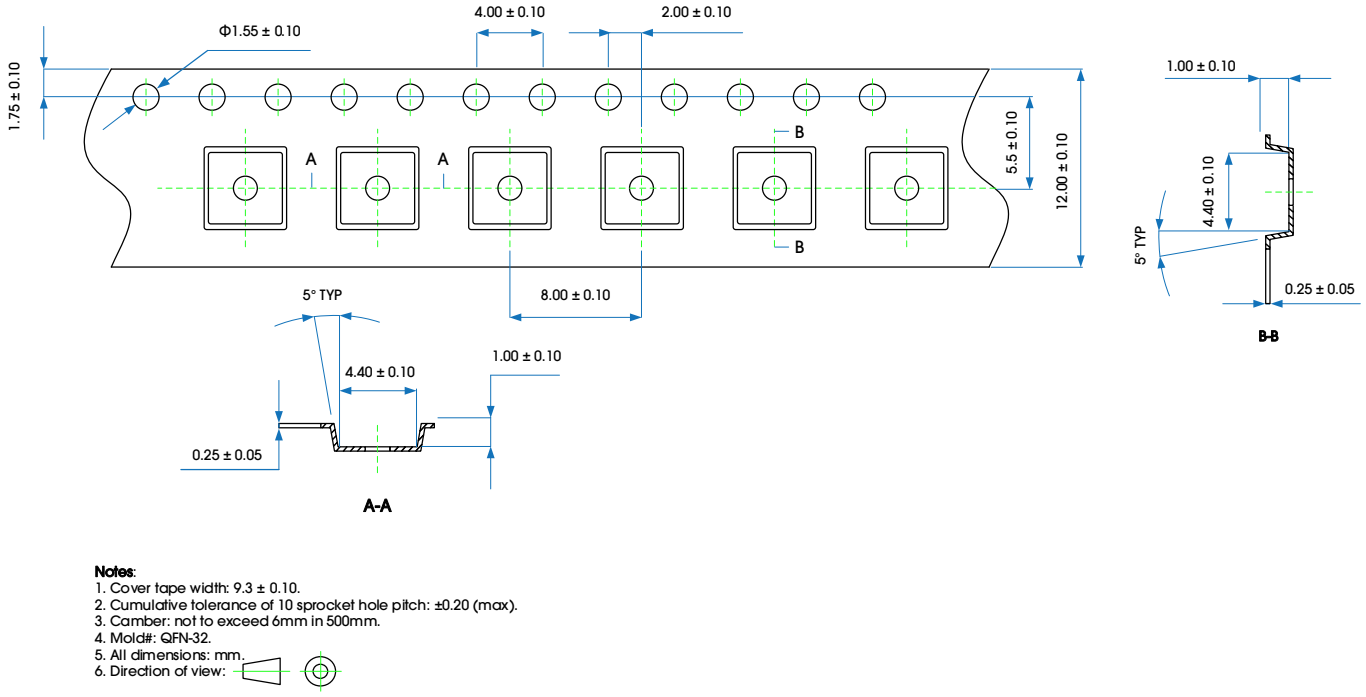


Figure 64. Carrier Tape Drawing

Table 71 provides information about tape and reel.

Table 71. Tape and Reel Information

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (MM)	CARTON SIZE (MM)
QFN-32	7''	1500	1	20	30000	240*20*265	455*275*255

Figure 65 shows the product loading orientation—pin 1 is assigned at Q2.

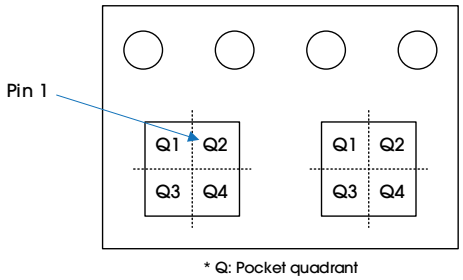


Figure 65. Product Loading Orientation

REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	01 December 2022	Rev A release.