AE98

10 Gb/s Ethernet Optical Switch Port

Features

- **Provides LAN/WAN PHY layer operations for IEEE 802.3 10 Gigabit Ethernet**
- **Includes MAC layer ethernet functionality plus TCP/UDP and IP hardware assist**
- **Supports 16-bit wide LVDS 622/645 MHz System Packet Interface Level 4 (SPI-4).**
- **Delivers network side data over full-duplex 16-bit wide LVDS interface at 622 MHz in WAN mode or 644 MHz in LAN mode**
- **Performs SONET/SDH compatible encapsulation for transmission over OC-192/ STMo-64 or faster fiber links**
- **Includes 128 kbytes of buffering for Rx frames**
- **Provides network and chip statistics**
- **Requires minimal number of power supplies and external components for simplified integration and operation**
- **Manufactured in 0.15 micron CMOS technology**

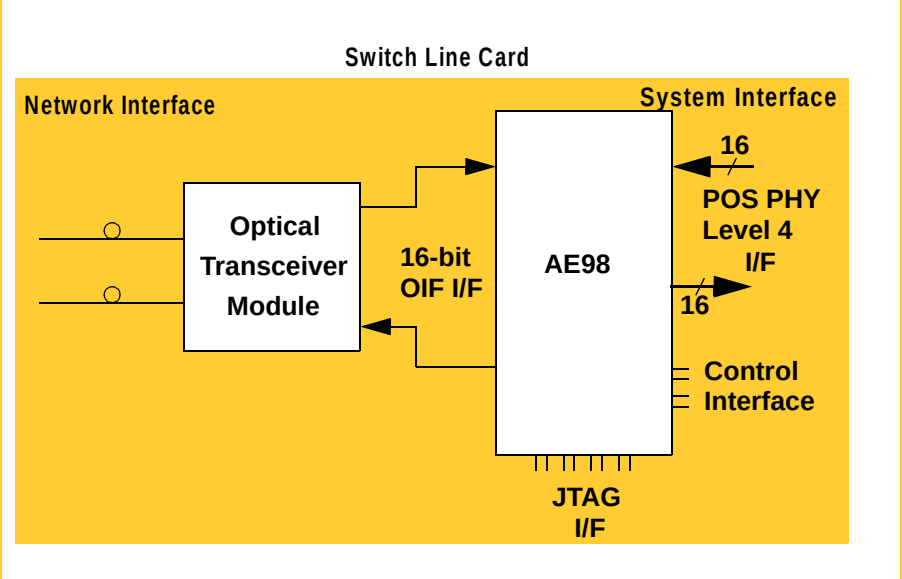
General Description

The Nortel Networks AE98 is a single-chip implementation of the PHY and MAC layer functions of a 10Gb/s Ethernet interface. The device is optimized for a System Packet Interface Level 4 (SPI-4) cell and packet interface for switches requiring cost-effective access to 10 Gb/s Ethernet pipes.

Typically the device accepts TCP/IP or UDP/IP packets, encapsulates them in Ethernet frames, encodes the data for efficient delineation and improved security, then packages it in SONET/ SDH compatible WIS frames for transmission over high performance fiber links. WIS encapsulation can be bypassed to support LAN applications. The AE98 operates in full-duplex mode, providing independent transmit and receive paths on one chip.

The High Performance Optical Component Solutions group of Nortel Networks offers a portfolio of optical ICs for use in high-performance networks applications. The AE98 is part of our family of 10 Gb/s

System block diagram



Advanced Information

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components which provides for power and chip count savings to the designer of fiber-based datacom or telecom solutions

Functional Description

Standard Interfaces

The AE98 includes an OIF SFI-4 compliant 16-bit LVDS XBI interface on the network side, and a 622/645 MHz System Packet Interface Level 4 (SPI-4) on the system side. The network interface facilitates the connection to optical transceiver modules capable of transmitting and receiving 802.3ae compliant Ethernet data streams. The system interface supports dual 10 Gb/s transmit and receive data rates with a flow control scheme to minimize the amount of buffering on the AE98. A separate management interface provides access for configuration and statistics reporting.

IEEE 802.3 compliance

The AE98 performs the tasks defined by the MAC, PCS, and WIS sub-layers, as defined by IEEE 802.3 for 10 Gigabit Ethernet. This includes Ethernet encapsulation and error checking, PCS 64b/66b encoding/decoding, and WIS framing and statistics gathering. The WIS sub-layers can be bypassed for LAN applications.

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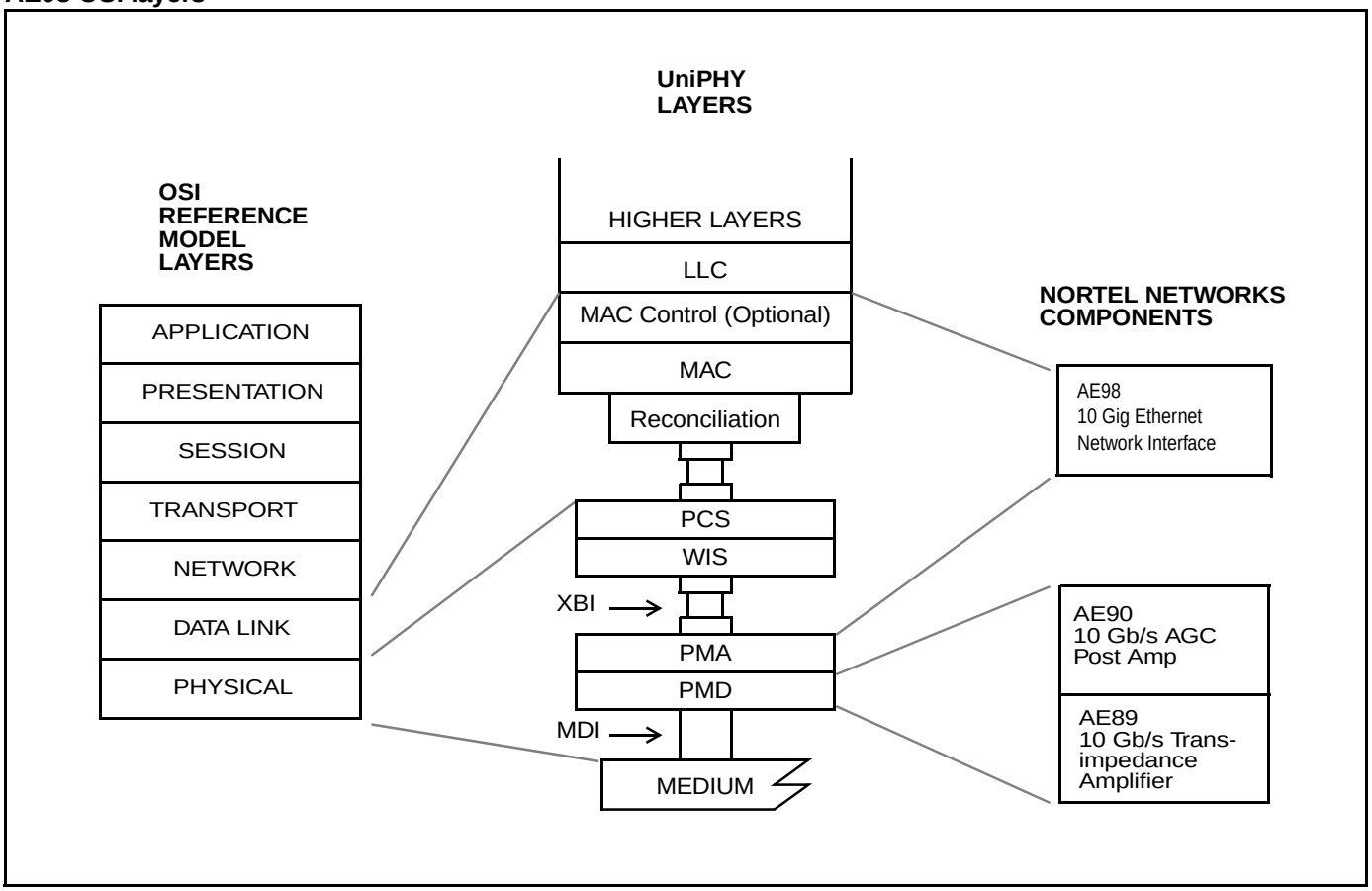
Typical Applications

The AE98 is intended for 10 Gb/s Ethernet port card applications on a switch router. It is designed to interface directly to a Network Processor Unit (NPU) Forwarder using the SPI-4 interface. Configuration and statistics monitoring on the AE98 is done through the low speed asynchronous peripheral bus.

AE98 OSI layers



Features

System Interface (SPI-4)

- System Packet Interface Level 4 (SPI-4) is an OIF group interface standard. (Also referred to as POS PHY Level 4).
- Standard 622/645 MHz 16 bit LVDS packet and cell interface for full duplex 10Gb/s data rates.
- Separate RX and TX flow control channels

Management Interface

- AE98 has a Intel/Motorola mode asychronous processor bus interface for configuration and monitoring.
- Control and status information is passed across the interface including selection of operating modes and line maintenance information.

Media Access Control (MAC)

- 32 kbyte buffer in transmit and 128 kbyte buffer in receive direction
- errored frame discard and statistics gathering
- TCP/UPD segment and IP packet checksum generation and checking with auto-recognition of all common Ethernet, TCP/UDP and IP types
- receive source and destination MAC address filtering
- generation and interpretation of Ethernet pause frames
- generation and removal of Ethernet preamble and start frame delimiter
- generation and removal of idle frames to manage inter-frame gap (IFG)
- padding generation (when required) and removal
- Ethernet frame check sequence (FCS) generation and checking
- simple “Quality of Service” algorithm for receive path frame discard, in the event of receive buffer overflow

Physical Coding Sub-layer (PCS)

- performs 64b/66b coding/decoding
- scrambles codeword data using $x^{58}+x^{19}+1$
- discovers codeword boundaries from incoming payload

WAN Interface Sub-layer (WIS)

- WIS frame (STS-192c/STM-64c compatible) section, line, and path overhead generation/termination, including B1, B2 and B3 BIP calculations/checking
- fixed transmit SPE pointer, arbitrary receive SPE pointer handling
- frame synchronization to A1/A2 bytes
- x^7+x^6+1 scrambling
- 64 bits @ 156/161 MHz to 16 bits @ 622/644 MHz conversion
- processor access to APS (K1/K2) overhead bytes
- support SDH STM-64 by use of “fixed stuff” in SPE

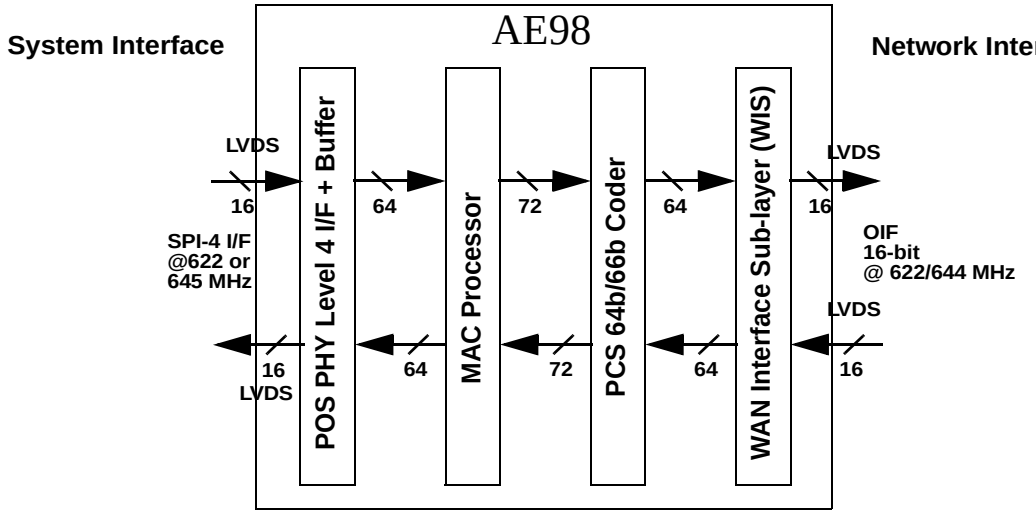
General

- loopback modes available at each layer for diagnostic purposes
- bypass of WIS layer for LAN application
- 622/644 MHz receive and transmit clock are only required clock sources for datapath
- general purpose interface for board control
- I^2C interface to retrieve MAC address from serial EEPROM

Pin Count

These are the functional pins required by the AE98:

- OIF transmit: 18 LVDS transmit pairs
- OIF receive: 17 LVDS receive pairs
- SPI-4: ~40 LVDS pins
- Management Interface: 16 data, 10 address? control?
- I^2C: 2 pins
- General Purpose I/O: 8 pins
- Debug Port: 17 pins
- Mode Interface: 2 pins
- JTAG: 6 pins



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For additional information on Nortel Networks products and services offered, please contact your local representative.

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