M-NARA

(AED30A)

ULTRA LOW POWER

MPEG LAYER3

AUDIO ENC/DECODER

PRELIMINARY DATA SHEET

VER1.2(2003.2.26)

MOBILE DOCTOR Co.

- INDEX -

1. GENERAL DESCRIPTION

M-NARA(AED30A) is a ultra low power digital audio encoder/decoder, capable of encoding/decoding ISO/IEC 11172-3 Layer III audio format. Fully hardwired design skill provides lower power consumption and cost than any other chip using DSP. Thus, M-NARA is ideally suited for portable electronics.

For user convenience, various interfaces are supported. Host data reading/writing is executed with the serial I2C I/F. With the serial I2S or 8bit PIO I/F, bit streams for encoding or decoding are transferred. The external AD/DA are interfaced with the I2S format.

Easily accessible host interface has various functions and controls, such as software reset, digital volume control, test mode, mute, interrupt, encoder/decoder status check, power down mode, ….

M-NARA has the capability of voice recoding/decoding with MPEG2 LAYER III algorithm(16kHz sampling freq. 8~32kbps mono). At that time, the external MCU doesn’t execute any operation. The voice signal from ADC is compressed and transmitted to external memory through I2S or parallel PIO interface.

For minimum power consumption, the external MCU can power down the encoder/decoder. In typical application, M-NARA is suitable for low power application in consumer digital audio system, multimedia and digital system.

2. FEATURES

- MPEG 1/2 Audio layer 3 encoder/decoder single chip
- Fully hardwired design for ultra low power and cost
- Various user interface (I2C, I2S, PIO)
- Host read/write access with I2C interface
- 16bits PCM data input/MP3 data output for encoder with I2C/I2S/PIO interface
- MP3 data input for decoder with I2C/I2S/PIO interface
- Internal PLL
- 12.288MHz single clock
- Need not program download
- Power down mode for reducing power consumption
- Power consumption – normal mode (encoder : 8mA, decoder : 6mA)
- 3.3/2.5V power supply
- 64 pin TQFP

2.1 Encoder Features

- Flexible encoding bit rate (MPEG1 : 32 ~ 320kbps, MPEG2 : 8 ~ 160kbps)
- Various audio source input (music, voice, radio, audio line-in, 16bit PCM data)
- Voice record/playback (16kHz sampling freq. 8~32kbps mono) function
- MPEG1 layer3 format
  - 32, 44.1, 48kHz 16-bit stereo ADC sampled data/16bits PCM data input
  - Flexible compression ratio(32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320kbps) stereo/joint-stereo/mono encoded data serial/parallel output
  - For music application
- MPEG2 layer3 format
  - 16, 22.05, 24kHz 16-bit stereo ADC sampled data/wave file data input
  - Flexible compression ratio(8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 144, 160kbps) stereo/joint-stereo/mono encoded data serial/parallel output
  - In case of 8Kbps case, only 16kHz mono encoding is possible.
  - For voice application(16kHz 8~32kbps mono encoding)

2.2 Decoder Features

- MPEG1/2 Layer3 bit stream decoder
- 8 steps tempo control
- Digital volume control
- Digital bass control
- Digital treble control
- Mute control
- Ancillary data support

2.3 Typical Applications

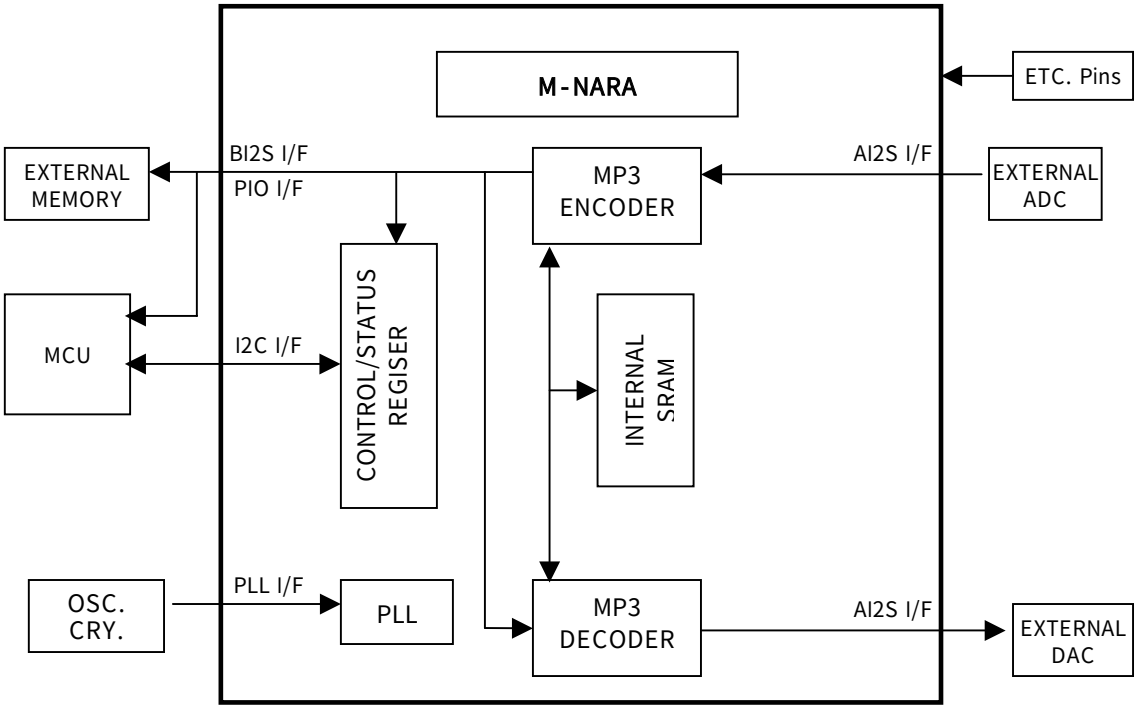
- Portable music player
- Voice recorder
- CD R/W recorder
- VoIP
- Sound card
- Digital audio/video recorder
- Mobile phone
- PDA
- Internet broadcasting system
- Notebook PC

3. FUNCTIONAL DESCRIPTION

3.1 Overview

M-NARA makes a low power operation on encoding/decoding with MP3 bitstream data. It has compactly-made hardwired core that can operate at low frequency. Due to that, power consumption is less than any other DSP encoder/decoder. With this architecture, there is no process to download the MP3 program.

3.2 Architecture



3.3 Internal PLL

The internal PLL is a low voltage, low cost, multi-clock generator. This can generate system clock and various tempo clocks such as ±5%, ±10%, ±15%, and ±20% offset against system clock. The input system clock is 12.288MHz.

3.4 External Audio Codec(ADC, DAC)

There is a I2S interface for the external AD/DA.

3.5 MPEG Codec/Arithmetic Logic/RAM

The MPEG codec is the MPEG1/2 layer3 encoder/decoder. The features of encoder/decoder are described at “2. FEATURES”.

3.6 DAC Mute

Host processor can control mute function.

3.7 Register Description

A standard I2C slave interface is implemented to control chip operation. With I2C I/F, it's possible to read from status registers, write to control registers, write 16bits PCM to encoder, write MP3 data to decoder and read MP3 output from encoder. With I2S/PIO interface, it's also possible to read/write PCM/MP3 data from/to encoder/decoder. All registers are composed of 8bit. The control registers are read/write and the status registers are read only.

3.7.1 Control Registers for ENC/DECODER

3.7.1.1 address 0x00 : interrupt masking, default 0xFF

- bit[7:5]: reserved
- bit[4] : decoder frame sync.
- bit[3] : encoder output buffer full, input buffer full
- bit[2] : encoder mute frame end
- bit[1] : encoder mute frame start
- bit[0] : encoder frame sync.

3.7.1.2 address 0x01 : interrupt enable MAX counter, default 0x01

- bit[7:0] : MAX counter

3.7.1.3 address 0x02 : software reset, default 0x00

- bit[7:5] : reserved
- bit[4] : enc/decoder core/register reset, auto cleared
- bit[3:2] : reserved
- bit[1] : encoder core reset, auto cleared
- bit[0] : decoder core reset, auto cleared

3.7.1.4 address 0x03 : External ADC control, default 0x10

- bit[7:5] : reserved
- bit[4] : external ADC output bypass to external DAC input enable
- bit[3:1] : reserved
- bit[0] : ADC input selection, 0=reserved, 1=external ADC input

3.7.1.5 address 0x04 : reserved

3.7.1.6 address 0x05 : External AD/DA control, default 0x10

- bit[7:6] : reserved
- bit[5] : external AD/DA channel polarity invert
- bit[4] : external AD/DA MSB justified
- bit[3:1] : reserved
- bit[0] : external AD/DA master clock enable

3.7.1.7 address 0x06 : reserved

3.7.1.8 address 0x07 : Internal PLL control (digital tempo control for decoder), default 0x0F

- bit[7:4] : reserved
- bit[3:0] : decoder fast/slow selection

Bit[3:0]	Decoder DAC Speed(%)
0000	-20
0001	-15
0010	-10
0011	-5
0100	+5
0101	+10
0110	+15
0111	+20
1XXX	0

3.7.1.9 address 0x08 : reserved

3.7.1.10 address 0x09 : reserved

3.7.1.11 address 0x0A : encoder control, default 0x00

- bit[7] : encoder power down
- bit[6:5] : reserved
- bit[4] : encoder enable, 1=start, 0=stop
- bit[3:0] : reserved

3.7.1.12 address 0x0B : decoder control, default 0x00

- bit[7] : decoder power down
- bit[6:5] : reserved
- bit[4] : decoder enable, 1=start, 0=stop
- bit[3:2] : reserved
- bit[1] : decoder pause
- bit[0] : decoder mute

3.7.1.13 address 0x0C : I2S bit stream IN/OUT control, default 0x00

- bit[7] : LSB first for output bit stream
- bit[6] : LSB first for input bit stream
- bit[5] : falling clock edge detection for output bit stream
- bit[4] : falling clock edge detection for input bit stream
- bit[3] : I2S encoder MP3 bit stream output enable
- bit[2] : I2S encoder 16bits PCM bit stream input enable
- bit[1] : reserved
- bit[0] : I2S decoder MP3 bit stream input enable

At 16bits PCM encoding mode(bit[2] = '1'), each bit[0] of register 0x04 and 0x05 must be set to '0'.

3.7.1.14 address 0x0D : PIO bit stream IN/OUT control, default 0x00

- bit[7:4] : reserved
- bit[3] : PIO encoder MP3 data output enable
- bit[2] : PIO encoder 16BITS PCM data input enable
- bit[1] : reserved
- bit[0] : PIO decoder MP3 data input enable

At 16bits PCM encoding mode(bit[2] = '1'), each bit[0] of register 0x04 and 0x05 must be set to '0'.

3.7.1.15 address 0x0E : reserved

3.7.2 Control Registers for ENCODER

3.7.2.1 address 0x10 : MPEG1/2 selection, default 0x01

- bit[7:1] : reserved
- bit[0] : MPEG1/2 selection, 1 = MPEG1 LAYER3, 0 = MPEG2 LAYER3

3.7.2.2 address 0x11 : MPEG2 mode, default 0xB2

- bit[7:6] : sampling frequency
- bit[5:4] : mode selection
- bit[3:0] : bit rate

At 8kbps case, only 16kHz mono encoding is possible.

Bit[7:6]	Sample freq.(kHz)	Bit[5:4]	mode	Bit[3:0]	Bit rate(kbps)
00	22.05	00	stereo	0000	reserved
01	24	01	joint-stereo	0001	8
10	16	10	reserved	0010	16
11	reserved	11	mono	0011	24
				0100	32
				0101	40
				0110	48
				0111	56
				1000	64
				1001	80
				1010	96
				1011	112
				1100	128
				1101	144
				1110	160
				1111	reserved

3.7.2.3 address 0x12 : MPEG1 mode, default 0x19

- bit[7:6] : sampling frequency
- bit[5:4] : mode selection
- bit[3:0] : bit rate

Bit[7:6]	Sample freq.(kHz)	Bit[5:4]	mode	Bit[3:0]	Bit rate(kbps)
00	44.1	00	stereo	0000	reserved
01	48	01	joint-stereo	0001	32
10	32	10	reserved	0010	40

11	reserved	11	mono	0011	48
				0100	56
				0101	64
				0110	80
				0111	96
				1000	112
				1001	128
				1010	160
				1011	192
				1100	224
				1101	256
				1110	320
				1111	reserved

3.7.2.4 address {0x14, 0x13} : low pass filter threshold data, default {0x02, 0x40}

- bit[7:2] : reserved @0x14
- bit[1:0] : high threshold data @0x14
- bit[7:0] : low threshold data @0x13

3.7.2.5 address {0x16, 0x15} : high pass filter threshold data, default {0x00, 0x00}

- bit[7:2] : reserved @0x16
- bit[1:0] : high threshold data @0x16
- bit[7:0] : low threshold data @0x15

3.7.2.6 address {0x19, 0x18, 0x17} : reserved

3.7.2.7 address 0x1A : PCM data input burst data number, default 0x20

- bit[7] : reserved
- bit[6:0] : burst data number

3.7.2.8 address 0x1B : MP3 data output burst data number, default 0x08

- bit[7:4] : reserved
- bit[3:0] : burst data number

3.7.2.9 address {0x1D, 0x1C} : PCM data write, default {0x00, 0x00}

- bit[7:0] : high data @0x1D
- bit[7:0] : low data @0x1C

3.7.2.10 address {0x1F, 0x1E} : reserved

3.7.3 Control Registers for DECODER

3.7.3.1 address 0x20 : MP3 data write, default 0x00

- bit[7:0] : MP3 data

3.7.3.2 address 0x21 : MP3 input burst data number, default 0x20

- bit[7:0] : MP3 input burst data number

3.7.3.8 address {0x25, 0x24, 0x23, 0x22} : digital volume, default {0x10, 0x7F, 0x7F, 0x10}

- bit[7:0] : digital volume RR @0x25
- bit[7:0] : digital volume RL @0x24
- bit[7:0] : digital volume LR @0x23
- bit[7:0] : digital volume LL @0x22

Bit[7]	sign	Bit[6:0]	Volume index(dB)
0	normal	00	16
1	Inverting	…	…
		10	0
		…	…
		7F	-111
		Y = -X + 16, X=bit[6:0], Y= dB	

3.7.3.4 address 0x26 : digital bass tone, default 0x00

- bit[7:5] : reserved
- bit[4:0] : digital bass tone index, Y = X – 16, X=bit[4:0], Y= dB

Bit[4:0]	Tone index(dB)
00	disable
01	-15
…	…
10	0
…	…
1F	15

3.7.3.5 address 0x27 : digital treble tone, default 0x00

- bit[7:5] : reserved
- bit[4:0] : digital treble tone index, Y = X – 16, X=bit[4:0], Y= dB

Bit[4:0]	Tone index(dB)
00	disable
01	-15
…	…
10	0
…	…
1F	15

3.7.3.6 address 0x28 : Pre scale control for bass/treble, default 0x00

- bit[7] : 0=auto, 1=manual
- bit[6:4] : reserved
- bit[3:0] : pre scale factor, Y = -X, X=bit[3:0], Y= dB

Bit[3:0]	pre scale factor (dB)
0	0
1	-1
…	…
F	-15

3.7.4 Status Registers for ENC/DECODER

3.7.4.1 address 0x30 : interrupt status, default 0x00

- bit[7:5] : reserved
- bit[4] : decoder frame sync., auto cleared
- bit[3] : encoder output buffer full, auto cleared
- bit[2] : encoder mute frame end, auto cleared
- bit[1] : encoder mute frame start, auto cleared
- bit[0] : encoder frame sync., auto cleared

3.7.4.2 address 0x31 : I2C I/F data input/output request, default 0xXX

- bit[7] : encoder MP3 data output request
- bit[6:5] : reserved
- bit[4] : encoder 16BITS PCM data input request
- bit[3:1] : reserved
- bit[0] : decoder MP3 data input request

3.7.4.3 address 0x32 : PIO I/F data input/output request, default 0xXX

- bit[7] : encoder MP3 data output request
- bit[6:5] : reserved
- bit[4] : encoder 16BITS PCM data input request
- bit[3:1] : reserved
- bit[0] : decoder MP3 data input request

3.7.5 Status Registers for ENCODER

3.7.5.1 address 0x40 : reserved, default 0xXX

- bit[7:0] : reserved

3.7.5.2 address 0x41 : Encoded MP3 data, default 0xXX

- bit[7:0] : MP3 data

3.7.5.3 address 0x42 : reserved, default 0xXX

- bit[7:0] : reserved

3.7.5.4 address {0x44, 0x43} : Mute frame counter, default {0xXX, 0xXX}

- bit[7:0] : high counter @0x44
- bit[7:0] : low counter @0x43

3.7.5.5 address {0x46, 0x45} : Frame counter, default {0xXX, 0xXX}

- bit[7:0] : high counter @0x46
- bit[7:0] : low counter @0x45

3.7.6 Status Registers for DECODER

3.7.6.1 address 0x50 : header information 1, default 0xXX

- bit[7] : reserved
- bit[6] : mpeg1/2, 0 = mpeg2, 1 = mpeg1
- bit[5:4] : layer, 0 = reserved, 1 = layer3, 2 = layer2, 3 = layer1
- bit[3] : protection
- bit[2] : sync. Error
- bit[1] : CRC error
- bit[0] : decoder error

3.7.6.2 address 0x51 : header information 2, default 0xXX

- bit[7:4] : bit rate index
- bit[3:2] : sampling freq
- bit[1] : padding
- bit[0] : private

Bit[7:4]	bit rate index(kbps)	Bit[3:2]	sampling freq(kHz)
0000	free format	00	44.1(MPEG1), 22.05(MPEG2)
0001	32(MPEG1), 8(MPEG2)	01	48.0(MPEG1), 24.00(MPEG2)
0010	40(MPEG1), 16(MPEG2)	10	32.0(MPEG1), 16.00(MPEG2)
0011	48(MPEG1), 24(MPEG2)	11	reserved
0100	56(MPEG1), 32(MPEG2)		
0101	64(MPEG1), 40(MPEG2)		
0110	80(MPEG1), 48(MPEG2)		
0111	96(MPEG1), 56(MPEG2)		
1000	112(MPEG1), 64(MPEG2)		
1001	128(MPEG1), 80(MPEG2)		
1010	160(MPEG1), 96(MPEG2)		
1011	192(MPEG1), 112(MPEG2)		
1100	224(MPEG1), 128(MPEG2)		
1101	256(MPEG1), 144(MPEG2)		
1110	320(MPEG1), 160(MPEG2)		
1111	reserved		

3.7.6.3 address 0x52 : header information 3, default 0xXX

- bit[7:6] : mode
- bit[5:4] : mode ext. : joint-stereo{intensity stereo on/off, m/s stereo on/off}
- bit[3] : copy
- bit[2] : original
- bit[1:0] : emphasis

Bit[7:6]	Mode	Bit[5:4]	mode ext.	Bit[1:0]	emphasis
00	Stereo	00	off, off	00	none
01	Joint-stereo	01	on, off	01	50/15uS
10	dual channel	10	off, on	10	reserved
11	single channel	11	on, on	11	CCITT J.17

3.7.6.4 address 0x53 : bit stream buffer counter, default 0xXX

- bit[7:0] : bit stream buffer counter

3.7.6.5 address {0x55, 0x54} : frame counter, default {0xXX, 0xXX}

- bit[7:0] : high counter @0x55
- bit[7:0] : low counter @0x54

3.7.6.6 address {0x57, 0x56} : CRC error counter, default {0xXX, 0xXX}

- bit[7:0] : high counter @0x57
- bit[7:0] : low counter @0x56

3.7.6.7 address {0x59, 0x58} : ancillary data counter, default {0xXX, 0xXX}

- bit[7:0] : high counter @0x59
- bit[7:0] : low counter @0x58

3.7.6.8 address 0x5A : ancillary data, default 0xXX

- bit[7:0] : ancillary data

4. EXTERNAL INTERFACE DESCRIPTION

4.1 Host Interface (I2C I/F)

Configuration setting and status information reading is done by standard I2C interface. With device address writing, this chip is selected. Next issue is command sequences. Consecutive data reading/writing can be done. Because I2C slave mode is used only, the clock port(I2CC) is used as input port. I/F ports(I2CC/I2CD) must be pull-up on external board.

4.1.1 Device Address Selection

Two input pins(I2CA2, I2CA1) are used to select I2C device address. Connect those pins either to VDD or to VSS. Bit[0] is for device read/write selection.'0' means writing and '1' means reading. See the following table for the proper device address selection.

I2C DEVICE ADDRESS							
A7	A6	A5	A4	A3	A2	A1	W/R
0	I2CA2	0	I2CA1	0	0	0	0/1

4.1.2 Read/Write Access

- write access

S	DEV_W	A	REG_ADD	A	DATA	A	P

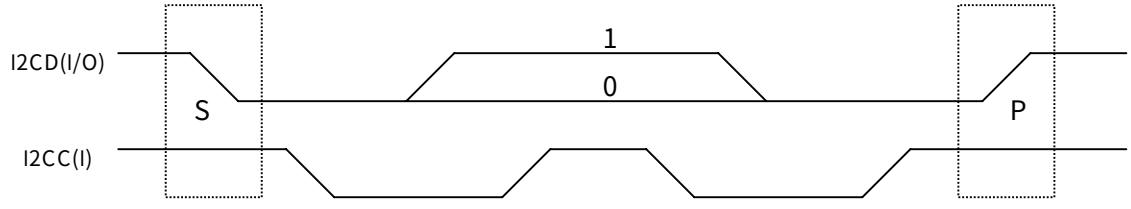
< bytes + ack.>

- read access

S	DEV_W	A	REG_ADD	A	S	DEV_R	A	DATA1	A	DATA2	N	P

< bytes + ack.>

- bus protocol



- ✓ S : START condition,
- ✓ P : STOP condition
- ✓ A : acknowledge(I2CD LOW)
- ✓ N : not acknowledge(I2CD HIGH)
- ✓ DEV_W : device address with bit[0]='0'
- ✓ DEV_R : device address with bit[0]='1'
- ✓ REG_ADD : register address to read/write
- ✓ DATA : data which master write to register
- ✓ DATA1, DATA2 : data which master read from register
- ✓ Black region : from master to slave
- ✓ White region : from slave to master
- ✓ In write access, data transfer number(bytes + ack.) >= 1
- ✓ In read access, data transfer number(bytes + ack.) >= 0

4.1.3 Control/Status Register Access

Register read/write is done with I2C read/write access process. Most of all register need one register read/write processing. If multi read processing is required like decoding ancillary data(register 0x5A), it is possible with data transfer number increasing in read access.

With I2C processing, following data transfer is possible, MP3 data writing(register 0x20) to decode, MP3 data reading(register 0x41) from encoder, 16bits PCM data writing(register {0x1D, 0x1C}) to encoder

4.2 1bit Serial Interface (BI2S I/F)

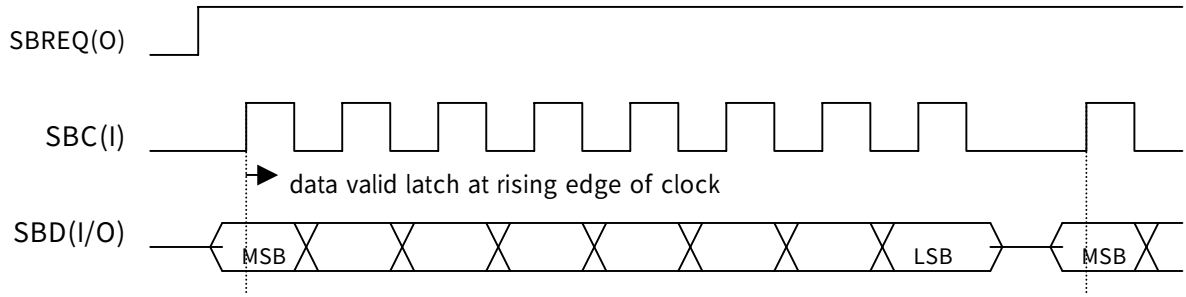
With I2S interface, 1bit serial bit stream(8bits encoder output/decoder input, 16bits encoder input) can be done. When internal buffer is empty at encoding/decoding, demand signal(SBREQ, SIBREQ) is asserted to '1'. Then data to encode/decode(SBD, SIBD) will be input/output with clock signal(SBC, SIBC). The serial data is accepted at rising clock edge(options). It is strongly recommended to hold the clock signal '0', if there is no input/output serial data. Three pins(SBC, SBD, SBREQ) are used at encoder output and decoder input mode, and 8bits MP3 data are used in this modes. Other pins(SIBC, SIBD, SIBREQ) are used at encoder input mode, this mode needs 16bits PCM input data.

4.2.1 Control Register Options

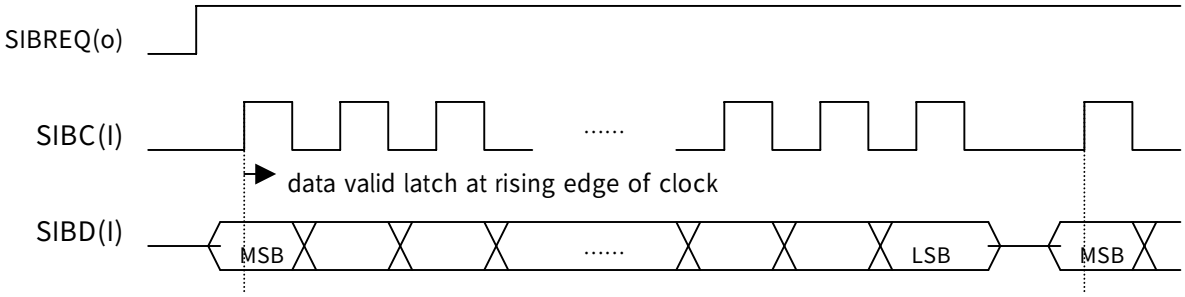
The serial I/F options are controlled by the I2S bit stream IN/OUT control register(0x0C). The bit[7] is for MSB/LSB first option of encoder output data, bit[6] for encoder/decoder input data. The bit[5] is for rising/falling clock edge option of encoder output data, bit[4] for encoder/decoder input data. The other bits(bit[3:0]) is for I2S interface selection.

4.2.2 Read/Write Access

- Encoder MP3 output(SBD output) / Decoder MP3 input(SBD input)



- Encoder 16bits PCM input



4.3 8bits Parallel Interface (PIO I/F)

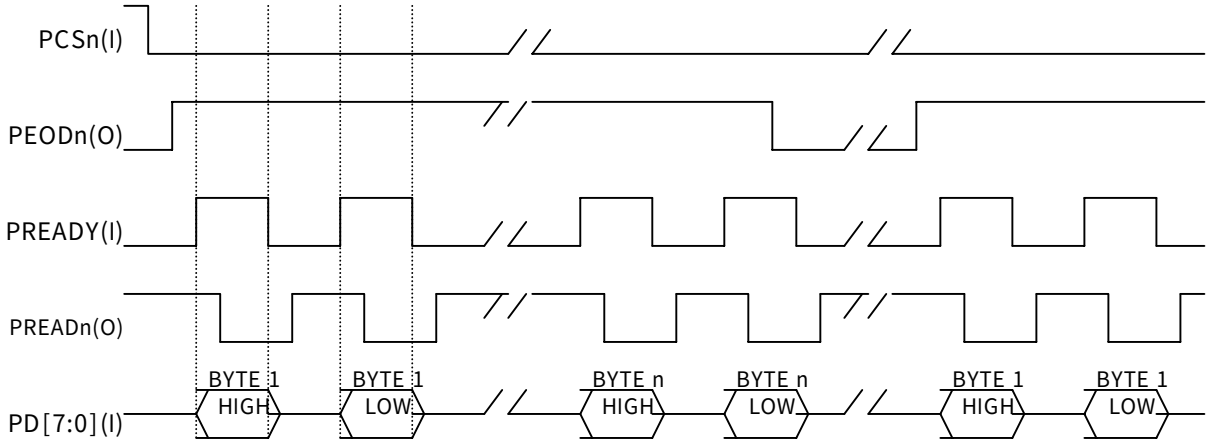
With PIO interface, 8bits parallel data transfer(8bits encoder output/decoder input, 16bits encoder input) can be done. This I/F consist of 8bits data pins(PD7, …, PD0) and the control pins(PCSn, PREADY, PEODn, PREADn, PWRITEn). When PEODn is '1', then it notices that available data output is ready or input buffer is empty. After verifying PEODn signal, the external MCPU sets PREADY signal to '1' when it is ready status of read/write. After that, PREADn/PWRITEn goes to '0' with data write/read. PREADY goes to '0' and PREADn/PWRITEn to '1'. The above procedure will be repeated until the data number register(0x1A, 0x1B, 0x21). After n byte read/write procedure, PEODn signal goes to '0'.

4.3.1 Control Register Options

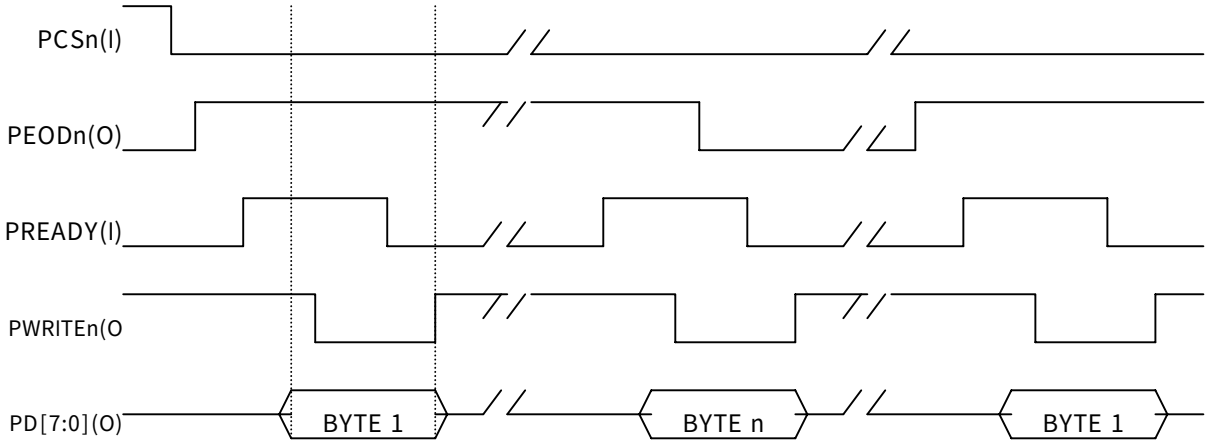
PIO I/F is controlled by the PIO bit stream IN/OUT control register(0x0D).

4.3.2 Read/Write Access

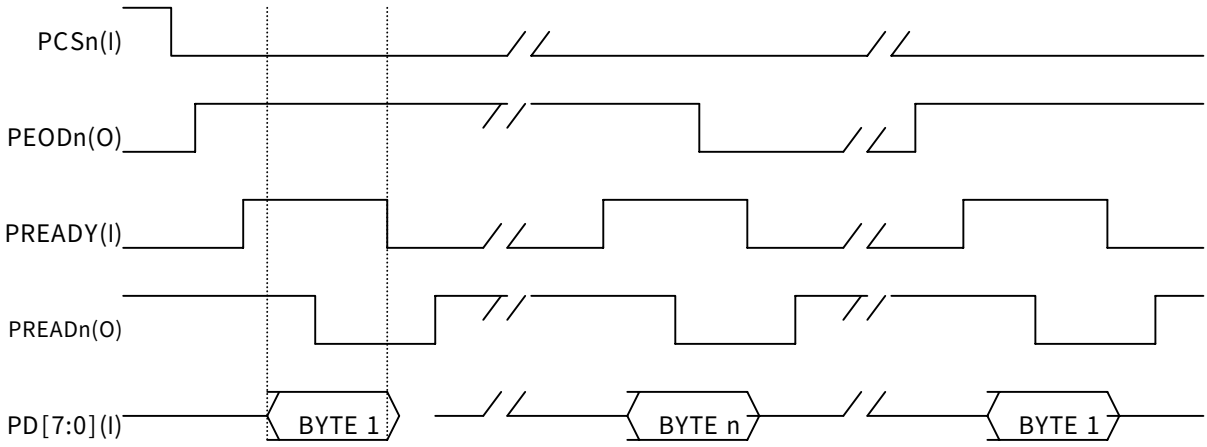
- Encoder 16bits PCM input



- Encoder MP3 output



- Decoder MP3 input



4.4 External Audio Codec Interface (AI2S I/F)

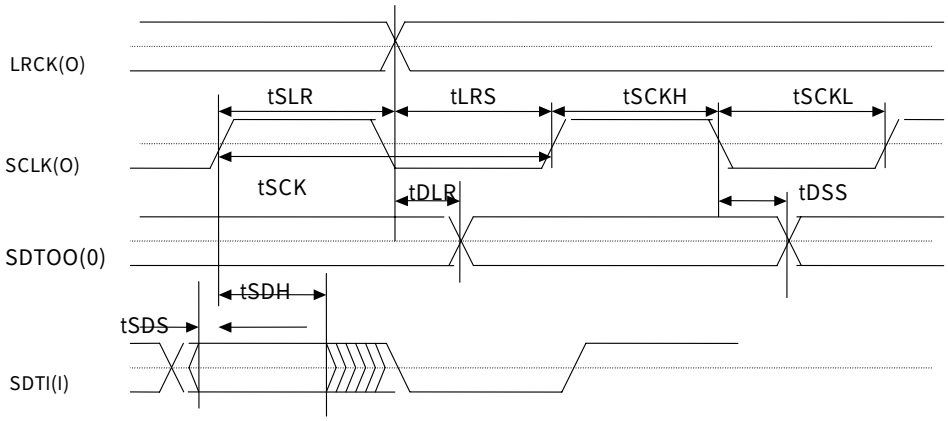
The data is 16-bit, MSB/LSB-first, 2's complement. The AD/DA master clock is controlled by the external AD/DA control register(address 0x05 bit[0]), the MSB/LSB justified mode by bit[4] and the channel polarity by bit[5]. The MCLK clock is 256fs and the SCLK clock is 32fs. *fs is sampling frequency. The LRCK and SCLK are synchronized with MCLK

The five pins(MCLK, SCLK, LRCK, SDTO, SDTI) are used for interface and there is no AD/DA power down interface pins..

4.4.1 Timing Characteristics

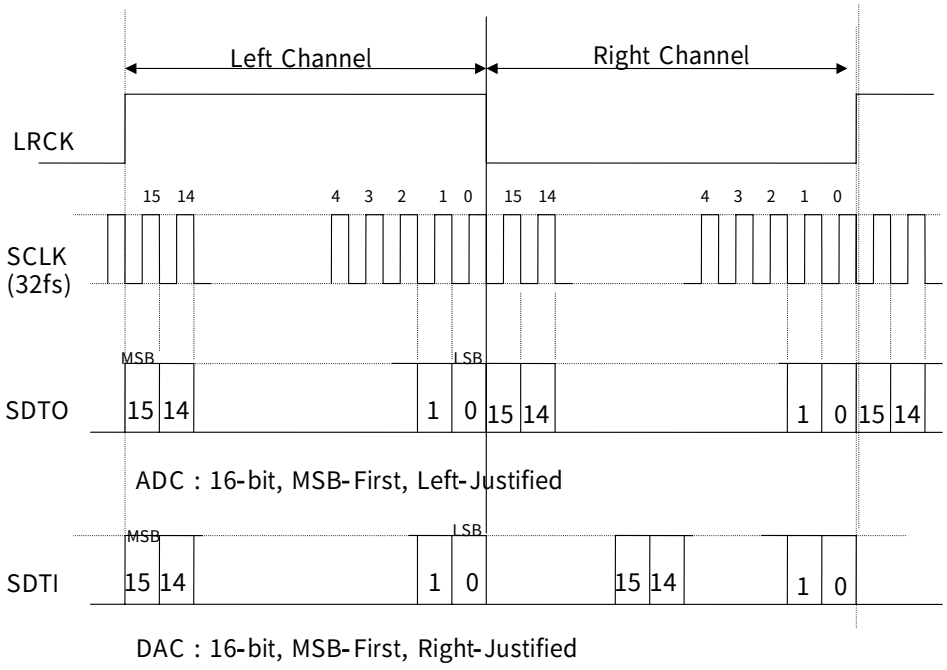
Parameter	Symbol	Min.	Typ.	Max.	Units
Master Clock 256fs	f_{CLK}	3.2768	11.2896	14.7456	MHz
LRCK Frequency fs	fs	12.8	44.1	57.6	kHz
Serial Interface Timing					
SCLK Period	t_{SCK}		8fs		256fs
SCLK Pulse Width Low	t_{SCKL}		4fs		256fs
Pulse Width High	t_{SCKH}		4fs		256fs
LRCK Edge to SCLK "rising"	t_{LRS}		4fs		256fs
SCLK "rising" to LRCK Edge	t_{SLR}		4fs		256fs
LRCK Edge to SDTO(MSB)	t_{DLR}	1fs			256fs
SCLK "falling" to SDTO	t_{DSS}			1fs	256fs
SDTI Hold Time	t_{SDH}	1fs			256fs
SDTI Setup Time	t_{SDS}	1fs			256fs

4.4.2 Timing Diagram



4.4.3 Interface format

The following format is MSB justified one. If bit numbers(15-14,~,4-3-2-1-0) are changed to “0-15,~,5-4-3-2-1”, it is LSB justified format.



4.5 PLL Interface

The CLKI input pin is for the crystal/osc. system clock. The inverted clock feeds back from CLKO output pin for crystal usage. With EXTCLK(PLLBYPASS) input pin to '1', it is possible to use direct external input clock through CLKI pin. The IREF analog input pin is for bias current input and it is set with BSEL input pin. For charge pump output, LF output pin is used. External capacitor should be connected between this pin and analog ground.

4.6 Interrupt Interface

The output pin(IRQn) is used for a interrupt request. This pin is active '0' and the duration of '0' state is controlled by interrupt MAX counter register(address 0x01). The counter number is the system clock number. See the interrupt status register(address 0x30). The interrupt request can be masked by the interrupt masking register(address 0x00).

4.7 Power Down/Reset Interface

There are 5 powers down mode. The PLL clock disable mode : This mode can be made when PWDNn pin is '0' and then all logic doesn't operate. MP3 en/decoder power down mode : with setting bit7 of register 0x0a/0x0b to high, it is power on mode(low) at power up initial.

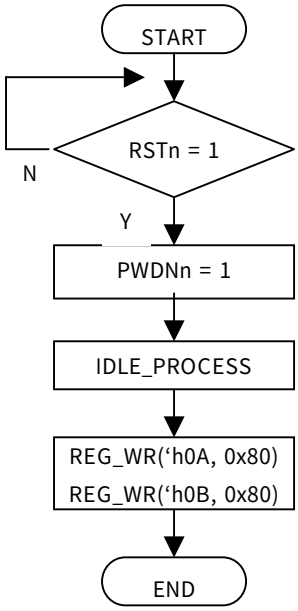
For normal mode, PWDNn signal must be inactive('1'). The RSTn input pin is for chip power reset. If it is '0', all logic of chip goes to initial state.

4.8 Power/Ground

- VDD0~3 : core power, 2.5V
- VSS0~3 : core ground
- VDDD0 : PLL digital power, 2.5V
- VSSD0 : PLL digital ground
- VDDA0~1 : PLL analog power, 2.5V
- VSSA0~1 : PLL analog ground
- VDDX0~2 : External I/O PAD power, 3.3V
- VSSX0~2 : External I/O PAD ground

5. FLOWCHART FOR SOFTWARE APPLICATIONS

5.1 Power Up Initial



// power switch on

// power reset release check : RSTn(pin 56) = 'high'

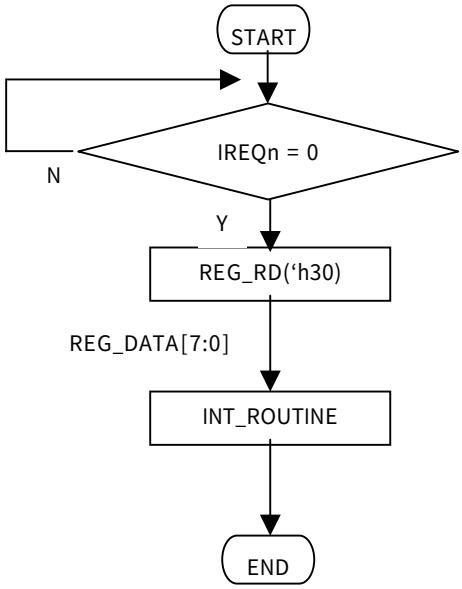
// chip power down release : PWDNn(pin 64) = 'high'

// idle processing for PLL stabilization : about 1mS

// encoder core power down, default power on
// decoder core power down, default power on

// go to next routine : encoding, decoding,….

5.2 Interrupt Routine



// interrupt routine start

// interrupt check : IRQn(pin 53) = 'low'

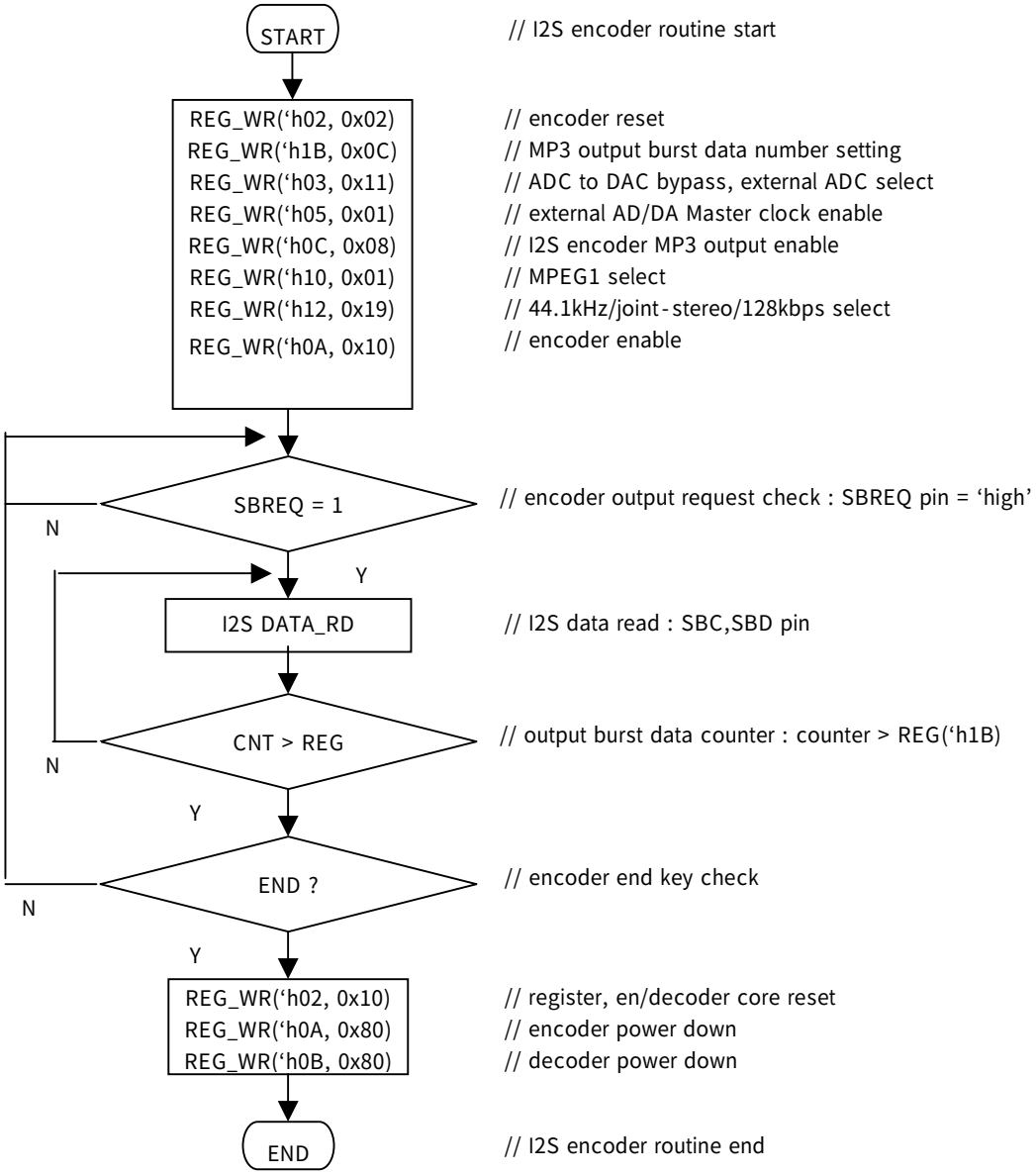
// interrupt status read

// REG_DATA(0x10) : decoder frame sync. routine
// REG_DATA(0x08) : encoder output buffer full routine
// REG_DATA(0x04) : encoder mute frame end routine
// REG_DATA(0x02) : encoder mute frame start routine
// REG_DATA(0x01) : encoder frame sync. routine

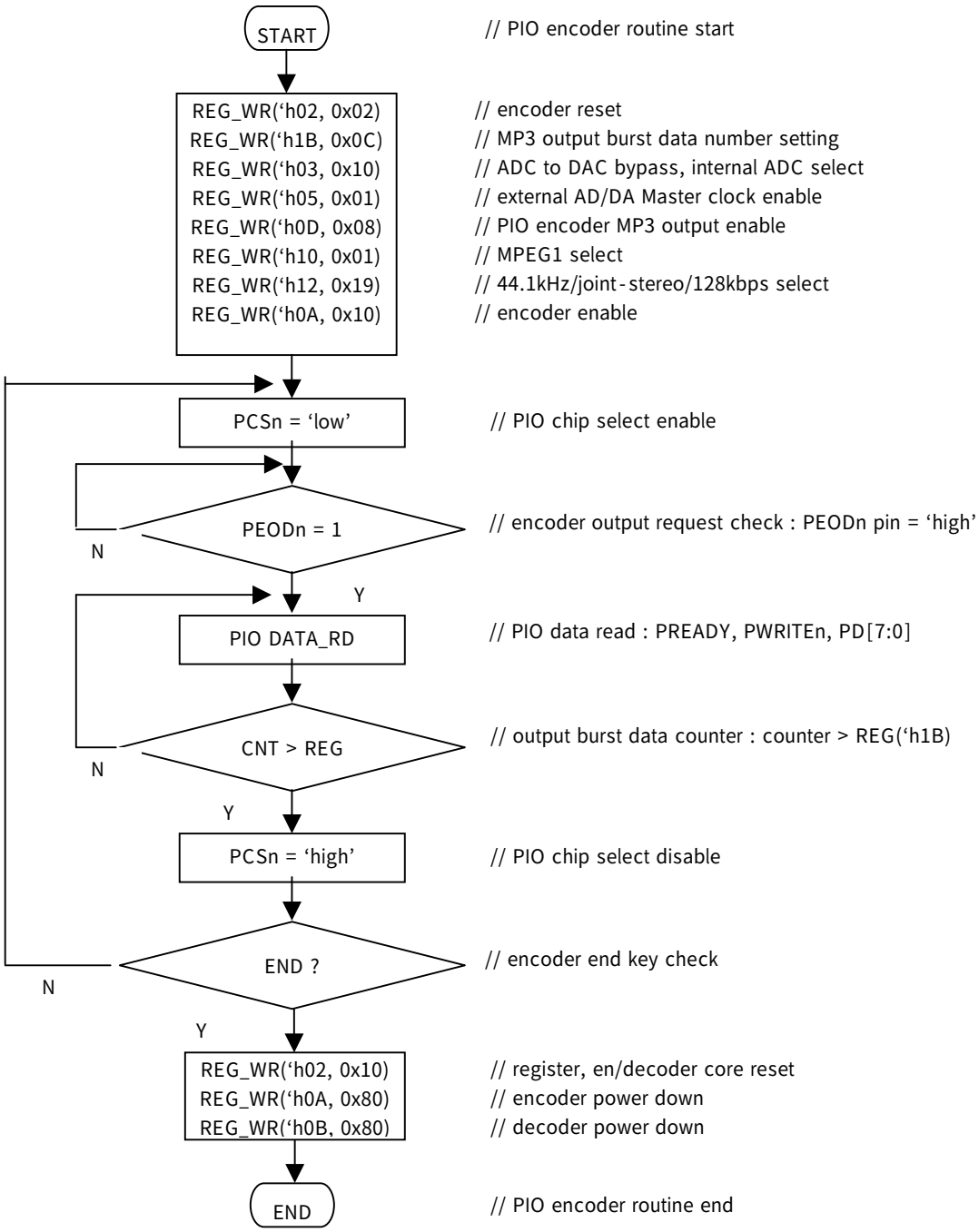
// interrupt routine end

5.3 MP3 Encoding With External Audio ADC Input

5.3.1 MP3 Encoding With External Audio ADC Input : with BI2S I/F

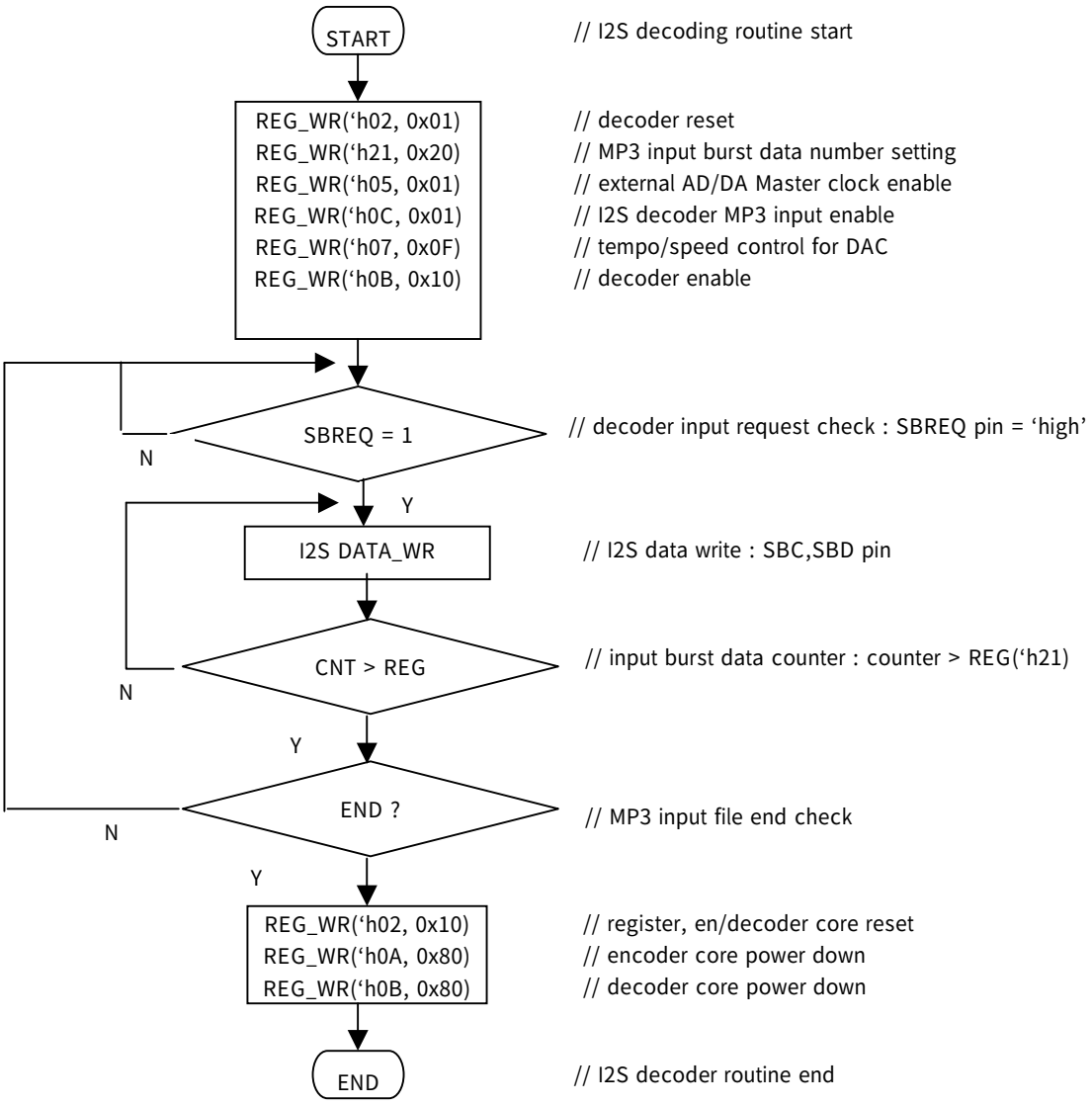


5.3.2 MP3 Encoding With External Audio ADC Input : with PIO I/F

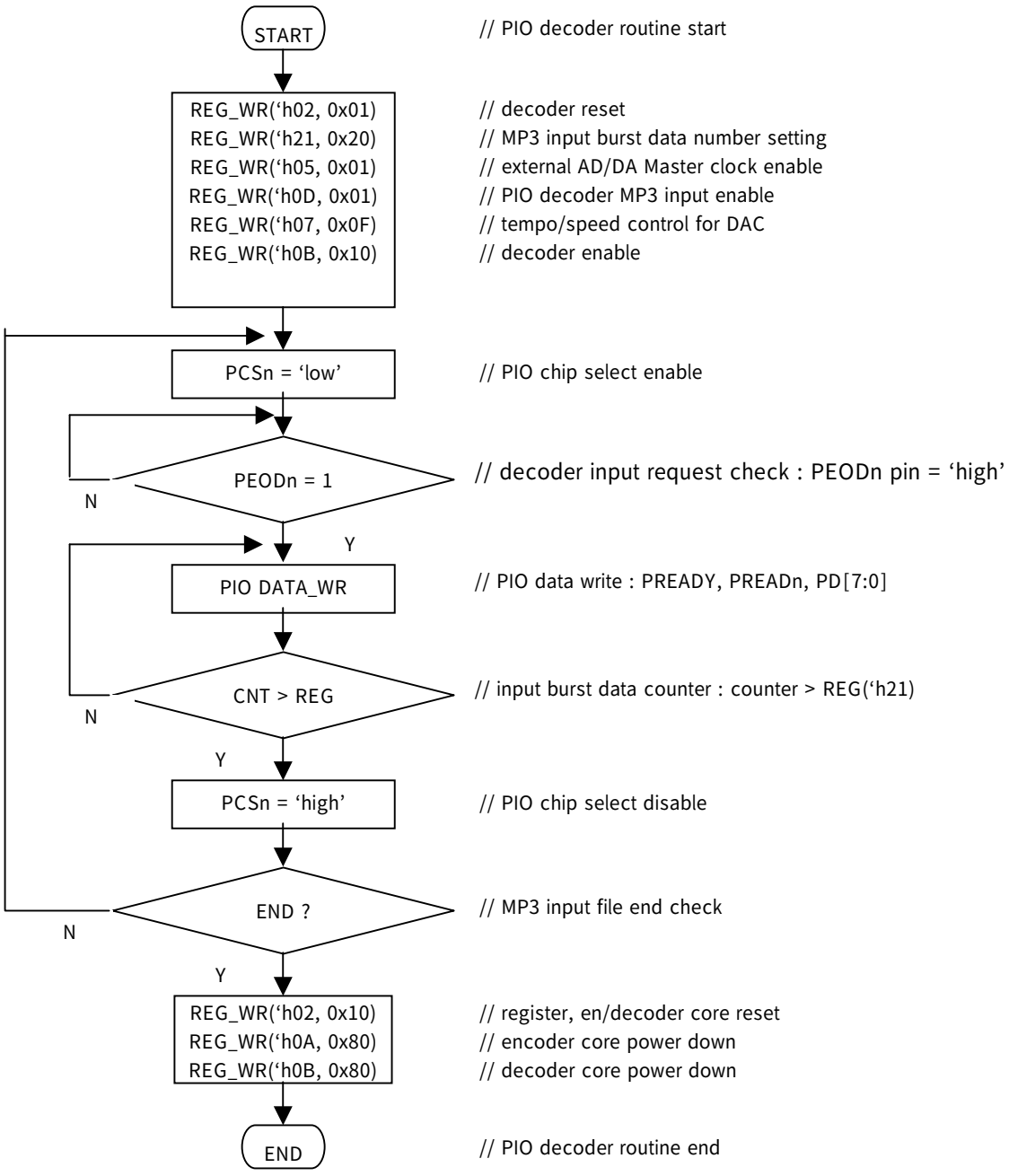


5.4 MP3 Decoding With External Audio DAC Output

5.4.1 MP3 Decoding With External Audio DAC Output : with BI2S I/F

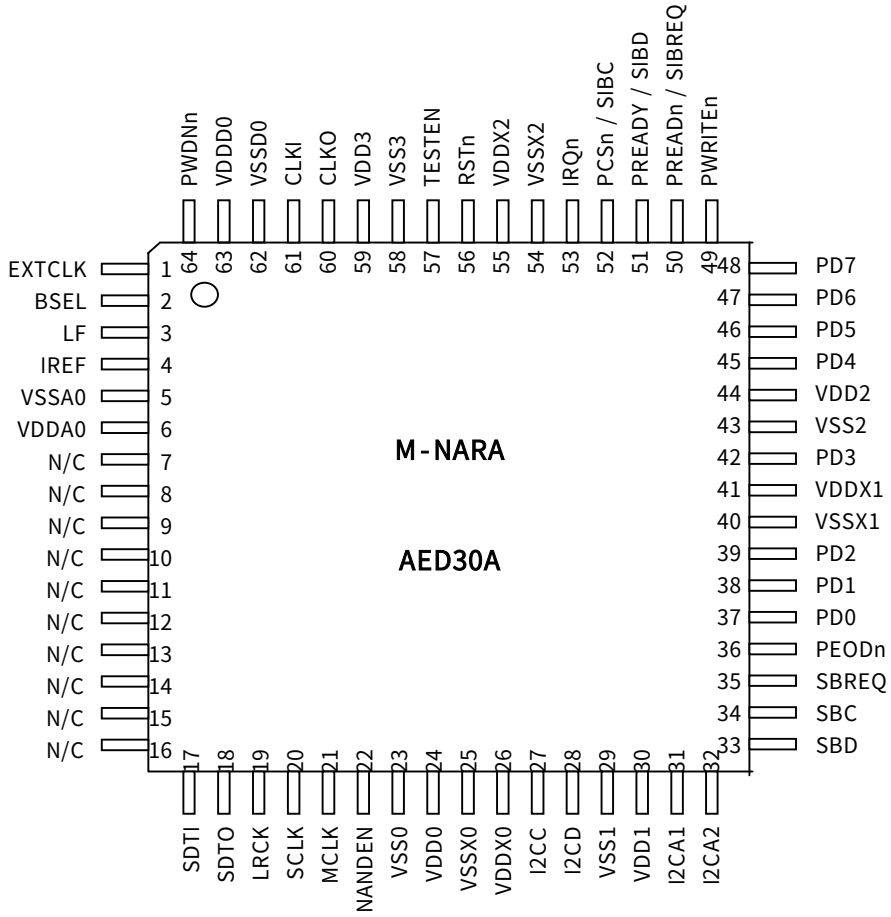


5.4.2 MP3 Decoding With External Audio DAC Output : with PIO I/F



6. PIN CONNECTIONS

6.1 Pin Configurations(Top View)



6.2 Pin Description

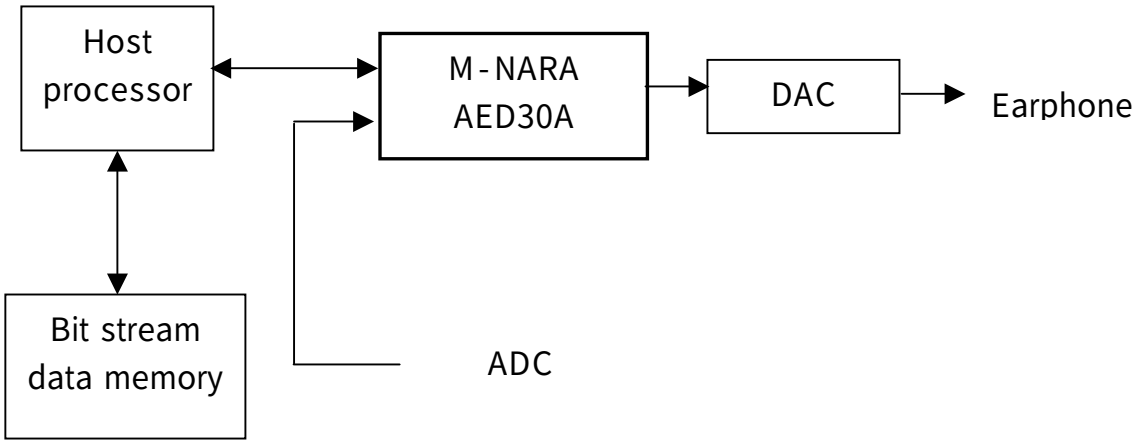
The pin names with small letter 'n' means active low signal(like as pin64 PWDNn).

PIN NO	PIN NAME	I/O	FUNCTION
1	EXTCLK	I	External clock select
2	BSEL	I	PLL IREF input enable
3	LF	O	PLL charge pump output(ANALOG PAD)
4	IREF	I	PLL bias current input(ANALOG PAD)
5	VSSA0	-	PLL analog VSS(2.5V)
6	VDDA0	-	PLL analog VDD(2.5V)
7	N/C	-	reserved
8	N/C	-	reserved
9	N/C	-	reserved
10	N/C	-	reserved
11	N/C	-	reserved
12	N/C	-	reserved
13	N/C	-	reserved
14	N/C	-	reserved
15	N/C	-	reserved
16	N/C	-	reserved
17	SDTI	I	External ADC serial data input
18	SDTO	O	External DAC serial data output
19	LRCK	I/O	External AD/DA channel clock output
20	SCLK	I/O	External AD/DA sampling clock output
21	MCLK	I/O	External AD/DA master clock output
22	NANDEN	I	Short to GND
23	VSS0	-	Digital core VSS(2.5V)
24	VDD0	-	Digital core VDD(2.5V)
25	VSSX0	-	Digital pad VSS(3.3V)
26	VDDX0	-	Digital pad VDD(3.3V)
27	I2CC	I	I2C clock(needs a external PULL-UP)
28	I2CD	I/O	I2C data(needs a external PULL-UP)
29	VSS1	-	Digital core VSS(2.5V)
30	VDD1	-	Digital core VDD(2.5V)
31	I2CA1	I	I2C device address selection 1 input(address bit4)
32	I2CA2	I	I2C device address selection 2 input(address bit6)

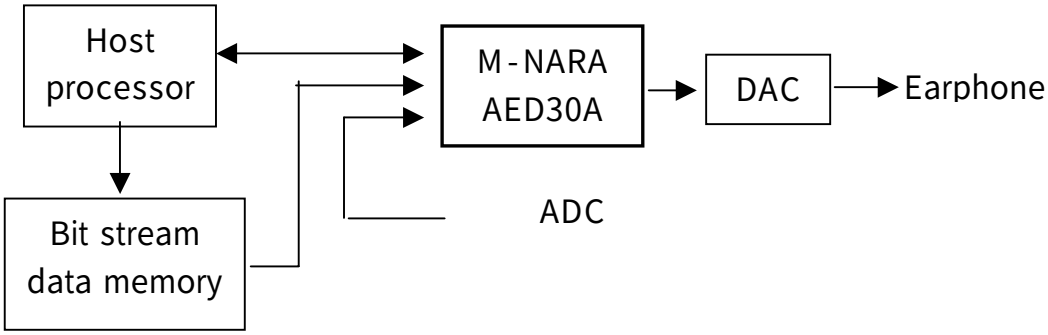
33	SBD	I/O	I2S bit stream data in/output(encoding output, decoding input)
34	SBC	I	I2S bit stream clock input(encoding output, decoding input)
35	SBREQ	O	I2S bit stream request output(encoding output, decoding input)
36	PEODn	O	PIO data end of DMA output
37	PD0	I/O	PIO data bit 0 in/output
38	PD1	I/O	PIO data bit 1 in/output
39	PD2	I/O	PIO data bit 2 in/output
40	VSSX1	-	Digital pad VSS(3.3V)
41	VDDX1	-	Digital pad VDD(3.3V)
42	PD3	I/O	PIO data bit 3 in/output
43	VSS2	-	Digital core VSS(2.5V)
44	VDD2	-	Digital core VDD(2.5V)
45	PD4	I/O	PIO data bit 4 in/output
46	PD5	I/O	PIO data bit 5 in/output
47	PD6	I/O	PIO data bit 6 in/output
48	PD7	I/O	PIO data bit 7 in/output
49	PWRITEn	O	PIO data write enable output
50	PREADn / SIBREQ	O	PIO data read enable output I2S bit stream request output(encoding input)
51	PREADY / SIBD	I	PIO ready to send/receive input I2S bit stream data input(encoding input)
52	PCSn / SIBC	I	PIO chip select input I2S bit stream clock input(encoding input)
53	IRQn	O	Chip interrupt output
54	VSSX2	-	Digital pad VSS(3.3V)
55	VDDX2	-	Digital pad VDD(3.3V)
56	RSTn	I	Power reset
57	TESTEN	I	Short to GND
58	VSS3	-	Digital core VSS(2.5V)
59	VDD3	-	Digital core VDD(2.5V)
60	CLKO	O	Crystal clock output
61	CLKI	I	Crystal clock input, osc. Clock input
62	VSSD0	-	PLL digital VSS
63	VDDD0	-	PLL digital VDD(2.5V)
64	PWDNn	I	Chip power down select

7. APPLICATION NOTE

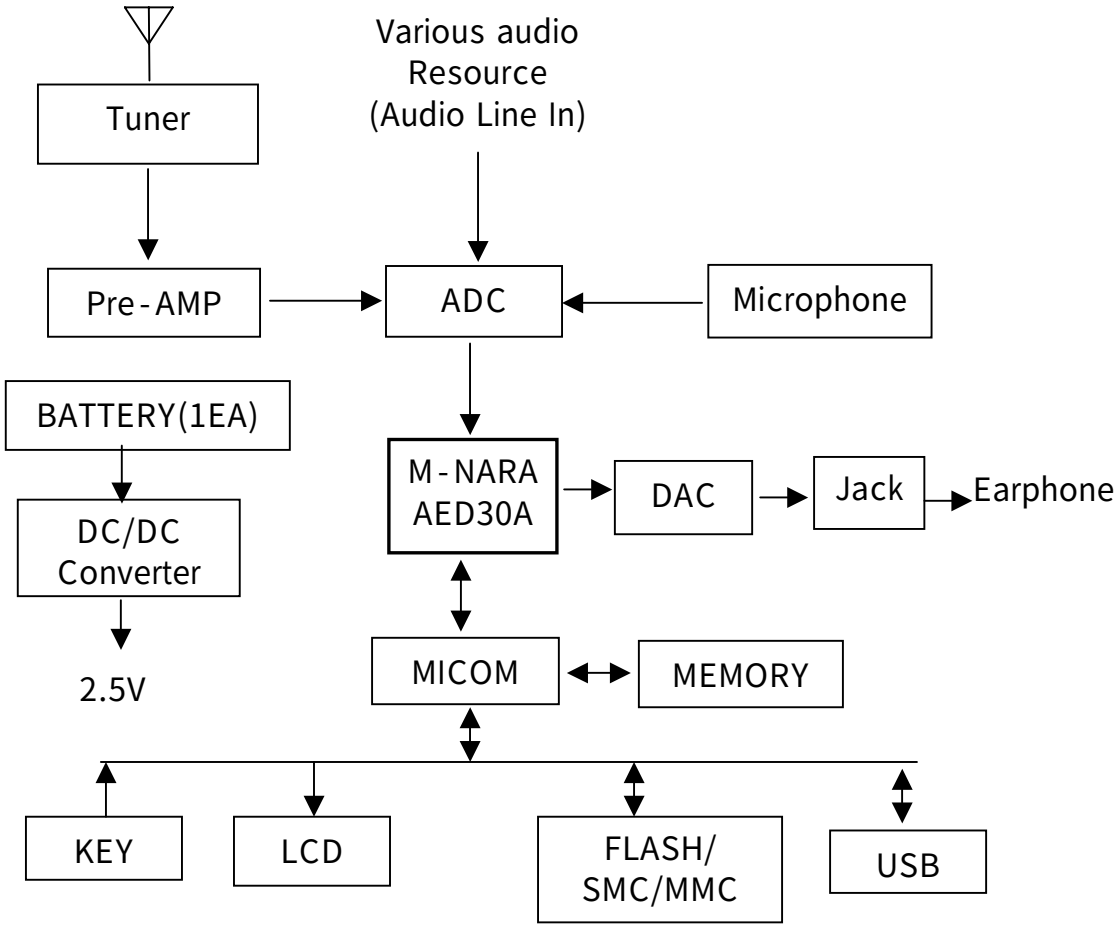
7.1 Indirect bit stream feeding



7.2 Direct bit stream feeding

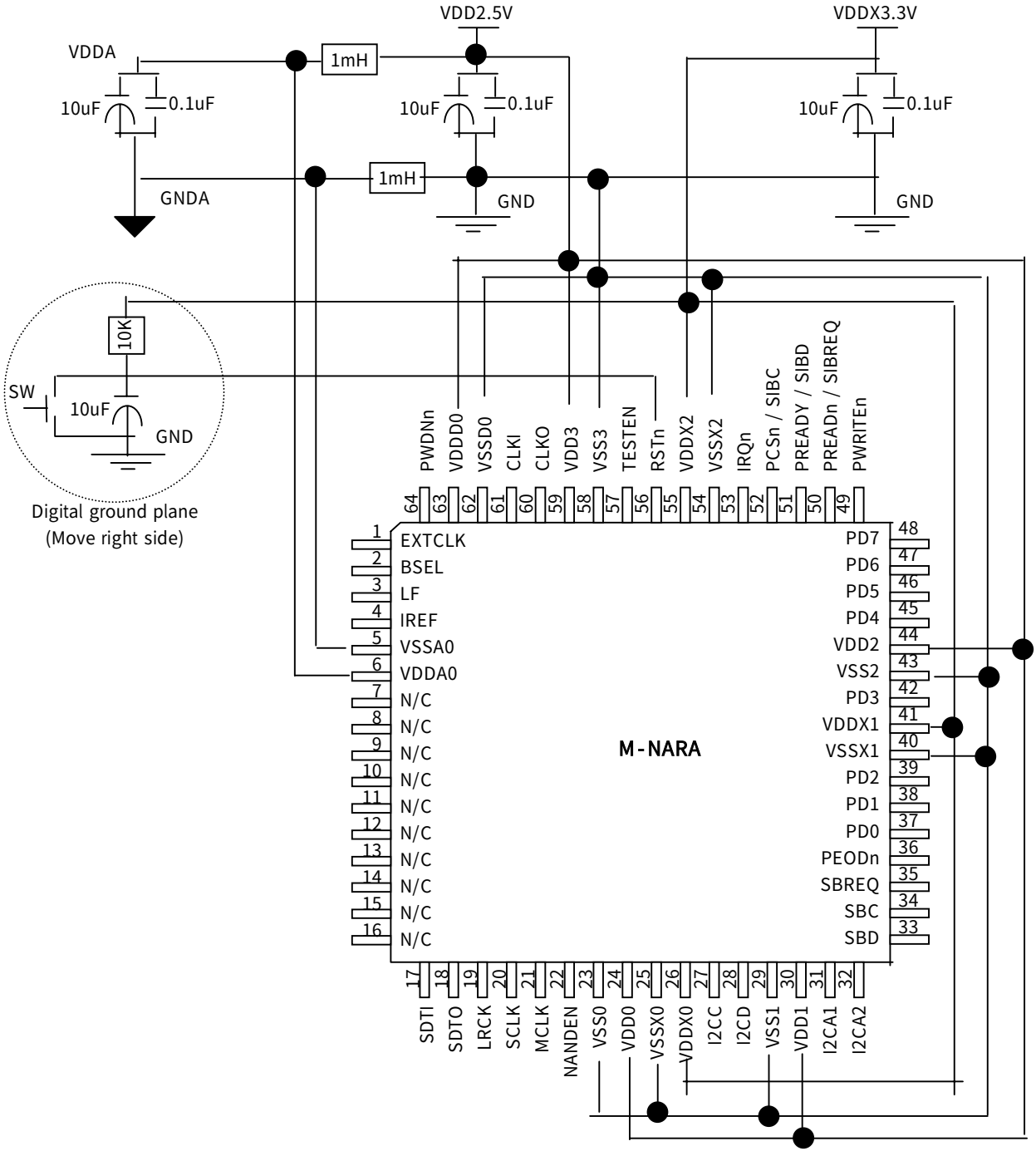


7.3 Radio Antenna



7.4 Power Connection Circuit

There are two power supplies(2.5V, 3.3V). VDD*(digital core), VDDD0(PLL digital) are supplied by VDD2.5V and the VDDX3.3V supplies to VDDX*(I/O pin power). The VDD2.5V is filtered by inductors and supplies to analog powers such as VDDA0(PLL analog). Also, the GND is filtered. VDDX3.3V can be replaced with VDD2.5V.



7.5 Application Circuit (Encoing/Decoding mode)

The uC/External Memory/External AD/DA are powered by VDDX*. Connect power/ground shown at “7.4 power connection circuit”.