Puma AEL2005

10 Gbps SFP+ Transceiver With Integrated EDC

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No	Date	Page Number	Old Rev	New Rev	Description
1	Nov. 9, 2007	8	1.0	1.1	Changed the LOSthresh and LOSthreshhyst fields to 6 bits.
2	Nov. 9, 2007	17	1.0	1.1	Formatting of tables 4, 5, and 6.
3	Nov. 9, 2007	14	1.0	1.1	Updated text in Section 6, SGMII Mode.
4	Nov. 9, 2007	77	1.0	1.1	Modified contents of LOS Mask register.
5	Nov. 9, 2007	81	1.0	1.1	Added Table 106, SGMII Configuration register.
6	Nov. 9, 2007	109	1.0	1.1	Reorganized Section 10, Mechanical Specifications
7	Nov. 9, 2007	112	1.0	1.1	Updated Figure 60, AEL2005 package pinout.
8	Nov. 9, 2007	---	1.0	1.1	Removed references to ‘un-retimed paths’ throughout document.
9	Dec. 18, 2007	15	1.1	1.2	Added Section 7, On-Chip Micro-Controller.
10	Dec 18, 2007	99, 100	1.1	1.2	Fixed typo - changed 2.5V to 3.3 V in power sequence diagram
11	Dec 18, 2007	51, 52	1.1	1.2	Added register 1.C04A, 1.C04B, 1.CA00, 1.CA12, 1.CA13, 1.CA1C, 1.CA1E to Section 15

1 Introduction

The Puma AEL2005 is a bidirectional single-channel 10 Gigabit Ethernet/10 Fibre Channel transceiver containing integrated EDC (Electronic Dispersion Compensation) circuits targeted for 10GBASE-LRM optical modules and 10Gbps SFP+ applications. The device also has a special SGMII mode which allows 1Gbps operation with SFP modules. The AEL2005 device offers an advanced combination of high performance and low power consumption. The consolidation of the receiver and transmitter physical layer (PHY) functions on a single chip is combined with the integration of an EDC block, integrated clock drivers, multiple loopback and PRBS for both the line side and the system side.

The high speeds and high integration of Puma make it the optimal choice for the SerDes device in XAUI-based transceiver designs. A flexible on-chip clock synthesis capability enables operation from a standard 156.25 MHz or 159.275 MHz crystal oscillator, or from a low-cost 50 MHz LVPECL or CMOS clock source. The CML serial interface supports a data rate of 10.3125 Gbps for datacom applications and 10.51875 for storage applications.

The Puma AEL2005 device is compliant with the following industry specifications:

- IEEE 802.3ae 10 Gigabit Ethernet
- IEEE 802.3aq 10 GBASE-LRM
- INCITS T11 10 Gigabit Fibre Channel
- XENPAK MSA, Revision 3.0
- X2 MSA, Revision 1.0b
- XPAK MSA, Revision 2.3
- SFP+ MSA, Draft Revision 2.2

2 Features and Benefits

Table 1. Puma AEL2005 Features and Benefits

Feature	Benefit
Minimal power consumption	Enables increased port density and less cooling
Integrated EDC	Allows operation with linear SFP+ modules
Advanced clock synthesis capability	Low-cost 50 MHz crystal oscillator support
1.2V and 3.3V power supplies	Dissipates very low power
On-chip clock generation and data recovery	Simplifies system clocking
Programmable bit and lane ordering	Eases board layout
Programmable 10 Gbps rise time control	Enhances data eye & power consumption
XAUI adjustable transmit pre-emphasis	Enables transmission across extended distances
XAUI receive equalization	Enables transmission across extended distances
3-tap 10Gbps transmit pre-emphasis	Enables extended reach to SFP+ module
Support for XENPAK DOM register set	Augments monitoring capabilities
Special SGMII mode	Allows operation with 1Gbps SFP modules
Multiple loopback features	Improves testability
PRBS, IEEE and packet-based test pattern generation	Improves testability
MDIO interface for device control and configuration	Industry standard
SDA/SCL interface for EEPROM communication	Industry standard
Traffic indicator LEDs	Improves testability and monitorability
Direct byte-by-byte SDA/SCL bus control	Enables design flexibility
10x10 mm QFN Package with 0.5mm pad pitch	Consumes minimal board space
15x15 mm BGA Package with 1.0mm pad pitch	Works with most PCB manufacturing processes
0.13 µm CMOS process	Enhanced power, cost, and integration

3 Applications

The Puma AEL2005 is ideal for use in high-speed 10 Gbps multi-mode fiber applications and either resides inside a XAUI module or on the linecard for SFP+ applications. For applications not requiring an integrated EDC, the AEL1002 device will provide an effective solution, while LAN/WAN applications can be addressed by the AEL1005 device.

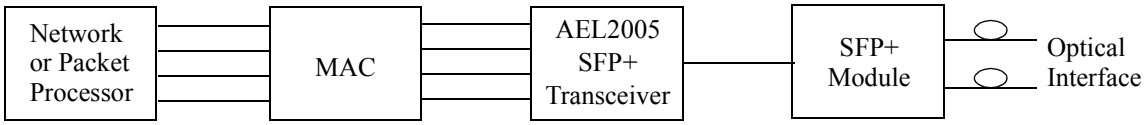


Figure 1. Puma AEL2005 with SFP+ Module

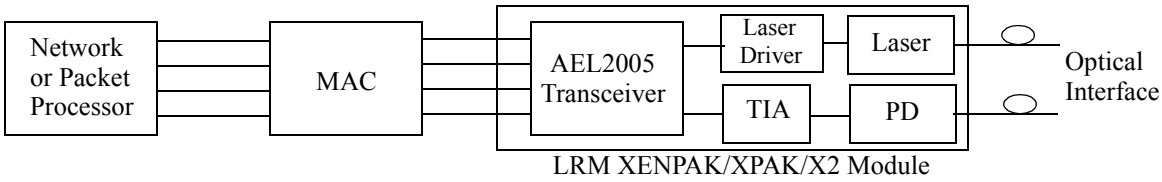


Figure 2. Puma AEL2005 Inside the Optical Module

4 Functional Description

A top-level view of the AEL2005 transceiver is shown in Figure 3, outlining the general interfaces of the device. The high-speed data path, including the 10 Gbps interface to the optical device and the XAUI MAC interface, are shown at the top of the drawing above the dotted line. The clocking, control, and configuration interfaces are shown below the dotted line. Additional details regarding each pin are available in Section 14.

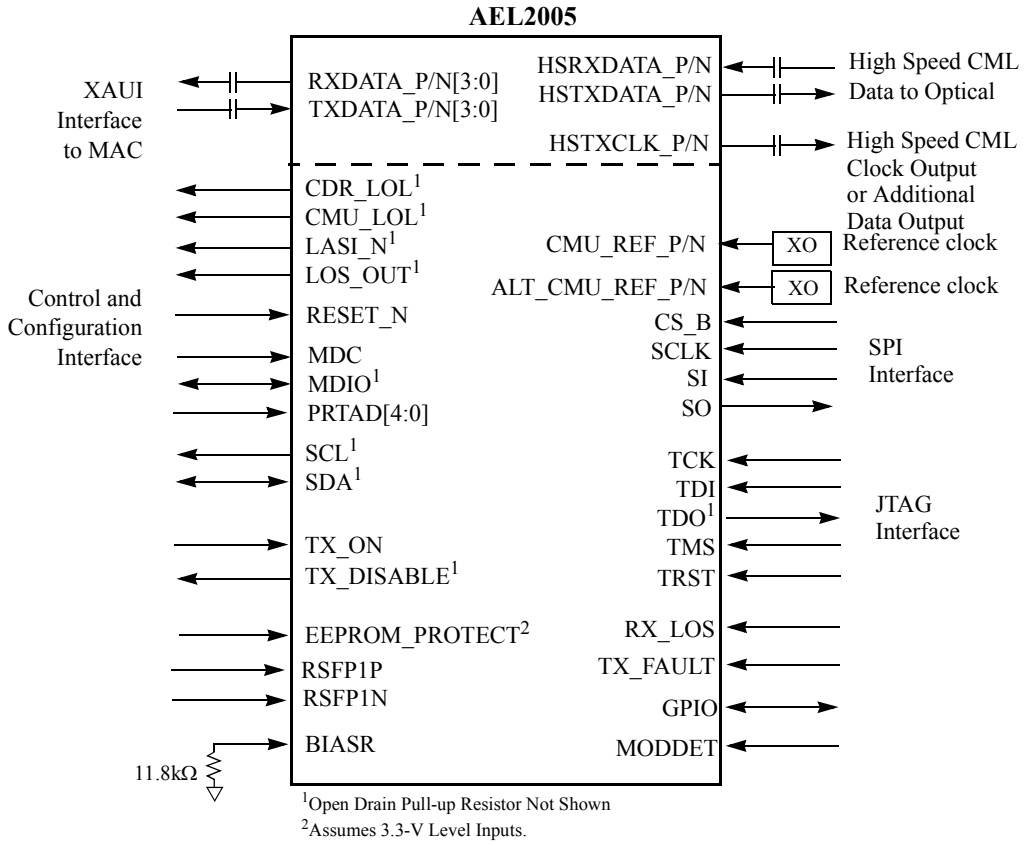


Figure 3. AEL2005 Transceiver Interfaces

An overall block diagram of the AEL2005 is shown in Figure 4. The Parallel-to-Serial path includes four 3.125 Gbps receivers, decode/alignment logic, a FIFO, an output encoder, and a 10 Gbps transmitter/clock driver. The Serial-to-Parallel path contains an EDC block, 10 Gbps receiver, decode logic, a FIFO, parallel output encoding logic, and four 3.125 Gbps transmitters. The AEL2005 also contains a management data I/O (MDIO) interface for device control and configuration, an SDA/SCL interface for EEPROM communication, (SPI interface) and loopback modes for the parallel and serial interfaces. A variety of loopback paths are also available and described in more detail in Section 10. The following subsections describe each block in Figure 4.

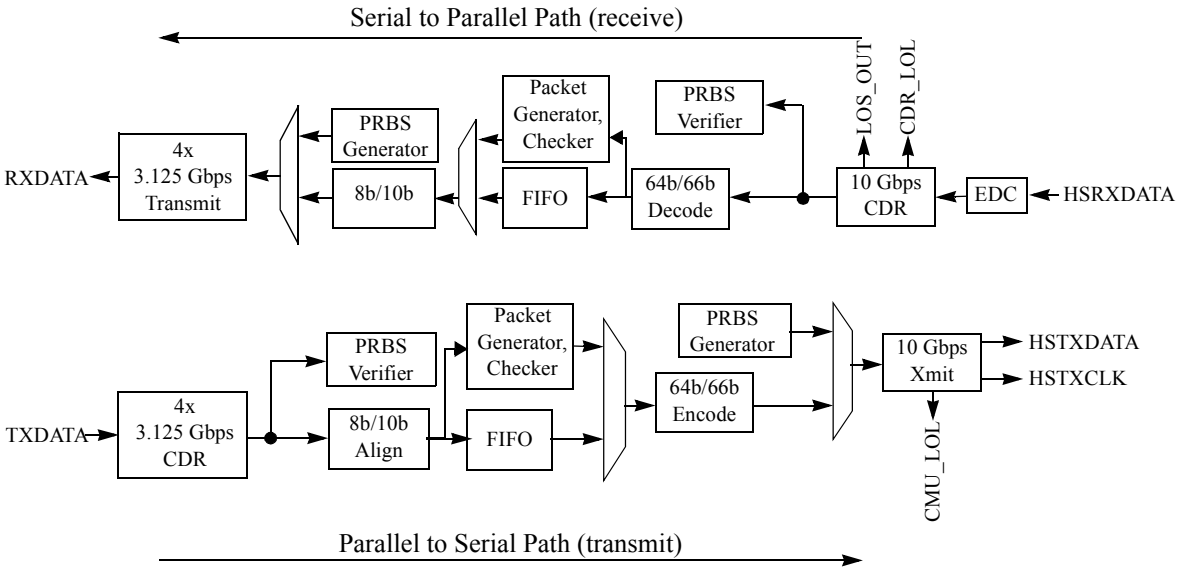


Figure 4. AEL2005 Block Diagram

4.1 Parallel to Serial Path (Transmit)

In normal operation, the AEL2005 receives parallel data on its four lane interface in XAUI format and retransmits it in serial fashion over the HSTXDATA pins. During this process, the incoming data has to be framed, aligned, and coded before transmission. An overall block diagram is shown in Figure 5. The function of each block is described in more detail in the following subsections.

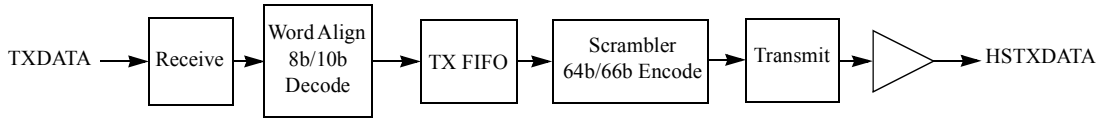


Figure 5. Parallel to Serial Transmit Path

4.1.1 XAUI Parallel Receive

The first components in the receive path are the four XAUI data input receivers and clock recovery units. These function at 3.125 Gbps or 3.1875 Gbps data rates for Ethernet & Fibre Channel operation, respectively. These units are connected to the four differential TXDATA_P/N[3:0] pairs and convert the four parallel streams into four 10-bit code words. The reference clock used for this is the external signal CMU_REF.

4.1.2 Word Align and Decode

The unaligned 10-bit words from the receive block are aligned and decoded before they are stored in the transmit input FIFO.

For each XAUI lane, the AEL2005 finds the 10-bit character boundary. The 10-bit character from each lane is converted into an 8-bit byte plus control information. The AEL2005 compares the control information from all four lanes to align the streams relative to one another and then writes the bytes into the transmit FIFO.

4.1.3 10GBASE-R Scrambler/Encoder, FIFO, and Rate Adjustment

After alignment, data is read out of the transmit FIFO, scrambled, encoded with 64b/66b, and then sent to the serial output transmitter.

The AEL2005 device includes on-chip rate adjustment capability via the insertion and deletion of IEEE 802.3ae |I| XGMII idle characters. This feature allows the device to be run in full plesiochronous mode.

4.1.4 Serial Output Transmitter

The serial output transmitter is shown in Figure 6 and is used to drive the HSTXDATA and HSTXCLK pins on the high speed CML interface. The CMU can take its reference clock from three sources: the external clock CMU_REF, the rcv_refRx clock from the serial receive block, or the output of the clock synthesizer. For 10GBASE-R, the reference is 156.25 MHz, so the CMU multiplies the frequency by 66 to produce its 10 GHz reference clock. For 10 Gigabit Fibre Channel, the reference is 159.375 MHz. This clock is used to clock out data on the HSTXDATA pins.

The HSTXCLK output clock can be configured in one of four ways:

- left turned off via the *pwrdnTranClock* bit in the Powerdown register at 1.C011 (default state).
- enabled to output the full frequency (10 GHz).
- set as a divide by 64 feedback clock using the *HSTXCLK_src* bits in the Transmit Config 1 register (address 1.C002).
- Enabled to output 10Gbps data

The CML serial interface supports the 10.3125 Gbps data rate for Ethernet applications and the 10.51875 Gbps data rate for Fibre Channel applications.

The CML channel can also be configured to support a range of options regarding differential output voltage, as summarized in Section 15.7.

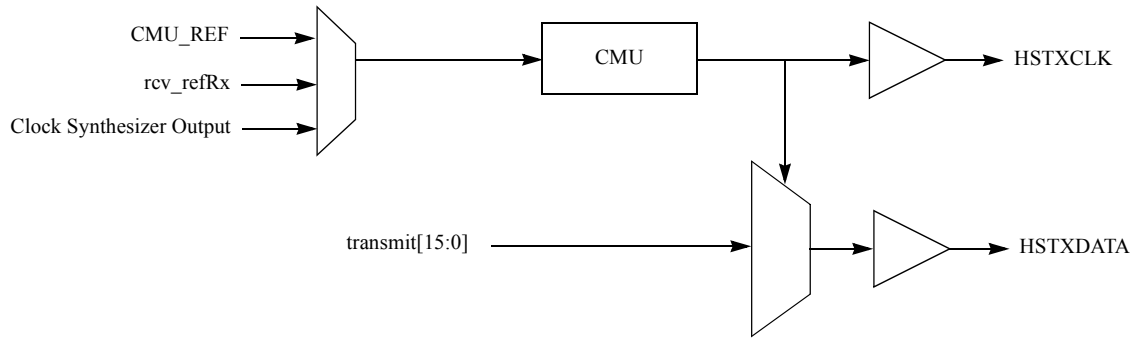


Figure 6. Serial Output Transmitter

Table 2. Serial Transmit Clock Frequencies

Mode	Reference	Input Frequency	Output Frequency (HSTXCLK)	Output Frequency (HSTXCLK) Divide by 64 Mode
10 Gigabit Ethernet	CMU_REF Clock Synthesizer	156.25 MHz	10.3125 GHz	161.13 MHz
10 Gigabit Fibre Channel	CMU_REF Clock Synthesizer	159.375 MHz	10.51875 GHz	164.36 MHz

CMU Loss of Lock (CMU_LOL)

The CMU_LOL loss of lock signal is asserted whenever the multiplied frequency of the reference clock (CMU_REF) and the output clock (HSTXCLK) differ by more than 1%.

Output Coupling for HSTXDATA and HSTXCLK

The AEL2005 includes two high speed differential outputs: the 10 Gbps data transmit channel HSTXDATA and the 10 GHz output clock HSTXCLK. Both 10 Gbps signals on the AEL2005 device are designed to be AC coupled.

Output Data Transmission Enable & XENPAK Low Power Startup (LPS) Mode

The AEL2005 includes an active low CMOS input pin, TX_ON, which serves as an enable for the high speed serial transmitter. When this pin is high, 10 Gbps transmission is enabled. When this pin is low, the AEL2005 device is placed into a global powerdown mode, and will dissipate less than 30 mW of power.

The TX_ON also provides access to the XENPAK Low Power Startup (LPS) mode. After an AEL2005 power-on reset operation is complete, the AEL2005 device will perform NVR and DOM read operations as usual. Following those, if the TX_ON signal is asserted, the AEL2005 device will start up in global powerdown mode. Upon de-assertion of TX_ON, the reset controller will complete its operation, after which the AEL2005 will be ready to pass data.

4.2 Serial to Parallel Path (Receive)

The serial to parallel path transfers data from the high speed CML interface (HSRXDATA) to the XAUI interface (RXDATA). During normal operation, the AEL2005 receives serial data on its HSRXDATA pins, then demuxes, descrambles, re-encodes, and transmits the resulting data on the four differential RXDATA_P/N[3:0] pairs. The exact operations depend on whether the part is configured to produce XAUI data, or is in loopback mode.

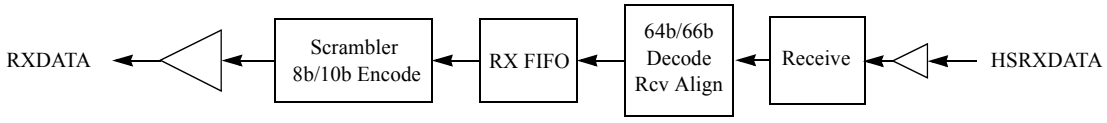


Figure 7. Serial to Parallel Receive Path

4.2.1 HSRXDATA Receive Channel

HSRXDATA is a 10 Gbps nominal data rate input. This channel can only be designed to be AC coupled. The EDC block cleans up any ISI in the received signal while the Clock and Data Recovery (CDR) unit for the AEL2005 samples HSRXDATA at the center and edges of the data eye, tracks any variations in its rate, and demultiplexes the incoming serial stream into a lower frequency parallel stream. This unit has a number of properties:

- The frequency of the incoming data can vary by up to $t_{TOL,HSRX}$ parts per million (Table 134) from the multiplied frequency of the reference clock CMU_REF.

Table 3. Serial Receive Clock Frequencies

Mode	Reference	Frequency
10 Gigabit Ethernet	CMU_REF Clock Syntheizer	156.25 MHz
10 Gigabit Fibre Channel	CMU_REF Clock Syntheizer	159.375 MHz

Loss of Signal (LOS_OUT)

The LOS of Signal (LOS_OUT) pin is asserted when the incoming signal amplitude on the HSRXDATA line is below a specified threshold during a 20 us period or when the RX_LOS input indicates an upstream loss of signal. The LOS detector is deasserted when the incoming amplitude rises above a hysteresis threshold to avoid LOS toggling on noise. The LOS assert and deassert thresholds are programmable LOSthresh[5:0] and LOSthreshhyst[5:0] in register 1.C010 shown in Table 96. The voltages indicated are the comparison thresholds at the output of the LOS peak detector.

CDR Loss of Lock (CDR_LOL)

The CDR_LOL signal is asserted whenever the CMU_REF reference clock and the divided-down recovered clock differ by more than 270 ppm.

4.2.2 64b/66b Serial Descramble/Decode, Alignment, Receive FIFO

Data from the HSRXDATA pins enters the front end decoding/descrambling block and is processed and stored in the receive FIFO. 10GBASE-R systems employ scrambling and 64b/66b encoding on the data input stream. The data is descrambled and written to the FIFO.

Rate adjustment support for insertion and deletion of IEEE 802.3ae |I| XGMII idle characters is also included in the receive path, allowing the device to be run in full plesiochronous mode.

4.2.3 Receive 8b/10b Encoding

After alignment, one byte is read from the FIFO each cycle and encoded by the 8b/10b logic. The resulting 10-bit value is sent to the XAUI transmitter.

4.2.4 XAUI Parallel Transmit

The final components in the parallel output path are the four 3.125 Gbps data output drivers. Figure 8 shows a simplified block diagram of the XAUI parallel interface. For simplicity, only one of the four channels is shown. The other three channels are identical.

These channels can also be configured to support a range of options regarding pre-emphasis and differential output voltage.

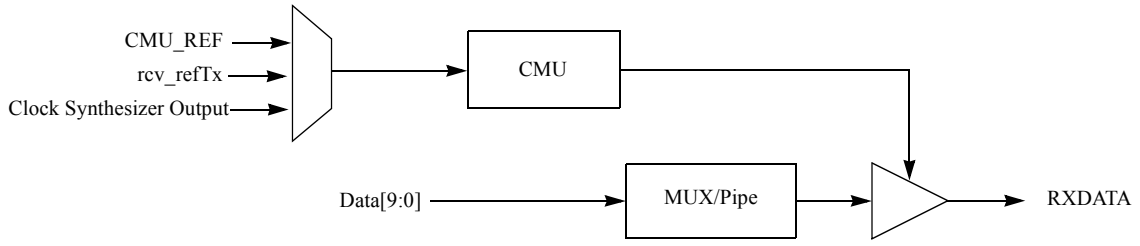


Figure 8. XAUI Parallel Transmit

4.3 EDC (Electronic Dispersion Compensation) Functionality

A multi-mode fiber (MMF) disperses the light from a laser, such that an optical pulse is split into multiple paths (“modes”) traveling at different speeds through the fiber, yielding multiple pulses that arrive at the receiver at different times. At 10Gbps data rates, the spread of these additional arrivals around the fundamental mode (the primary path carrying the most optical energy) can cause significant inter-symbol interference (ISI), preventing accurate recovery of the signal. Each transmitted symbol causes pre-cursor ISI to the preceding symbols due to stray modes that travel faster than its fundamental mode. It also causes post-cursor ISI to the subsequent symbols, due to the modes traveling slower than the fundamental mode. The EDC function in AEL2005 cancels out these effects, allowing customers to deploy 10GbE using their existing installed base of multi-mode fiber.

Figure 9 shows the EDC block diagram. It consists of a feed forward equalizer stage (FFE) to cancel the pre-cursor ISI, and a decision feedback equalizer stage (DFE) to cancel out post-cursor ISI. Both stages are self-adaptive, allowing the AEL2005 to adapt to a variety of MMFs with even time-varying dispersive conditions automatically. Note that the AEL2005 includes separate branches in the feedback stage to accurately compensate for signal distortions at the center of the data eye, as well as the edge of the data eye.

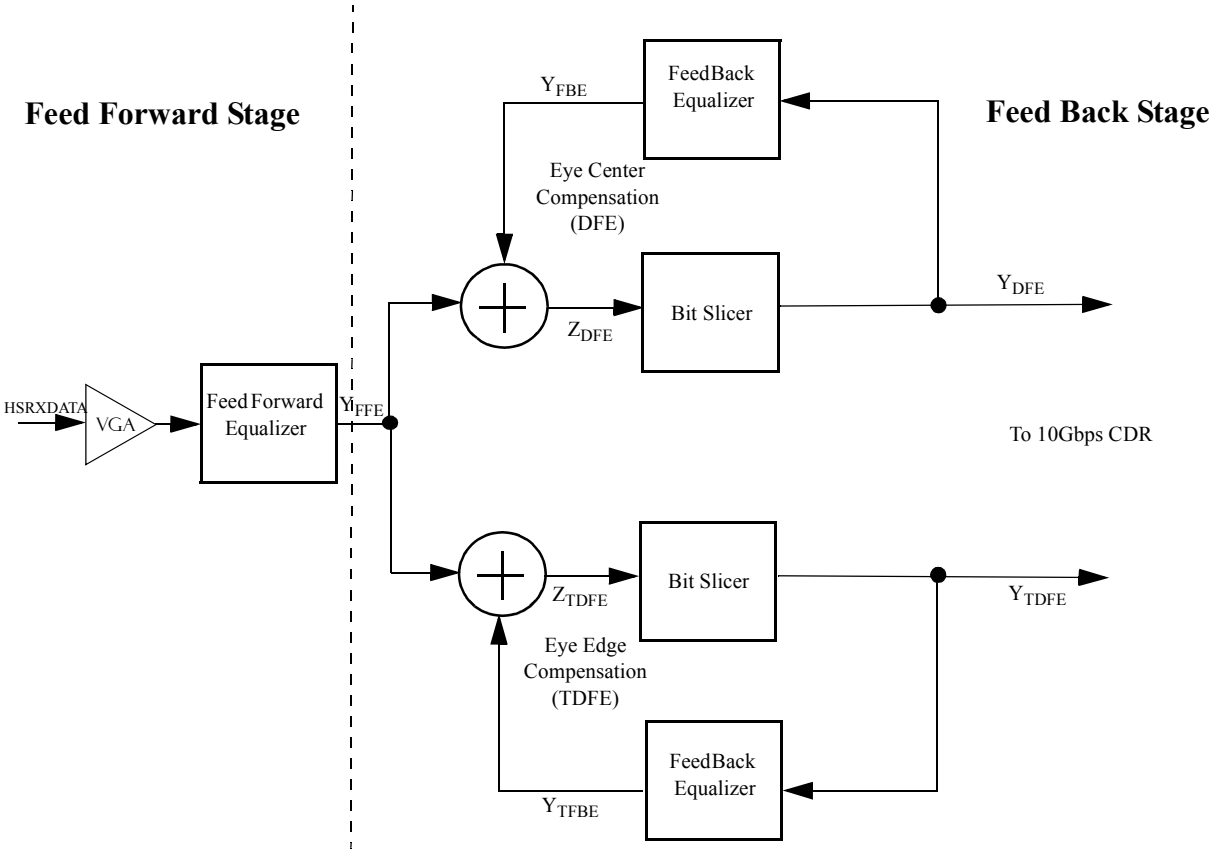


Figure 9. Electronic Dispersion Compensation Block Diagram

4.3.1 Feed Forward Stage

The feed forward stage is shown in Figure 10. It consists of a feed forward equalizer (FFE), situated between a pre-amplification stage and a post-amplification stage.

The pre-amplification stage consists of a variable gain amplifier (VGA1), while post-amplification is performed by a cascaded amplifier pair. The gain level of the pre-amplification stage is controlled by digitally tuned gain level G_1. VGA1 is designed to provide the FFE with an ample input signal level while maintaining linearity, while the post-amplification stage yields sufficient range of gain, to compensate for attenuation in the signal as it passes through the FFE. The FFE is a fractional (T/2) adaptive finite impulse response (FIR) filter, made up of a 12-tap delay line with digitally tuned h_{FFE} coefficients.

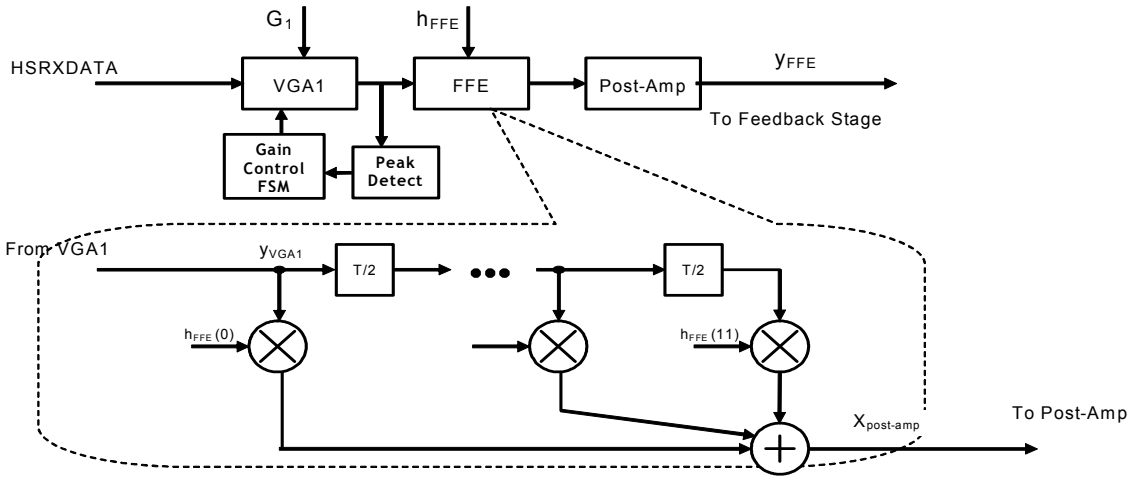


Figure 10. Feed Forward Stage Block Diagram

It is set to T/2 nominally, where T represents the symbol interval. This provides a high degree of adaptation flexibility. The FIR filter coefficients are adapted using a proprietary variant of the least-mean-squared (LMS) algorithm, designed to cancel distortions caused by the laser transmitter, the channel and the detector, while also removing pre-cursor ISI for the signal. In general, pre-cursor ISI is eliminated from the signal when it leaves the feed forward stage.

4.3.2 Feedback Stage

The feedback stage contains separate branches to correct for post-cursor ISI at the center, as well as at the edge of the data eye, with the former (the DFE, or data branch) ensuring accurate symbol detection, and the latter (the TDFE, or timing branch) reducing jitter in the CDR's recovered clock output.

The block diagram of the feedback stage is shown in Figure 11. The eye-center correction branch (DFE) contains a feedback equalizer (FBE, a 4-tap filter). The filter co-efficients h_{FBE} are digitally tuned and are adapted using a proprietary LMS type algorithm to minimize the data error.

The eye-edge timing compensation branch (TDFE) produces a signal that enables the CDR unit to perform accurate clock recovery. It similarly contains a decision feedback equalizer (TFBE, a 4-tap filter). The co-efficients h_{TFBE} are digitally tuned and adapted using a proprietary LMS type algorithm to cause the zero crossings to coincide with the edge of the data eye.

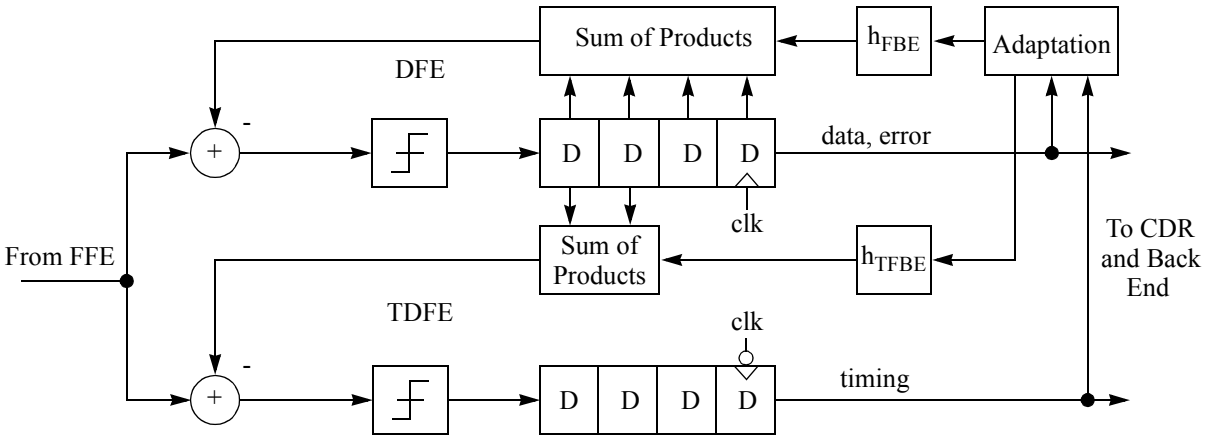


Figure 11. Feed Back Stage Block Diagram

4.3.3 EDC Adaptation

The EDC adaptation consists of a carefully sequenced multi-step process which is controlled by the on-chip adaptation controller block. The purpose of the adaptation controller is to initialize adaptation settings such as feedforward equalizer filter coefficients and gain targets at a good point when the chip is brought out of reset. Adaptation parameters such as FFE, FBE and TFBE coefficients and VGA gain are updated continuously to account for changes in the operating environment (power supply and temperature) and channel conditions over time at a rate of 10s of Hz.

A variety of registers control adaptation initialization and timing. The error slicer threshold in 1.C503 is used by the LMS algorithm to calculate the adaptation error at a given point in time. The front-end VGA peak target (at the VGA output) is set in 1.C847 to maintain a good signal level into the feedforward equalizer as a compromise between noise and linearity and will be set based on ROSA chacteristics. The feedforward equalizer coefficients can be initializeded at the start of adaptation in 1.C620-1.C62C to provide a good starting filter response.

The adaptation microcode which will be provided by Aeluros in 1.C800-1.C820 controls the timing of coefficient and gain updates to ensure correct tracking of changing conditions. The equalizer coefficients may be read back in 1.C62D - 1.C636 to determine where the equalizer has landed.

5 10G Transmit Pre-emphasis

The AEL2005 device supports transmit pre-emphasis on the 10G transmitter. There are 3 taps of pre-emphasis which are controlled from the 1.C014 and 1.C015 registers.

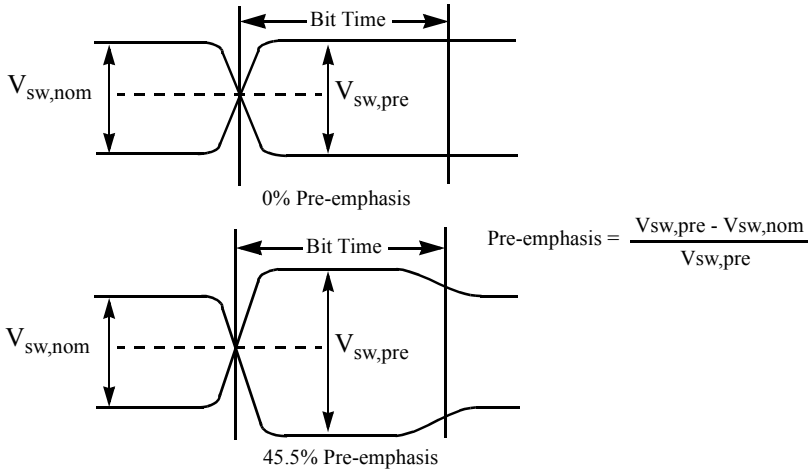


Figure 12. Effects of Transmit Pre-emphasis

The effects of pre-emphasis have been shown above. The 3 taps equate to pre, post and main tap of pre-emphasis. When pre-emphasis is turned off the main tap is added to the pre and post tap without any inversion. When pre-emphasis is turned on the side taps are shifted in time and have sign inversion.

The pre and post taps have 5 bits of programmability and the main tap have 6 bits of programmability.

6 SGMII Mode

The AEL2005 supports two 1.25Gbps SGMII low latency pass-thru channels, which can be configured through registers 1.C01F and 1.C220. The HSRXDATA_P/N and the HSTXDATA_P/N pins serve as the input and output ports of channel0 on the network side, while RSFP1_P/N and HSTXCLK_P/N pins serve similar functions for channel 1. On the system side, any Xaui lane can be configured as the system interface for either of the two channels.

The register used for configuring SGMII mode is described in Table 106.

7 On-Chip Micro-Controller

Sabercat contains a proprietary on-chip micro-controller (uC). It is designed to be used for internal management tasks within the chip, and is generally not available for user applications.

7.1 uC Block Diagram

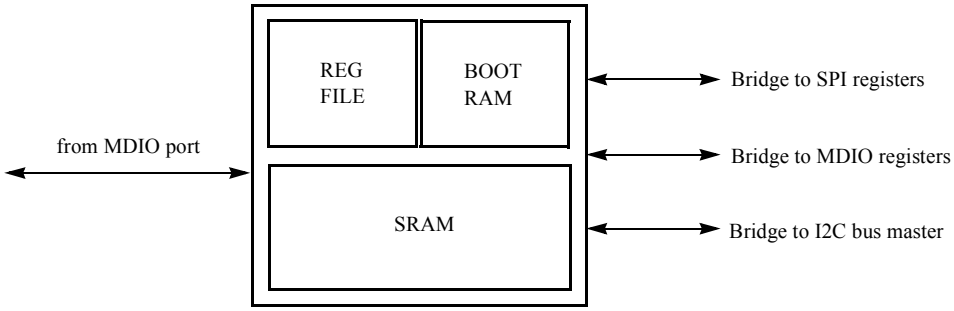


Figure 13. Embedded Micro-Controller

A block diagram for the embedded micro-controller is shown in Figure 13. As shown, the micro-controller consists of a *boot memory* and an *embedded SRAM* in addition to the program register file. The boot memory contains a hardwired boot program which, upon power up, may be configured to automatically load additional firmware from an external EEPROM into the embedded SRAM. This newly loaded firmware subsequently executes out of the SRAM, making the boot memory available for use as a scratch space or as a stack. Sixteen program registers are available for use by the firmware.

All state information within the uC can be accessed from the chip's MDIO port. This includes inspecting and altering the boot program, the SRAM content, and all program registers in the controller.

The uC module has access to every SPI and MDIO register in the chip, as well as its I2C bus. As such, uC may be used to perform a variety of tasks, such as:

- Patching configuration register (beyond the C000 - C07F range)
- Monitoring status registers and taking corrective actions (e.g. EDC parameter optimization)

All MDIO/SPI/I2C accesses issued by uC go through an arbitrator unit to ensure that they can proceed concurrently with accesses coming from the MDIO/SPI ports, without causing any conflicts.

7.2 uC Configuration

By default, the uC is held in reset upon power up. Its subsequent behavior is determined by two configuration registers (mapped to MDIO registers 1.C04A and 1.C04B), which may be modified either through the I2C patch process or via MDIO write operations. These registers are defined in Table 109 and Table 110.

To enable the embedded micro-controller, 1.C04A.15 should be cleared to 0. This initiates the boot process, where the hardwired boot program fetches additional instructions from an external EEPROM into its on-chip SRAM, using

the patchable parameters *uc_eepaddr* (1.C04B) and *uc_eepsize* (1.C04A.7:4). Subsequently, program flow is transferred to the newly loaded program.

7.3 uC Control and Status

All internal states of the on-chip micro-controller can be accessed through MDIO registers. Several registers of particular interest are shown in Table 133. Note however that these registers are accessible only when the uC is enabled (1.C04A.15 = 0).

The program counter contains the current instruction pointer. When the micro-controller is running, the value of the program counter should change periodically when read via MDIO.

The PAUSE and SSTEP bits can be used to place the micro-controller into a single-step operation mode. When the PAUSE bit is set to 1, the execution of the firmware is stopped. Subsequently, the user may cause *n* more instructions to be executed, by writing the integer n into the SSTEP register. The status bit PAUSED returns 1 whenever program execution is stopped. For debug purposes, the micro-controller may also be configured to immediately enter single-step mode (PAUSED) when enabled. This is accomplished by setting 1.C04A.14 to 1 before enabling the micro-controller.

The firmware for the microcontroller on the AEL2005 can also be downloaded directly into the device either through MDIO or by using the SPI interface on an external microcontroller.

8 GPIO Interface

AEL2005 has 4 configurable GPIO pins, which are CDR_LOL (B5), CMU_LOL (B4), MODDET (N13) and GPIO (N11). These pins can be programmed into inputs, outputs or LED drivers according to specific applications.

1.C214 contains control and status bits for the 4 GPIO pins (4 bits for each lane), as shown in Table 120. Table illustrates all available operation modes. Writing 0x0 to any lane will not change its operation mode. For example, if some one writes 0xA000 to 0.C214 to configure lane 3 (pin N11), the other three GPIO pins won't be affect by this write. GPIO status is accessible by reading 1.C214. Table 4 shows definitions of status bits.

To simplify the scenario, only describes one of the common ways of using these GPIO pins: CDR_LOL and CMU_LOL drive status LEDs; MODDET monitors SFP+ MOD_ABS signal; GPIO controls SFP+ rate select pin RS0 and RS1. However, all of these functions can be extended to any other lanes.

8.1 LED Drivers

By setting GPIO control register 1.C214 to 0x0099, CMU_LOL (B4) and CDR_LOL (B5) are configured to drive external LED indicators. The integrated truth tables define the meaning of LED indicators. 1.C216 (LED0_TT) contains the truth table index for CDR_LOL, while 1.C217 (LED1_TT) contains the truth table index for CMU_LOL. As shown in Table 1, the truth table index is defined by the variable {rx_status, rx_active, tx_status, tx_active}. A LED is light on when the conditions that corresponds to bit '1' in the truth table are satisfied. Two examples are given in the following.

Table 4. Encoding of LED Indicators

		tx_status = 1		tx_status = 0	
		tx_active = 1	tx_active = 0	tx_active = 1	tx_active = 0
rx_status = 1	Rx_active = 1	Led_TT[15]	Led_TT[14]	Led_TT[13]	Led_TT[12]
	Rx_active = 0	Led_TT[11]	Led_TT[10]	Led_TT[9]	Led_TT[8]
rx_status = 0	Rx_active = 1	Led_TT[7]	Led_TT[6]	Led_TT[5]	Led_TT[4]
	Rx_active = 0	Led_TT[3]	Led_TT[2]	Led_TT[1]	Led_TT[0]

8.1.1 Example 1: Configure CDR_LOL Pin to Indicate Link-up Status

In this case, LED needs to turn ON when both tx_status and rx_status are TRUE (ignoring the state of tx_active and rx_active). Therefore, bits 15, 14, 11, and 10 of the corresponding led0_TT register (1.C216) should be set to 1 as shown in the table below, indicating that the LED is ON whenever tx_status = 1 and rx_status = 1, and OFF otherwise. In other words, led0_TT (1.C216) = 0b1100_1100_0000_0000 = 0xcc00.

Table 5. Configuring CDR_LOL Pin to Indicate Link-up Status

		tx_status = 1		tx_status = 0	
		tx_active = 1	tx_active = 0	tx_active = 1	tx_active = 0
rx_status = 1	Rx_active = 1	1	1	0	0
	Rx_active = 0	1	1	0	0
rx_status = 0	Rx_active = 1	0	0	0	0
	Rx_active = 0	0	0	0	0

8.1.2 Example 2: Configure CMU_LOL Pin to Indicate Traffic Activity

In this case, the LED needs to turn ON when both tx_active and rx_active are TRUE (ignoring the state of tx_status and rx_status). Therefore, bits 15, 13, 7 and 5 of 1.C216 should be set to 1, indicating that the LED is ON whenever tx_active = 1 and rx_active =1, and OFF otherwise. In other words, led1_TT(1.C217) = 0b1010_0000_1010_0000 = 0xa.

Table 6. Configuring CMU_LOL Pin to Indicate Traffic Activity

		tx_status = 1		tx_status = 0	
		tx_active = 1	tx_active = 0	tx_active = 1	tx_active = 0
rx_status = 1	Rx_active = 1	1	0	1	0
	Rx_active = 0	0	0	0	0
rx_status = 0	Rx_active = 1	1	0	1	0
	Rx_active = 0	0	0	0	0

8.2 MODDET Input

MOD_ABS is an output from the SFP+, which is asserted low when modules are inserted. (Note that a pull-up resistor is required on the system side for MOD_ABS) In many cases, it is useful to generate an interrupt on LASI signal when module presence is changed. AEL2005 supports this feature with its GPIO pins. Not only can all GPIO pins be configured to inputs, users can also choose the interrupt mode. The available options are: no interrupt; raise interrupt on any state transition; raise interrupt on 1 to 0 transition; raise interrupt on 0 to 1 transition. The interrupt status for each lane is available at 1.C215:3:0. By writing "1101" to the corresponding control bits in 1.C214, LASI will be de-asserted. Note that LASI is not clear-after-read in this case.

For instance, one could connect MOD_ABS to MODDET (N13) and set GPIO control register 1.C214 to 0x0200. In this way, the MODDET (N13) pin is configured to input and it generates an interrupt to LASI both when SFP+ is inserted or removed. The input value is available at bit 8 of 1.C214. After an interrupt is issued, 1.C215 bit 2 will become and stay '1'. LASI and the status bit won't be cleared until one writes "1101" to 1.C214.11:8.

8.3 Rate Select Output

SFP+ requires control signals to select operation rate via RS0 and RS1. By setting GPIO control register 1.C214 to 0xa000/0xb000, the GPIO (N11) pin of AEL2005 drives '0'/'1' statically.

* Mapping between internal signals and pin number: gpio0->CDR_LOL(B5), gpio1 ->CMU_LOL(B4), gpio2->MODDET(N13), gpio3->GPIO(N11)

Table 7. GPIO Control Mode Table A

Write gpio_ctrl with this value	Operating Mode
0000	No change to operating mode, data or interrupt states.
0001	Input mode, Interrupt disabled. In this mode. gpio2 = MODDET, gpio3 = GPIO.
001?	Input mode. Raise interrupt on any state transition. In this mode, gpio2 = MODDET, gpio3 = GPIO.
010?	Input mode. Raise interrupt on 1 to 0 transition. In this mode, gpio2 = MODDET, gpio3 = GPIO.
011?	Input mode. Raise interrupt on 0 to 1 transition. In this mode, gpio2 = MODDET, gpio3 = GPIO.

Table 7. GPIO Control Mode Table A (Continued)

Write gpio_ctrl with this value	Operating Mode
1000	Indicator (LED) mode 0 In this mode, gpio0 = RX CDR_LOL indicator, gpio1 = RX link activity indicator, (gpio2, gpio3) = observation port
1001	Indicator (LED) mode 1 In this mode, gpio0 = TX link activity indicator, gpio1 = RX link activity indicator, (gpio2, gpio3) = observation port
1010	Drive “0” to pin statically
1011	Drive “1” to pin statically
1100	Reserved
1101	Clears Interrupt

Table 8. GPIO Status Mode Table B

gpio_ctrl returns	Status
000d	Input mode. Interrupt disabled. Current input value is d
001d	Input mode. Raise interrupt on any state transition. Current input value is d
010d	Input mode. Raise interrupt on 1 to 0 transition. Current input value is d
011d	Input mode. Raise interrupt on 0 to 1 transition. Current input value is d
100m	Pin is currently configured into indicator (LED) mode m
1010	Currently driving d to pin statically
110?	Reserved
111?	Blinker output mode

8.4 Link Alarm Status Interrupt

The AEL2005 Link Alarm Status Interrupt indicates when some type of fault condition has been detected within the module where the AEL2005 resides. These faults can either be internally generated or externally polled via the serial SDA/SCL bus. The LASI_N signal can be used to drive the LASI output of a XENPAK module. Figure 14 shows the logic for the output; it is generated from the contents of the LASI status and LASI control registers.

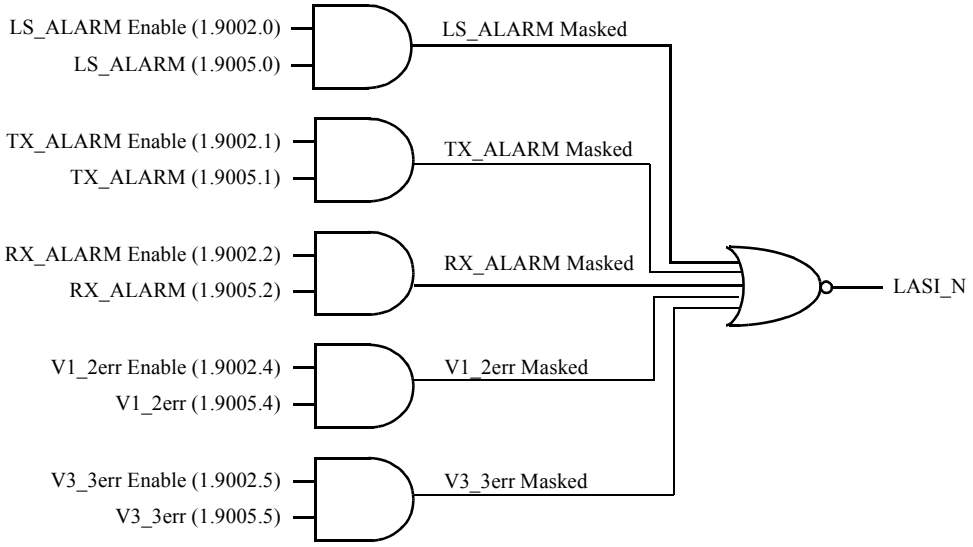


Figure 14. Link Alarm Status Interrupt Generation

LS_ALARM is generated as shown in Figure 15. LINK_STATUS is generated as the logical AND of three register bits: PMD Receive Detect, 10GBASE-R Lock, and PHY XGXS lane align. Whenever there is a change in LINK_STATUS, the set-reset flip-flop driving LS_ALARM is set. LS_ALARM remains asserted until the next MDIO read to the LASI status register (1.9005).

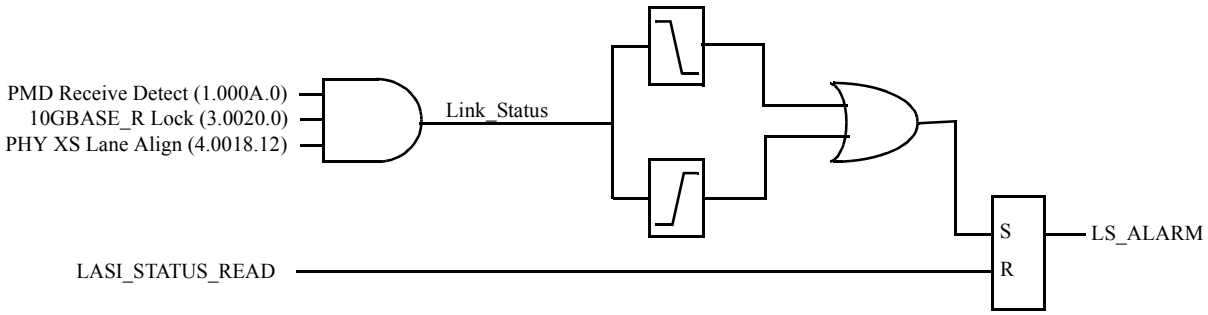


Figure 15. LS_ALARM Generation

The transmit alarm generation logic is shown in Figure 16. TX_ALARM is asserted whenever the temperature, output power, or laser bias go outside of the limits defined in the DOM High/Low Alarm registers, or whenever a transmit fault occurs within the PMA/PMD, PCS, or PHY XS blocks. The Transmit fault, bit 6, consists of the logical OR of the last three faults, and provides an additional means of identifying fault conditions.

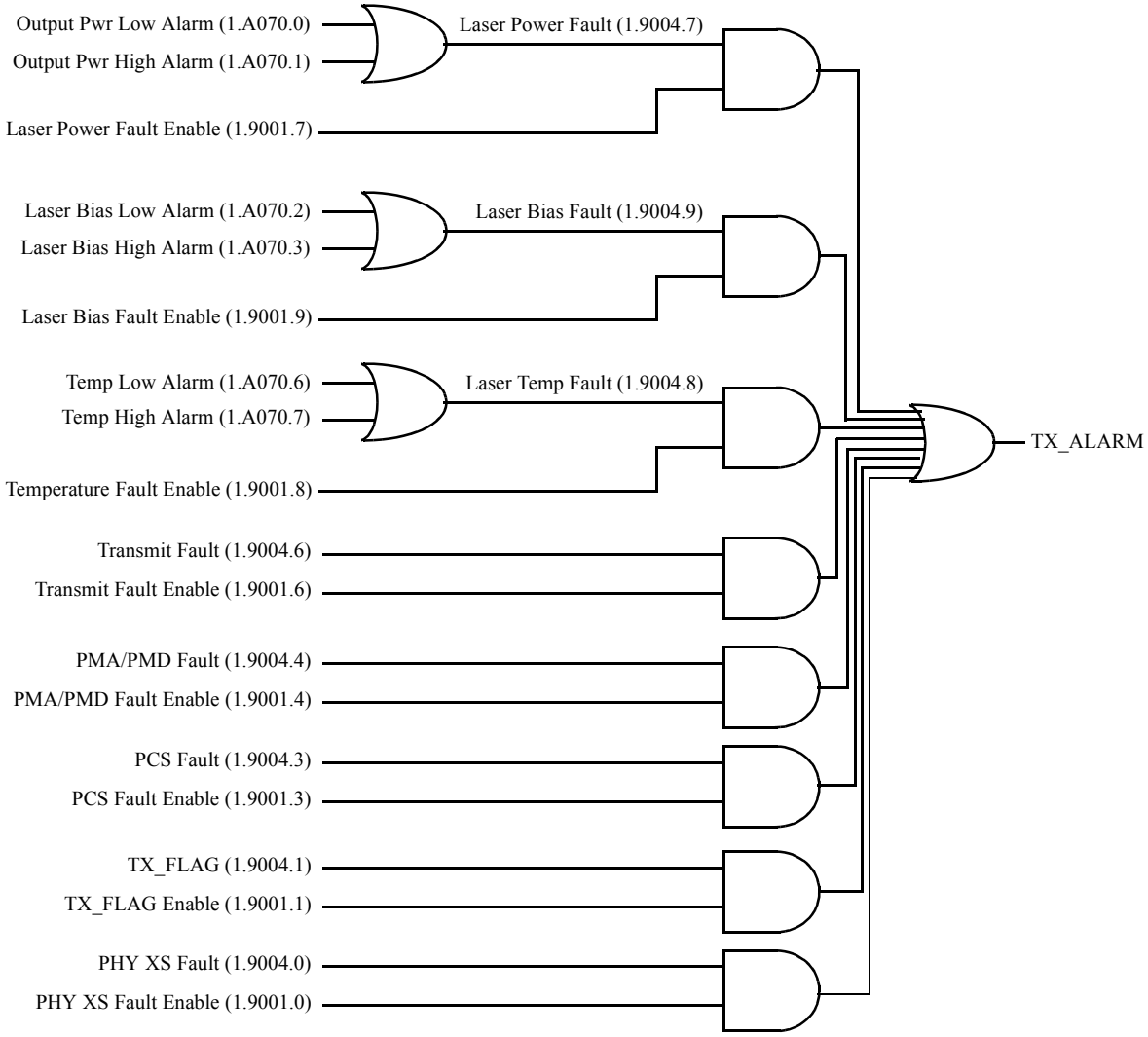


Figure 16. Transmit Alarm (TX_ALARM) Generation

The receive alarm generation logic is shown in Figure 17. RX_ALARM is asserted whenever the receive optical power goes outside of the limits defined in the DOM High/Low Alarm registers, or whenever a receive fault occurs within the PMA/PMD, PCS, or PHY XS blocks.

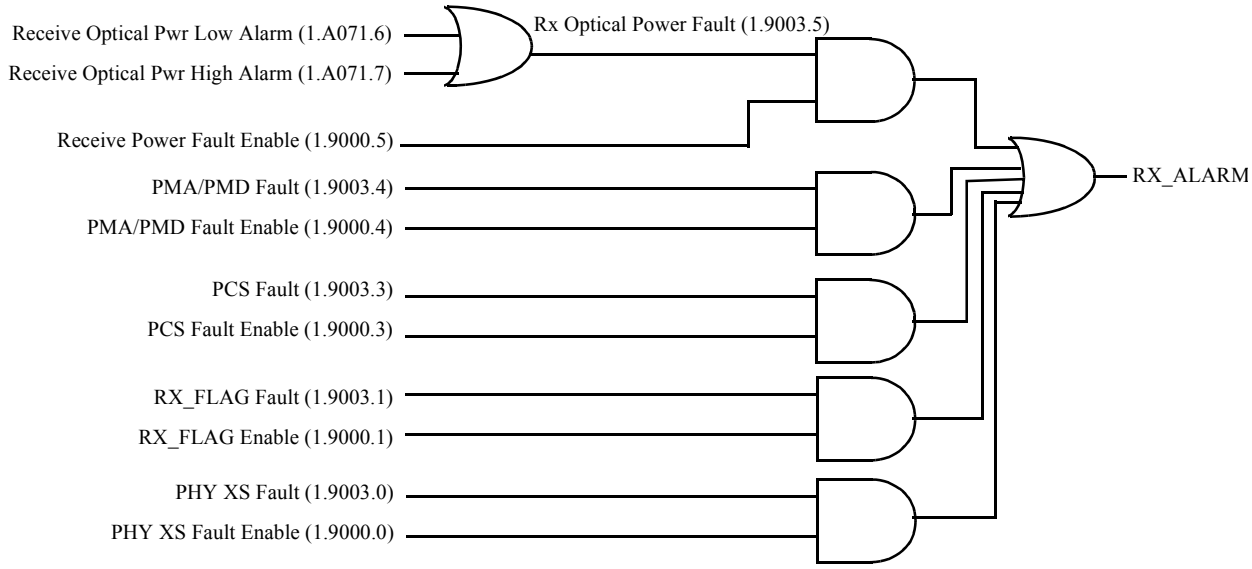


Figure 17. Receive Alarm (RX_ALARM) Generation

Logic to verify the validity of the module 1.2-V and 3.3-V power supplies is included, with the resultant values stored in the LASI status register. The equivalent circuit is shown in Figure 18. The 1.2-V Vdd supply, internally scaled by 0.5, or the 3.3-V supply, internally scaled by 0.182 is compared against one of four thresholds: +/- 5%, +/- 10%, +/- 15%, or +/- 20%, as selected by register 1.C00F. If the value falls outside the chosen range, the corresponding error bit in the 1.9005 LASI register is asserted. Selection of the range is chosen as shown in Figure 18.

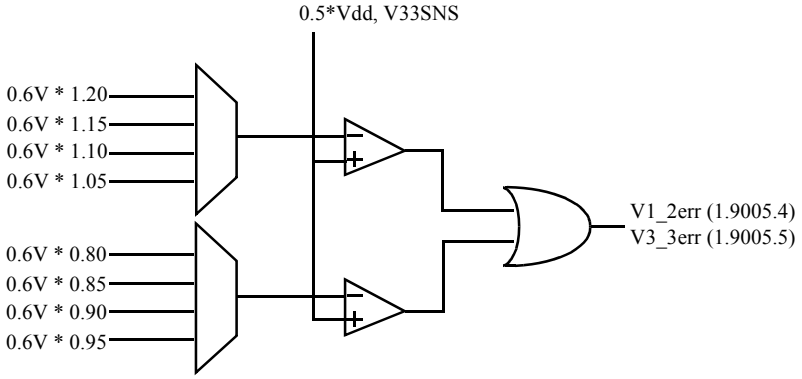


Figure 18. Power Supply Sensing Error Generation

Logic for generation of the TX_FLAG and RX_FLAG error signals is shown in Figure 19 and Figure 20 below.

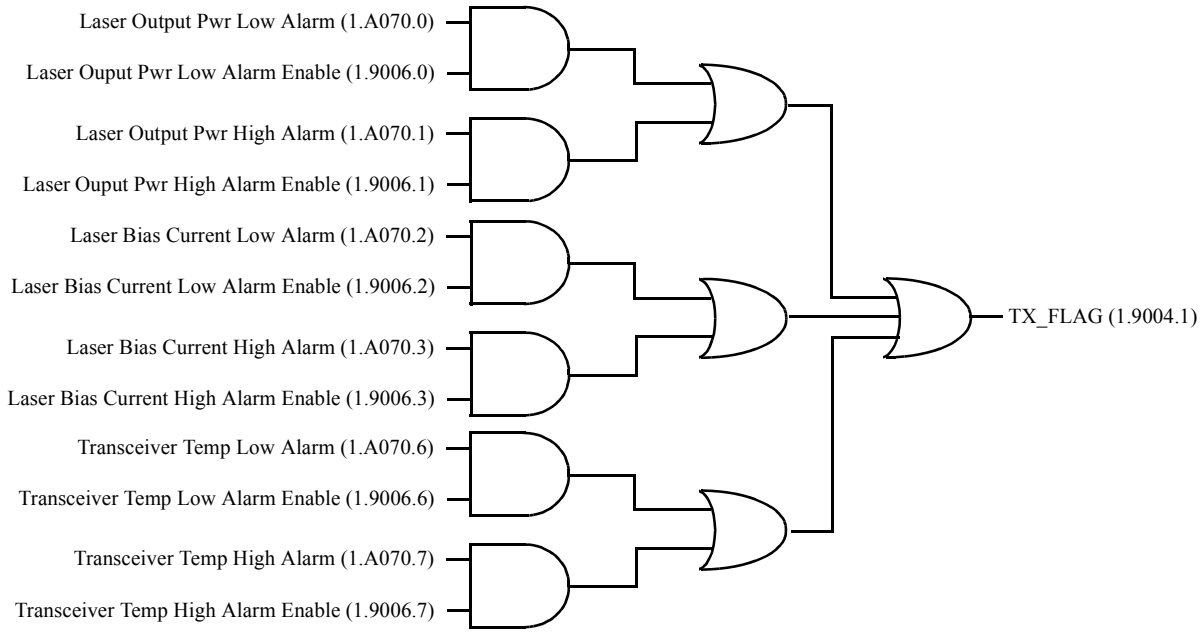


Figure 19. Transmit Flag (TX_FLAG) Generation

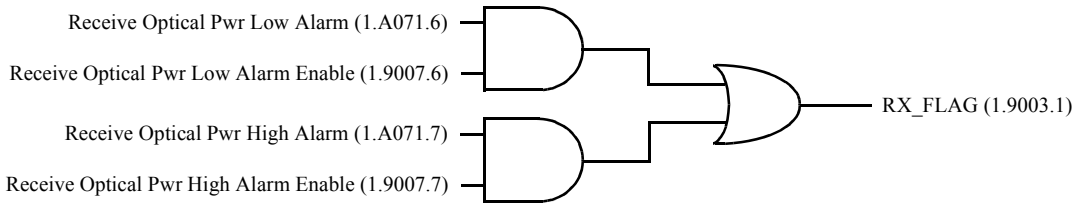


Figure 20. Receive Flag (RX_FLAG) Generation

9 Clocking Modes

The AEL2005 device contains support for various clocking modes to enable implementation of LAN/SAN or LAN-only module implementations, and to allow use of a low cost 50 MHz crystal oscillator. Control bit references for each mode relate to register bits in register 1.C001, as described in Table 88.

9.1 Basic LAN Clocking

The basic AEL2005 LAN Clocking configuration is shown in Figure 21. All major blocks, including the CDRs and the transmitters for both the 10 Gbps and XAUI interfaces, are clocked by the external clock CMU_REF. The rate adjustment feature in the core logic adds or removes IEEE 802.3ae |I| characters to accommodate slight differences in frequency between the incoming data and the reference clock. CMU_REF should be provided at the 10 Gigabit Ethernet frequency of 156.25 MHz, or for SAN operation, at the 10 Gigabit Fibre Channel frequency of 159.375 MHz.

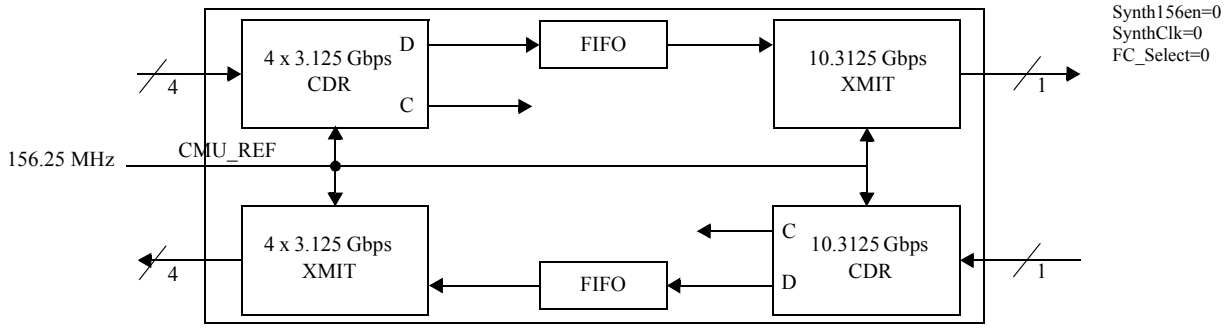


Figure 21. Basic LAN Clocking Mode

9.2 Basic SAN Clocking

The onboard clock synthesizer available in the AEL2005 device can be used to implement a dual 10 Gigabit Ethernet / 10 Gigabit Fibre Channel optical module. In this case, the clock synthesizer will account for the 2% clock frequency difference between these two standards by converting a 156.25 MHz reference to 159.375 MHz. Basic SAN operation is shown in Figure 22, while SAN operation using the clock synthesizer is shown in Figure 23.

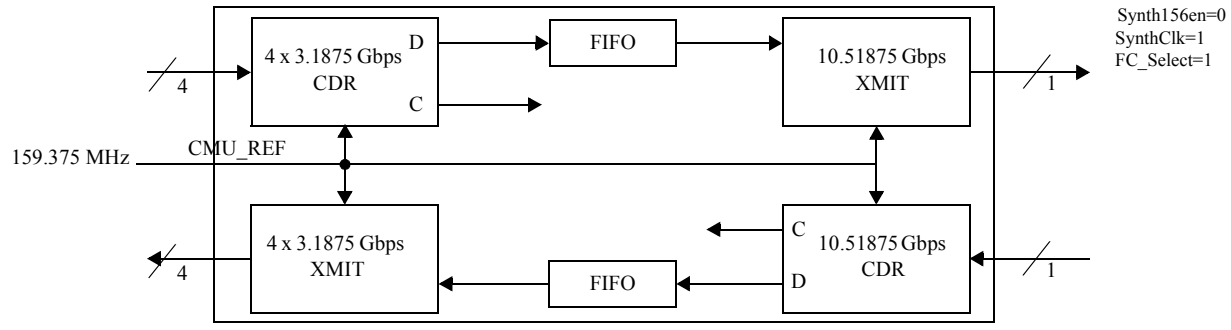


Figure 22. One XO SAN Clocking Mode (159.375 MHz)

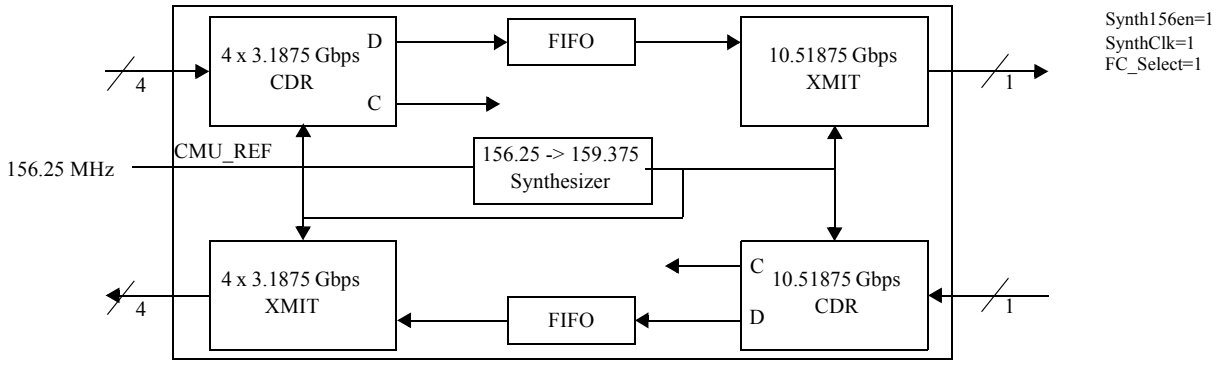


Figure 23. One XO SAN Clocking Mode (156.25 MHz)

9.3 50 MHz Clocking

The onboard clock synthesizer available in the AEL2005 device can be used to implement either a 10 Gigabit Ethernet or a 10 Gigabit Fibre Channel module based off of a low-cost 50 MHz crystal oscillator. LAN, SAN and SGMIIoperation for 50 MHz operation are shown in Figure 24, Figure 25 and Figure 26 respectively.

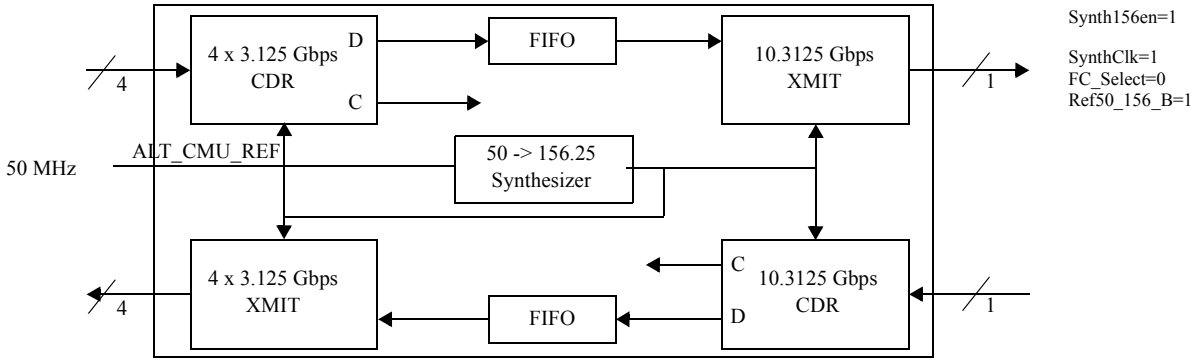


Figure 24. 50 MHz LAN Clocking Mode

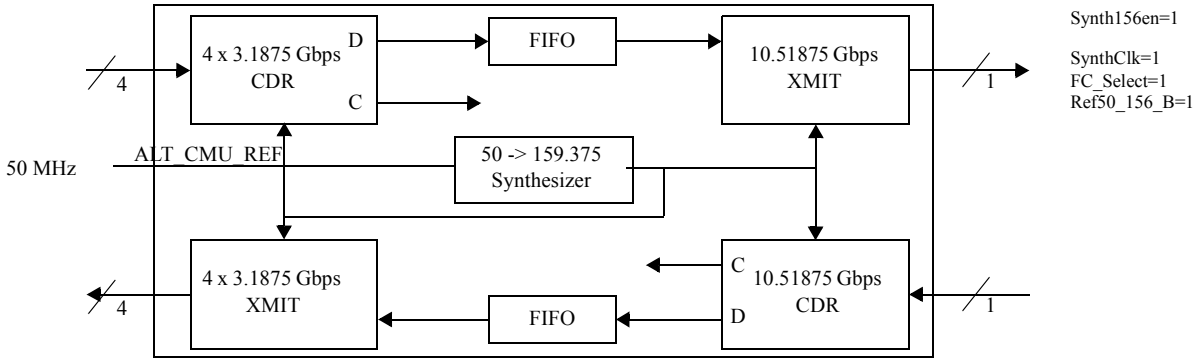


Figure 25. 50 MHz SAN Clocking Mode

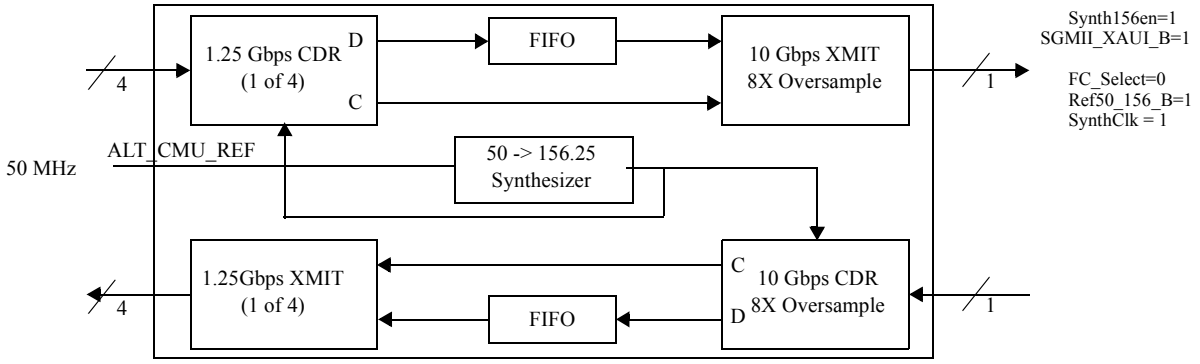


Figure 26. 50 MHz SGMII Clocking Mode

10 Test & Loopback Modes

The AEL2005 provides for loopback testing on both the high-speed serial and parallel interfaces as explained in the following subsections. Note that the line loopback and system loopback functions cannot be simultaneously enabled. A summary of these loopback modes is shown in Table 9.

Table 9. AEL2005 Loopback Modes

Loopback Mode	Enable Bit	Rate Adjust	Alt Pattern Bit	HSTX-DATA Default	HSTX-DATA Alternate	RXDATA Default	RXDATA Alternate
PHY XS System	4.C000.14	no	4.C000.15	0000	TXDATA	TXDATA	TXDATA
PCS System	3.0000.14	yes	3.C000.5	00FF	TXDATA	TXDATA	TXDATA
PMA System	1.0000.0	yes	3.C000.5	0000	TXDATA	TXDATA	TXDATA
PHY XS Line	4.0000.14	yes	-	HSRXDATA	HSRXDATA	HSRXDATA	HSRXDATA
PMA Line	1.C001.4	no	1.C001.9	HSRXDATA	HSRXDATA	HSRXDATA	HSRXDATA

10.1 System Loopback Modes (XAUI CDR to XAUI Transmit)

Three independent forms of system loopback are provided, providing the ability to incorporate a range of AEL2005 device blocks into the loopback path. Each of these three paths involves routing the data from the XAUI input pins (TXDATA) to the XAUI output pins (RXDATA). These three paths are illustrated in Figure 27.

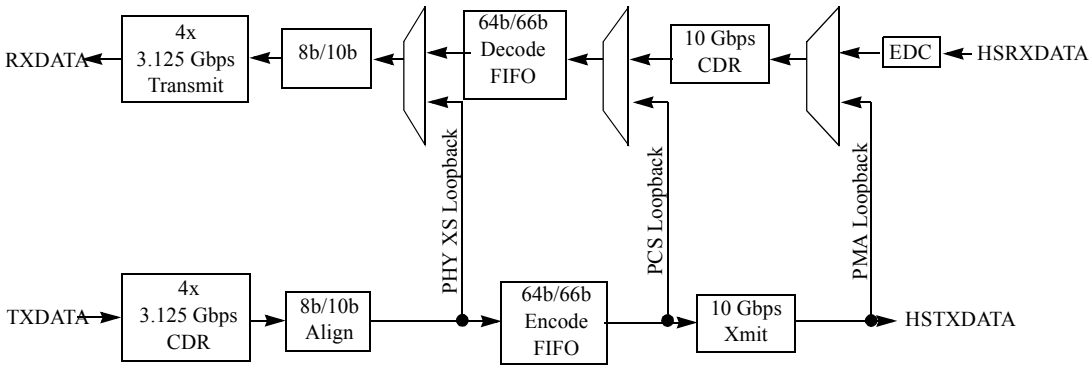


Figure 27. System Loopback Modes

10.1.1 PHY XS System Loopback

The PHY XS System Loopback is the shallowest of the three available system loopback paths. This path connects the data from the output of the 10GBASE-X logic in the device transmit path to the input of the 10GBASE-X logic on the device receive path. This path includes the 8b/10b encoder/decoder and XAUI alignment functions. The AEL2005 device is placed in this mode by setting bit 14 of the PHY XS System Loopback Control Register (address 4.C000) or bit 2 of the Optional Settings Register (address 1.C017) as shown in Table 64 and Table 102.

When in PHY XS System Loopback, a continuous stream of zeros is propagated through the remainder of the transmit data path. As an option when in PHY XS System Loopback, loopback data can be propagated through the remainder of the transmit data path as well as back along the loopback path by setting bit 15 of the PHY XS System Loopback Control Register (address 4.C000) or bit 9 of the Optional Settings Register (address 1.C017) as shown in Table 64 and Table 102.

Note that externally-generated PRBS data provided to an AEL2005 device in PHY XS system loopback mode may not be returned to the AEL2005 device pins as intended if the internal 8b/10b encoder logic is not disabled. This can be accomplished by setting bit 8 of the Logic Configuration Register at address 1.C20C as shown in Table 117.

10.1.2 PCS System Loopback

The PCS System Loopback provides a deeper system loopback path, and is compliant with the PCS System Loopback defined in the IEEE 802.3ae standard, Clause 49.2.14.4. This path connects the data from the output of the PCS logic in the device transmit path to the input of the PCS logic on the device receive path. This path includes the 64b/66b encoder and scrambler functions, as well as the blocks included in the PHY XS system loopback path. The AEL2005 device is placed in this mode by setting bit 14 of the PCS Control 1 register (address 3.0000) or bit 1 of the Optional Settings Register (address 1.C017) as shown in Table 33 and Table 102.

When in PCS System Loopback, a continuous 0x00FF data word stream is propagated through the remainder of the transmit data path. As an option, the loopback data can be propagated through the remainder of the transmit data path as well as back along the loopback path by setting bit 5 of the PCS System Loopback Control Register (address 3.C000) or bit 9 of the Optional Settings Register (address 1.C017) as shown in Table 51 and Table 102.

10.1.3 PMA System Loopback

The PMA System Loopback provides the deepest available system loopback path, and is compliant with the PMA System Loopback defined in the IEEE 802.3ae standard, Clause 51.8. This path occurs at the 10 Gbps serial interface. The AEL2005 device is placed in this mode by setting bit 0 of the PMA Control 1 register (address 1.0000) or bit 0 of the Optional Settings Register (address 1.C017) as shown in Table 19 and Table 102.

When in PMA System Loopback, a continuous stream of zeros is propagated through the remainder of the transmit data path. As an option, the loopback data can be propagated through the remainder of the transmit data path as well as back along the loopback path by setting bit 5 of the PCS System Loopback Control Register (address 3.C000) or bit 9 of the Optional Settings Register (address 1.C017) as shown in Table 51 and Table 102.

Note that the PMA System Loopback path does not include the PMA/PMD Signal Detect circuitry. As a result, the PMA/PMD Signal Detect indicated in register 1.000A will continue to monitor the HSRXDATA pins, rather than reflecting the presence of correct data in the loopback path, even when in PMA System Loopback mode.

10.1.4 System Loopback Clocking Modes

For PHY XS loopback of the XAUI interface, the recovered clock is used to synchronize the parallel transmitter as illustrated in Figure 28. PMA and PCS System Loopback make use of the CMU_REF as the general system reference clock.

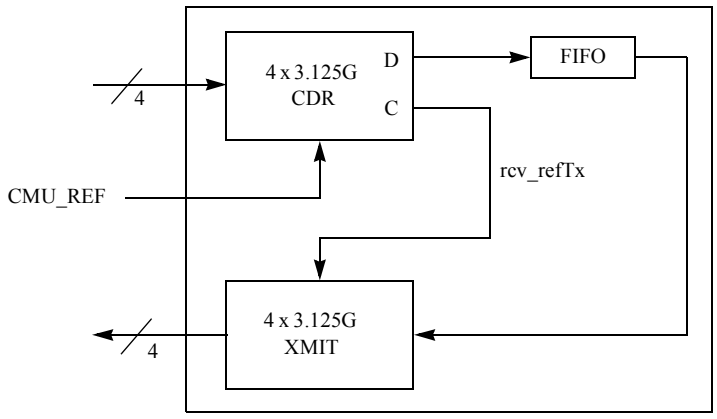


Figure 28. PHY XS System Loopback Clocking Configuration

10.2 Line Loopback Modes (HSRXDATA to HSTXDATA)

Two independent forms of line loopback are provided, providing flexibility regarding which AEL2005 device blocks will be incorporated into the loopback path. Each of these two paths involves routing the data from the high-speed receive pins (HSRXDATA) to the high-speed transmit pins (HSTXDATA). These paths are illustrated in Figure 29.

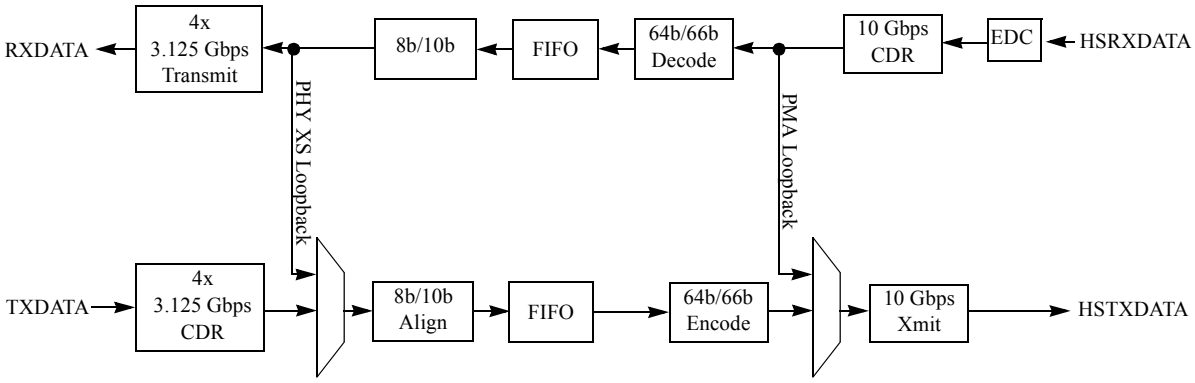


Figure 29. Line Loopback Modes

10.2.1 PMA Line Loopback

The PMA Line Loopback provides a shallow line loopback path. This path occurs at the 10 Gbps serial interface, immediately following the 10 Gbps CDR. The AEL2005 device is placed in this mode by setting bit 4 of the Mode Selection Register (address 1.C001) as shown in Table 88.

The loopback data will be propagated through the remainder of the receive data path as well as back along the loopback path when in PMA Line Loopback mode.

10.2.2 PHY XS Line Loopback

The PHY XS Line Loopback provides a deep line loopback path and is compliant with the PHY XS system loopback defined in IEEE 802.3ae, Clause 48.3.3. This path occurs at the XAUI interface of the AEL2005 device, and therefore includes the bulk of the AEL2005 digital logic. The AEL2005 device is placed in this mode by setting bit 14 of the PHY XS Control 1 register (address 4.0000) or bit 3 of the Optional Settings Register (address 1.C017) as shown in Table 52 and Table 102.

The loopback data will be propagated through the remainder of the receive data path as well as back along the loopback path when in PHY XS Line Loopback mode.

10.2.3 PMA Line Loopback Clocking Modes

In PMA Line Loopback mode, received 10 Gbps data is looped back onto the transmitter using the clocking approach shown in Figure 30. This ensures that the transmitter is run synchronously with the recovered clock. PHY XS Line Loopback makes use of CMU_REF as the general system reference clock.

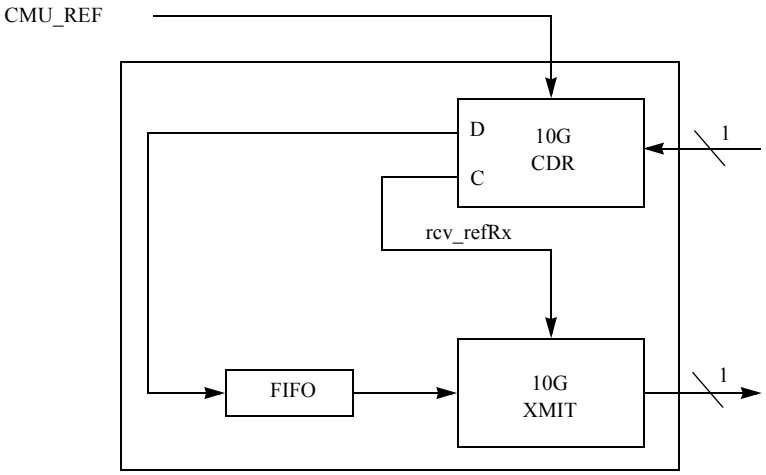


Figure 30. PMA Line Loopback Clocking

10.3 PRBS Pattern Generators and Checkers

The AEL2005 device includes PRBS pattern generators on the 10 Gbps and XAUI transmit outputs, and corresponding checkers at the 10 Gbps and XAUI receive inputs.

In the device transmit path, as shown in Figure 4, a 2-input Mux is used to select between a PRBS data pattern and TXDATA. The AEL2005 implements four PRBS modes on the 10 Gbps outputs, as selected in Table 103:

- prbs_mode0: $x^{23}+x^{18}+1$
- prbs_mode1: $x^{31}+x^{28}+1$
- prbs_mode2: transmit recirculate seed
- prbs_mode3: $x^{9}+x^{5}+1$

The AEL2005 also contains a PRBS checker in the 10 Gbps CML input, which implements the complementary check function to PRBS generation. This check is done on a bit-by-bit basis.

In the device receive path, as shown in Figure 4, a 2-input Mux is used to select between a PRBS data pattern and the receive data. The PRBS signal on the XAUI output can take any of the following forms as listed in Table 91.

- prbs_mode0: $x^{23}+x^{18}+1$
- prbs_mode1: $x^{31}+x^{28}+1$
- prbs_mode2: transmit recirculate seed
- prbs_mode3: $x^{9}+x^{5}+1$

The AEL2005 also contains a PRBS checker in the XAUI input, which implements the complementary check function to PRBS generation. This check is done on a bit-by-bit basis.

Note that the PRBS checkers will indicate 3 errors per single bit error in the pattern. This is compliant with IEEE 802.3ae, as described in section 49.2.12, and represents the bit error propagating through at each of the three taps within the PRBS pattern checker.

Also note that as with any Ethernet PHY, PRBS data will not successfully traverse the digital core of the device. This is a result of the lack of 8b/10b or 64b/66b encoding or ethernet packet-compliance of PRBS data. For implementation of tests that include the AEL2005 PCS layer, use an external Ethernet packet generator or the AEL2005 packet generators and checkers described in Section 10.4.

10.4 Internal Packet Generators and Checkers

The Puma AEL2005 device integrates on-board Ethernet and Fibre Channel packet generator and checker circuitry. A packet generator and checker pair is included in each of the receive (serial-to-parallel) and transmit (parallel-to-serial) directions. These circuits allow the user to verify the functionality of the AEL2005 device, or to generate Ethernet or Fibre Channel traffic for testing of other devices. The generator/checker pairs may also be used for production testing of optical modules that make use of the AEL2005 device.

The following 4 types of data can be generated by the AEL2005 packet generator

- Idle (a continuous stream of idles)
- CRPAT
- CJPAT
- Incremental - a programmable length of up to 2400 columns

The idle pattern and inter-packet gap can be configured to generate 10 Gbps Fibre Channel specific characters. The generator can be run in continuous mode, or can be configured to send up to 2^{16} packets and then stop.

The corresponding packet checker will display the following statistics. The 2 counters will saturate at 2^{16}-1.

- Number of packets received
- Number of corrupted packets
- Length of last packet received

Additional detail on this functionality is included in the descriptions to registers 1.C320-1.C33F, as shown in Table 125 and Table 126.

A block diagram of the AEL2005 device showing the pattern generator/checker pairs is shown in Figure 31.

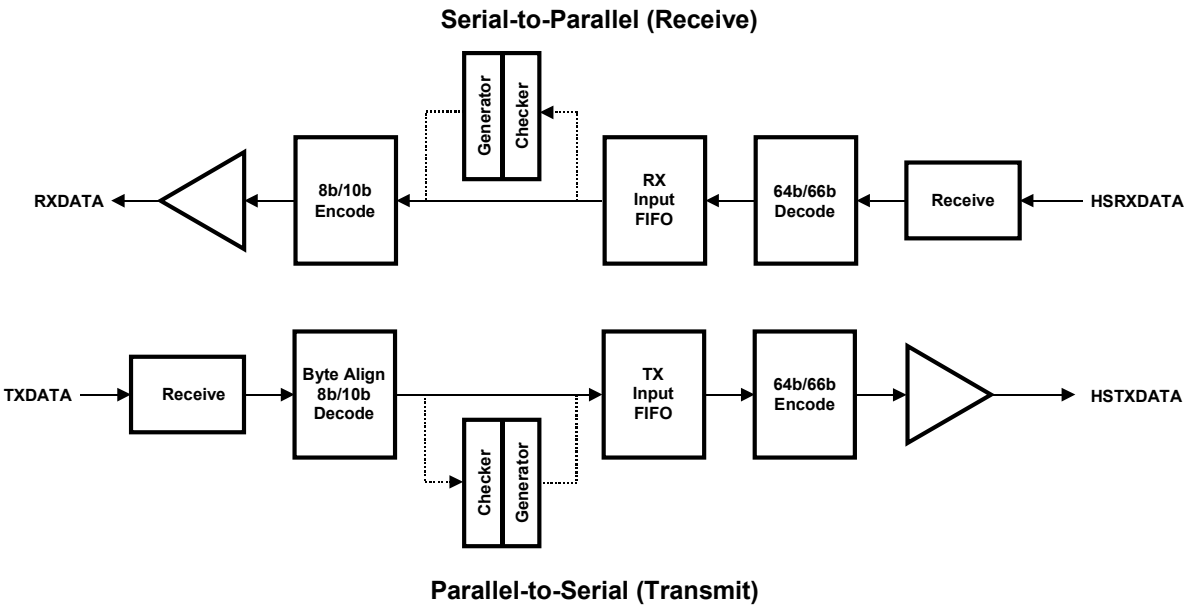


Figure 31. Packet Generator & Checker Locations

10.4.1 Configuring the Packet Generator

Serial-to-Parallel (Receive) Direction

Number of Packets. The pattern generator can be programmed in either of two ways; it can be set to generate a continuous stream of packets by writing 0x0000 to register 1.C320, or it can generate a burst of up to 65,536 packets by programming register 1.C320 with the integer N where N is the desired number of packets.

Packet Type. Programming bits 1.C323.13:12 will produce different types of packet streams, as shown in Table 10. Setting the generator to "Incrementing Payload" mode will result in a packet of fixed size having a payload that consists of 8-bit words cycling through all integer values from 0x00 to 0xFF.

Table 10. Packet Generator Modes for Receive Path

1.C323.13:12	Pattern
00	Idle
01	CRPAT
10	CJPAT
11	Incrementing Payload

Packet Size. If the packet type is set to "Incrementing Payload" then writing an integer M to 1.C32C.11:0 will result in a packet that has a length of M columns, or 4×(M) bytes. Note the packet size, as specified here, does not include the 8-byte pre-amble and start-of-frame delimiter and the 4-byte CRC.

IPG Length. The value written into 1.C32D.9:0 will set the length of the inter-packet gap (IPG) in columns (i.e. 4-byte groups). Therefore, setting 1.C32D.9:0 to P will result in 4×P bytes in the IPG, including the terminate column.

Note that the exact contents of the 8-byte preamble, source and destination addresees may be programmed using registers 1.C321-1.C323 and 1.C326-1.C32B. The exact contents of the terminate column may be programmed using

registers 1.C322-1.C323. The exact contents of the idle stream may be programmed using registers 1.C324-1.C325 and 1.C32C.

Parallel-to-Serial (Transmit) Direction

Number of Packets. The pattern generator can be programmed in of two ways; it can be set to generate a continuous stream of packets by writing 0x0000 to register 1.C330, or it can generate a burst of up to 65,536 packets by programming register 1.C330 with the integer N where N is the desired number of packets.

Packet Type. Programming 1.C333.13:12 will produce different types of packet streams, as shown in Table 11. Setting the generator to "Incrementing Payload" mode will result in a packet of fixed size having a payload that consists of 8-bit words cycling through all integer values from 0x00 to 0xFF..

Table 11. Packet Generator Modes for Transmit Path

1.C333.13:12	Pattern
00	Idle
01	CRPAT
10	CJPAT
11	Incrementing Payload

Packet Size. If the packet type is set to "Incrementing Payload" then writing an integer M to 1.C33C.11:0 will result in a packet that has a length of M columns, or 4×(M) bytes. Note the packet size, as specified here, does not include the 8-byte pre-amble and start-of-frame delimiter and the 4-byte CRC.

IPG Length. The value written into 1.C33D.9:0 will set the length of the inter-packet gap (IPG) in columns (i.e. 4-byte groups). Therefore setting 1.C33D.9:0 to P will result in 4×P bytes in the IPG, including the terminate column.

Note that the exact contents of the 8-byte preamble, source and destination addresses may be programmed using registers 1.C331-1.C333 and 1.C336- 1.C33B. The exact contents of the terminate column may be programmed using registers 1.C335-1.C336 and 1.C339. The exact contents of the idle stream may be programmed using registers 1.C337-1.C338 and 1.C339.

10.4.2 Initiating Packet Transmission

Serial-to-Parallel (Receive) Direction

If register 1.C320 is set to zero, the result will be a continuous stream of packets and IPGs. The pattern generator can then be activated by setting bit 1.C323.5 to 1.

If a fixed number of packets is to be sent, then bit 1.C323.5 should be set to 1 in order to arm the packet generator. This will initiate a preliminary packet burst, followed by a stream of idles. Subsequently, bit 1.C323.6 should be toggled from 0 to 1 or from 1 to 0 to initiate the actual generation of the desired packet burst.

Parallel-to-Serial (Transmit) Direction

If register 1.C330 is set to zero, the result will be a continuous stream of packets and IPGs. The pattern generator can then be activated by setting bit 1.C333.5 to 1.

If a fixed number of packets is to be sent, then bit 1.C333.5 should be set to 1 in order to arm the packet generator. This will initiate a preliminary packet burst, followed by a stream of idles. Subsequently, bit 1.C333.6 should be toggled from 0 to 1 or from 1 to 0 to initiate the actual generation of the desired packet burst.

10.4.3 Using the Checker

Serial-to-Parallel (Receive) Direction

Register 1.C32E counts the number of CRC errors, defined as the number of errored packets. Finally, the length, in columns, of the last packet received is recorded in 1.C32F. Note that while the packet length number does not include the 2-column pre-amble and start-of-frame delimiter, it does include the 1-column CRC.

These counters are cleared by setting 1.C323.4 to 1 to enable the checker. After a test has been run, the counters must be cleared by setting 1.C323.6 first to 0 and then to 1.

Note that clearing 1.C32F requires that register 1.C33F also be cleared.

Parallel-to-Serial (Transmit) Direction

Register 1.C33E counts the number of CRC errors, defined as the number of errored packets. Finally, the length, in columns, of the last packet received is recorded in 1.C33F. Note the packet length number does not include the 2-column pre-amble and start-of-frame delimiter but that it does include the 1-column CRC.

These counters are cleared by setting 1.C333.4 to 1 to enable the checker. After a test has been run, the counters must be cleared by setting 1.C333.6 to 0 and then to 1.

Note that clearing 1.C33F requires that register 1.C32F also be cleared.

10.4.4 Example Sequences of Operation

In this example, the AEL2005 device is configured as shown in Figure 32.

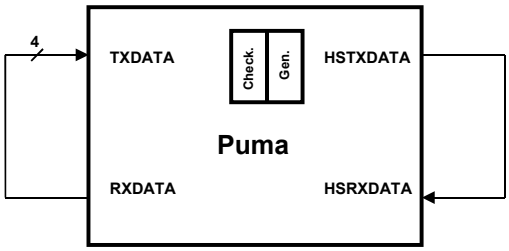


Figure 32. AEL2005 Example Configuration for Packet Generator & Checker Testing

Many variations on this basic configuration can be made. As an alternative example, a XAUI device may be placed in the XAUI loopback path in Figure 32. As yet another example, another 10 Gbps serial device may be placed in the 10 Gbps loopback path in Figure 32.

When running a test using both a packet generator and checker, the following sequence of register writes is suggested. As shown in Figure 32, the generator and checker in the transmit direction are used, and a fixed number of packets is to be sent and checked.

1. Configure packet generator mode, packet size, number of packets to be transmitted, and IPG length.
2. Arm the pattern generator by setting 1.C333.5 to 1.
3. Enable the checker by setting both 1.C323.4 and 1.C333.4 to 1.
4. Clear all counters by setting both 1.C323.6 and 1.C333.6 to 0 and then to 1.
5. Initiate the packet burst by toggling 1.C333.7 from 0 to 1 and then back to 0.
6. Check the pattern checker counters by reading the corresponding registers twice and verify that the transmitted burst was received by the checker.

10.4.5 CJPAT Generation

Another common configuration for the packet generators is for generation of the CJPAT pattern at the XAUI outputs. The appropriate steps to set the AEL2005 device to produce a continuous CJPAT signal are listed below:

1. Set register 1.C006.1:0 to 00 to ensure the device is not in PRBS mode.
2. Set register 1.C320.15:0 to 0x0000 to set the device for continuous packet generation.
3. Set register 1.C323.13:12 to enable CJPAT generation
4. Set register 1.C323.5 to 1 and then toggle 1.C323.7

11 MDIO Port

The Management Data Input Output (MDIO) port is used to configure the component, to exercise certain test modes, and to check the status of the device. This interface is consistent with IEEE 802.3ae clause 45. For more information on the MDIO interface, refer to IEEE 802.3ae, Clause 45.

Four transactions are supported:

- Address
- Write Data
- Read Data
- Read Data Increment

Figure 33 shows a representative MDIO transaction. Each transaction is 64 MDC clock cycles long and contains 32 cycles preamble, 2 cycles start of frame, 2 cycles op code, 5 cycles port address, 5 cycles device address, 2 cycles turnaround and 16 cycles of address/data.

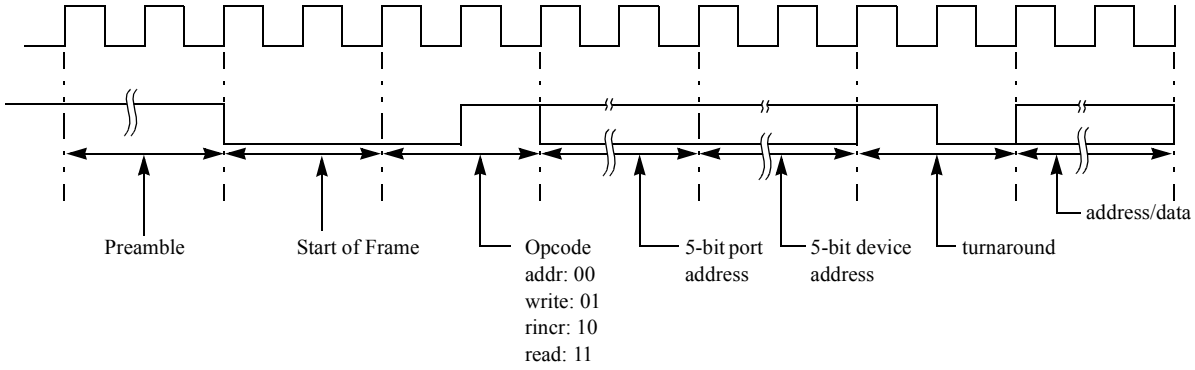


Figure 33. MDIO Transaction Format

11.1 MDIO Address Transaction

During every address transaction the register address is stored along with opcode, port address and device address. The MDIO PHY address is set equal to the value on the incoming MDIO pin. The AEL2005 supports MDIO device addresses 1, 3, and 4.

11.2 MDIO Write Transaction

During a write MDIO transaction, as soon as the write data is received and stored into the 16 bits of the status register, a one-shot transaction follows where the data is written to the address specified in the status register.

11.3 MDIO Read Transaction

During a read MDIO transaction, once the port address is received, the MDIO logic does a one-shot transaction where it reads the data from the location specified in the status register. This falls into the Hi-z part of the turnaround cycles. Once the turnaround is complete, the MMD (MDIO logic) will drive the MDIO bus with data from the status register.

11.4 MDIO Read Increment Transaction

This transaction is similar to the read transaction except that subsequent address transactions are skipped. Once the address is stored (first transaction), the MMD will keep incrementing the address in the status register when it sees the opcode for a read increment. After that point it is a read operation as described above.

12 SDA/SCL Interface

The SDA/SCL interface is used for communication with an external general purpose EEPROM. The SDA/SCL is a 2-pin industry standard bus consisting of a clock pin (SCL) and a bidirectional data pin (SDA). The AEL2005 supports up to a 100 kHz clock rate.

As with MDIO, this serial interface has open drain drivers and an external pullup resistor. However, it has a higher input threshold because it is intended to communicate with 2.5V and 3.3V devices. The SDA line must be connected to a positive supply by a pull-up resistor located on the bus. The AEL2005 contains a Schmitt input on both the SDA and SCL signals.

12.1 Configuration

The XENPAK specification contains a mapping table showing the correspondence between MDIO registers addresses and bytes in the serial EEPROM . On the rising edge of RESET_N, such as occurs at device start-up, the AEL2005 reads this entire EEPROM and writes its contents into the XENPAK register set. The EEPROM device address is hard-wired to be 1010000. CMU_REF must be running for the interface to operate properly.

12.2 Update via Control/Status Register

The entire register map can be re-read from the EEPROM or written back into the EEPROM using the NVR Control Status register (MDIO address 1.8000) defined in the XENPAK specification. The AEL2005 reads the EEPROM and writes the MDIO registers when bit 5 is set to 0. The AEL2005 reads the MDIO register contents and writes them out to EEPROM when bit 5 is set to 1. Due to the long access times for the EEPROM, it will take many MDIO clock cycles to complete this transaction. The status of an access is indicated in bits 3:2. See the register descriptions for more details on the Control/Status register.

12.3 Reading Optical Monitoring Information

The serial bus is also used to read in optical monitoring information, as described in the Digital Optical Monitoring (DOM) section of the Version 3.0 XENPAK specification. DOM information is stored in a second serial device on the SDA/SCL bus. The serial address of this device is 1010 for the four most significant bits and field 2:0 of MDIO register 1.807A for the three least significant bits. The DOM Control/Status register (MDIO address 1.A100) controls this update. See the description for the DOM Control/Status register Table 80 on page 70 for more details.

12.4 Format for Serial Bus Operations

The AEL2005 always operates as a master on the SDA/SCL bus. As a master device, the AEL2005 drives the clock line SCL and generates read and write requests using SDA. A valid read or write sequence is a series of the three different symbol types shown in Figure 34. A falling edge on SDA when SCL is high indicates the start of a transaction. A rising edge of SDA when SCL is high shows where a transaction ends. For data bits, SDA is held constant the entire time SCL is high. An acknowledgment is indicated by a steady low level on SDA when SCL is high. Setup, hold, and pulse width timings for SDA and SCL can be found in Table 139 on page 105.

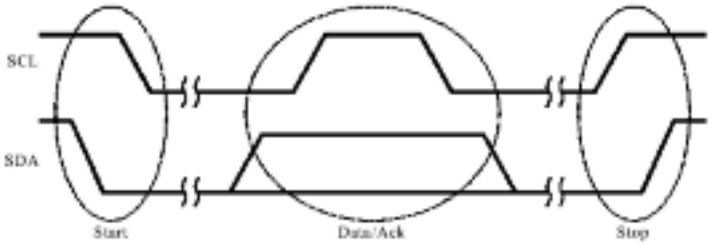


Figure 34. SDA/SCL Serial Bus Symbols

12.5 EEPROM Read and Write

The AEL2005 uses the serial read and sequential write operations supported by the EEPROM and optical monitor devices. The serial read sequence is shown in Figure 35. The AEL2005 first sets the access address to 0 using a dummy write operation, then sequentially reads through the entire memory and loads the values into the corresponding MDIO registers. If updates are pending for both the main and optical monitoring register sets, the AEL2005 will queue the later arriving request until the prior one has completed.

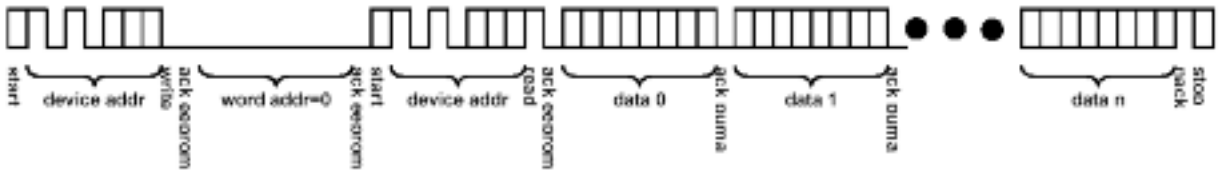


Figure 35. EEPROM Serial Read

The eight byte page write sequence used by the AEL2005 is shown in Figure 36. After the 1010000 device address, the AEL2005 sends the address of the first byte in the page to be written, followed by eight bytes of data and the stop symbol. When the EEPROM receives the stop symbol, it begins its internal erase/program cycle, which takes up to 10ms to complete. The AEL2005 repeats this sequence for every page in the device, waiting at least 10ms between writes to ensure that the previous transaction has finished.

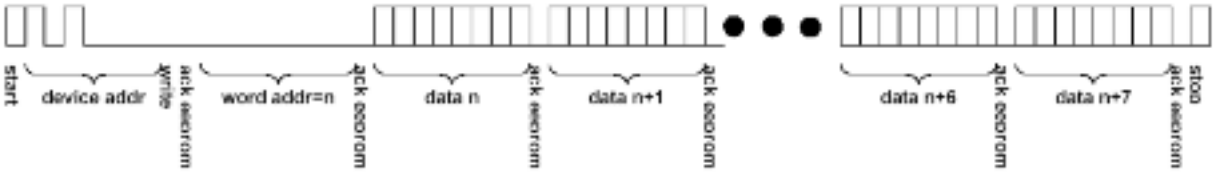


Figure 36. EEPROM Page Write Sequence

12.6 Multi-master Operation and Arbitration

The AEL2005 can share the serial bus with other master devices. To accommodate this, it only starts a transaction when the bus is idle and it obeys rules for clock synchronization and arbitration. Waiting for the bus to be idle solves

most contention problems, but the serial protocol must still deal with the case where two or more masters attempt to start a transaction simultaneously.

Figure 37 shows how two or more master devices cooperate to produce a valid clock. Since the SCL driver is open drain, it will be zero whenever one or more masters pull it low. The minimum low time of the bus is automatically satisfied because it is greater than or equal to the minimum low time that any single device produces.

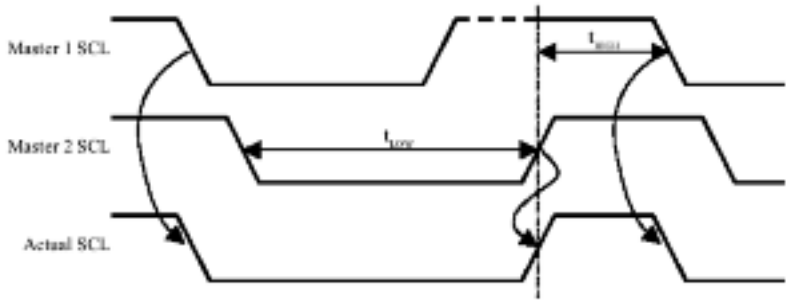


Figure 37. Clock Synchronization on the SDA/SCL Serial Bus

Producing a minimum valid high time requires additional work on the part of the master. When a master releases the clock, it waits to begin counting off the high time until it actually sees SCL go high. This prevents creation of a truncated high pulse where the rising edge is set by the latest master releasing SCL and the falling edge by the earliest master pulling it low again.

Since only one transaction can complete on the bus at a time, the protocol must have provisions for deciding which master gets to use the bus when there is contention. The arbitration protocol is shown in Figure 38. Each master drives its preferred bit pattern on the SDA line. Since the SDA driver is open drain, the actual SDA value will be the wired-AND of the individual values. At the rising and falling edges of SCL, each master compares the actual value on SDA with the value it drove; if they differ, that master abandons its operation and retries when the bus is idle again. As long as two masters are driving the same bit pattern on the bus, this arbitration process will continue for multiple bit times. In the special case that they are both trying to send the exact same pattern, arbitration never completes; both complete their operation successfully.

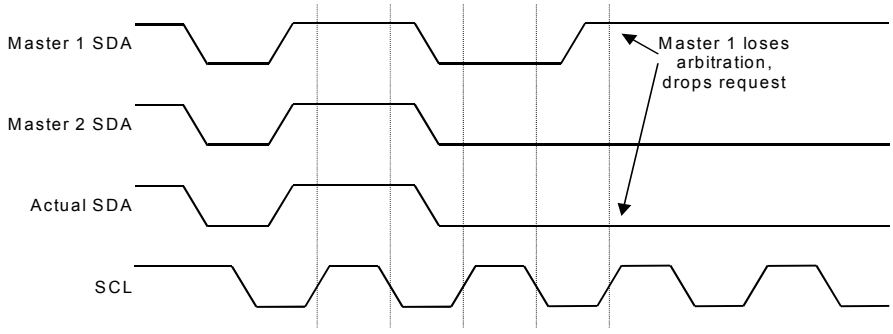


Figure 38. Arbitration on the SDA/SCL Serial Bus

12.7 4Kb Serial EEPROM Support

In addition to support for the 256x8 serial EEPROM required by the XENPAK MSA, the AEL2005 device can support larger, 512x8, serial EEPROMs. This additional space is typically used to store a temperature to output current modulation table, or to provide additional register patch space. The AEL2005 device automatically

determines whether there is an EEPROM in the system, and if so, what its size is, upon initial attempts to read the device. The results of this initial read operation are reflected in register 1.C20F, as described in Table 119.

12.8 SDA/SCL Byte-by-Byte Operations

The AEL2005 device supports byte-by-byte read and write operations to any address on the SDA/SCL bus through register-based commands initiated through the MDIO interface. The registers associated with these operations are highlighted in Table 123. An example SDA/SCL operation, used to set register 0x41 within the device at SDA/SCL address 0xA4 to 0x3F is outlined below:

- Set 1.C30B to 0x003F - This operation specifies the desired data (0x3F)
- Set 1.C30A to 0xA441 - This operations simultaneously sets the device address to 0xA4 (bits 15:9, padded by an extra '0'), the address within the device to 0x41 (bits 7:0), and initiates a write command (bit 8 set to 0)

Verification of this value can be done through the following commands:

- Set 1.C30A to 0xA541 - This operation sets the device address and word address as per the previous command, but initiates a read command instead of a write command (bit 8 set to 1)
- Read register 1.C30B.15:8 - This register will contain the value read from the SDA/SCL bus.

Register 1.C30C, bits 1:0, can also be used to monitor the success or failure of this SDA/SCL operation.

Register 1.C30C, bits 1:0, can also be used to monitor the success or failure of this SDA/SCL operation. These bits will reflect the status of the last SDA/SCL operation, and will not change or clear until a new operation is performed.

12.9 EEPROM-Based Patching Support

The AEL2005 register set definition includes support for a 256-byte non-volatile memory (NVR), implemented via EEPROM, and as described in Table 67. Within this 256-byte space, 89 bytes are dedicated to vendor specific utilization, from which the AEL2005 device uses 16 bytes for initialization-time configuration updates to internal registers between 1.C001 and 1.C07F. This permits an optical module to initialize using a set of vendor-specified configuration settings to ensure support for individual requirements and modifications to the default AEL2005 configuration, simply by modifying the contents of the in-module EEPROM.

The AEL2005 configuration update is initiated at reset from EEPROM on the part of the AEL2005 device.

The 16 bytes associated with AEL2005 device configuration update support are split into 8 distinct pairs, each able to modify half the bits within a single register in the 1.C001 - 1.C07F register space. Within each address pair, the odd address allocates bits 6:0 to designate the offset from 1.C000, and bit 7 to designate whether the high order byte or low order byte should be modified. The subsequent even address is used to contain the new data intended for the identified register.

An example setting for these 16 bytes is shown in Table 12. In this case, the first patch operation modifies register 1.C001, in this case to set bit 1, RXDATA_transpose, and bit 0, TXDATA_transpose, in order to transpose the XAUI receive and transmit lanes, as may be required based upon a particular board design. The following two patch operations are used to apply maximum pre-emphasis to all four XAUI RXDATA lanes, as controlled in register 1.C00B. Finally, the 4th patch operation is used to remove the PCS receive fault condition from the PHY XS receive fault detection circuit, as controlled by register 1.C017. In this last case, bit 15 is disabled, and the default setting for the high order byte in register 1.C017 of 0xFE is therefore changed to 0x7E. The remaining odd addresses are set to 0x00, thus indicating a lack of patch update.

Table 12. Example Register Settings for Patch Support

Address	Low/High Order Byte	Offset	Address	Data	Result
1.80C7	0	0x1F	1.80C8	0x03	Set register 1.C001[7:0] to 0x03
1.80C9	0	0x0B	1.80CA	0xFF	Set register 1.C00B[7:0] to 0xFF
1.80CB	1	0x0B	1.80CC	0x0F	Set register 1.C00B[15:8] to 0x0F
1.80CD	1	0x17	1.80CE	0x7E	Set register 1.C017[15:8] to 0x7E
1.80CF	0	0x00	1.80D0	0x00	No update
1.80D1	0	0x00	1.80D2	0x00	No update
1.80D3	0	0x00	1.80D4	0x00	No update
1.80D5	0	0x00	1.80D6	0x00	No update

This configuration update capability provides a powerful and flexible tool to optical module designers working with the AEL2005 device to customize boot-up operation to meet their particular needs. In this way, modifications typically applied via MDIO operations can be managed at a module level, simplifying module utilization by the end system customer.

When a 4kb EEPROM is used, as described in Section 12.7, an additional 128 bytes of EEPROM patch space are provided, as reflected with the AEL2005 device in addresses 1.C480 through 1.C4FF.

Unused registers in the EEPROM patching space should be set to 0x00 so as to avoid unintentional modifications to the AEL2005 device registers.

13 SPI Interface

The Serial Peripheral Interface (SPI) port provides external access to the adaptation and offset cancellation control registers, and allows observation of statistics necessary for optionally performing offset cancellation and adaptation using an external micro-controller. This interface is compatible with that which is used in many popular microprocessors and serial EEPROMs.

13.1 SPI Operations

The AEL2005 SPI port supports three types of operations.

- Enable / disable operations involving zero bytes of data
- Read / write operations involving exactly one byte of data, and
- Read / write operations involving a 16-bit address and one or more bytes of data.

Figure 39 shows a timing diagram for each type of supported SPI operations. AEL2005 samples SI on the rising edge of SCLK, and drives SO off the falling edge of SCLK.

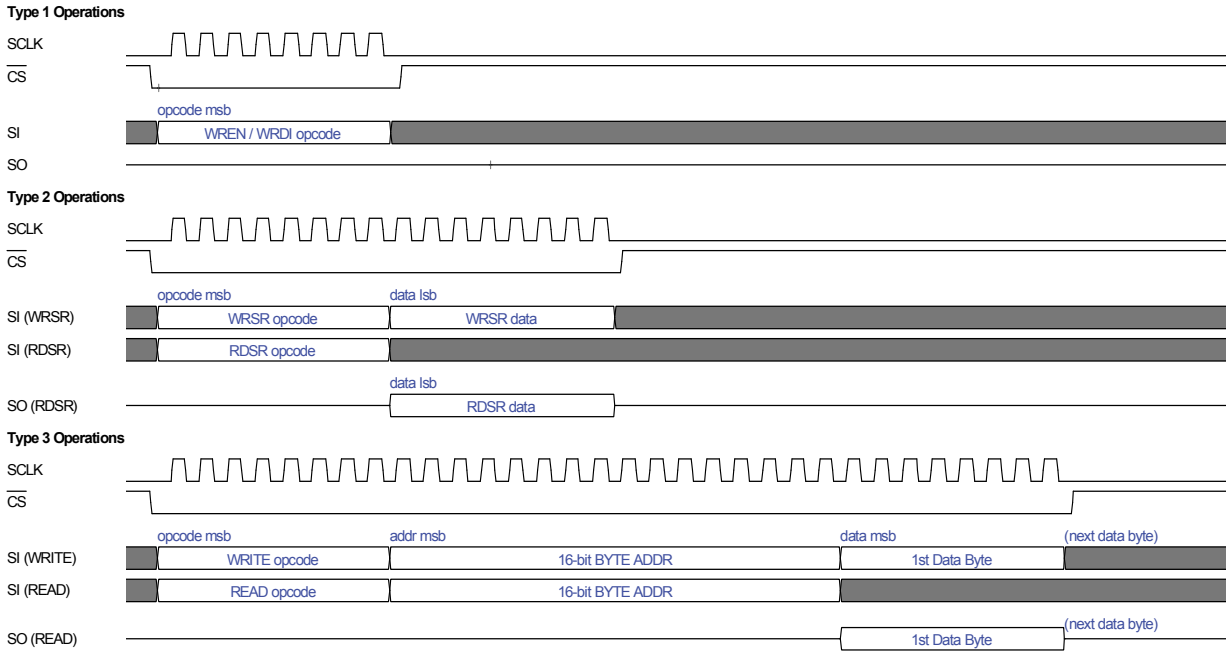


Figure 39. SPI Operations

13.2 SPI Instructions

The SPI instructions supported by AEL2005 are listed below.

Table 13. SPI Instructions

Instruction	Opcode	Operation	Type
WREN	0000_x110	Write Enable	1
WRDI	0000_x100	Write Disable	1
WRSR	0000_x001	Write Status Register	2
RDSR	0000_x101	Read Status Register	2
WRITE BYTE	0000_0010	Write One Byte	3
WRITE WORD	0000_1010	Write 16 Bits Atomically	3
READ BYTE	0000_0011	Read One Byte	3
READ WORD	0000_1011	Read 16 Bits Atomically	3

The SPI port is disabled for write operations upon chip power-on, and must be enabled using the WREN instruction before the first write operation is issued. The port may subsequently be disabled for write again using the WRDI instruction.

The WRSR and RDSR instructions are used to write and read the SPI port status register, which has the format shown below. Bits 0 and 1 of the status register are read-only bits.

Table 14. SPI Status Register

Bits	Description	Type
7:3	Reserved	RW
2	Address Page Select	RW
1	Write - Enabled	RO
0	Busy	RO

Two pages of SPI registers, each consisting of 32768 double-bytes, can be addressed by the AEL2005 SPI port. Page 0 contains double-bytes at address 0x0000 - 0x7FFF, while page 1 contains 0x8000 - 0xFFFF. These are the same addresses used by the MDIO port. The WRSR instruction is used to select one of these two pages to be accessed. Writing a 0 into bit 2 of the SPI port status register selects page 0, while writing a 1 selects page 1.

A 16-bit byte address (the top 15 bits of which corresponds to the lower 15 bit of the above-mentioned double-byte address) within the selected page is shifted in through SI for type 3 operations. Auto address increment is supported, such that multiple bytes within a contiguous address range can be written using a single WRITE instruction without intervening address phases, as long as CS_B is asserted. If the address is auto-incremented beyond the highest address within the selected page, it rolls over to the starting address of the given page (ie. 0xFFFF rolls over to 0x8000).

The AEL2005 SPI port allows data to be written either one byte at a time, or a double-byte at a time atomically. Using the WRITE BYTE instruction, each byte is written into the selected SPI register as soon as it is shifted in via SI. However, when the WRITE WORD opcode is used, the low byte within the given address is written at the same time as the high byte, after both have been shifted in via SI. Similarly, the READ BYTE instruction is used to read out the registers one byte at a time, while the READ WORD opcode captures an entire double-byte atomically, before

shifting the bits via SO. To provide this atomic access behavior, the WRITE WORD and READ WORD instructions expect an even-valued 16-bit byte address from SI.

13.3 Example SPI Operation

As an example, the following sequence of SPI operations may be used to write the high byte at address C508.

1. **WREN** - *Enable write, if this is the first access after power on.*
2. **WRSR [bit 2 = 1]** - *Select page 1 (C508 is in page 1), if page 1 is not already selected.*
3. **WRITE BYTE [byte addr = 8A11] [data]** - *8A11 is derived from the following operation.*

   ((C508 << 1) & FFFF) | 0x0001, where 0x0001 selects the high byte

All SPI - accessible registers are also accessible via the MDIO port, using the same double-byte addresses. However, concurrent accesses to the same address using both ports is not supported.

14 Pin Descriptions

Table 15 describes the pins of the AEL2005 device.

Table 15. AEL2005 Pin Descriptions

Pin Name	BGA Pin	I/O	Description
Clock Interface			
CMU_REF_P CMU_REF_N	P6,N6	I	156.25, 159.375MHz reference clock inputs. This is the clock reference for the AEL2005 device. If unused, connect one pin to GND with a 820 Ω resistor while connecting the other to 1.2V via a 300Ω resistor.
ALT_CMU_REF_P ALT_CMU_REF_N	P8,N8	I	50 MHz reference clock inputs. This is the clock reference for the AEL2005 device. If unused, connect one pin to GND with a 820 Ω resistor while connecting the other to 1.2V via a 300Ω resistor.
High Speed CML Interface			
HSRXDATA_P HSRXDATA_N	C14,D14	I	CML receive channel. The data rate on this channel is nominally 10.3125 Gbps for 10GBASE-R, and 10.51875 Gbps for 10G Fibre Channel.
HSTXDATA_P HSTXDATA_N	G14,H14	O	CML transmit channel. The data rate on this channel is nominally 10.3125 Gbps for 10GBASE-R, and 10.51875 Gbps for 10G Fibre Channel.
HSTXCLK_P HSTXCLK_N	K14,L14	O	CML transmit clock. The output transmit clock is used to allow retiming of data at the laser driver. This clock can also be used to trigger high-speed test equipment. This clock is disabled by default to save power, and should be left unconnected if not in use.
XAUI Interface			
RXDATA_P[3:0] RXDATA_N[3:0]	F3,E2,D3,C2 F4,E1,D4,C1	O	XAUI parallel output data. Data from the high speed CML receive pins (HSRXDATA) is de-serialized to four XAUI channels. RXDATA has a nominal data rate 3.125 Gbps for XAUI and 3.1875 Gbps for Fibre Channel.
TXDATA_P[3:0] TXDATA_N[3:0]	K3,J2,H3,G2 K4,J1,H4,G1	I	XAUI parallel input data. Data from these four XAUI channels is driven onto the high speed CML transmit pins (HSTXDATA). TXDATA has a nominal data rate of 3.125 Gbps for XAUI and 3.1875 for Fibre Channel.
General Control and Configuration Signals (CMOS)			
CDR_LOL	B5	O	Receive CDR loss of lock. Active high open drain output.
CMU_LOL	B4	O	Transmit CMU loss of lock. Active high open drain output.
LASI_N	A2	O	Active low, open drain link alarm status interrupt. Active high open drain output.
LOS_OUT	A4	O	Receive loss of signal detection. Assertion of this pin indicates that a receive loss of signal was detected during normal operation. Active high open drain output.
PRTAD[4:0]	C11,B12,A12, B11,A10	I	Port address for MDIO interface. These pins are 1.2V CMOS compatible, and active high.
RESET_N	B3	I	Active low reset pin. Assertion of this pin by external logic resets the AEL2005 device, and is reflected in the reset register bits in 1.0000, 3.0000 and 4.0000.

Table 15. AEL2005 Pin Descriptions (Continued)

Pin Name	BGA Pin	I/O	Description
TX_ON	P1	I	High-speed data transmission enable. Powers down the output driver when low. Also enables XENPAK LPS mode.
TX_DISABLE	N2	O	High-speed data transmission disable output. Asserted as per register 1.C012 to reflect the logical OR of the contents of register 1.0009.0 and the inverse of the TX_ON pin. Used to turn off downstream transmitter elements in the event of a transmission disable request. Open drain output. Pull low to VSS if not in use.
RX_LOS	L1	I	External receive loss of signal. Used to receive a fault signal from an upstream device in the receive path. Logic low indicates LOS. Polarity can be inverted via register 1.C017. Pull high to 1.2-V or 2.5-V if not in use.
TX_FAULT	M1	I	External transmit fault. Used to receive a fault signal from an upstream device in the transmit path. Logic high indicates a transmit fault. Polarity can be inverted via register 1.C017. Pull low to VSS if not in use.
EEPROM_PROTECT	P11	I	EEPROM write protect pin. Prevents EEPROM write operations to nonvolatile register space addresses other than addresses 119 to 166 (1.807E-1.80AD) when high. Pull to VSS if not in use.
GPIO	N11	I/O	General Purpose IO signal
MODDET	N13	I	SFP+ module detect. 1 indicates the module is detached and 0 indicates that the module is attached
SGMII Interface Signals			
RSFP1P, RSFP1N	N14 ,P14	I	Second port on SGMII data pins. Run as a standard 100 ohm differential pair
MDIO Interface Signals			
MDC	M4	I	MDIO clock input, compatible with IEEE 802.3ae, Clause 45
MDIO	N4	I/O	MDIO data port, compatible with IEEE 802.3ae, Clause 45. Open drain.
SPI Interface Signals			
CS_B	M7	I	SPI Chip Select
SCLK	P3	I	SPI Clock Input
SI	L6	I	SPI Data Input
SO	P4	O	SPI Data Output
SDA/SCL Interface Signals			
SCL	P2	O	SDA/SCL interface clock. Open drain. Always connect to pull-up resistor.
SDA	N3	I/O	SDA/SCL interface bidirectional data pin. Open drain. Always connect to pull-up resistor.
Configuration Resistor Signals			
BIASR	P12	I	External bias resistor. The AEL2005 requires one external resistor to be connected between BIASR and VSS, and has a nominal resistance of 11.8kΩ
JTAG Signals (CMOS)			
TCK	N10	I	JTAG test clock. Pull to VSS if not in use.
TDI	P9	I	JTAG test data in. Pull to VSS if not in use. Active high.

Table 15. AEL2005 Pin Descriptions (Continued)

Pin Name	BGA Pin	I/O	Description
TDO	N9	O	JTAG test data out. Open drain output. Active high.
TMS	P10	I	JTAG test mode select. Pull to VDD if not in use. Active high.
TRST	M9	I	JTAG test reset. Pull to VSS if not in use. Active low.
Power and Ground Signals			
VDD	See Figure 59	I	1.2V supply.
VDDH	See Figure 59	I	3.3V supply.
VSS	See Figure 59	I	Ground.
Other Pins			
RSRV1, RSRV2, RSRV3, RSRV9	M10, B9, A8, P13	-	These pins are reserved and should be left unconnected.

15 Registers

The AEL2005 supports portions of the IEEE 802.3ae Clause 45, 10 Gigabit Ethernet register specification and the XENPAK Multisource Agreement, Revision 3.0. In addition to these standard registers, the AEL2005 includes additional registers for device configuration and debug. The entire register set is described in this section.

In the description of each register field, there is an entry describing its write-ability. This can contain the following:

- R/W - register field is read/write
- RO - register field is read only
- LL - Latching Low - Used with bits that monitor some state internal to the AEL2005. When the condition for the bit to go low is reached, the bit stays low until the next time it is read. Once it is read, its value reverts to the current state of the condition it monitors.
- LH - Latching High - When the condition for the bit to go high is reached, the bit stays high until the next time it is read. Once it is read, its value reverts to the current state of the condition it monitors.
- SC - Writable and self clearing. A write to an SC register may trigger certain actions within the chip. The value of the register subsequently reverts automatically to its reset value after a certain condition within the chip is met.
- NR - Non Rollover - Counter is saturating.
- RGS - register is read only, and serves as the snapshot trigger point for the read group with an address range that most closely follows the given RGS address.
- RG - register is read only, and is part of a read group. A read group is defined as all of the RG registers located between two consecutive RGS register addresses, or between the final RGS address and the end of available valid registers. The value of a RG register is updated only when a corresponding RGS register is read. All RG registers within the same read group are updated atomically, i.e. a "snapshot" is taken for the entire group.
- WGC - register is read / write, and serves as the commit trigger point for the write group with an address range that most closely precedes the given WGC address.
- WG - register is read / write, and is part of a write group. A write group is defined as all of the WG registers located between two consecutive WGC register addresses, or between the beginning of available valid registers and the first WGC address. The value written to a WG address is held temporarily in a shadow memory, and is only transferred to the proper register when the corresponding WGC register is written. All dirty WG registers within the same write group are updated atomically, i.e. a "commit" action is performed for the entire group.

15.1 Register Overview

The AEL2005 supports the IEEE 802.3ae Clause 45 register set for MDIO Manageable Device (MMD) addresses 1 (PMA/PMD), 3 (PCS), and 4 (PHY XS). A summary of these registers is shown in Table 16. In these tables, the number to the left of the decimal point indicates the MDIO device address. The 4-digit number to the right of the decimal point indicates the 16-bit register address.

Table 16. PMA/PMD, PCS and PHY XS Registers

Register Address (hex)	Register Name
1.0000	PMA/PMD control 1
1.0001	PMA/PMD status 1
1.0002,1.0003	PMA/PMD device identifier
1.0004	PMA/PMD speed ability
1.0005, 1.0006	PMA/PMD devices in package
1.0007	10G PMA/PMD control 2
1.0008	10G PMA/PMD status 2
1.0009	10G PMA/PMD transmit disable
1.000A	10G PMA/PMD receive signal detect

Table 16. PMA/PMD, PCS and PHY XS Registers (Continued)

Register Address (hex)	Register Name
1.000B	10G PMA/PMD extended ability
1.000E, 1.000F	10G PMA/PMD package identifier
3.0000	PCS control 1
3.0001	PCS status 1
3.0002, 3.0003	PCS device identifier
3.0004	PCS speed ability
3.0005, 3.0006	PCS devices in package
3.0007	10G PCS control 2
3.0008	10G PCS status 2
3.000E, 3.000F	PCS package identifier
3.0018	10GBASE-X PCS Status
3.0019	10GBASE-X PCS Test Control
3.0020	10GBASE-R PCS status 1
3.0021	10GBASE-R PCS status 2
3.0022, 3.0023, 3.0024, 3.0025	10GBASE-R PCS test pattern seed A
3.0026, 3.0027, 3.0028, 3.0029	10GBASE-R PCS test pattern seed B
3.002A	10GBASE-R PCS test pattern control
3.002B	10GBASE-R PCS test pattern error counter
3.C000	PCS system loopback control
4.0000	PHY XS control 1
4.0001	PHY XS status 1
4.0002, 4.0003	PHY XS device identifier
4.0004	PHY XS speed ability
4.0005, 4.0006	PHY XS devices in package
4.0008	PHY XS status 2
4.000E, 4.000F	PHY XS package identifier
4.0018	PHY XS lane status
4.0019	PHY XS 10GBASE-X test control
4.C000	PHY XS system loopback control

In addition to the standards specific registers, the AEL2005 also implements the XENPAK-specific MDIO registers, many of which are uploaded from one or more serial devices on the SDA/SCL bus. Table 17 shows a list of these registers and the corresponding serial address mapping. For the serial address, the value to the left of the period is the device address and the value to the right is the byte number. The device address "M" is formed by concatenating the serial EEPROM prefix "1010" with bits 2:0 in the *Digital Optical Monitoring Capability Byte* register (1.807A) and a trailing “0”. In all these registers, only the lower eight bits are used and backed up; the upper bytes are ignored.

Reads and writes to the serial device at address A0 that backs up the base XENPAK register set are controlled by the NVR Control/Status Register (1.8000). Updates from the Digital Optical Monitoring Device at serial address "M" are controlled by the *Digital Optical Monitoring Control/Status* Register (1.A100).

Table 17. XENPAK Register Set

Register Address (hex)	Serial Address (hex)	Register Name
1.8000		NVR Control/Status
1.8007 - 1.8079	A0.0-A0.72	XENPAK Register Set

Table 17. XENPAK Register Set (Continued)

Register Address (hex)	Serial Address (hex)	Register Name
1.807A	A0.73	Digital Optical Monitoring Capability Byte
1.807B-1.807C	A0.74-A0.75	Optional
1.807D	A0.76	Basic Field Checksum
1.807E-1.80AD	A0.77-A0.A6	Customer Writeable Area
1.80AE-1.80C6	A0.A7-A0.BF	Vendor Specific
1.80C7-1.80D6	A0.C0-A0.CF	AEL2005 Configuration Updates
1.80D7-1.8106	A0.D0-A0.FF	Vendor Specific
1.9000		RX_ALARM Control
1.9001		TX_ALARM Control
1.9002		LASI Control
1.9003		RX_ALARM Status
1.9004		TX_ALARM Status
1.9005		LASI Status
1.9006		TX_FLAG Control
1.9007		RX_FLAG Control
1.A000-1.A001	M.00-M.01	Transceiver Temp High Alarm
1.A002-1.A003	M.02-M.03	Transceiver Temp Low Alarm
1.A004-1.A005	M.04-M.05	Transceiver Temp High Warning
1.A006-1.A007	M.06-M.07	Transceiver Temp Low Warning
1.A008-1.A00F		Reserved
1.A010-1.A011	M.10-M.11	Laser Bias High Alarm
1.A012-1.A013	M.12-M.13	Laser Bias Low Alarm
1.A014-1.A015	M.14-M.15	Laser Bias High Warning
1.A016-1.A017	M.16-M.17	Laser Bias Low Warning
1.A018-1.A019	M.18-M.19	Laser Output Power High Alarm
1.A01A-1.A01B	M.1A-M.1B	Laser Output Power Low Alarm
1.A01C-1.A01D	M.1C-M.1D	Laser Output Power High Warning
1.A01E-1.A01F	M.1E-M.1F	Laser Output Power Low Warning
1.A020-1.A021	M.20-M.21	Receive Optical Power High Alarm
1.A022-1.A023	M.22-M.23	Receive Optical Power Low Alarm
1.A024-1.A025	M.24-M.25	Receive Optical Power High Warning
1.A026-1.A027	M.26-M.27	Receive Optical Power Low Warning
1.A028-1.A047	M.28-M.47	Reserved
1.A048-1.A05F		Reserved
1.A060-1.A061	M.60-M.61	Transceiver Temp
1.A062-1.A063		Reserved
1.A064-1.A065	M.64-M.65	Laser Bias Current
1.A066-1.A067	M.66-M.67	Laser Output Power
1.A068-1.A069	M.68-M.69	Receive Optical Power
1.A06A-1.A06D	M.6A-M.6D	Reserved
1.A06E		DOM Status Bits

Table 17. XENPAK Register Set (Continued)

Register Address (hex)	Serial Address (hex)	Register Name
1.A06F	M.6F [7:1]	Extended DOM Capability
1.A070		TX_FLAG Status
1.A071		RX_FLAG Status
1.A072-1.A073	M.72-M.73	Reserved
1.A074		TX_FLAG Status 2
1.A075		RX_FLAG Status 2
1.A076-1.A0BF	M.76-M.BF	Reserved
1.A0C0-1.A0FF		Reserved
1.A100		DOM Control/Status

The AEL2005 device implements those registers corresponding to DOM addresses as shown in Table 17. For read & write support of other locations within a DOM device, make use of the byte-by-byte operation described in Section 12.8 is recommended.

The AEL2005 device-specific registers are shown in Table 18.

Table 18. AEL2005 Device Specific Registers

Register Address (hex)	Register Name
1.C001	Mode Selection Register
1.C002	Transmit Configuration Register 1
1.C003	Receive Configuration Register
1.C005	Reserved
1.C006 - 1.C007	XAUI Configuration Registers
1.C008 - 1.C00A	Reserved
1.C00B - 1.C00C	XAUI Transmit Registers
1.C00D - 1.C00E	Reserved
1.C00F	Power Supply Sensing Threshold Register
1.C010	LOS Mask Register
1.C011	Powerdown Control Register
1.C012	TX_DISABLE Register
1.C013	Reserved
1.C014	Tx [re-emphasis Enable Register
1.C015	Tx Pre-emphasis Register
1.C016	Rate Adjustment Configuration Register
1.C017	Optional Settings Register
1.C018	Transmit Configuration Register 2
1.C019	Fault Mask Register
1.C01A - 1.C01D	Reserved
1.C01E	10 Gbps Output Swing Register
1.C01F	SGMII Configuration Register.
1.C020 - 1.C02A	Reserved
1.C02B	Transmit Rise Time Control Register
1.C02C - 1.C049	Reserved
1.C04A	Embedded micro-controller Configuration Register

Table 18. AEL2005 Device Specific Registers (Continued)

Register Address (hex)	Register Name
1.C04B	Embedded micro-controller EEPROM Register
1.C04C - 1.C079	Reserved
1.C07A	Override Register 1
1.C07B	Override Register 2
1.C07C - 1.C07E	DOM Update Limit Registers
1.C07F - 1.C1FF	Reserved
1.C200 - 1.C201	Transmit Seed for PRBS Generators
1.C202 - 1.C203	Logic Configuration Registers
1.C204 - 1.C20B	Reserved
1.C20C	Logic Configuration Register
1.C20D	SGMII Configuration Register
1.C20E	Reserved
1.C20F	Checksum Verification Register
1.C210 - 1.C213	Reserved
1.C214 - 1.C215	GPIO and LED Traffic Registers
1.C216 - 1.C219	LED Acticity Truth Table Registers
1.C217 - 1.C21F	Reserved
1.C220	Un-retimed SGMII Register
1.C221 - 1.C2FF	Reserved
1.C30A - 1.C30D	SDA/SCL Read/Write Registers
1.C30E - 1.C30F	Reserved
1.C310 - 1.C313	BER Counter Registers
1.C314 - 1.C319	Reserved
1.C320 - 1.C33F	Pattern Generator Registers
1.C340 - 1.C3FF	Reserved
1.C400 - 1.C4FF	4kb EEPROM Registers
1.C500 - 1.C5AF	Reserved
1.C5B0	Error Slicer Threshold Register
1.C5B1 - 1.C61F	Reserved
1.C620 - 1.C626	Initial / Override FFE Registers
1.C627 - 1.C62C	Initial / Override DFE Registers
1.C62D -1.C638	Adaptation Observation Registers
1.C639 - 1.C83F	Reserved
1.C840 - 1.C843	AGCP Parameter Registers
1.C844 - 1.C9FF	Reserved
1.CA00, 1.CA12, 1.CA13, 1.CA1C, 1.CA1E	Micro-controller control / status registers

15.2 PMA/PMD Registers

Setting the low power bit will power down the device and drop overall power consumption to under 30 mW. The AEL2005 device will exit power down mode in the same state it was in prior to asserting the low power bit. A reset request will take precedence over a powerdown request.

Table 19. PMA/PMD Control 1 Register (MDIO Device Address = 1, Register Address = 0x0000)

Bit(s)	Name	R/W	Default	Description
15	Reset	R/W	0	Setting to 1 resets chip. Self clearing upon completion of chip reset.
14	Reserved	RO	X	
13	Speed Selection	RO	1	Must be set to 1.
12	Reserved	RO	X	
11	Low Power Mode	R/W	0	1 = Power down all circuits except those needed for MDIO operation 0 = Normal operation
10:7	Reserved	RO	X	
6:2	Speed selection	RO	10000	Must be set to the default value of 10000.
1	Reserved	RO	X	
0	PMA System Loopback	R/W	0	1 = Enable PMA System Loopback 0 = Disable PMA System Loopback

Table 20 shows the fields for the PMA/PMD status 1 register. Receive Link Status is set to 0 whenever loss of signal (LOS_OUT) is asserted and features the same conditions as the PMA/PMD Receive Fault signal in register 1.0008.10

Table 20. PMA/PMD Status 1 Register (MDIO Device Address = 1, Register Address = 0x0001)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	PMA/PMD Fault	RO	0	1 = Fault detected. 0 = No fault detected. Fault is logical OR of 1.0008.11 and 1.0008.10
6:3	Reserved	RO	X	
2	PMA/PMD Receive Link Status	RO/LL	1	1 = PMA/PMD Receive Link Up. 0 = PMA/PMD Receive Link Down.
1	Low Power Ability	RO	1	Always returns 1.
0	Reserved	RO	X	

15.3 PMA/PMD Registers

The PMA/PMD device identifier contains the transceiver vendor OUI as read from an external EEPROM into addresses 1.8039-8036.

Table 21. PMA/PMD Device Identifier Upper 16 Bits (MDIO Device Address = 1, Register Address = 0x0002)

Bit(s)	Name	R/W	Default	Description
15:0	PMA/PMD Identifier	RO	0x0000	Returns contents of 1.8036-8037

Table 22. PMA/PMD Device Identifier Lower 16 Bits (MDIO Device Address = 1, Register Address = 0x0003)

Bit(s)	Name	R/W	Default	Description
15:0	PMA/PMD Identifier	RO	0x0000	Returns contents of 1.8038-8039

The PMA/PMD Speed Ability and Devices in Package registers describe the capabilities and contents of the parts. Both these fields have fixed values.

Table 23. PMA/PMD Speed Ability (MDIO Device Address = 1, Register Address = 0x0004)

Bit(s)	Name	R/W	Default	Description
15:1	Reserved	RO	X	
0	10G Capable	RO	1	Returns 1.

Table 24. PMA/PMD Devices in Package: Upper 16 Bits (MDIO Device Address = 1, Register Address = 0x0005)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	DTE XS present	RO	0	Returns 0.
4	Phy XS present	RO	1	Returns 1.
3	PCS present	RO	1	Returns 1.
2	WIS present	RO	0	Returns 0.
1	PMA/PMD present	RO	1	Returns 1.
0	Clause 22 register present	RO	0	Returns 0.

Table 25. PMA/PMD Devices in Package: Lower 16 Bits (MDIO Device Address = 1, Register Address = 0x0006)

Bit(s)	Name	R/W	Default	Description
15:14	Vendor-specific device present	RO	0	Returns 00.
13:0	Reserved	RO	X	

The 10G PMA/PMD control 2 register sets the type of PMA/PMD in use. This register is interpreted from XENPAK register D.8018. If the value contained in the NVR register is invalid, the PMA/PMD Type value will default to ‘110. If the value of 1.C001.10 (LAN_Only_register) is 1, then bit 2 will always be 0. Any changes in the value of bit 2 will also be reflected in register 2.0007, bit 0 and 3.0007, bit 1, and any changes in those bits will be reflected in this bit.

Table 26. 10G PMA/PMD Control 2 Register (MDIO Device Address = 1, Register Address = 0x0007)

Bit(s)	Name	R/W	Default	Description
15:4	Reserved	RO	X	
3 2 1:0	PMA/PMD Type	RO R/W RO	1000	1 0 0 0 = 10GBASE-LRM PMA/PMD type[1] 0 1 1 1 = 10GBASE-SR PMA/PMD type 0 1 1 0 = 10GBASE-LR PMA/PMD type 0 1 0 1 = 10GBASE-ER PMA/PMD type 0 1 0 0 = Reserved 0 0 1 1 = Reserved 0 0 1 0 = Reserved 0 0 0 1 = Reserved 0 0 0 0 = Reserved.

1. The 10GBASE-LRM PMA/PMD type code in 1.0007.3:0 can be turned off by setting register bit 1.C07B bit 12 in the Override Register 2 to 0.

Table 27 shows the PMA/PMD status 2 register. The different reach capabilities are copied into this register from the corresponding values in XENPAK register D.8018. Certain inputs to the transmit and receive faults are masked by default through the Fault Mask Register located at 1.C019 and the Optional Settings Register located at 1.C017.

Table 27. 10G PMA/PMD Status 2 Register (MDIO Device Address = 1, Register Address = 0x0008)

Bit(s)	Name	R/W	Default	Description
15:14	Device Present	RO	10	Returns 10.
13	Transmit fault ability	RO	1	Returns 1.
12	Receive fault ability	RO	1	Returns 1.
11	Transmit Fault	RO/LH	0	Returns the logical OR of TX_FAULT pin, the 10G CMU loss of lock signal, PCS transmit fault and PHY XS transmit fault, as controlled by 1.C017.
10	Receive Fault	RO/LH	0	Returns the logical OR of the RX_LOS pin, the internal LOS signal, the 10G CMU loss of lock, and the 10G CDR loss of lock, as controlled by 1.C017.
9	Reserved	RO	X	
8	PMD Transmit disable ability	RO	1	Returns 1.
7	10GBASE-SR ability	RO	--	1 = 10GBASE-SR capable. 0 = not 10GBASE-SR capable. Set equal to XENPAK 1.8018.0.
6	10GBASE-LR ability	RO	--	1 = 10GBASE-LR capable. 0 = not 10GBASE-LR capable. Set equal to XENPAK 1.8018.1
5	10GBASE-ER ability	RO	--	1 = 10GBASE-ER capable. 0 = not 10GBASE-ER capable. Set equal to XENPAK 1.8018.2.
4	10GBASE-LX4 ability	RO	0	Returns 0.
3	10GBASE-SW ability	RO	0	1 = 10GBASE-SW capable. 0 = not 10GBASE-SW capable. Set equal to XENPAK 1.8018.0.
2	10GBASE-LW ability	RO	0	1 = 10GBASE-LW capable. 0 = not 10GBASE-LW capable. Set equal to XENPAK 1.8018.1
1	10GBASE-EW ability	RO	0	1 = 10GBASE-EW capable. 0 = not 10GBASE-EW capable. Set equal to XENPAK 1.8018.2.
0	PMA Loopback ability	RO	1	Returns 1.

The AEL2005 transmit disable function and TX_DISABLE pin are the logical OR of the inverse of the TX_ON pin and this Global PMA/PMD Transmit Disable function.

Table 28. 10G PMA/PMD Transmit Disable Register (MDIO Device Address = 1, Register Address = 0x0009)

Bit(s)	Name	R/W	Default	Description
15:1	Reserved	RO	X	
0	Global PMA/PMD Transmit Disable	R/W	0	1 = Disable Transmitter 0 = Enable Transmitter

The AEL2005 returns the logical AND of the complement of its Loss of Signal (LOS_OUT) output and the RX_LOS pin as PMA/PMD Receive Signal Detect. Either item is maskable through the Fault Mask Register located at 1.C019

Table 29. 10G PMA/PMD Receive Signal Detect Register (MDIO Device Address = 1, Register Address = 0x000A)

Bit(s)	Name	R/W	Default	Description
15:1	Reserved	RO	X	
0	PMA/PMD Receive Signal Detect	RO	1	1 = Signal detected on receive. 0 = Signal not detected on receive.

Table 30. 10G PMA/PMD Receive Signal Detect Register (MDIO Device Address = 1, Register Address = 0x000B)

Bit(s)	Name	R/W	Default	Description
15:2	Reserved	RO	X	
1	10 GBASE-LRM ability	RO	1	1 = 10 GBASE-LRM is supported[1] 0 = 10 GBASE-LRM is not supported
0	10 GBASE-LX4 ability	RO	0	Returns 0

1. 10 GBASE-LRM support can be turned off if register bit 1.C07B bit 12 in Override Register 2 is set to 0.

The AEL2005 uses device 1 (PMA/PMD) for the XENPAK registers; the PMA/PMD package identifier returns the value read from the external EEPROM registers 43-46 and MDIO registers 1.8032 - 1.8035.

Table 31. PMA/PMD Package Identifier: Upper 16 Bits (MDIO Device Address = 1, Register Address = 0x000E)

Bit(s)	Name	R/W	Default	Description
15:0	PMA/PMD Package Identifier	RO	0x0000	Returns the upper 16-bits of the PMA/PMD package identifier.

Table 32. PMA/PMD Package Identifier: Lower 16 Bits (MDIO Device Address = 1, Register Address = 0x000F)

Bit(s)	Name	R/W	Default	Description
15:0	PMA/PMD Package Identifier	RO	0x0000	Returns the lower 16-bits of the PMA/PMD package identifier.

15.4 PCS Registers

Table 33 shows the fields in the PCS control 1 register.

Table 33. PCS Control 1 Register (MDIO Device Address = 3, Register Address = 0x0000)

Bit(s)	Name	R/W	Default	Description
15	Reset	R/W	0	Setting to 1 resets chip. Self clearing.
14	PCS System Loopback	R/W	0	1 = Enables PCS System Loopback. 0 = Disable PCS System Loopback.
13	Speed Selection	RO	1	Must be set to 1.
12	Reserved	RO	X	
11	Low Power	R/W	0	1 = Power down loopbacks, CMU's, transmit, and receive. 0 = Normal operation.
10:7	Reserved	RO	X	
6:2	Speed selection	RO	10000	Must be set to the default value of 10000.
1:0	Reserved	RO	X	

Table 34 shows the fields for the PCS status 1 register.

Table 34. PCS Status 1 Register (MDIO Device Address = 3, Register Address = 0x0001)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	PCS Fault	RO	0	1 = Fault detected. 0 = No fault detected. Fault is logical OR of 3.0008.11 and 3.0008.10
6:3	Reserved	RO	X	
2	PCS Receive Link Status	RO/LL	1	1 = PCS Receive Link Up. 0 = PCS Receive Link Down.
1	Low Power Ability	RO	1	Always returns 1.
0	Reserved	RO	X	

The PCS device identifier registers are identical to their PMA/PMD counterparts.

Table 35. PCS Device Identifier Upper 16 Bits (MDIO Device Address = 3, Register Address = 0x0002)

Bit(s)	Name	R/W	Default	Description
15:0	PCS Identifier	RO	0x0000	Returns contents of 1.8036-8037

Table 36. PCS Device Identifier Lower 16 Bits (MDIO Device Address = 3, Register Address = 0x0003)

Bit(s)	Name	R/W	Default	Description
15:0	PCS Identifier	RO	0x0000	Returns contents of 1.8038-8039.

The PCS Speed Ability and Devices in Package registers are identical to the PMA/PMD versions.

Table 37. PCS Speed Ability (MDIO Device Address = 3, Register Address = 0x0004)

Bit(s)	Name	R/W	Default	Description
15:1	Reserved	RO	X	
0	10G Capable	RO	1	Returns 1.

Table 38. PCS Devices in Package: Upper 16 Bits (MDIO Device Address = 3, Register Address = 0x0005)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	DTE XS present	RO	0	Returns 0.
4	Phy XS present	RO	1	Returns 1.
3	PCS present	RO	1	Returns 1.
2	WIS present	RO	0	Returns 0.
1	PMA/PMD present	RO	1	Returns 1.
0	Clause 22 register present	RO	0	Returns 0.

Table 39. PCS Devices in Package Lower: 16 Bits (MDIO Device Address = 3, Register Address = 0x0006)

Bit(s)	Name	R/W	Default	Description
15:14	Vendor specific device present	RO	00	Returns 00.
13:0	Reserved	RO	X	

Any changes in the value of register 3.0007, bit 1 will also be reflected in register 1.0007, bit 2 and 2.0007, bit 0, and any changes in those bits will be reflected in this bit.

Table 40. 10G PCS Control 2 Register (MDIO Device Address = 3, Register Address = 0x0007)

Bit(s)	Name	R/W	Default	Description
15:2	Reserved	RO	X	
1	PCS Type	R/W	0	Indicates 10GBASE-R
0	Reserved	RO	X	

Table 41 shows the PCS Status 2 register. The fault bits are asserted whenever the PCS layer detects a fault. Certain inputs to the transmit and receive faults are masked by default through the Fault Mask Register located at 1.C019 and the Optional Settings Register located at 1.C017.

Table 41. 10G PCS Status 2 Register (MDIO Device Address = 3, Register Address = 0x0008)

Bit(s)	Name	R/W	Default	Description
15:14	Device Present	RO	10	Returns 10.
13:12	Reserved	RO	X	
11	Transmit Fault	RO/LH	0	Returns the logical OR of the value of the E2O elastic FIFO error signal and the PHY XS Transmit Fault, as controlled by 1.C017.

Table 41. 10G PCS Status 2 Register (MDIO Device Address = 3, Register Address = 0x0008)

Bit(s)	Name	R/W	Default	Description
10	Receive Fault	RO/LH	0	Returns the logical OR of the O2E elastic FIFO error signal, the inverse of the 10GBASE-R block lock signal, the 10GBASE-R PCS high BER, and the PMA Receive Fault, as controlled by 1.C017.
9:3	Reserved	RO	X	
2	10GBASE-W capable	RO	0	Returns 0.
1	10GBASE-X capable	RO	0	Returns 0.
0	10GBASE-R capable	RO	1	Returns 1.

The PCS Package Identifier returns 0, as the XENPAK register set uses device address 1.

Table 42. PCS Package Identifier Upper: 16 Bits (MDIO Device Address = 3, Register Address = 0x000E)

Bit(s)	Name	R/W	Default	Description
15:0	PCS Package Identifier	RO	0x0000	Returns 0.

Table 43. PCS Package Identifier Lower: 16 Bits (MDIO Device Address = 3, Register Address = 0x000F)

Bit(s)	Name	R/W	Default	Description
15:0	PCS Package Identifier	RO	0x0000	Returns 0.

Since the AEL2005 does not support 10GBASE-X, the corresponding status and test control registers are all 0's.

Table 44. 10GBASE-X PCS Status (MDIO Device Address = 3, Register Address = 0x0018)

Bit(s)	Name	R/W	Default	Description
15:0	Reserved	RO	X	

Table 45. 10GBASE-X PCS Test Control (MDIO Device Address = 3, Register Address = 0x0019)

Bit(s)	Name	R/W	Default	Description
15:0	Reserved	RO	X	

The 10GBASE-R status registers allow readout of some internal variables from the PCS finite state machine. See Clause 49 of the IEEE 802.3ae specification for details. The 10GBASE-R receive link status register reflects the logical AND of the inverse of the 10GBASE-R PCS high BER register and the 10GBASE-R block lock register.

Table 46. 10GBASE-R PCS Status 1 (MDIO Device Address = 3, Register Address = 0x0020)

Bit(s)	Name	R/W	Default	Description
15:13	Reserved	RO	X	
12	10GBASE-R receive link status	RO	0	1 = 10GBASE-R receive link up. 0 = 10GBASE-R receive link down.
11:4	Reserved	RO	X	
3	PRBS9 pattern testing ability	RO	1	Returns 1
2	PRBS31 pattern testing ability	RO	1	Returns 1.

Table 46. 10GBASE-R PCS Status 1 (MDIO Device Address = 3, Register Address = 0x0020)

Bit(s)	Name	R/W	Default	Description
1	10GBASE-R PCS high BER	RO	0	1 = 10GBASE-R reporting a high BER. 0 = 10GBASE-R not reporting a high BER.
0	10GBASE-R block lock	RO	0	1 = 10GBASE-R locked to receive blocks. 0 = 10GBASE-R not locked to receive blocks.

Table 47. 10GBASE-R PCS Status 2 (MDIO Device Address = 3, Register Address = 0x0021)

Bit(s)	Name	R/W	Default	Description
15	Latched block lock	RO/LL	0	1 = 10GBASE-R locked to receive blocks. 0 = 10GBASE-R not locked to receive blocks.
14	Latched high BER	RO/LH	0	1 = 10GBASE-R reporting a high BER. 0 = 10GBASE-R not reporting a high BER.
13:8	BER	RO	0	BER counter.[1]
7:0	Error block counter	RO	0x00	Error block counter.[1]

1. These counters will saturate at their maximum value and not roll over to 0.

The eight PCS test pattern and test pattern control registers are used to implement and activate the test modes described in the IEEE 802.3ae specification. See clause 49 for details. This PRBS31 test pattern is inverted as specified by the IEEE802.3ae specification. The square wave test pattern consists of 8 1's followed by 8 0's.

Table 48. 10GBASE-R Test Patterns (MDIO Device Address = 3)

Register Address	Bit(s)	Name	R/W	Default	Description
0x0025	15:10	Reserved	RO	X	
	9:0	Test Pattern Seed A 3	R/W	2AA	Test pattern seed A bits 48:57
0x0024	15:0	Test Pattern Seed A 2	R/W	AAAA	Test pattern seed A bits 32:47
0x0023	15:0	Test Pattern Seed A 1	R/W	AAAA	Test pattern seed A bits 16:31
0x0022	15:0	Test Pattern Seed A 0	R/W	AAAA	Test pattern seed A bits 0:15
0x0029	15:10	Reserved	RO	X	
	9:0	Test Pattern Seed B 3	R/W	2AA	Test pattern seed B bits 48:57
0x0028	15:0	Test Pattern Seed B 2	R/W	AAAA	Test pattern seed B bits 32:47
0x0027	15:0	Test Pattern Seed B 1	R/W	AAAA	Test pattern seed B bits 16:31
0x0026	15:0	Test Pattern Seed B 0	R/W	AAAA	Test pattern seed B bits 0:15

Table 49. 10GBASE-R PCS Test Pattern Control (MDIO Device Address = 3, Register Address = 0x002A)

Bit(s)	Name	R/W	Default	Description
15:7	Reserved	RO	X	
6	PRBS9 transmit pattern enable	R/W	0	1 = Enable PRBS9 transmit pattern mode. 0 = Disable PRBS9 transmit pattern mode.
5	PRBS31 receive pattern enable	R/W	0	1 = Enable PRBS31 receive pattern mode. 0 = Disable PRBS31 receive pattern mode.
4	PRBS31 transmit pattern enable	R/W	0	1 = Enable PRBS31 transmit pattern mode. 0 = Disable PRBS31 transmit pattern mode.
3	Transmit test pattern enable	R/W	0	1 = Enable transmit test pattern testing. 0 = Disable transmit test pattern testing.
2	Receive test pattern enable	R/W	0	1 = Enable receive test pattern testing. 0 = Disable receive test pattern testing.
1	Test pattern select	R/W	0	1 = Square wave test pattern. 0 = Pseudo random test pattern.
0	Data pattern select	R/W	0	1 = Zeros data pattern. 0 = LF data pattern.

Table 50. 10GBASE-R PCS Test Pattern Error Counter (MDIO Device Address = 3, Register Address = 0x002B)

Bit(s)	Name	R/W	Default	Description
15:0	Test pattern error counter	RO	000	Test pattern error counter.

Table 51. PCS System Loopback Control (MDIO Device Address = 3, Register Address = 0xC000)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	PCS System Loopback Selection	R/W	0	0 = Send 00FF Uncoded 1 = Send Transmit Data from XAUI
4:0	Reserved	RO	X	

15.5 PHY XS Registers

The PHY XS registers contain control and status information for the XAUI links.

Table 52. PHY XS Control 1 Register (MDIO Device Address = 4, Register Address = 0x0000)

Bit(s)	Name	R/W	Default	Description
15	Reset	R/W	0	Setting to 1 resets chip. Self clearing.
14	PHY XS Line Loopback	R/W	0	1 = Enables PHY XS Line Loopback. 0 = Disables PHY XS Line Loopback.
13	Speed Selection	RO	1	Must be set to 1.
12	Reserved	RO	X	
11	Low Power	R/W	0	1 = Power down loopbacks, CMU's, transmit, and receive. 0 = Normal operation.
10:7	Reserved	RO	X	
6:2	Speed selection	RO	10000	Must be set to the default value of 10000.
1:0	Reserved	RO	X	

Table 53 shows the fields for the PHY XS status 1 register. Only the PHY XS Fault and PCS Receive Link Status field are active. These reflect the state of fault bits at addresses 4.0008.10, 4.0008.11 and 4.0018.12, respectively.

Table 53. PHY XS Status 1 Register (MDIO Device Address = 4, Register Address = 0x0001)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	PHY XS Fault	RO	0	1 = Fault detected. 0 = No fault detected. Fault is logical OR of 4.0008.11 and 4.0008.10
6:3	Reserved	RO	X	
2	PHY XS Transmit Link Status	RO/LL	1	1 = PHY XS transmit link up. 0 = PHY XS transmit link down.
1	Low Power Ability	RO	1	Always returns 1.
0	Reserved	RO	X	

The PHY XS device identifier registers are identical to their PMA/PMD counterparts.

Table 54. PHY XS Device Identifier: Upper 16 Bits (MDIO Device Address = 4, Register Address = 0x0002)

Bit(s)	Name	R/W	Default	Description
15:0	PHY XS Identifier	RO	0x0000	Returns contents of 1.8036-8037

Table 55. PHY XS Device Identifier: Lower 16 Bits (MDIO Device Address = 4, Register Address = 0x0003)

Bit(s)	Name	R/W	Default	Description
15:0	PHY XS Identifier	RO	0x0000	Returns contents of 1.8038-8039

The PHY XS Speed Ability and Devices in Package registers are identical to the PMA/PMD versions.

Table 56. PHY XS Speed Ability (MDIO Device Address = 4, Register Address = 0x0004)

Bit(s)	Name	R/W	Default	Description
15:1	Reserved	RO	X	
0	10G capable	RO	1	Returns 1.

Table 57. PHY XS Devices in Package: Upper 16 Bits (MDIO Device Address = 4, Register Address = 0x0005)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	DTE XS present	RO	0	Returns 0.
4	Phy XS present	RO	1	Returns 1.
3	PCS present	RO	1	Returns 1.
2	WIS present	RO	0	Returns 0.
1	PMA/PMD present	RO	1	Returns 1.
0	Clause 22 register present	RO	0	Returns 0.

Table 58. PHY XS Devices in Package Lower: 16 Bits (MDIO Device Address = 4, Register Address = 0x0006)

Bit(s)	Name	R/W	Default	Description
15:14	Vendor specific device present	RO	00	Returns 00.
13:0	Reserved	RO	X	

Table 59 shows the status 2 register. The fault bits are asserted whenever the PHY XS layer detects a fault. Certain inputs to the transmit and receive faults are masked by default through the Fault Mask Register located at 1.C019 and the Optional Settings Register located at 1.C017.

Table 59. PHY XS Status 2 Register (MDIO Device Address = 4, Register Address = 0x0008)

Bit(s)	Name	R/W	Default	Description
15:14	Device Present	RO	10	Returns 10.
13:12	Reserved	RO	X	
11	Transmit Fault	RO/LH	0	Returns the logical OR of E2O elastic FIFO error signal and the XAUI lane deskew error signal, as controlled by 1.C017.
10	Receive Fault	RO/LH	0	Returns the logical OR of the O2E elastic FIFO error signal, the PMA/PMD Receive Fault, and the PCS Receive Fault, as controlled by 1.C017.
9:0	Reserved	RO	X	

The PHY XS Package Identifier returns 0, as the XENPAK register set uses device address 1.

Table 60. PHY XS Package Identifier: Upper 16 Bits (MDIO Device Address = 4, Register Address = 0x000E)

Bit(s)	Name	R/W	Default	Description
15:0	PHY XS Package Identifier	RO	0x0000	Returns 0.

Table 61. PHY XS Package Identifier Lower: 16 Bits (MDIO Device Address = 4, Register Address = 0x000F)

Bit(s)	Name	R/W	Default	Description
15:0	PHY XS Package Identifier	RO	0x0000	Returns 0.

The PHY XS status register is shown in Table 62. The lane synchronization fields indicate whether the four individual 8b/10b decoders have synchronized to the incoming data stream. The lane alignment status indicates that the relative alignment of the system receive channels has been determined.

Table 62. PHY XS Lane Status (MDIO Device Address = 4, Register Address = 0x0018)

Bit(s)	Name	R/W	Default	Description
15:13	Reserved	RO	X	
12	PHY XS Lane Alignment Status	RO	0	1 = Transmit lanes aligned. 0 = Transmit lanes not aligned.
11	Pattern testing ability	RO	1	Returns 1.
10	System Loopback Ability	RO	1	Device is capable of system loopback.
9:4	Reserved	RO	X	
3	Lane 3 Sync	RO	0	1 = Lane synchronized. 0 = Lane not synchronized.

Table 62. PHY XS Lane Status (MDIO Device Address = 4, Register Address = 0x0018) (Continued)

Bit(s)	Name	R/W	Default	Description
2	Lane 2 Sync	RO	0	1 = Lane synchronized. 0 = Lane not synchronized.
1	Lane 1 Sync	RO	0	1 = Lane synchronized. 0 = Lane not synchronized.
0	Lane 0 Sync	RO	0	1 = Lane synchronized. 0 = Lane not synchronized.

Table 63. 10GBASE-X PHY XS Test Control (MDIO Device Address = 4, Register Address = 0x0019)

Bit(s)	Name	R/W	Default	Description
15:3	Reserved	RO	X	
2	Transmit test pattern enable	RW	0	1 = Receive test pattern enabled. 0 = Receive test pattern not enabled.
1:0	Test Pattern Select	RW	00	11 = Reserved. 10 = Mixed frequency test pattern. 01 = Low frequency test pattern. 00 = High frequency test pattern.

PHY XS System Loopback can be controlled via register 4.C000.

Table 64. PHY XS System Loopback Control (MDIO Device Address = 4, Register Address = 0xC000)

Bit(s)	Name	R/W	Default	Description
15	PHY XS System Loopback Selection	R/W	0	PHY XS system loopback 10G Selection 1 = Send transmit data from XAUI 0 = Send all 0's unscrambled
14	PHY XS System Loopback Enable	R/W	0	1 = Enable loopback 0 = Disable loopback
13:0	Reserved	RO	X	

15.6 XENPAK Registers

This section describes the register set specific to XENPAK. These registers fall into three categories: base nonvolatile registers, Link Alarm Status Interrupt (LASI), and Digital Optical Monitoring.

15.6.1 XENPAK Nonvolatile Registers

Update of non-volatile registers is controlled by the NVR Control/Status register, shown in Table 65. An NVR read is implemented upon reset. Subsequently, a write to this register that sets bit 5 to 0 and bits 1:0 to 11 will cause MDIO registers 1.8007 to 1.8106 to be re-read from the external serial device over the SDA/SCL bus. A write to this register that sets bit 5 to 1 and bits 1:0 to 11 will cause the external serial device at address 0xA0 to be overwritten with the values stored in MDIO registers 1.8007 to 1.8106. The status of a read or write operation is indicated in bits 3:2. During an EEPROM write/read NVR operation, MDIO writes and reads to the NVR memory via the MDIO interface are not permitted.

When the EEPROM_PROTECT pin is asserted, write operations to NVR addresses other than addresses 119 to 166 (1.807E-1.80AD) are prohibited.

The low power initialization bit is set by the module manufacturer, and causes no operation within the AEL2005.

Table 65. NVR Control/Status Register (MDIO Device Address = 1, Register Address = 0x8000)

Bit(s)	Name	R/W	Default	Description
15:9	Reserved	RO	X	
8	Low power initialization	RO	0	Always 0
7:6	Reserved	RO	X	
5	Command	R/W	0	0 = read NVR. 1 = write NVR.
4	Reserved	RO	X	Returns 0.
3:2	Command Status	RO/LH	00	00 = Idle. 01 = Command completed successfully. 10 = Command in progress. 11 = Command failed.
1:0	Extended Command	R/W	11	11 = R/W all NVR contents.

XENPAK registers 1.8007 through 1.8079 and the customer area registers 1.807E through 1.80AD are read from and written to the corresponding registers in the serial EEPROM. The only function of the AEL2005 with these registers is to make them available via the MDIO port.

The basic field checksum is stored in 1.807D. The AEL2005 does not calculate or check this value; it only transfers the value between MDIO and the serial EEPROM.

In the table below, the bit column for the first entry is interpreted as follows:

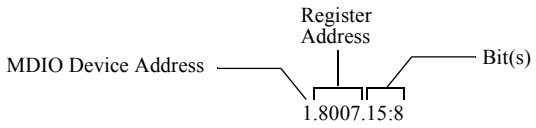


Table 66. XENPAK Registers

Bit(s)	Name	R/W	Default	Description
1.8007.15:8 - 1.8079.15:8	Reserved	RO	X	Unused upper byte.
1.8007.7:0 - 1.8079.7:0	XENPAK NVR	R/W[1]	X	Corresponds to bytes A0.0-A0.72 in serial EEPROM.
1.807A	DOM Capability	RO	X	See Table 80
1.807B.15:8 1.807C.15:8	Reserved	RO	X	Unused upper byte.
1.807B.7:0 1.807C.7:0	Optional Capability	RO	X	Corresponds to bytes A0.74-A0.75 in serial EEPROM.
1.807D.15:8	Reserved	RO	X	Unused upper byte.
1.807D.7:0	Basic Field Checksum	R/W[1]	X	Corresponds to byte A0.76 in serial EEPROM.
1.807E.15:8 1.80AD.15:8	Reserved	RO	X	Unused upper byte.
1.807E.7:0 - 1.80AD.7:0	Customer Writeable	R/W	X	Corresponds to bytes A0.77-A0.A6 in serial EEPROM.

1. Read Only if EEPROM_PROTECT pin is asserted

The XENPAK specification provides for 89 bytes of vendor specific nonvolatile storage. The AEL2005 uses 16 of these bytes to update its internal configuration registers between addresses 1.C001 and 1.C07F, as described in Section 12.9. Should a 4kb EEPROM be used, an additional 128 bytes of patch registers are available in registers 1.C480-1.C4FF.

Table 67. Vendor Specific Registers

Bit(s)	Name	R/W	Default	Description
1.80AE.15:8 - 1.8106.15:8	Reserved	RO	X	Unused upper byte.
1.80AE.7:0 - 1.80C6.7:0	Vendor specific registers	R/W[1]	X	Unused by the AEL2005.
1.80C7.6:0 - 1.80D5.6:0 (odd addr only)	AEL2005 configuration address offset	R/W[1,2]	X	Address offset. Register address = 1.C000 + offset. 0x00 indicates an unused entry.
1.80C7.7- 1.80D5.7 (odd addr only)	AEL2005 configuration byte indicator	R/W[1,2]	X	0 = Low order byte (7:0). 1 = High order byte (15:8).
1.80C8.7:0 - 1.80D6.7:0 (even addr only)	AEL2005 Configuration data	R/W[1,2]	X	Configuration data.
1.80D7 - 1.8106	Vendor specific registers	R/W[1,2]	X	Unused by the AEL2005

1. Read Only if EEPROM_PROTECT pin is asserted
2. Set unused registers to 0x00 to prevent unintended configuration modifications

15.6.2 Link Alarm Status Interrupt (LASI) Registers

The Link Alarm Status Interrupt (LASI Registers) are used to generate the LASI_N signal. Use of individual bits is described in the functional description of the LASI block. The control registers RX_ALARM Control, TX_ALARM Control, and LASI Control provide masks to select which inputs become part of the LASI output. The Status registers LASI_Status, RX_ALARM Status, TX_ALARM Status can be read to determine what error condition caused LASI_N assertion. Refer to Section 8.4 on page 19 for more information on the Link Alarm Status Interrupt function.

Note that bit 6 of register 1.9001 defaults to ‘0 when in the Optional Settings Mode as described in Table 102

Table 68. RX_ALARM Control (MDIO Device Address = 1, Register Address = 0x9000)

Bit(s)	Name	R/W	Default	Description
15:10	Reserved	RO	X	
9	WIS Enable	R/W	0	WIS Local Fault Enable.
8:6	Reserved	R/W	X	
5	Optical Power Enable	R/W	1	Receive Optical Power Fault Enable.
4	PMA/PMD Enable	R/W	1	PMA/PMD Receiver Local Fault Enable.
3	PCS Enable	R/W	1	PCS Receive Local Fault Enable.
2	Reserved	R/W	X	
1	RX_FLAG Enable	R/W	0	RX_FLAG Enable
0	PHY XS Enable	R/W	1	PHY XS Receive Local Fault Enable.

Table 69. TX_ALARM Control (MDIO Device Address = 1, Register Address = 0x9001)

Bit(s)	Name	R/W	Default	Description
15:10	Reserved	RO	X	
9	Laser Bias Enable	R/W	1	Laser Bias Current Fault Enable.
8	Laser Temp Enable	R/W	1	Laser Temperature Fault Enable.
7	Laser Power Enable	R/W	1	Laser Power Fault Enable.
6	Transmit Fault Enable	R/W	0	Transmitter Fault Enable.
5	Reserved	R/W	X	
4	PMA/PMD Enable	R/W	1	PMA/PMD Transmit Local Fault Enable.
3	PCS Enable	R/W	1	PCS Transmit Local Fault Enable.
2	Reserved	R/W	X	
1	TX_FLAG Enable	R/W	0	TX_FLAG Enable
0	PHY XS Enable	R/W	1	PHY XS Transmit Local Fault Enable.

Table 70. LASI Control (MDIO Device Address = 1, Register Address = 0x9002)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	V3_3err_EN	R/W	0	3.3-V Out of spec enable.
4	V1_2err_EN	R/W	0	1.2-V Out of spec enable.
3	Reserved	RO	X	
2	RX_ALARM_EN	R/W	0	RX_ALARM Enable.
1	TX_ALARM_EN	R/W	0	TX_ALARM Enable.
0	LS_ALARM_EN	R/W	0	LS_ALARM Enable.

Table 71. RX_ALARM Status (MDIO Device Address = 1, Register Address = 0x9003)

Bit(s)	Name	R/W	Default	Description
15:10	Reserved	RO	X	
9	WIS fault	RO/LH	0	Returns 0.
8:6	Reserved	RO	X	
5	Optical Power	RO/LH[1]	0	Receive Optical Power Fault.
4	PMA/PMD fault	RO/LH	0	Mirrors the value of 1.0008.10.
3	PCS fault	RO/LH	0	Mirrors the value of 3.0008.10.
2	Reserved	RO	X	
1	RX_FLAG	RO	0	
0	PHY XS fault	RO/LH	0	Mirrors the value of 4.0008.10.

1. This bit will be read only if bit 9 of the Optional Settings Register at 1.C017 is set to 1, and RO/LH if it is set to 0.

Table 72. TX_ALARM Status (MDIO Device Address = 1, Register Address = 0x9004)

Bit(s)	Name	R/W	Default	Description
15:10	Reserved	RO	X	
9	Laser Bias fault	RO	0	Laser Bias Current Fault.
8	Laser Temp fault	RO	0	Laser Temperature Fault.

Table 72. TX_ALARM Status (MDIO Device Address = 1, Register Address = 0x9004)

Bit(s)	Name	R/W	Default	Description
7	Laser Power fault	RO	0	Laser Power Fault.
6	Transmit fault	RO/LH	0	Reflects logical OR of bits 0, 3 & 4.
5	Reserved	RO	X	
4	PMA/PMD fault	RO/LH	0	Mirrors the value of 1.0008.11
3	PCS fault	RO/LH	0	Mirrors the value of 3.0008.11.
2	Reserved	RO	X	
1	TX_FLAG	RO	0	
0	PHY XS fault	RO/LH	0	Mirrors the value of 4.0008.11.

Table 73 shows the LASI Status bits. Generation of the alarm signals is shown in the LASI functional description. Registers 1.A06E, 1.A070, 1.A071, 1.A074 & 1.A075 are internally generated, are readable from the MDIO, and writeable to the DOM NVR from the AEL2005 device. However, these registers are not writeable from the MDIO and are not uploaded from the DOM.

Table 73. LASI Status (MDIO Device Address = 1, Register Address = 0x9005)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	V3_3err	RO	0	3.3-V Supply out of range
4	V1_2err	RO	0	1.2-V Supply out of range
3	Reserved	RO	X	
2	RX_ALARM	RO	0	RX_ALARM signal.
1	TX_ALARM	RO	0	TX_ALARM signal.
0	LS_ALARM	RO/LH	0	LS_ALARM signal.

Table 74. TX_FLAG Control (MDIO Device Address = 1, Register Address = 0x9006)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	High Temp en	R/W	0	Temperature High Alarm Enable.
6	Low Temp en	R/W	0	Temperature Low Alarm Enable.
5:4	Reserved	RO	X	
3	High Bias En	R/W	0	Laser Bias Current High Alarm Enable.
2	Low Bias En	R/W	0	Laser Bias Current Low Alarm Enable.
1	High Out En	R/W	0	Laser Output Power High Alarm Enable.
0	Low Out En	R/W	0	Laser Output Power Low Alarm Enable.

Table 75. RX_FLAG Control (MDIO Device Address = 1, Register Address = 0x9007)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	High In En	R/W	0	Receive Optical Power High Alarm Enable.

Table 75. RX_FLAG Control (MDIO Device Address = 1, Register Address = 0x9007)

Bit(s)	Name	R/W	Default	Description
6	Low In En	R/W	0	Receive Optical Power Low Alarm Enable.
5:0	Reserved	RO	X	

Table 76. TX_FLAG Status (MDIO Device Address = 1, Register Address = 0xA070)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	High Temp	RO/LH[1]	0	Temperature High Alarm.
6	Low Temp	RO/LH[1]	0	Temperature Low Alarm.
5:4	Reserved	RO	X	
3	High Bias	RO/LH[1]	0	Laser Bias Current High Alarm.
2	Low Bias	RO/LH[1]	0	Laser Bias Current Low Alarm.
1	High Out Pwr	RO/LH[1]	0	Laser Output Power High Alarm.
0	Low Out Pwr	RO/LH[1]	0	Laser Output Power Low Alarm.

1. These bits will be RO/LH if bit 9 of the Optional Settings Register at 1.C017 is set to 1, and RO if it is set to 0.

Table 77. RX_FLAG Status (MDIO Device Address = 1, Register Address = 0xA071)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	High In Pwr	RO/LH[1]	0	Receive Optical Power High Alarm.
6	Low In Pwr	RO/LH[1]	0	Receive Optical Power Low Alarm.
5:0	Reserved	RO	X	

1. These bits will be RO/LH if bit 9 of the Optional Settings Register at 1.C017 is set to 1, and RO if it is set to 0.

Table 78. TX_FLAG Status 2 (MDIO Device Address = 1, Register Address = 0xA074)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	High Temp Warning	RO/LH[1]	0	Temperature High Warning.
6	Low Temp Warning	RO/LH[1]	0	Temperature Low Warning.
5:4	Reserved	RO	X	
3	High Bias Warning	RO/LH[1]	0	Laser Bias Current High Warning.
2	Low Bias Warning	RO/LH[1]	0	Laser Bias Current Low Warning.
1	High Out Pwr Warning	RO/LH[1]	0	Laser Output Power High Warning.
0	Low Out Pwr Warning	RO/LH[1]	0	Laser Output Power Low Warning.

1. These bits will be RO/LH if bit 9 of the Optional Settings Register at 1.C017 is set to 1, and RO if it is set to 0.

Table 79. RX_FLAG Status 2 (MDIO Device Address = 1, Register Address = 0xA075)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	High In Pwr Warning	RO/LH[1]	0	Receive Optical Power High Warning.
6	Low In Pwr Warning	RO/LH[1]	0	Receive Optical Power Low Warning.
5:0	Reserved	RO	X	

1. These bits will be RO/LH if bit 9 of the Optional Settings Register at 1.C017 is set to 1, and RO if it is set to 0.

15.6.3 Digital Optical Monitoring Registers

The majority of the Digital Optical Monitoring registers (DOM) are described in the section. The exceptions are the DOM registers used for generating Link Alarm Status Interrupt, which are listed in the LASI Section above.

Table 80 shows fields in the *Digital Optical Monitoring Capability* register. These values are loaded from the serial EEPROM at address A0.73. Bit 5 should always be set to 0. Bits 2:0 are used to set the address of the serial device from which the *Alarm Limit*, *Warning Limit*, and *Parameter Value* registers are uploaded. Note that updates of two-byte data fields are gated to ensure that a complete 16-bit DOM data bit has been read prior to modifying internal DOM registers.

Table 80. Digital Optical Monitoring Capability (MDIO Device Address = 1, Register Address = 0x807A)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	DOM Register implemented	RO	X	1 = Implemented. 0 = Not implemented.
6	DOM implemented	RO	X	Mirrors the value of 1.807A.7
5	WDM by lane DOM capability	RO	X	Should be 0.
4	Laser Bias Scale Factor	RO	X	0 = 2 µA 1 = 10 µA
3	Reserved	RO	X	
2:0	External DOM Device Address	RO	XXX	Complete address is 1010 + this field + 0, such that a value of 010 corresponds to 0xA4, and a value of 001 to 0xA2.

The values stored in the DOM registers are not valid until the first update from an external device has occurred. Bit 0 of the Status bits register is set to one once this first update has completed.

Table 81. DOM Status Bits (MDIO Device Address = 1, Register Address = 0xA06E)

Bit(s)	Name	R/W	Default	Description
15:1	Reserved	RO	X	
0	Data_Ready_Bar	RO	1	1 = First read from external monitor device not complete. 0 = First read from external monitor device complete.

The AEL2005 implements all the monitoring, alarm and warning registers, so it returns 1's in the capability registers. If the external device used in tandem with the AEL2005 does not support one or more of the monitoring functions, the appropriate bits should be cleared by the initialization sequence.

Table 82. Extended DOM Capability (MDIO Device Address = 1, Register Address = 0xA06F)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7	Temperature Monitoring	R/W	1	Temperature monitoring capable.
6	Laser Bias Monitoring	R/W	1	Laser bias current monitoring capable.
5	Output Power Monitoring	R/W	1	Output optical power monitoring capable.
4	Receive Power Monitoring	R/W	1	Received optical power monitoring capable.
3	Alarm Flags Implemented	R/W	1	DOM alarm flags implemented.
2	Warning Flags Implemented	R/W	1	DOM warning flags implemented.
1	LASI Inputs Implemented	R/W	1	LASI function inputs implemented.
0	Reserved	RO	X	

The entire DOM MDIO space, as implemented in the AEL2005 device, is uploaded once at device reset. Additional updates to the DOM MDIO registers from the external monitoring device are initiated by writing to the digital optical monitoring control/status register. Writing 00 into the 1:0 field causes a single update to the register set. Writing 01,10, or 11 causes the AEL2005 to periodically poll the monitored values in the external registers. During the first read to the DOM register space, all registers are uploaded. The range to be uploaded during the second and subsequent reads is controlled by the dom_update_r1 and dom_update_r2 fields, found in the DOM update limit register at 1.C07C and 1.C07D and described in Table 112 and Table 113. If the dom_update_* bit is set, the DOM values within the corresponding limit range (inclusive) are updated. These periodic updates must share the SDA/SCL bus with the nonvolatile register memory; if an NVR operation is initiated via an MDIO write to the NVR control/status register (1.8000), the DOM monitored values will not be updated while the NVR operation completes. The timing for these periodic updates can be selected via register 1.C07E, as described in Table 114.

Table 83. Optional Digital Optical Monitoring Control/Status (MDIO Device Address = 1, Register Address = 0xA100)

Bit(s)	Name	R/W	Default	Description
15:4	Reserved	RO	X	
3:2	Command Status	RO/LH	00	00 = Idle. 01 = Command completed successfully. 10 = Command in progress. 11 = Command failed.
1:0	Update Commands	R/W	00	00 = Write initiates single update of DOM registers from external device. 01 = Update DOM registers at slow rate 10 = Update DOM registers at medium rate. 11 = Update DOM registers at fast rate.

There are four parameters that are monitored as part of the DOM specification: temperature, laser bias current, laser output power, and receive optical power. Each parameter has four limits: High Alarm, Low Alarm, High Warning, and Low Warning. The limits and the quantities themselves are all 16-bits. The temperature limits and value are two's complement numbers. All other quantities are unsigned. See Section 15.6.2, "Link Alarm Status Interrupt (LASI) Registers" for more details on how these registers are used.

MDIO reads from the following registers A060/A061, A064/A065, A066/A067, A068/A069, A03A/A03B, A03C/A03D, A03E/A03F, A040/A041, A042/A043, A044/A045 and A046/A047 will be treated as paired reads, and an inifinite lock option has been implemented on the unread register in the pair. Optionally, a 100 ms lock is implemented on the unread register in the pair if register bit 1.C07A.7 (Table 108) in the Override Register 1 is set to 0. Note that should the upper register in any of these pairs be read first, initiating a lock, and then the lower register

and the upper registers are read back-to-back, this will cause the second back-to-back reads to have DOM data from 2 separate I2C loads.

Table 84. Temperature Monitoring Registers

Bit(s)	Name	R/W	Default	Description
1.A000.15:8 1.A001.15:8	Reserved	RO	X X	
1.A000.7:0 1.A001.7:0	Temp High Alarm	R/W	0x7F 0xFF	Temperature High Alarm MSB. Temperature High Alarm LSB.
1.A002.15:8 1.A003.15:8	Reserved	RO	X X	
1.A002.7:0 1.A003.7:0	Temp Low Alarm	R/W	0x80 0x00	Temperature Low Alarm MSB. Temperature Low Alarm LSB.
1.A004.15:8 1.A005.15:8	Reserved	RO	X X	
1.A004.7:0 1.A005.7:0	Temp High Warning	R/W	0x7F 0xFF	Temperature High Warning MSB. Temperature High Warning LSB.
1.A006.15:8 1.A007.15:8	Reserved	RO	X X	
1.A006.7:0 1.A007.7:0	Temp Low Warning	R/W	0x80 0x00	Temperature Low Warning MSB. Temperature Low Warning LSB.
1.A060.15:8 1.A061.15:8	Reserved	RO	X X	
1.A060.7:0 1.A061.7:0	Temperature	R/W	0x00 0x00	Transceiver Temperature MSB. Transceiver Temperature LSB.

Table 85. Laser Bias Monitoring Registers

Bit(s)	Name	R/W	Default	Description
1.A010.15:8 1.A011.15:8	Reserved	RO	X X	
1.A010.7:0 1.A011.7:0	Laser Bias High Alarm	R/W	0xFF 0xFF	Laser Bias High Alarm MSB. Laser Bias High Alarm LSB.
1.A012.15:8 1.A013.15:8	Reserved	RO	X X	
1.A012.7:0 1.A013.7:0	Laser Bias Low Alarm	R/W	0x00 0x00	Laser Bias Low Alarm MSB. Laser Bias Low Alarm LSB.
1.A014.15:8 1.A015.15:8	Reserved	RO	X X	
1.A014.7:0 1.A015.7:0	Laser Bias High Warning	R/W	0xFF 0xFF	Laser Bias High Warning MSB. Laser Bias High Warning LSB.
1.A016.15:8 1.A017.15:8	Reserved	RO	X X	
1.A016.7:0 1.A017.7:0	Laser Bias Low Warning	R/W	0x00 0x00	Laser Bias Low Warning MSB. Laser Bias Low Warning LSB.
1.A064.15:8 1.A065.15:8	Reserved	RO	X X	
1.A064.7:0 1.A065.7:0	Laser Bias	R/W	0x80 0x00	Laser Bias Current MSB. Laser Bias Current LSB.

Table 86. Laser Output Power Monitoring Registers

Bit(s)	Name	R/W	Default	Description
1.A018.15:8 1.A019.15:8	Reserved	RO	X X	
1.A018.7:0 1.A019.7:0	Output Power High Alarm	R/W	0xFF 0xFF	Laser Output Power High Alarm MSB. Laser Output Power High Alarm LSB.
1.A01A.15:8 1.A01B.15:8	Reserved	RO	X X	
1.A01A.7:0 1.A01B.7:0	Output Power Low Alarm	R/W	0x00 0x00	Laser Output Power Low Alarm MSB. Laser Output Power Low Alarm LSB.
1.A01C.15:8 1.A01D.15:8	Reserved	RO	X X	
1.A01C.7:0 1.A01D.7:0	Output Power High Warning	R/W	0xFF 0xFF	Laser Output Power High Warning MSB. Laser Output Power High Warning LSB.
1.A01E.15:8 1.A01F.15:8	Reserved	RO	X X	
1.A01E.7:0 1.A01F.7:0	Output Power Low Warning	R/W	0x00 0x00	Laser Output Power Low Warning MSB. Laser Output Power Low Warning LSB.
1.A066.15:8 1.A067.15:8	Reserved	RO	X X	
1.A066.7:0 1.A067.7:0	Output Power	R/W	0x80 0x00	Laser Output Power MSB. Laser Output Power LSB.

Table 87. Receive Optical Power Monitoring Registers

Bit(s)	Name	R/W	Default	Description
1.A020.15:8 1.A021.15:8	Reserved	RO	X X	
1.A020.7:0 1.A021.7:0	Input Power High Alarm	R/W	0xFF 0xFF	Receive Optical Power High Alarm MSB Receive Optical Power High Alarm LSB
1.A022.15:8 1.A023.15:8	Reserved	RO	X X	
1.A022.7:0 1.A023.7:0	Input Power Low Alarm	R/W	0x00 0x00	Receive Optical Power Low Alarm MSB. Receive Optical Power Low Alarm LSB.
1.A024.15:8 1.A025.15:8	Reserved	RO	X X	
1.A024.7:0 1.A025.7:0	Input Power High Warning	R/W	0xFF 0xFF	Receive Optical Power High Warning MSB. Receive Optical Power High Warning LSB.
1.A026.15:8 1.A027.15:8	Reserved	RO	X X	
1.A026.7:0 1.A027.7:0	Input Power Low Warning	R/W	0x00 0x00	Receive Optical Power Low Warning MSB. Receive Optical Power Low Warning LSB.
1.A068.15:8 1.A069.15:8	Reserved	RO	X X	
1.A068.7:0 1.A069.7:0	Input Power	R/W	0x80 0x00	Receive Optical Power Temperature MSB. Receive Optical Power Temperature LSB.

15.7 AEL2005 Device-Specific Registers

The AEL2005 has an additional set of registers which are used to configure the device and to allow inspection of its internal state.

Table 88. AEL2005 Mode Selection Register (MDIO Device Address = 1, Register Address = 0xC001)

Bit(s)	Name	R/W	Default	Description
15	Reserved	RO	X	Reserved
14	FC_Select	R/W	0	1 = Fibre Channel Mode Selected 0 = Ethernet Mode Selected
13	SSPen	R/W	0	1 = Enable SSP Mode 0 = Disable SSP Mode
12	SynthClk	R/W	0	1 = Use CMU_REF for clock synthesizer 0 = Reserved
11	Synth156En	R/W	0	1 = Enable clock synthesizer 0 = Disable clock synthesizer
10:8	Reserved	RO	X	Reserved
7	Ref50_156_B	R/W	0	1 = 50 MHz reference clock 0 = 156.25 / 159.375 MHz reference clock
6	SGMII_XAUI_B	R/W	0	1 = SGMII (Gigabit Ethernet) Mode 0 = XAUI (10 Gigabit Ethernet) Mode
5	HSRXDATA_invert	R/W	0	1 = Invert P and N on HSRXDATA. 0 = No inversion on HSRXDATA.
4	PMA Line Loopback Enable	R/W	0	PMA Line Loopback Enable 1 = Enable PMA Line Loopback 0 = Disable PMA Line Loopback
3	Reserved	RO	X	Reserved
2	HSTXDATA_invert	R/W	0	1 = Invert P and N on HSTXDATA. 0 = No inversion on HSTXDATA.
1	TXDATA_transpose	R/W	0	Transpose switch for XAUI receive lanes (TXDATA). 1 = X3 → X0,X2 → X1,X1 → X2,X0 → X3. 0 = No transpose.
0	RXDATA_transpose	R/W	0	Transpose switch for XAUI transmit lanes (RXDATA). 1 = X3 → X0,X2 → X1,X1→ X2,X0 → X3. 0 = No transpose.

Bit mappings for the transmit configuration registers are shown in Table 89 and Table 103.

Table 89. Transmit Configuration Register 1 (MDIO Device Address 1, Register Address 0xC002)

Bit(s)	Name	R/W	Default	Description
15:2	Reserved	RO	X	
1:0	HSTXCLK_src	R/W	00	00 = Output full frequency clock 01 = Data on HSTXDATA and HSTXCLK 10 = Output divided-down by-64 clock 11 = Data on HSTXCLK, HSTXDATA powered off

Bit mappings for the Receive Configuration register are shown in Table 90. The "PRBS Clear" bit should be set to clear the "PRBS Error" bit. This error bit is "sticky"; it is asserted and remains asserted until the "Clear Error" bit is set.

Table 90. Receive Configuration Register (MDIO Device Address 1, Register Address 0xC003)

Bit(s)	Name	R/W	Default	Description
15:12	Reserved	RO	X	Reserved
11	CDRLOLstartB	R/W	0	Starts LOL evaluation
10:2	Reserved	RO	X	Reserved
1	PRBS_error	RO	0	0 = no error detected 1 = error detected
0	PRBS_clear	R/W	1	1 = Clear PRBS error flag 0 = Enable PRBS checking and log error

The XAUI Configuration register below includes control for the XAUI PRBS generator. This generator supports four independent PRBS patterns. Note that the PRBS23 and PRBS31 patterns should be inverted for the purpose of interfacing to external O.151-based test equipment. This inversion can be done either through the XAUI Configuration register located at address 1.C007, or on the tester. The 32-bit seed can be set via registers 1.C200 and 1.C201, as described in Table 115.

Table 91. XAUI Configuration Register: Upper 16 Bits (MDIO Device Address = 1, Register Address = 0xC006)

Bit(s)	Name	R/W	Default	Description
15	XAUI PRBS_error3	RO	0	0 = no error detected 1 = error detected
14	XAUI PRBS_error2	RO	0	
13	XAUI PRBS_error1	RO	0	
12	XAUI PRBS_error0	RO	0	
11	XAUI PRBS_clear3	R/W	1	1 = clear PRBS error flag 0 = enable PRBS checking and log error
10	XAUI PRBS_clear2	R/W	1	
9	XAUI PRBS_clear1	R/W	1	
8	XAUI PRBS_clear0	R/W	1	
7	XAUI PRBS_enable3	R/W	0	1 = Initiate pattern generation 0 = Disable pattern generation
6	XAUI PRBS_enable2	R/W	0	
5	XAUI PRBS_enable1	R/W	0	
4	XAUI PRBS_enable0	R/W	0	
3:2	XAUI PRBS_mode	R/W	00	00 = 2^23-1 PRBS 01 = 2^31-1 PRBS 10 = Transmit/Recirculate 32-bit seed 11 = 2^10-1 PRBS
1:0	XAUI_source	R/W	00	00 = transmit input data or system loopback data 01 = transmit PRBS data 10 = reserved 11 = reserved

Table 92. XAUI Configuration Register: Lower 16 Bits (MDIO Device Address = 1, Register Address = 0xC007)

Bit(s)	Name	R/W	Default	Description
15	RXDATA_invert3	R/W	0	1 = Invert P and N on RXDATA[1][1] 1 = No Inversion on RXDATA[1]
14	RXDATA_invert2	R/W	0	
13	RXDATA_invert1	R/W	0	
12	RXDATA_invert0	R/W	0	
11	TXDATA_invert3	R/W	0	1 = Invert P and N on TXDATA[1][1] 0 = No inversion on TXDATA[1]
10	TXDATA_invert2	R/W	0	
9	TXDATA_invert1	R/W	0	
8	TXDATA_invert0	R/W	0	
7:0	Reserved	RO	X	Reserved

1. Each of these two bits will invert the polarity of PHY XS Line Loopback data as well. To ensure proper functionality, set these two bits to the same value when in PHY XS Line Loopback mode.

Table 93. XAUI Transmit Register: Upper 16 Bits (MDIO Device Address = 1, Register Address = 0xC00B)

Bit(s)	Name	R/W	Default	Description
15:12	Reserved	RO	X	
11:9	XAUI_TEQ3[2:0]	R/W	000	XAUI transmit equalization. 000 = 0% transmit preemphasis 001 = 6.5% transmit preemphasis 010 = 13% transmit preemphasis 011 = 19.5% transmit preemphasis 100 = 26% transmit preemphasis 101 = 32.5% transmit preemphasis 110 = 39% transmit preemphasis 111 = 45.5% transmit preemphasis
8:6	XAUI_TEQ2[2:0]	R/W	000	
5:3	XAUI_TEQ1[2:0]	R/W	000	
2:0	XAUI_TEQ0[2:0]	R/W	000	

Table 94. XAUI Transmit Register: Lower 16 Bits (MDIO Device Address = 1, Register Address = 0xC00C)

Bit(s)	Name	R/W	Default	Description
15:12	Reserved	RO	X	
11:9	XAUI_BIAS3[2:0]	R/W	000	XAUI transmit bias - sets minimum output eye height. 000 = Full current 001 = 7/8 current 010 = 6/8 current 011 = 5/8 current 100 = 4/8 current 101 = 3/8 current 110 = 2/8 current 111 = XAUI output disabled
8:6	XAUI_BIAS2[2:0]	R/W	000	
5:3	XAUI_BIAS1[2:0]	R/W	000	
2:0	XAUI_BIAS0[2:0]	R/W	000	

The Power Supply Sensing Threshold register provides the ability to set the power supply thresholds as used by the LASI registers and described in Section 8.4

Table 95. Power Supply Sensing Threshold Register (MDIO Device Address 1, Register Address 0xC00F)

Bit(s)	Name	R/W	Default	Description
15:14	V33tsel	R/W	10	3.3-V Threshold select 00 = 5% 01 = 10% 10 = 15% 11 = 20%
13:12	Reserved	RO	X	
11:10	V12tsel	R/W	10	1.2-V Threshold select 00 = 5% 01 = 10% 10 = 15% 11 = 20%
9:0	Reserved	RO	X	

The LOS mask register defines the inputs to the LOS_OUT device pin. By default, the LOS_OUT pin reflects the logical OR of the RX_LOS input pin and the internally generated LOS signal. Either parameter can be masked out via this register.

Table 96. LOS Mask Register (MDIO Device Address = 1, Register Address = 0xC010)

Bit(s)	Name	R/W	Default	Description
15:14	Reserved	RO	X	Reserved
13	LOS_opt_IntLOS_mask	R/W	0	Mask the internal LOS signal as a gating input to the LOS chip output. 0 = include internal LOS in LOS output. 1 = exclude internal LOS from LOS output.
12	LOS_opt_RxLOS_mask	R/W	0	Mask the input RX_LOS pin as a gating input to the LOS chip output. 0 = include RX_LOS in LOS output. 1 = exclude RX_LOS from LOS output.
11:6	LOSthreshhyst	R/W	0x12	Loss of signal threshold hysteresis.
5:0	LOSthresh	R/W	0x0A	Loss of signal threshold.

The Powerdown Control register allows individual blocks in the design to be powered up and down separately. Bit mappings shown in Table 97 and Table 98. All blocks may also be powered down by asserting the Low Power bit in the PCS Control 1 register.

Table 97. Powerdown Register (MDIO Device Address = 1, Register Address = 0xC011)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	
5	pwrdnTranClock	R/W	1	0 = Power up Transmit clock 1 = Power down Transmit clock
4:0	Reserved	RO	X	Reserved.

Table 98. TX_DISABLE Register (MDIO Device Address = 1, Register Address = 0xC012)

Bit(s)	Name	R/W	Default	Description
15:12	Reserved	RO	X	Reserved
11	TX_DISABLE polarity	R/W	0	TX_DISABLE output polarity control 0 = TX_DISABLE is active high 1 = TX_DISABLE is active low
10:0	Reserved	RO	X	Reserved

Table 99. Transmit Pre-emphasis Register (MDIO Device Address = 1, Register Address = 0xC014)

Bit(s)	Name	R/W	Default	Description
15:11	drvd2[4:0]	R/W	01011	Tap 2 Amplitude Control 300uA * Value
10:5	drvd1[4:0]	R/W	10101	Tap 1 Amplitude Control 300uA * Value
4:0	drvd0[4:0]	R/W	01011	Tap 0 Amplitude Control 150uA * Value

Table 100. Transmit Pre-emphasis Enable Register (MDIO Device Address = 1, Register Address = 0xC015)

Bit(s)	Name	R/W	Default	Description
15:14	Reserved	RO	X	Reserved
13	peEn	R/W	0	Transmit Pre-emphasis on HSTXDATA 0 : Disabled 1 : Enabled
12:0	Reserved	RO	X	Reserved

Table 101. Rate Adjustment Configuration Register (MDIO Device Address = 1, Register Address = 0xC016)

Bit(s)	Name	R/W	Default	Description
15:6	Reserved	RO	X	Reserved
5	Transmit Rate Adaptation Disable	R/W	0	0 = Rate adjustment enabled 1 = Rate adjustment disabled
4	Receive Rate Adaptation Disable	R/W	0	0 = Rate adjustment enabled 1 = Rate adjustment disabled
3:0	Reserved	RO	X	Reserved

The Optional Settings Register contains bit settings to enable the various loopback modes in the AEL2005, options to invert the polarity of the EEPROM_PROTECT, TX_FAULT, and RX_LOS pins, and mask bits to provide the capability to remove certain inputs to the PMA, PCS, and PHY XS fault conditions. The fault mask bits provided in the Optional Settings Register affect the propagation of upstream fault conditions as inputs to downstream faults. Additional fault mask control is available in the Fault Mask Register at 1.C019. For each fault mask, a setting of 1 indicates that the term will not be included in the fault calculation.

The Optional Settings Mode, enabled by bit 9, causes two specific modifications to the device functionality. The first is to propagate data during loopback mode to both the loopback path and to continue along the transmit or receive path on the device. In addition, enabling this mode causes the Receive Optical Power Fault (1.9003.5), the Laser Bias Fault (1.9004.9), Laser Temp Fault (1.9004.8), and Laser Power Fault (1.9004.7) to reflect the current value of those

faults, and not to latch high, causes the TX_FLAG Status (1.A070 & 1.A074) and RX_FLAG Status (1.A071 & 1.A075) registers to latch high, and causes the default value of register 1.9001.6 to be set to ‘0.

Table 102. Optional Settings Register (MDIO Device Address = 1, Register Address = 0xC017)

Bit(s)	Name	R/W	Default	Description
15	PCS Receive Fault Condition Mask	R/W	1	Affects PHY XS Receive Fault (4.0008.10)
14	PMA/PMD Receive Fault Mask	R/W	1	Affects PHY XS Receive Fault (4.0008.10)
13	PMA/PMD Receive Fault Mask	R/W	1	Affects PCS Receive Fault (3.0008.10)
12	PCS Transmit Fault Mask	R/W	1	Affects PMA/PMD Transmit Fault (1.0008.11)
11	PHY XS Transmit Fault Mask	R/W	1	Affects PMA/PMD Transmit Fault (1.0008.11)
10	PHY XS Transmit Fault Mask	R/W	1	Affects PCS Transmit Fault (3.0008.11)
9	Optional Settings Mode	R/W	1	Adjusts various device settings as described above
8:7	Reserved	RO	X	
6	TX_FAULT Pin Polarity	R/W	0	1 = Pin is Active Low 0 = Pin is Active High
5	RX_LOS Pin Polarity	R/W	0	1 = Pin is Active High 0 = Pin is Active Low
4	Enable MDIO Delay	R/W	1	1 = Add 30-80ns of delay to MDIO out 0 = Add 2 inverter delays to MDIO path
3	PHY XS Line Loopback	R/W	0	1 = Enables Loopback 0 = Disables Loopback Identical to bit 4.0000.14
2	PHY XS System Loopback	R/W	0	1 = Enables Loopback 0 = Disables Loopback Identical to bit 4.C000.14
1	PCS System Loopback	R/W	0	1 = Enables Loopback 0 = Disables Loopback Identical to bit 3.0000.14
0	PMA System Loopback	R/W	0	1 = Enables Loopback 0 = Disables Loopback Identical to bit 1.0000.0

Transmit Configuration register 2 includes control for the 10 Gbps PRBS generator. This generator supports three independent PRBS patterns. Note that the PRBS23 and PRBS31 patterns should be inverted for the purpose of interfacing to external O.151-based test equipment. This inversion can be done either through the AEL2005 Mode

Selection register located at address 1.C001, or on the tester. The 32-bit seed can be set via registers 1.C200 and 1.C201, as described in Table 115.

Table 103. Transmit Configuration Register 2 (MDIO Device Address 1, Register Address 0xC018)

Bit(s)	Name	R/W	Default	Description
15:14	Reserved	R/W	X	
13	PRBS_enable	R/W	0	Enables PRBS streams for PRBS generator. 0 = disable pattern generation 1 = Initiate pattern generation
12:11	PRBS_mode	R/W	00	00 = 2^23-1 PRBS 01 = 2^31-1 PRBS 10 = transmit/recirculate 32b seed 11 = reserved
10:9	xmit_source	R/W	00	00 = transmit input data 01 = transmit PRBS data 10 = reserved 11 = reserved
8:6	txDACadj[2:0]	R/W	000	Control bits for transmit DACs
5:0	Reserved	R/W	X	Reserved

The fault mask register provides the capability to mask out inputs to each of the PMA/PMD, PCS, and PHY XS transmit and receive faults. This enables each of these fault signals to be modified to suppress individual parameters from contributing to a fault condition. Setting any of these bits to 1 will remove it from the referenced fault.

Table 104. Fault Mask Register (MDIO Device Address = 1, Register Address = 0xC019)

Bit(s)	Name	R/W	Default	Description
15	CDR Freeze mask	R/W	0	10G CDR freeze mask 1 = Freeze CDR when LOS is asserted 0 = Do not freeze CDR
14	Receive LOS mask	R/W	0	PMA/PMD Receive Fault (1.0008.10)
13	10G receive CDR_LOL mask	R/W	0	PMA/PMD Receive Fault (1.0008.10)
12	10G receive CMU_LOL mask	R/W	1	PMA/PMD Receive Fault (1.0008.10)
11	RX_LOS pin mask	R/W	0	PMD Receive Signal Detect (1.000A.0)
10	LOS mask	R/W	0	PMD Receive Signal Detect (1.000A.0)
9	XAUI lane deskew mask	R/W	0	PHY XS Transmit Fault (4.0008.11)
8	64/66B high BER mask	R/W	1	PCS Receive Fault (3.0008.10)
7	64/66B block lock mask	R/W	0	PCS Receive Fault (3.0008.10)
6	O2E FIFO error mask	R/W	0	PHY XS Receive Fault (4.0008.10)
5	E2O FIFO error mask	R/W	1	PHY XS Transmit Fault (4.0008.11)
4	O2E FIFO error mask	R/W	1	PCS Receive Fault (3.0008.10)
3	E2O FIFO error mask	R/W	0	PCS Transmit Fault (3.0008.11)
2	RX_LOS pin mask	R/W	0	PMA/PMD Receive Fault (1.0008.10)
1	10G Transmit CMU_LOL mask	R/W	0	PMA/PMD Transmit Fault (1.0008.11)
0	TX_Fault pin mask	R/W	1	PMA/PMD Transmit Fault (1.0008.11)

The 10 Gbps Output Swing Register controls the transmit swing for the HSTXDATA and HSTXCLK outputs. Each is controlled by an 8-bit register value, within which entries 0-186 provide a linear function of output swing. Any

larger entries will truncate to the maximum setting of 186. The specifications listed in Section 16.2 represent operation under default settings

Table 105. 10 Gbps Clock Output Swing Register (MDIO Device Address = 1, Register Address = 0xC01E)

Bit(s)	Name	R/W	Default	Description
15:8	HSTXCLK Output Swing	R/W	0xBD	Output swing for HSTXCLK i = 130uA * Value
7:0	Reserved	RO	X	Reserved

Table 106. SGMII Configuration Register — (MDIO Device Address, Register Address = 0xC01F)

Bit(s)	Name	R/W	Description
15	Reserved	RO	Reserved.
14	SGMII_EN1	R/W	SGMII channel 1 enable. 0 = disable SGMII channel 1. 1 = enable SGMII channel 1.
13	SGMII_EN0_OE	R/W	Enables SGMII channel 0 optical to electrical (network to system) path. 0 = SGMII channel 0 optical to electrical disabled. 1 = SGMII channel 0 optical to electrical enabled.
12	SGMII_EN0_EO	R/W	Enables SGMII channel 0 electrical to optical (system to network) path. 0 = SGMII channel 0 electrical to optical path disabled. 1 = SGMII channel 0 electrical to optical pathenabled.
11:10	XTSGMII_DATA1	R/W	XAUI transmit lane select. This field selects the XAUI transmit lane that will transmit data received on the HSRDATA_/N pins and is encoded as follows: 00 = XAUI transmit lane 0 (RXDATA0). 01 = XAUI transmit lane 1 (RXDATA1). 10 = XAUI transmit lane 2 (RXDATA2). 11 = XAUI transmit lane 3 (RXDATA3).
9:8	XTSGMII_DATA0	R/W	XAUI transmit lane select. This field selects the XAUI transmit lane that will transmit data received on RSFP1_P/N pins and is encoded as follows: 00 = XAUI transmit lane 0 (RXDATA0). 01 = XAUI transmit lane 1 (RXDATA1). 10 = XAUI transmit lane 2 (RXDATA2). 11 = XAUI transmit lane 3 (RXDATA3).

Table 106. SGMII Configuration Register — (MDIO Device Address, Register Address = 0xC01F)

Bit(s)	Name	R/W	Description
7:6	XRSGMII_DATA1	R/W	XAUI receive lane select. This field selects the XAUI receive lane that will transmit data out on the HSTXCLK_P/N pins and is encoded as follows: 00 = XAUI receive lane 0 (TXDATA0). 01 = XAUI receive lane 1 (TXDATA1). 10 = XAUI receive lane 2 (TXDATA2). 11 = XAUI receive lane 3 (TXDATA3).
5:4	XRSGMII_DATA0	R/W	XAUI receive lane select. This field selects the XAUI receive lane that will transmit data out on the HSTXDATA_P/N pins and is encoded as follows: 00 = XAUI receive lane 0 (TXDATA0). 01 = XAUI receive lane 1 (TXDATA1). 10 = XAUI receive lane 2 (TXDATA2). 11 = XAUI receive lane 3 (TXDATA3).
3:0	Reserved	RO	Reserved.

Table 107. Programmable Rise Time Control Register (MDIO Device Address 1, Register Address 0xC02B)

Bit(s)	Name	R/W	Default	Description
15:8	Reserved	RO	X	
7:6	Rise_Time_Control	R/W	00	Modify the rise time characteristic of the 10 Gbps transmit buffer. 11 = Fastest setting 01 = Second-fastest setting 00 = Default setting 10 = Slowest setting
5:0	Reserved	RO	X	

Table 108. Override Register 1 (MDIO Device Address 1, Register Address 0xC07A)

Bit(s)	Name	R/W	Default	Description
15:13	Reserved	RW	X	Reserved
12	dom_updt_r2	RW	1	DOM update range 2 1 = Upload the range stored in 1.C07D during periodic updates 0 = Do no upload the range in 1.C07D
11	dom_updt_r1	RW	1	DOM update range 1 1 = Upload the range stored in 1.C07C during periodic updates 0 = Do no upload the range in 1.C07C

Table 108. Override Register 1 (MDIO Device Address 1, Register Address 0xC07A)

Bit(s)	Name	R/W	Default	Description
10	dom_updt_ovrd	RW	0	Inhibits DOM updates after read to A060-A069 after MDIO read to other half of register 0 = 100ms lock enforced after read on complementary Axxx register 1 = no lock enforced
9	Reserved	RW	X	Reserved
8	sq_wave_ovrd	RW	0	Square wave test mode 1 = Output 0x00FF to 10G 0 = Output 0x0F0F to 10G
7	dom_inft_lock	RW	1	DOM infinite lock option 1 = Unread register in monitored pair is locked infinitely 0 = Unread register in monitored pair is locked for 100ms
6:0	Reserved	RW	X	Reserved

Table 109. Embedded Micro-Controller Configuration Register

Bit(s)	Name	Description	Reset Value	RW
1.C04A.3:0	uc_bootopt[3:0]	uC boot option flags	0000	RW
1.C04A.7:4	uc_eepsize[3:0]	uC program size (1=256 instruction, 0,2,3 = reserved)	0111	RW
1.C04A.10:8	uc_clkdiv[2:0]	uC clock divide ratio. Effective freq = 156Mhz / (2**n)	010	RW
1.C04A.11	Reserved	Reserved	0	RW
1.C04A.12	uc_init_mask	If 1, start running immediately without waiting for the end of the chip's reset sequence	0	RW
1.C04A.13	uc_boot_mask	If 1, preserve the firmware (if modified) when resetting.	0	RW
1.C04A.14	uc_porv_pause	Reset value for PAUSE bit	0	RW
1.C04A.15	uc_disable	Disables uC, stops uc_clk	1	RW

Table 110. Embedded Micro-Controller EEPROM Address

Bit(s)	Name	Description	Reset Value	RW
1.C04B.15:0	uc_eepaddr[15:0]	uC EEPROM boot location, uc_eepaddr[15:9] = boot device ID, uc_eepaddr[8] = 0, uc_eepaddr[7:0] = boot address	0xAC00	RW

Table 111. Override Register 2 (MDIO Device Address 1, Register Address 0xC07B)

Bit(s)	Name	R/W	Default	Description
15:13	Reserved	RW	X	Reserved
12	lrm_enable	RW	1	1 = 1.0007.3:0 reflects the 10 GBASE-LRM PMA-PMD type code in 1.C07A.11:8 0 = 10 GBASE-LRM ability turned off
11:8	lrm_code	RW	0x8	IEEE 10 GBASE-LRM code as defined in IEEE 802.3aq/D2.0
7:0	Reserved	RW	X	Reserved

Registers 1.C07C and 1.C07D outline the data ranges to be used for DOM uploads for periodic updates. Note that The DOM periodic update ranges that are specified in 1.C07C and 1.C07D need a minimum of 4 locations and the start addresses must be even.

Table 112. DOM Update Limit Register 1 (MDIO Device Address 1, Register Address 0xC07C)

Bit(s)	Name	R/W	Default	Description
15:8	dom_end_r1	RW	0x69	Ending address for range 1 periodic DOM update. MDIO address is A000+dom_end_r1
7:0	dom_start_r1	RW	0x60	Starting address for range 1 periodic DOM update. MDIO address is A000+dom_start_r1

Table 113. DOM Update Limit Register 2 (MDIO Device Address 1, Register Address 0xC07D)

Bit(s)	Name	R/W	Default	Description
15:8	dom_end_r2	RW	0x47	Ending address for range 2 periodic DOM update. MDIO address is A000+dom_end_r2
7:0	dom_start_r2	RW	0x3A	Starting address for range 2 periodic DOM update. MDIO address is A000+dom_start_r2

Table 114. DOM Update Limit Register 3 (MDIO Device Address 1, Register Address 0xC07E)

Bit(s)	Name	R/W	Default	Description
15:9	Reserved	RO	X	Reserved
8:6	DOM_Update_Rate_Slow	RW	100	Periodic DOM Update Rate at Slow setting, as established by 1.A100 000 = 8 ms 001 = 50 ms 010 = 100 ms 011 = 1 s 100 = 5 s 101 = 10 s 110 = 30 s 111 = 60 s

Table 114. DOM Update Limit Register 3 (MDIO Device Address 1, Register Address 0xC07E)

Bit(s)	Name	R/W	Default	Description
5:3	DOM_Update_Rate_Medium	RW	100	Periodic DOM Update Rate at Medium setting, as established by 1.A100 000 = 4 ms 001 = 8 ms 010 = 50 ms 011 = 100 ms 100 = 1 s 101 = 5 s 110 = 10 s 111 = 30 s
2:0	DOM_Update_Rate_Fast	RW	011	Periodic DOM Update Rate at Fast setting, as established by 1.A100 000 = 2 ms 001 = 4 ms 010 = 8 ms 011 = 50 ms 100 = 100 ms 101 = 1 s 110 = 5 s 111 = 10 s

Table 115. Transmit Seed for 10 Gbps and XAUI PRBS Generators

Bit(s)	Name	R/W	Default	Description
1.C200.15:0	prbs_seed[15:0]	RW	0xAAAA	Transmit PRBS least significant dualoct
1.C201.15:0	prbs_seed[31:16]	RW	0xAAAA	Transmit PRBS most significant dualoct

Table 116. Logic Configuration Register (MDIO Device Address 1, Register Address 0xC202)

Bit(s)	Name	R/W	Default	Description
15:7	Reserved	RO	X	
6	10G Receive FIFO Error	RO	0	Indicates 10G serial receive FIFO error has occurred
5	10G Transmit FIFO Error	RO	0	Indicates 10G serial transmit FIFO error has occurred
4:0	Reserved	RO	X	

Table 117. Logic Configuration Register (MDIO Device Address 1, Register Address 0xC20C)

Bit(s)	Name	R/W	Default	Description
15:9	Reserved	RO	X	
8	10GBASE-X Logic Bypass	R/W	0	1 = Bypass 10GBASE-X logic (Includes 8b/10b) 0 = Do not bypass 10GBASE-X logic
7:4	Reserved	RO	X	
3	10GBASE-R Logic Bypass	R/W	0	1 = Bypass 10GBASE-R logic (Includes 64b/66b) 0 = Do not bypass 10GBASE-R logic
2:0	Reserved	RO	X	

Table 118. SGMII Configuration Register (MDIO Device Address 1, Register Address 0xC20D)

Bit(s)	Name	R/W	Default	Description
15:12	Reserved	RO	X	
11:10	xtsgmiiMode[1:0]	R/W	0x3	Select mode for SGMII transmit data when SGMII_XAUI_B is set 00 = Data on lane set by xtsgmiiData[1:0] 01 = Data on lane set by xtsgmiiData[1:0], half rate clock on other lanes 10 = Data on lane set by xtsgmiiData[1:0], half rate clock on lane + 1 11 = Broadcast SGMII data on all lanes
9:8	xtsgmiiData[1:0]	R/W	0x0	Select XAUI lane for SGMII transmit data when SGMII_XAUI_B is set 00 = Lane 0, 01 = Lane1, 10 = Lane2, 11 = Lane3
7:6	xrsgmiiData[1:0]	R/W	0x00	Select XAUI lane for SGMII receive data when SGMII_XAUI_B is set. Power down unused lanes 00 = Lane 0, 01 = Lane1, 10 = Lane2, 11 = Lane3
5:0	Reserved	R/W	0x00	Reserved

Table 119. Checksum Verification Register (MDIO Device Address 1, Register Address 0xC20F)

Bit(s)	Name	R/W	Default	Description
15:13	patch_deviceID	RW	100	Bits [3:1] of the patch EEPROM device ID. Th default ID is “A8” (1010_100x), only bits [3:1] are configurable
12	Reserved	RO	X	
11:10	nvr_size	RO	00	Detected NVR size: 00 = No EEPROM 01 = 2K EEPROM 10 = 4K EEPROM 11 = Reserved
9	DOM_wr_en	RW	0	DOM Write Enable Bit 1 = Enable DOM write with 1.8000 register 0 = Enable NVR write with 1.8000 register Note that this function is disabled when the EEPROM Protect pin has been set.
8	Checksum Verified	RO	0	1 = Internally calculated checksum on EEPROM read matches EEPROM location 118 0 = Checksums do not match
7:0	Checksum	RO	0x00	The internally calculated checksum

Table 120. GPIO and Activity LED Register (MDIO Device Address 1, Register Address 0xC214)

Bit(s)	Name	R/W	Default	Description
15:12	GPIO3_CTRL	RW	1000	General Purpose IO Lane 3 Control and Status
11:8	GPIO2_CTRL	RW	0000	General Purpose IO Lane 2 Control and Status
7:4	GPIO1_CTRL	RW	1000	General Purpose IO Lane 1 Control and Status
3:0	GPIO0_CTRL	RW	1000	General Purpose IO Lane 0 Control and Status

Table 121. GPIO and Activity LED Register (MDIO Device Address 1, Register Address 0xC215)

Bit(s)	Name	R/W	Default	Description
15:5	Reserved	RO	0x000	Reserved
4	LED_Time2x	RW	0	Double the LED toggle time
3:0	gpio_intr	RO	0000	Interrupt from GPIO lanes [3:0]

Table 122. LED Activity Truth Table Register

Bit(s)	Name	R/W	Default	Description
1.C216.15:0	LED0_TT	RW	0x4444	LED0 (Tx Activity) Truth Table
1.C217.15:0	LED1_TT	RW	0x0F00	LED1 (Rx Activity) Truth Table
1.C218.15:0	LED2_TT	RW	0x0000	LED0 (Spare Activity) Truth Table
1.C219.15:0	LED3_TT	RW	0x0000	LED0 (Spare Activity) Truth Table

Registers 1.C30A to 1.C30D govern control over external SDA/SCL operations initiated by the AEL2005 device. This functionality is disabled when the EEPROM Protect pin has been set.

Table 123. SDA/SCL Read/Write Registers

Bit(s)	Name	R/W	Default	Description
1.C30A.15:9	snoop_dev_addr	RW	0x00	SDA/SCL Slave Address Complete address is this field + 0, such that a value of 1010 001 corresponds to 0xA2
1.C30A.8	snoop_dev_addr[0]	RW	0	SDA/SCL R/W Bit 0 = Write 1 = Read
1.C30A.7:0	snoop_word_addr	RW	0x00	Word Address
1.C30B.15:8	snoop_rd_data	RO	0x00	Read Data
1.C30B.7:0	snoop_wr_data	RW	0x00	Write Data
1.C30C.15:2	Reserved	RO	X	Reserved
1.C30C.1:0	snoop_op_stat	RO	0x00	Status from SDA/SCL Operation 00 = No operation performed 01 = Operation passed 10 = Operation failed 11 = Operation in progress
1.C30D.15:0	Reserved	RO	X	Reserved

Registers 1.C310 to 1.C313 govern control over an internal BER counter, tied to the serial receive PRBS checkers. For more information, see the Puma AEL1001 & AEL2005 BER Testing Application Note.

Table 124. BER Counter Registers

Bit(s)	Name	R/W	Default	Description
1.C310.15:0	BER_Meas_Cnt	RW	0x0000	Bit Errors to be measured for 10G Receive PRBS. The value in this register is 3 times the number of BERs registered.
1.C311.15:3	Reserved	RO	X	Reserved
1.C311.2	BER_Result Ready	RO	0	1 = BER Timer test results are valid
1.C311.1	BER_Test_Done	RO	0	1 = BER Timer test complete

Table 124. BER Counter Registers

Bit(s)	Name	R/W	Default	Description
1.C311.0	Start_BER_Test	RW	0	Set to 1 to initiate BER timer test. Self-clearing when complete
1.C312.15:0	BER_Counter[15:0]	RO	0x0000	BER Timer test results in micro-seconds
1.C313:15:0	BER_Counter[31:16]	RO	0x0000	BER Timer test results in micro-seconds

Registers 1.C320 through 1.C32F govern control over the packet-level pattern tester described in Section 10.4. Table 125 describes registers associated with the serial-to-parallel device receive path

Table 125. Pattern Tester Receive Registers

Bit(s)	Name	R/W	Default	Description
1.C320.15:0	mpackNum_g	RW	0x0000	Continuous number of packets to be generated. 0x0000 corresponds to continuous packet generation
1.C321.15:8	mdPream_gc	RW	0x55	XGMII data for preamble
1.C321.7:0	mdStart_gc	RW	0xFB	XGMII data for |S| character
1.C322.15:8	mdTerm_gc	RW	0xFD	XGMII data for |T| character
1.C322.7:0	mdSFD_gc	RW	0xD5	XGMII data for Start of Frame Delimiter
1.C323.15	Reserved	RO	X	Reserved
1.C323.14	mmode_ErrCnt_c	RW	1	If set, mcrcErrCnt_c and mIdleErrCnt_c show number of packets and length of last packet
1.C323.13:12	mmode_g	RW	00	Generator mode (0:idle, 1:CRPAT, 2:CJPAT, 3:Increment)
1.C323.11	museSIdleAsType	RW	0	If set mdSpecIdleLSB_gc is used as the packet type (instead of special idle)
1.C323.10	mtranspose_c	RW	1	Transpose XGMII data (0 for 10GFC)
1.C323.9	mtranspose_g	RW	1	Transpose XGMII data (0 for 10GFC)
1.C323.8	men10GFCcrc_gc	RW	0	If set CRC is calculated compliant to 10GFC
1.C323.7	mstartTgl_g	RW	0	Toggling the bit starts generator again
1.C323.6	mclrCntTgl_c	RW	0	Toggling the bit clears the counter on next IPG
1.C323.5	menable_g	RW	0	Enable generator (0 stops the gnerator, auto resets on 1->0)
1.C323.4	menable_c	RW	0	Enable the checker (0 stops the checker and resets it)
1.C323.3	mcTerm_gc	RW	1	XGMII control for |T| character
1.C323.2	mcSFD_gc	RW	0	XGMII control for SFD
1.C323.1	mcPream_gc	RW	0	XGMII control for preamble 1010
1.C323.0	mcStart_gc	RW	1	XGMII control for |S| character
1.C324.15:0	mdSpecIdleMSB_gc	RW	0x0707	XGMII data for special |I| upper half
1.C325.15:0	mdSpecIdleLSB_gc	RW	0x0707	XGMII data for special |I| lower half
1.C326.15:0	mdSrcDst0LSB_g	RW	0x0102	XGMII data for frame address - dst[0:1] generator

Table 125. Pattern Tester Receive Registers

Bit(s)	Name	R/W	Default	Description
1.C327.15:0	mdSrcDst0MSB_g	RW	0x0304	XGMII data for frame address - dst[2:3] generator
1.C328.15:0	mdSrcDst1MSB_g	RW	0x0506	XGMII data for frame address - dst[2:3] generator
1.C329.15:0	mdSrcDst1LSB_g	RW	0x0708	XGMII data for frame address - src[0:1] generator
1.C32A.15:0	mdSrcDst2MSB_g	RW	0x090A	XGMII data for frame address - src[2:3] generator
1.C32B.15:0	mdSrcDst2LSB_g	RW	0x0B0C	XGMII data for frame address - src[4:5] generator
1.C32C.15:12	mcSpecIdleLSB_gc	RW	1111	XGMII control for special |I|
1.C32C.11:0	mpackLen_g	RW	12'd 2400	Length of packet in columns if in increment mode
1.C32D.15:10	Reserved	RO	X	Reserved
1.C32D.9:0	mipgLen_g	RW	0x4	IPG length in columns
1.C32E.15:0	mcrcErrCnt_c	RO	0x0000	Number of CRC errors/Number of packets received
1.C32F.15:0	midleErrCnt_c	RO	0x0000	Number of IPG discrepancies/Length of last packet received

Table 126 describes registers associated with the parallel-to-serial device transmit

Table 126. Pattern Tester Transmit Registers

Bit(s)	Name	R/W	Default	Description
1.C330.15:0	mpackNum_g	RW	0x0000	Continuous number of packets to be generated. 0x0000 corresponds to continuous packet generation
1.C331.15:8	mdPream_gc	RW	0x55	XGMII data for preamble
1.C331.7:0	mdStart_gc	RW	0xFB	XGMII data for |S| character
1.C332.15:8	mdTerm_gc	RW	0xFD	XGMII data for |T| character
1.C332.7:0	mdSFD_gc	RW	0xD5	XGMII data for Start of Frame Delimiter
1.C333.15	Reserved	RO	X	Reserved
1.C333.14	mmode_ErrCnt_c	RW	1	If set, mcrcErrCnt_c and mIdleErrCnt_c show number of packets and length of last packet
1.C333.13:12	mmode_g	RW	00	Generator mode (0:idle, 1:CRPAT, 2:CJPAT, 3:Increment)
1.C333.11	museSIdleAsType	RW	0	If set mdSpecIdleLSB_gc is used as the packet type (instead of special idle)
1.C333.10	mtranspose_c	RW	1	Transpose XGMII data (0 for 10GFC)
1.C333.9	mtranspose_g	RW	1	Transpose XGMII data (0 for 10GFC)
1.C333.8	men10GFCcrc_gc	RW	0	If set CRC is calculated compliant to 10GFC
1.C333.7	mstartTgl_g	RW	0	Toggling the bit starts generator again
1.C333.6	mclrCntTgl_c	RW	0	Toggling the bit clears the counter on next IPG

Table 126. Pattern Tester Transmit Registers

Bit(s)	Name	R/W	Default	Description
1.C333.5	menable_g	RW	0	Enable generator (0 stops the gnerator, auto resets on 1->0)
1.C333.4	menable_c	RW	0	Enable the checker (0 stops the checker and resets it)
1.C333.3	mcTerm_gc	RW	1	XGMII control for |T| character
1.C333.2	mcSFD_gc	RW	0	XGMII control for SFD
1.C333.1	mcPream_gc	RW	0	XGMII control for preamble 1010
1.C333.0	mcStart_gc	RW	1	XGMII control for |S| character
1.C334.15:0	mdSpecIdleMSB_gc	RW	0x0707	XGMII data for special |I| upper half
1.C335.15:0	mdSpecIdleLSB_gc	RW	0x0707	XGMII data for special |I| lower half
1.C336.15:0	mdSrcDst0LSB_g	RW	0x0102	XGMII data for frame address - dst[0:1] generator
1.C337.15:0	mdSrcDst0MSB_g	RW	0x0304	XGMII data for frame address - dst[2:3] generator
1.C338.15:0	mdSrcDst1MSB_g	RW	0x0506	XGMII data for frame address - dst[2:3] generator
1.C339.15:0	mdSrcDst1LSB_g	RW	0x0708	XGMII data for frame address - src[0:1] generator
1.C33A.15:0	mdSrcDst2MSB_g	RW	0x090A	XGMII data for frame address - src[2:3] generator
1.C33B.15:0	mdSrcDst2LSB_g	RW	0x0B0C	XGMII data for frame address - src[4:5] generator
1.C33C.15:12	mcSpecIdleLSB_gc	RW	1111	XGMII control for special |I|
1.C33C.11:0	mpackLen_g	RW	12'd 2400	Length of packet in columns if in increment mode
1.C33D.15:10	Reserved	RO	X	Reserved
1.C33D.9:0	mipgLen_g	RW	0x4	IPG length in columns
1.C33E.15:0	mcrcErrCnt_c	RO	0x0000	Number of CRC errors/Number of packets received
1.C33F.15:0	midleErrCnt_c	RO	0x0000	Number of IPG discrepancies/Length of last packet received

Table 127. Error Slicer Threshold Register

Bit(s)	Name	R/W	Default	Description
1.C5B0.15:12	ocal_slcavg_dirs[3:0]	RW	0000	Initial Excursion Direction
1.C5B0.11:8	ocal_slcavg_period[3:0]	RW	0000	Move 1 LSB every 2^period cycles
1.C5B0.7:6	Reserved	RW	X	Reserved
1.C5B0.5:1	ocal_slcavg_range[4:0]	RW	00000	Move at most this many LSBs away from the calibrated thershold
1.C5B0.0	ocal_slcavg_enable	RW	0	1 : Enable error slicer threshold averaging 0 : Otherwise

Table 128. Initial / Override FFE Register

Bit(s)	Name	R/W	Default	Description
1.C620.15:8	ovr_hffe01_val[7:0]	WG	1100_1110	Co-eff ovrd / init value (-50)
1.C620.7:0	ovr_hffe00_val[7:0]	WG	0001_0100	Co-eff ovrd / init value (20)
1.C621.15:8	ovr_hffe03_val[7:0]	WG	0001_1110	Co-eff ovrd / init value (30)
1.C621.7:0	ovr_hffe02_val[7:0]	WG	0001_1001	Co-eff ovrd / init value (25)
1.C622.15:8	ovr_hffe05_val[7:0]	WG	0000_0000	Co-eff ovrd / init value (0)
1.C622.7:0	ovr_hffe04_val[7:0]	WG	1011_1010	Co-eff ovrd / init value (-70)
1.C623.15:8	ovr_hffe07_val[7:0]	WG	0000_0000	Co-eff ovrd / init value (0)
1.C623.7:0	ovr_hffe06_val[7:0]	WG	0111_1111	Co-eff ovrd / init value (127)
1.C624.15:8	ovr_hffe09_val[7:0]	WG	1100_0100	Co-eff ovrd / init value (-60)
1.C624.7:0	ovr_hffe08_val[7:0]	WG	1101_1000	Co-eff ovrd / init value (-40)
1.C625.15:8	ovr_hffe11_val[7:0]	WG	1110_0010	Co-eff ovrd / init value (-30)
1.C625.7:0	ovr_hffe10_val[7:0]	WG	0011_1100	Co-eff ovrd / init value (60)
1.C626.15:7	Reserved	RO	X	Reserved
1.C626.6:0	ovr_hffe_cmctl[6:0]	WG	000_0000	Common mode control ovrd [6] and value (0)

Table 129. Initial / Override DFE Register

Bit(s)	Name	R/W	Default	Description
1.C627.15:8	ovr_hfbe02_val[7:0]	WG	0101_0000	Co-eff ovrd / init value (80)
1.C627.7:0	ovr_hfbe01_val[7:0]	WG	0111_1111	Co-eff ovrd / init value (127)
1.C628.15:8	ovr_hfbe04_val[7:0]	WG	1000_0001	Co-eff ovrd / init value (-127)
1.C628.7:0	ovr_hfbe03_val[7:0]	WG	1000_0001	Co-eff ovrd / init value (-127)

Table 130. Initial / Override Flag FFE / DFE Register

Bit(s)	Name	R/W	Default	Description
1.C62B.15:8	Reserved	RO	X	Reserved
1.C62B.7:4	ovr_hfbe_flags[3:0]	WG	0000	Flags for overriding hfbe01(LSB) to hfbe04(MSB)
1.C62B.3:0	Reserved	RO	X	Reserved
1.C62C.15:12	Reserved	RO	X	Reserved
1.C62C.11:0	ovr_hffe_flags[11:0]	WG	0x000	Flags for overriding hffe00(LSB) to hffe11(MSB)

Table 131. Adaptation Observation Register

Bit(s)	Name	R/W	Default	Description
1.C62D.15:8	hffe01[7:0]	RG		hffe01 equalizer co-efficient in 2's compliment format
1.C62D.7:0	hffe00[7:0]	RG		hffe00 equalizer co-efficient in 2's compliment format

Table 131. Adaptation Observation Register

Bit(s)	Name	R/W	Default	Description
1.C62E.15:8	hffe03[7:0]	RG		hffe03 equalizer co-efficient in 2's compliment format
1.C62E.7:0	hffe02[7:0]	RG		hffe02 equalizer co-efficient in 2's compliment format
1.C62F.15:8	hffe05[7:0]	RG		hffe05 equalizer co-efficient in 2's compliment format
1.C62F.7:0	hffe04[7:0]	RG		hffe04 equalizer co-efficient in 2's compliment format
1.C630.15:8	hffe07[7:0]	RG		hffe07 equalizer co-efficient in 2's compliment format
1.C630.7:0	hffe06[7:0]	RG		hffe06 equalizer co-efficient in 2's compliment format
1.C631.15:8	hffe09[7:0]	RG		hffe09 equalizer co-efficient in 2's compliment format
1.C631.7:0	hffe08[7:0]	RG		hffe08 equalizer co-efficient in 2's compliment format
1.C632.15:8	hffe11[7:0]	RG		hffe11 equalizer co-efficient in 2's compliment format
1.C632.7:0	hffe10[7:0]	RG		hffe10 equalizer co-efficient in 2's compliment format
1.C633.15:8	hfbe02[7:0]	RG		hfbe02 equalizer co-efficient in 2's compliment format
1.C633.7:0	hfbe01[7:0]	RG		hfbe01 equalizer co-efficient in 2's compliment format
1.C634.15:8	hfbe04[7:0]	RG		hfbe04 equalizer co-efficient in 2's compliment format
1.C634.7:0	hfbe03[7:0]	RG		hfbe03 equalizer co-efficient in 2's compliment format
1.C637.15:6	Reserved	RO	X	Reserved
1.C637.5:0	hffe_cmctl[5:0]	RG		hffe common mode control
1.C638.15:8	Reserved	RO	X	Reserved
1.C638.7:0	cursor_filt[7:0]	RO		Filtered (40Khz) version of hffe cursor

Table 132. AGCP Parameter Registers

Bit(s)	Name	R/W	Default	Description
1.C840.15:4	Reserved	RO	X	Reserved
1.C840.3	agcp_vgaCmpress	RO		Comparator result
1.C840.2	agcp_caldone	RO		Offset calibration done
1.C840.1	agcp_agcLOL	RO		Loss of AGC Lock
1.C840.0	agcp_agcAcquired	RO		Completed initial acquisition
1.C841.15:9	Reserved	RO	X	Reserved
1.C841.8:0	agcp_vgactl	RO		Binary value of VGA control
1.C842.15	Reserved	RO	X	Reserved
1.C842.14:8	agcp_dacctlOffs	RO		Control of the reference DAC

Table 132. AGCP Parameter Registers

Bit(s)	Name	R/W	Default	Description
1.C842.7:6	Reserved	RO	X	Reserved
1.C842.5:0	agcp_peak	RO		Current best unsigned binary estimate of peak
1.C843.15:7	Reserved	RO	X	Reserved
1.C843.6:0	agcp_est_zero	RO		Estimated effective DAC zero (w/ offset)

Table 133. uC Control / Status Registers

Bit(s)	Name	Description	Reset Value	RW
1.CA00.15:0	pc[15:0]	Program Counter	0000000000000100	RW
1.C012.15:1	RESERVED	Reserved (do not modify these bits)	000000000000000	RW
1.CA12.0	pause	PAUSE control bit	0	RW
1.CA13.15:0	sstep[15:0]	Number of instructions to step through. Only writable when PAUSE bit is set	0000000000000000	RW
1.CA1C.15:1	RESERVED	Reserved	-	RO
1.CA1C. 0	paused	Paused status bit	-	RO
1.CA1E.15:0	fw_version	Boot Firmware revision ID	0000000000000001	RO
1.CA1E.15:0	uc_version	uC revision ID	0000000000000001	RO

16 Electrical Specifications

This section contains the electrical specifications for the AEL2005 device and is divided into the following interfaces.

- Section 16.1, "Conventions"
- Section 16.2, "SFP+ Interface DC and AC Specifications"
- Section 16.3, "XAUI Interface AC Specifications"
- Section 16.4, "CMU_REF Clock Input"
- Section 16.5, "CMOS Interface"
- Section 16.6, "MDIO Interface"
- Section 16.7, "SDA/SCL Interface"
- Section 16.9, "Operating Conditions"

16.1 Conventions

The conventions used in setting voltage swings are shown in Figure 40. The "single ended voltage swing" describes the change in voltage that either half of the differential pair undergoes when transitioning from low to high. The "Differential peak-to-peak voltage" is the swing that the difference of the of the two signals undergoes when the voltage level transitions from low to high. The common mode voltage is defined as the voltage at which Signal+ and Signal- cross.

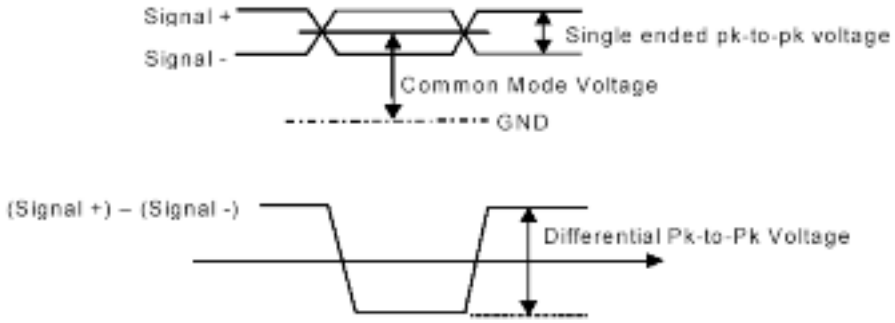


Figure 40. Voltage Parameter Definitions

16.2 SFP+ Interface DC and AC Specifications

An equivalent circuit for the AEL2005 10 Gbps output is shown in Figure 41.

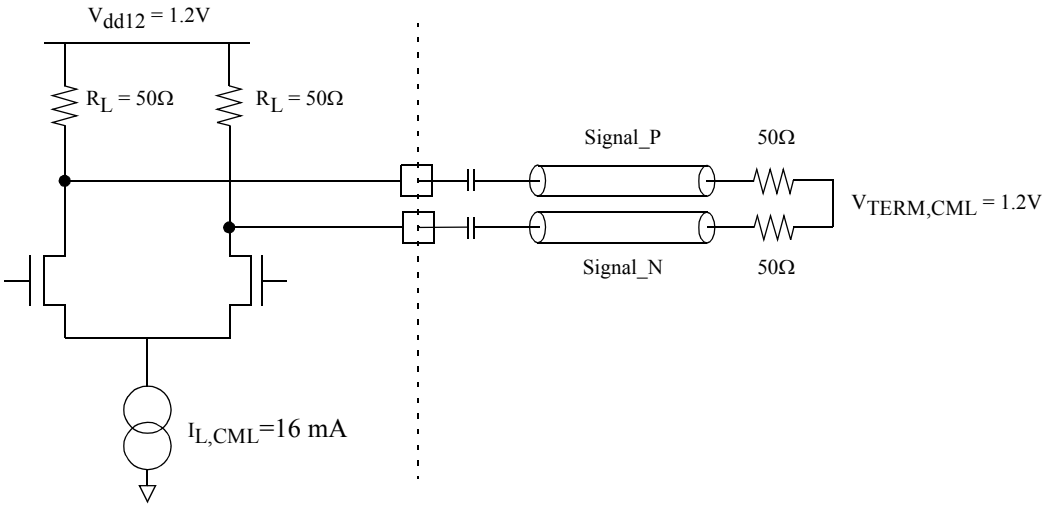


Figure 41. AC-coupled CML Output Equivalent Circuit

The AEL2005 device transmit mask for module applications is shown in Figure 42.

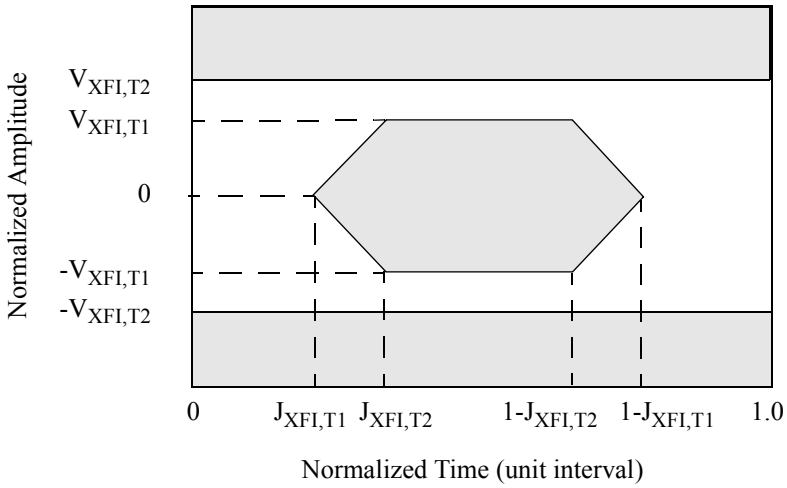


Figure 42. High Speed CML Transmit Jitter Mask

Table 134 lists the high speed I/O specifications for the HSRXDATA, HSTXDATA, and HSTXCLK pins as described in Section 4.1.4 and Section 4.2.1.

Table 134. SFI DC and AC Characteristics

Name	Description	Min	Nom	Max	Units
f_{CML}	HSTXDATA/HSRXDATA raw data rate	9.95	-	10.52	Gbps
$t_{TOL,HSRX}$[1]	reference/HSRXDATA frequency offset tolerance	-100	0	100	ppm
$t_{TOL,HSTX}$[2]	reference/HSTXDATA frequency offset tolerance	0	0	0	ppm
$t_{DR}/t_{DF,CML}$	CML output data 20/80% rise/fall time	30	35	45	ps
	CML output data 20/80% rise/fall time, fastest setting	20	30	40	ps
$v_{CK,CML}$	CML clock differential output swing in /64 mode	700	800	900	mV_{pp}
$v_{CK,CML}$	CML clock differential output swing at 10 Gbps	150	200	300	mV_{pp}
$S_{11,in}$	CML differential input return loss @ 5GHz	15	-	-	dB
$S_{22,out}$	CML differential output return loss @ 5GHz	15	-	-	dB
$V_{XFI,T1}$	SFI Transmitter Mask Min eye height	75	-	-	mV
$V_{XFI,T2}$	SFI Transmitter Mask Max eye height	-	-	400	mV
$J_{XFI,T1}$	SFI Transmitter Mask Jitter Value	-	-	0.14	UI
$J_{XFI,T2}$	SFI Transmitter Mask Jitter Value	-	-	0.35	UI
$V_{XFI,R1}$	SFI Receiver Mask Min eye height	125	-	-	mV
$V_{XFI,R2}$	SFI Receiver Mask Max eye height	-	-	500	mV

1. The serial CDR reference source and frequency will vary depending on the mode of operation. See the serial input receiver functional description for more details.
2. The serial transmitter will always transmit at the same frequency as its reference clock. However, the reference clock may be derived from the parallel input receiver recovered clock. See the serial output transmitter functional description for more details.

16.3 XAUI Interface AC Specifications

This section describes the AC specifications for the XAUI interface signals, including the differential RXDATA[3:0] and TXDATA[3:0] pins as described in Section 4.1.1 and Section 4.2.4.

16.3.1 XAUI SerDes Inputs (TXDATA)

The AEL2005 contains four sets of differential 3.125 / 3.1875 Gbps TXDATA_N/TXDATA_P inputs designed to be compatible with the 10 Gigabit Ethernet XAUI and 10 Gigabit Fibre Channel XAUI specifications. An equivalent circuit is shown in Figure 43. The circuit is designed to be AC coupled. The common mode level for TXDATA_P and TXDATA_N is set internally. TXDATA_P and TXDATA_N are terminated differentially to one another on chip, with a nominal differential resistance of 100Ω. The AEL2005 XAUI receive eye mask is shown in Figure 44.

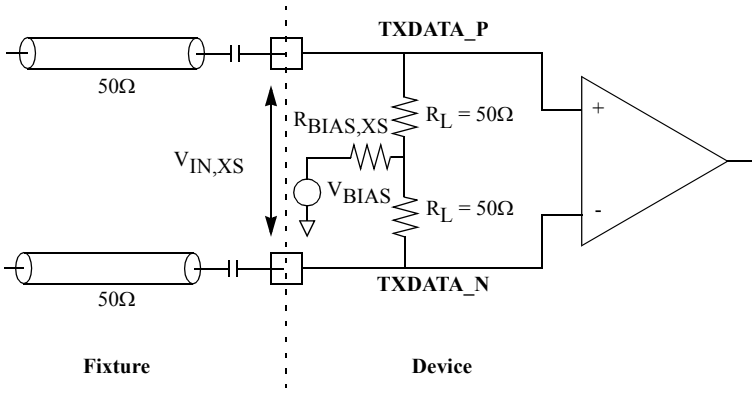


Figure 43. Equivalent Input Circuit for XAUI Receiver

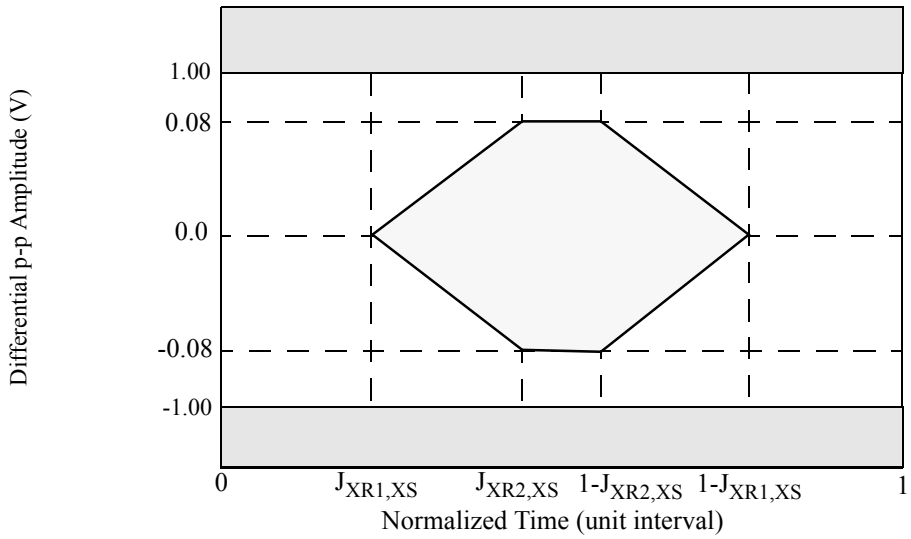


Figure 44. Receive Eye Mask for XAUI Receiver

16.3.2 XAUI SerDes Outputs (RXDATA)

The AEL2005 provides parallel data on the RXDATA pins. A simplified version of the output circuit and test fixture is shown in Figure 45. The output differential pair is terminated to the supply VDD. The output current has two different components: half the current is inversely proportional to the sheet resistance, and the other half has a constant value.

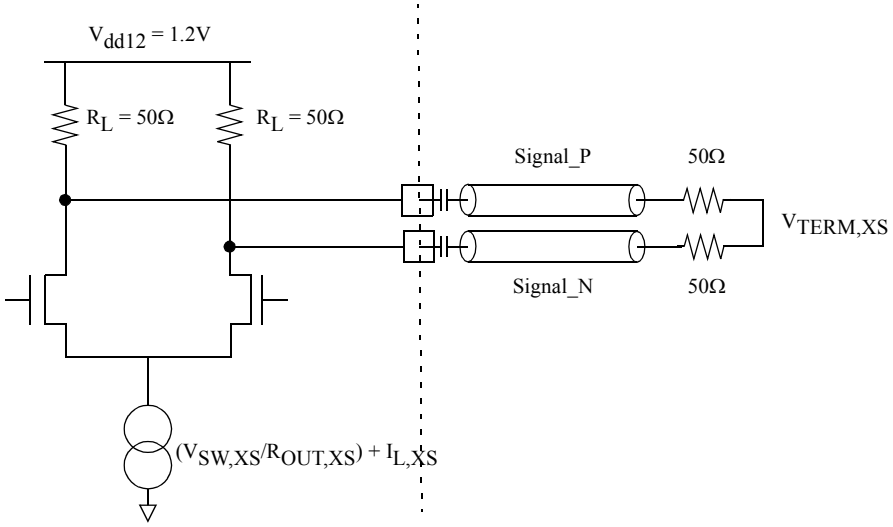


Figure 45. CML AC-Coupled Equivalent Output Circuit

The AEL2005 includes a simple one-tap equalizer that is useful in driving longer printed circuit traces. This equalizer pre-emphasizes the output signal whenever there is a data transition. The amount of pre-emphasis can vary between 0 and 45.5%, and is programmed using the XAUI Transmit register 1 (1.COOB). Figure 46 shows the effect of different register settings. Note that pre-emphasis doesn't increase the overall swing, but instead reduces the output amplitude when there is no transition.

The overall swing level can also be programmed using the XAUI Transmit register 2 (1.COOC) register.

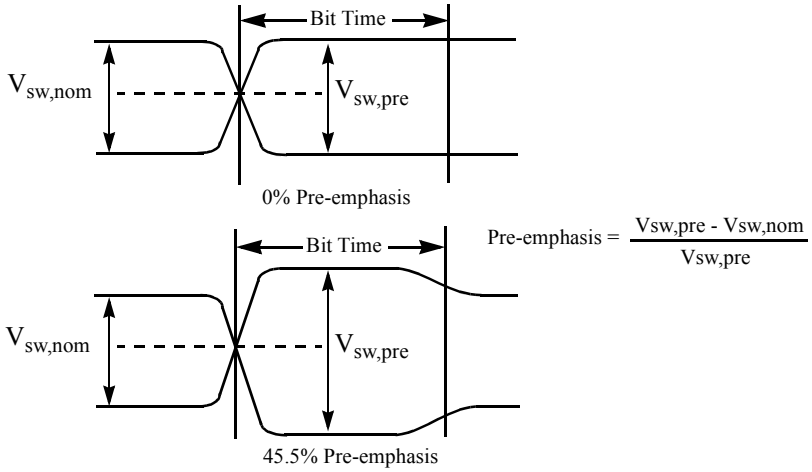


Figure 46. Effects of Transmit Pre-emphasis

The AEL2005 XAUI transmit eye mask is shown in Figure 47. As per the directions of IEEE 802.3ae, this eye mask is measured using the CJPAT data pattern.

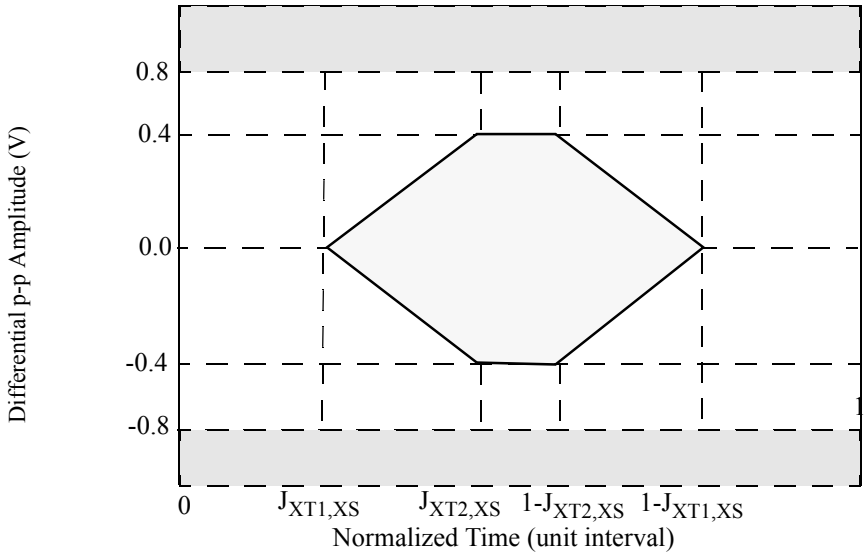


Figure 47. Transmit Eye Mask for SerDes Outputs

16.3.3 XAUI SerDes Specification Table

Table 135. XAUI SerDes Specifications

Name	Description	Min	Nom	Max	Units
$t_{BIT,XS}$	XAUI bit time	312	-	320	ps
$J_{XR1,XS}$	Total input jitter tolerance at signal crossover	0.32	-	-	UI
$J_{XR1,XS,DJ}$	Deterministic jitter tolerance at signal crossover	0.18	-	-	UI
$J_{XR2,XS}$	Total input jitter at $V_{IN,XS,min}$	0.5			UI
$J_{XT1,XS}$	Total output jitter at signal crossover	-	-	0.17	UI
$J_{XT1,XS,DJ}$	Deterministic output jitter at signal crossover	-	-	0.08	UI
$J_{XT2,XS}$	Total output jitter at $V_{SW,min}$	-	-	0.4	UI
$J_{TOL,XAUI,20MHz}$[1]	XAUI sinusoidal jitter tolerance at 20 MHz	0.1	-	-	UI_{pp}
$J_{TOL,XAUI,1.875MHz}$[1]	XAUI sinusoidal jitter tolerance at 1.875 MHz	0.1	-	-	UI_{pp}
$J_{TOL,XAUI,22KHz}$[1]	XAUI sinusoidal jitter tolerance at 22 KHz	8.5	-	-	UI_{pp}
$t_{TOL,RX}$[2]	reference/TXDATA frequency offset tolerance	-100	0	100	ppm
$t_{TOL,TX}$[3]	reference/RXDATA frequency offset tolerance	0	0	0	ppm
$v_{IN,XS}$	Input swing, differential peak-peak	160	-	2000	mV
v_{SW}[4]	Output swing, differential peak-peak	800	-	1600	mV
$S_{11,IN,XS}$	Differential input return loss 0.1-2.5 GHz	10	-	-	dB
$S_{11,IN,XS,CM}$	Common mode input return loss 0.1-2.5 GHz	6	-	-	dB
S22,OUT,XS,625MHz	Differential output return loss @ 625 MHz	10	-	-	dB
$S_{22,OUT,XS,1563MHz}$	Differential output return loss @ 1.563 GHz	6	-	-	dB
$S_{22,OUT,XS,3125MHz}$	Differential output return loss @ 3.125 GHz	3	-	-	dB

1. Sinusoidal jitter is added to a stressed eye containing 0.37 UIpp of deterministic jitter and 0.55 UIpp of total jitter. This specification includes all but 10^{-12} of the jitter population.
2. The XAUI CDR (TXDATA) reference source and frequency will vary depending on the mode of operation. See the parallel input receiver functional description for more details.

3. The XAUI transmitter (RXDATA) will always transmit at the same frequency as its reference clock. However, the reference clock may be derived from the parallel input receiver recovered clock. See the serial output transmitter functional description for more details.
4. Measured with single ended termination resistance of 50Ω, VDD = VTERM = 1.2V. This value is programmable via register settings.

16.4 CMU_REF Clock Input

The reference clock CMU_REF, described in Section 9, is designed to be AC coupled as shown in Figure 48. The AEL2005 sets the desired input common mode internally.

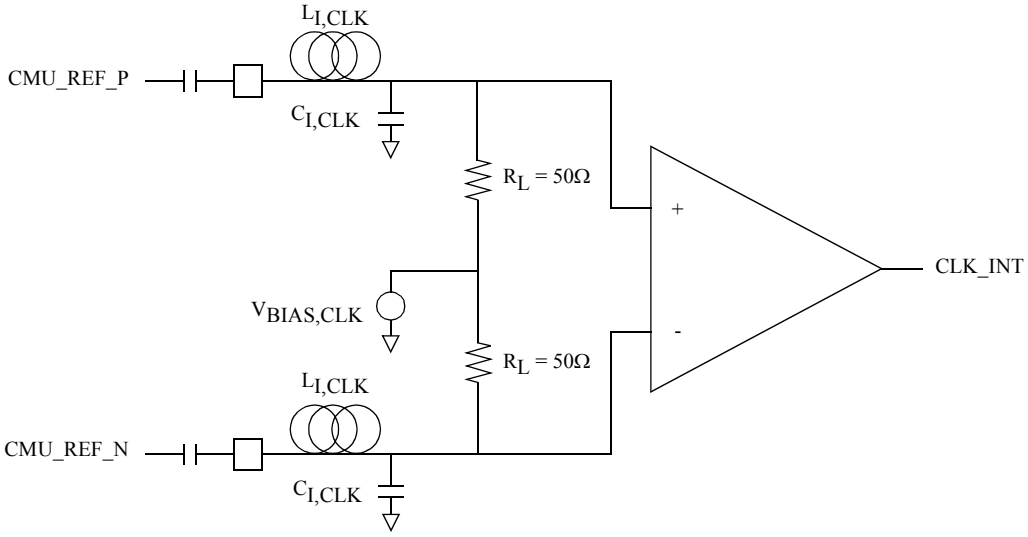


Figure 48. CMU_REF Representative Circuit

The AEL2005 device also supports a 50 MHz CMOS clock source for low cost operation. For operation with a CMOS clock, two additional components are required, as outlined in Figure 49.

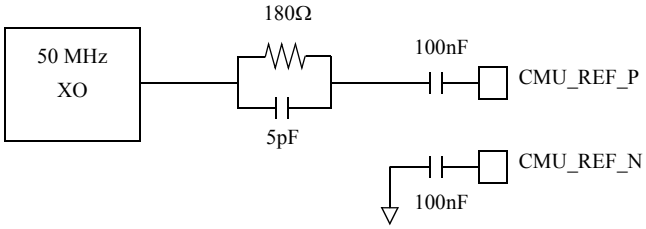


Figure 49. CMOS Clock Source Configuration

The specifications for CMU_REF are shown in Table 136.

Table 136. CMU_REF Specifications

Name	Description	Min	Nom	Max	Units
f_{REF}	Clock frequency	50	-	160	MHz
$t_{DUTY,REF}$	Clock duty cycle	40	50	60	%
$t_{R,CLK}/t_{F,CLK}$	Input signal rise/fall times (20% - 80%)	200	500	650	ps
$v_{IN,CML}$	Differential peak-peak input swing	400	-	2400	mV
$R_{L,CLK}$	Input termination resistance	40	50	60	Ω
$L_{I,CLK}$	Input inductance	-	-	4	nH
$C_{I,CLK}$	Input capacitance	-	-	5	pF

16.5 CMOS Interface

AC and DC specifications for the CMOS inputs and outputs are listed in Table 137. Since all these signals are asynchronous, there are no setup or hold times defined. The CMOS pins are defined in the General Control and Configuration portion of Table 15 in Section 14, "Pin Descriptions".

Table 137. CMOS I/O Specifications

Name	Description	Min	Nom	Max	Units
$V_{IL,CMOS}$	CMOS input low voltage	-0.3	0	0.36	V
$V_{IH,CMOS}$	CMOS input high voltage	0.8	-	3.6	V
I_I[1]	CMOS input leakage current	-1	-	1	uA
I_{OFF}[2]	CMOS off output current	-1	-	1	uA
$I_{OL,CMOS}$	Output current for VOL = 0.2V	4.0	-	20	mA
$L_{I,CMOS}$	CMOS I/O inductance	-	-	8	nH
$C_{I,CMOS}$	CMOS I/O capacitance	-	-	5	pF

1. Measured at compliance voltages of 0-V and 3.3-V.
2. Measured at a compliance voltage of 3.3-V.

16.6 MDIO Interface

The Management Data Input/Output (MDIO) port, described in Section 11, complies with Clause 45 of the IEEE 802.3ae specification. A representative MDIO driver/receiver is shown in Figure 50. MDIO uses an open drain driver with a pullup resistor to 1.2V. The MDIO pins are identical in implementation to the AEL2005 CMOS pins, but are described herein in comparison with the MDIO specification.

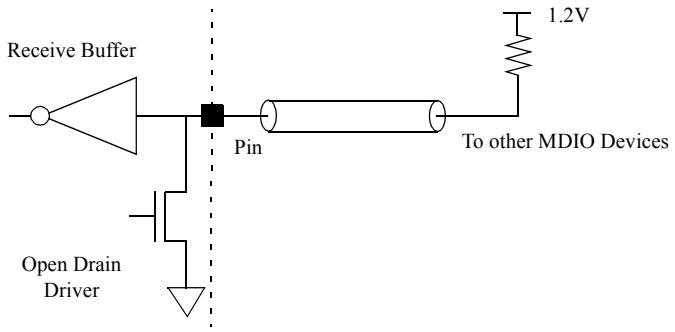


Figure 50. Representative MDIO Circuit

Representative MDIO Read and Write waveforms are shown in Figure 51. The AEL2005 samples MDIO on the rising edge of MDC for input and drives MDIO after the rising edge of MDC for output. Note that setup, hold, and output timings are defined from the maximum v_{IL} and minimum v_{IH} levels.

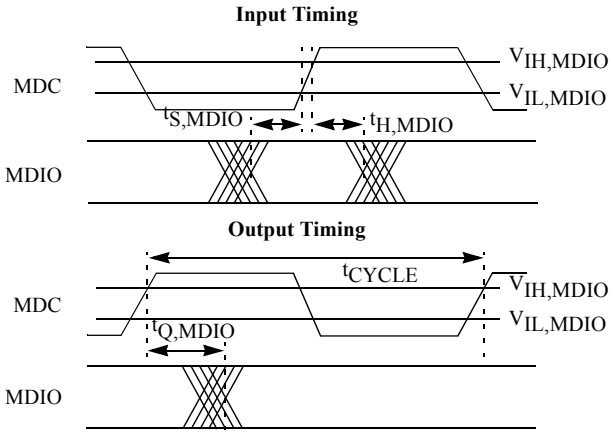


Figure 51. MDIO Input and Output Waveforms

Values for MDIO parameters are shown in Table 138.

Table 138. MDIO DC and AC Characteristics

Name	Description	Min	Nom	Max	Units
$t_{CYCLE,MDIO}$	MDC cycle time	400	-	-	ns
$t_{LOW,MDC}$	MDC low time	160	-	-	ns
$t_{HIGH,MDC}$	MDC high time	160	-	-	ns
$t_{S,MDIO}$[1]	MDIO input to MDC setup time	10	-	-	ns
$t_{H,MDIO}$[2]	MDC to MDIO input hold time	10	-	-	ns
$t_{Q,MDIO}$[3]	MDC to MDIO output time	0	-	150	ns
$V_{IL,MDIO}$	MDIO input low voltage	-0.3	0	0.36	V
$V_{IH,MDIO}$	MDIO input high voltage	0.84	-	3.6	V
$I_{I,MDIO}$[4]	MDIO leakage current	-1	-	1	uA
$I_{OL,MDIO}$	MDIO Output current for VOL = 0.2V	6.5	-	20	mA
$dI_{OL}/dt_{,MDIO}$	MDIO Output current rate of change	-10	-	10	mA/ns
$L_{I,MDIO}$	MDIO input inductance	-	-	8	nH
$C_{I,MDIO}$	MDIO input capacitance	-	-	5	pF

1. Measured from minimum MDIO V_{IH} to maximum MDC V_{IL} for MDIO rising edge.
   Measured from maximum MDIO V_{IL} to maximum MDC V_{IL} for MDIO falling edge.
2. Measured from minimum MDC V_{IH} to maximum MDIO V_{IL} for MDIO rising edge.
   Measured from minimum MDC V_{IH} to minimum MDIO V_{IH} for MDIO falling edge.
3. This specification can be monitored via the settings available in Register 1.C017, bit 4, as outlined in Table 102.
   Measured from minimum MDC V_{IH} to maximum MDIO V_{IL} for MDIO rising edge and MDC rising edge.
   Measured from minimum MDC V_{IH} to minimum MDIO V_{IH} for MDIO falling edge and MDC rising edge.
   Measured from maximum MDC V_{IL} to maximum MDIO V_{IL} for MDIO rising edge and MDC falling edge.
   Measured from maximum MDC V_{IL} to minimum MDIO V_{IH} for MDIO falling edge and MDC falling edge.
4. Measured at compliance voltages of 0-V and 3.3-V.

16.7 SDA/SCL Interface

The SDA and SCL pins, described in Section 12, implement a 2-wire serial interface compatible with popular serial EEPROM and Diagnostic Monitor devices. As with MDIO, this serial interface has open drain drivers and an external pullup resistor. However, it has a higher input threshold because it is intended to communicate with 2.5V and 3.3V devices.

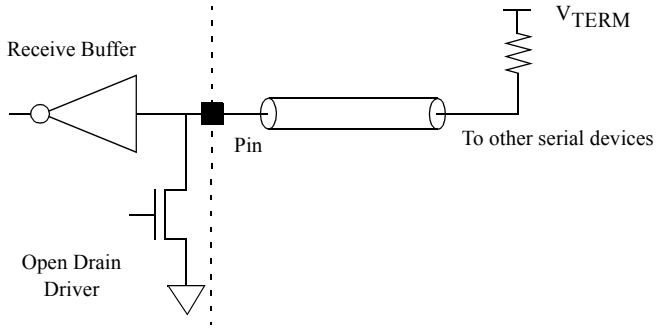


Figure 52. Representative SDA/SCL Circuit

Representative SDA and SCL data timing is shown in Figure 53. Because of the extremely low operating frequency of this bus, the same timing is used for data input to the AEL2005 and data output from the AEL2005. Note that setup, hold, and output timings are defined from the maximum V_{IL} and minimum V_{IH} levels.

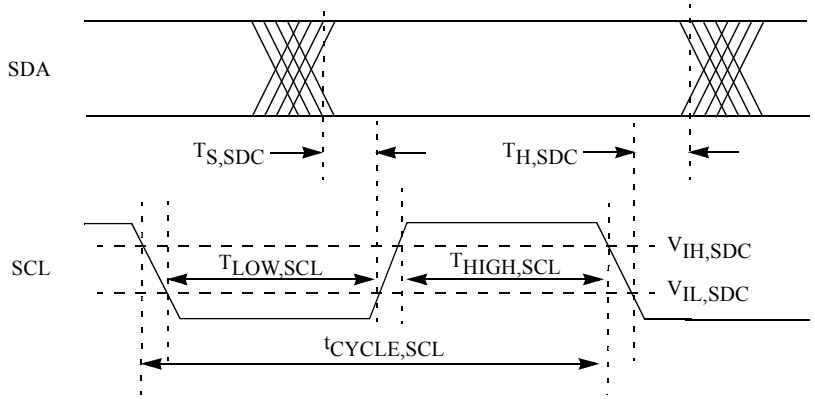


Figure 53. SDA/SCL Data Input and Output Waveforms

Timing for the start and stop conditions is shown in Figure 54. As described in the functional description of the serial bus, start and stop are special case situations where SDA transitions during the time that SCL is high. There are additional setup and hold constraints that apply to these transitions than are different than those for data.

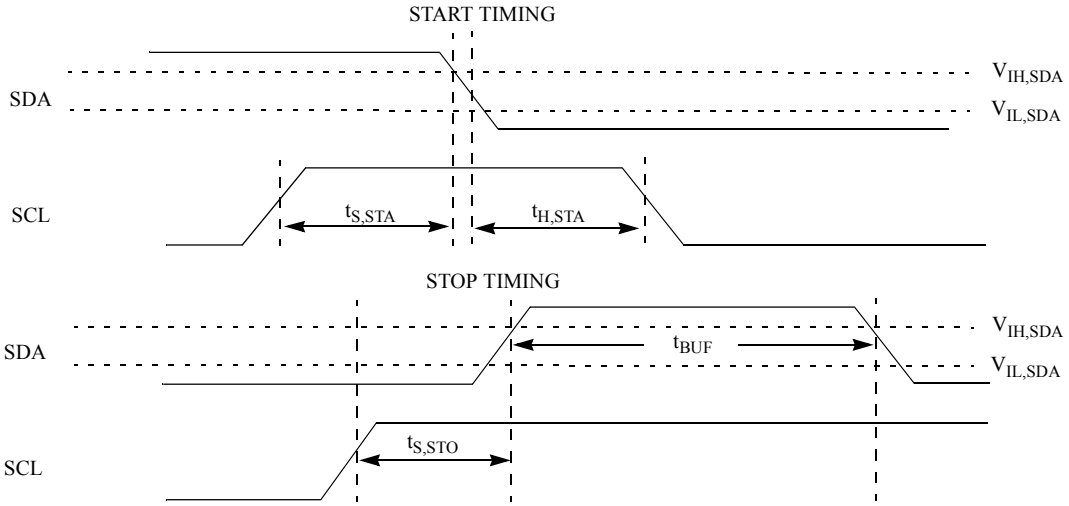


Figure 54. SDA/SCL Output Start and Stop Timing

Values for SDA/SCL parameters are shown in Table 139.

Table 139. SDA/SCL DC and AC Characteristics

Name	Description	min	nom	max	units
$t_{CYCLE,SCL}$	Serial bus cycle time	10	-	-	µs
$t_{LOW,SCL}$	SCL low time	4.7	-	-	µs
$t_{HIGH,SCL}$[1]	SCL high time	4	-	-	µs
$t_{S,SDC}$[1]	SDA to SCL rising edge setup time	250	-	-	ns
$t_{H,SDC}$[1]	SCL falling edge to SDA hold time	0	-	-	ns
$t_{S,STA}$[1]	SDA falling to SCL rising setup time for start bit	4.7	-	-	µs
$t_{H,STA}$[1]	SDA falling to SCL falling hold time for start bit	4	-	-	µs
$t_{S,STO}$[1]	SCL rising to SDA rising setup time for stop bit	4	-	-	µs
$t_{R,SDC}$[1]	Serial input rise times (10% - 90%)	20	-	1000	ns
$t_{F,SDC}$[1]	Serial input fall times (10% - 90%)	20	-	300	ns
$V_{IL,SDC}$	Serial data/clock low voltage	-0.3	-	0.3*VDDH	V
$V_{IH,SDC}$	Serial data/clock high voltage	0.7*VDDH	-	3.6	V
$I_{I,SDC}$[2]	SDA/SCL leakage current	-1	-	1	uA
$I_{OL,SDC}$	SDA/SCL output current for VOL=0.4V	3	-	25	mA
$dI_{OL}/dt_{,SDC}$	SDA/SCL output current rate of change	-10		10	mA/ns
$L_{I,SDC}$	SDA,SCL input inductance	-	-	8	nH
$C_{I,SDC}$	SDA,SCL input capacitance	-	-	5	pF

1. All output timings are defined for a maximum SDA/SCL capacitance of 400 pF. Setup and hold times assume equal capacitance on SDA and SCL.
2. Measured at compliance voltages of 0V and 3.3V

16.8 Power-On Sequence

The AEL2005 device power-on sequence is described in this section. During the configuration process, several internal device operations occur: The contents of external NVR EEPROM and DOM register spaces are read through the AEL2005 SDA/SCL interface, internal circuitry is brought up to speed and PLLs calibrated, and internal registers are set to their default values. Timing specifications for these steps are shown below.

16.8.1 Basic AEL2005 Device Power-On Sequence

The basic AEL2005 device power-on sequence is shown in Figure 55. In this configuration, after both power supplies have reached the 90% mark, 4 distinct timing stages occur prior to completion of device configuration. The first, represented by T_{rst}, represents the power-on reset (POR) requirement for the AEL2005 device, and reflects the Aeluros recommendation that the external RESET_N pin be held low by the system during and shortly after the initial power supply ramp. The next two, T_{NVR} and T_{DOM}, represent internal device activity relating to the upload of the NVR and DOM memories, respectively, via the SDA/SCL interface. The final, T_{wait}, represents the final configuration step, after which the device is ready for full operation.

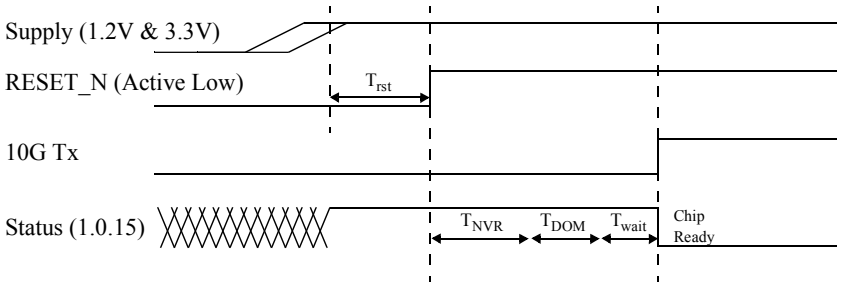


Figure 55. Standard Power-On Sequence

16.8.2 AEL2005 Device Low Power Startup (LPS) Power Sequencing

The XENPAK Low Power Startup (LPS) AEL2005 device power-on sequence is shown in Figure 56. In this configuration, the external TX_ON pin provides a system-controlled input to delay device power-up. In this case, after the T_{wait} time window has completed, the AEL2005 device returns to a power-down state until the TX_ON pin is pulled high. One final delay, T_{txon_delay}, is then introduced between release of the TX_ON pin and the AEL2005 device being available for use.

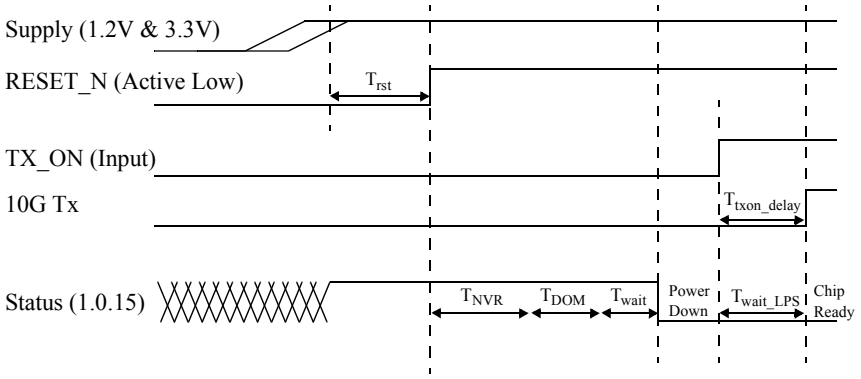


Figure 56. LPS Power-On Sequence

16.8.3 AEL2005 Device TX_ON Timing

AEL2005 device TX_ON timing is represented in Figure 57. In this figure, device operation of a fully powered-on device is shown during and after application of the TX_ON pin.

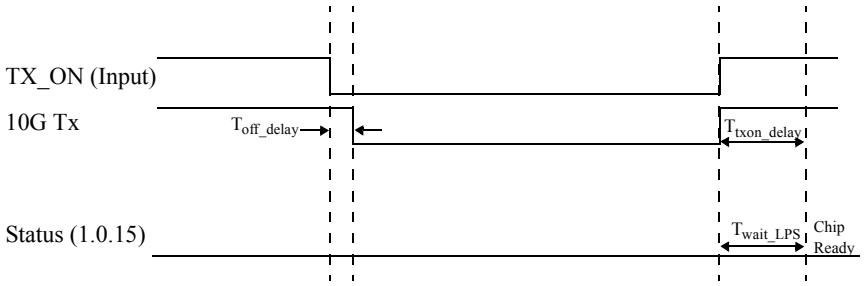


Figure 57. TX_ON Timing Sequence

16.8.4 Power-on Timing Specifications

Timing specifications associated with these sequences are shown in Table 140.

Table 140. Power-on Timing Specifications

Name	Description	Min	Nom	Max	Units
T_{rst}	Time delay between power supply reaching threshold limit and reset signal	100			us
T_{wait}	Power on autoconfiguration - internal circuits			25	ms
T_{NVR}	Power on autoconfiguration - NVR upload			65[1]	ms
T_{DOM}	Power on autoconfiguration - DOM upload			30	ms
T_{txon_delay}	LPS power on delay - 10 Gbps transmit drivers			25	ms
T_{wait_LPS}	LPS power on delay - Status signal			25	ms
T_{off_delay}	LPS power down delay			100	ns

1. The T_{NVR} Max value is 65 ms only if FC mode is selected by patching register bit 1.C001.14 to 1. If FC mode is not selected then T_{NVR} Max is at 43 ms. For more details on NVR operation in FC mode, please refer to the Puma AEL2005 Fibre-Channel Mode EEPROM Operation.

16.9 Operating Conditions

Table 141. Operating Conditions

Name	Description	Min	Nom	Max	Units
T_C	Case temperature under bias	0	25	85	^oC
VDD	Core power supply voltage	1.14	1.2	1.26	V
VDDH	I/O power supply voltage	3.15	3.3	3.45	V
IDD	Core power supply current	-	1220	1300	mA
IDDH	I/O power supply current	60	61	62	mA
HSTXCLK Current	Additional current from Vdd for HSTXCLK	30	40	50	mA
HSTXCLK Current (2)	Additional current from Vddh for HSTXCLK	7	8	10	mA
$\Theta_{JA\ BGA}$	Junction-to-ambient thermal resistance	-	28	-	$^oC/W$
$\Theta_{JA\ QFN}$	Junction-to-ambient thermal resistance	-	25	-	$^oC/W$
	Power consumption	-	1660[1]	-	mW
	Power consumption (power-down mode)	-	-	80	mW

1. Normal operating conditions with on chip crystal oscillator powered down, XAUI output swing at 400mV diff p-p and slow edge rates on 10G transmitter

Table 142. Absolute Maximum Ratings

Name	Description	Min	Nom	Max	Units
VDD	Core power supply voltage	-	-	1.5	V
VDDH	I/O power supply voltage	-	-	3.6	V
V_{XAUI}	Voltage applied to XAUI pins	-0.4	-	2.3	V
V_{CMOS}	Voltage applied to CMOS pins	-0.7	-	3.7	V
T_S	Storage temperature	-40	-	125	^oC
$V_{ESD,10G,HBM}$	Electrostatic discharge tolerance for HSTXDATA, HSRXDATA, and HSTXCLK, Human Body Model	500	-	-	V
$V_{ESD,10G,CDM}$	Electrostatic discharge tolerance for HSTXDATA, HSRXDATA, and HSTXCLK, Charged Device model	250	-	-	V
$V_{ESD,HBM}$	Electrostatic discharge tolerance for pins not covered by $V_{ESD,10G}$, Human Body Model	2000	-	-	V
$V_{ESD,CDM}$	Electrostatic discharge tolerance for pins not covered by $V_{ESD,10G}$, Charged Device Model	500	-	-	V

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

17 Mechanical Specifications

The AEL2005 is housed in one of the following packages:

- 196-pin PBGA
- 124-pin QFN

17.1 196-Pin PBGA Package

The 196-pin PBGA package has a 1.0 mm pad spacing. Figure 58 shows a package outline drawing of the AEL2005 device.

- All dimensions are in millimeters (mm)
- Terminal positions are designated per JESD 95-1, SPP010

The pin 1 identifier can be chamfer, ink mark, or metallized mark. However, it will be within the indicated zone.

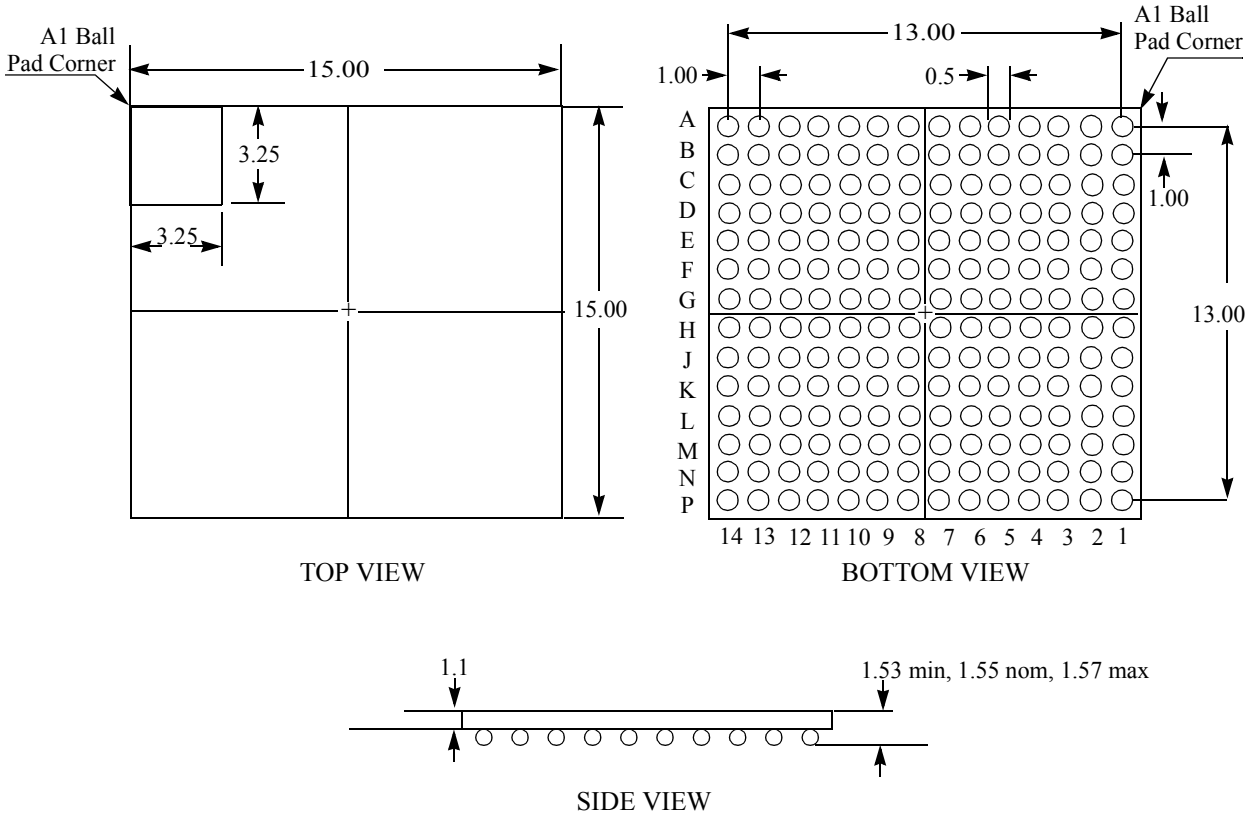


Figure 58. AEL2005 PBGA Package Drawing

Figure 59 shows a top view of the AEL2005 PBGA package, also known as the PCB view.

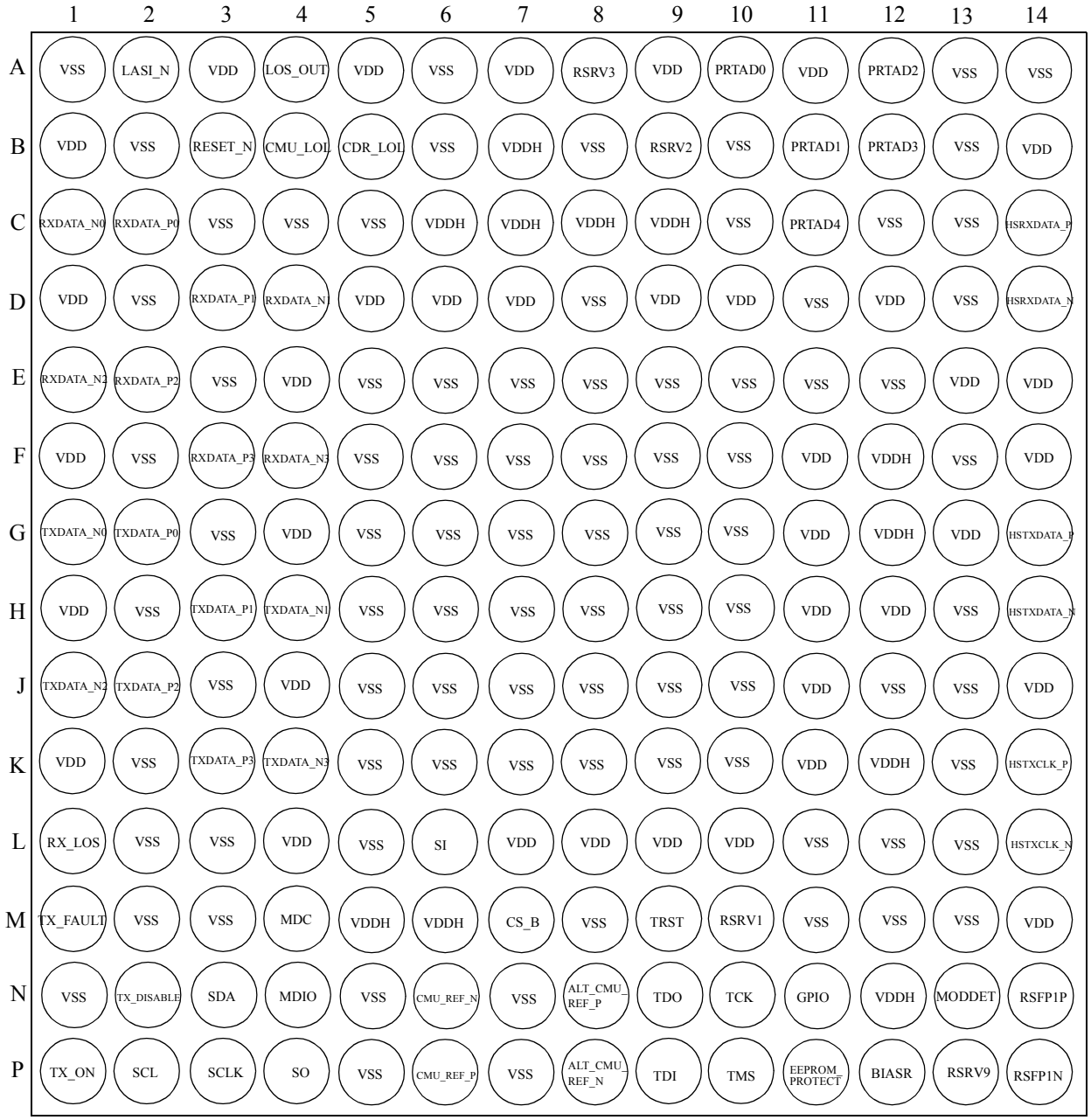


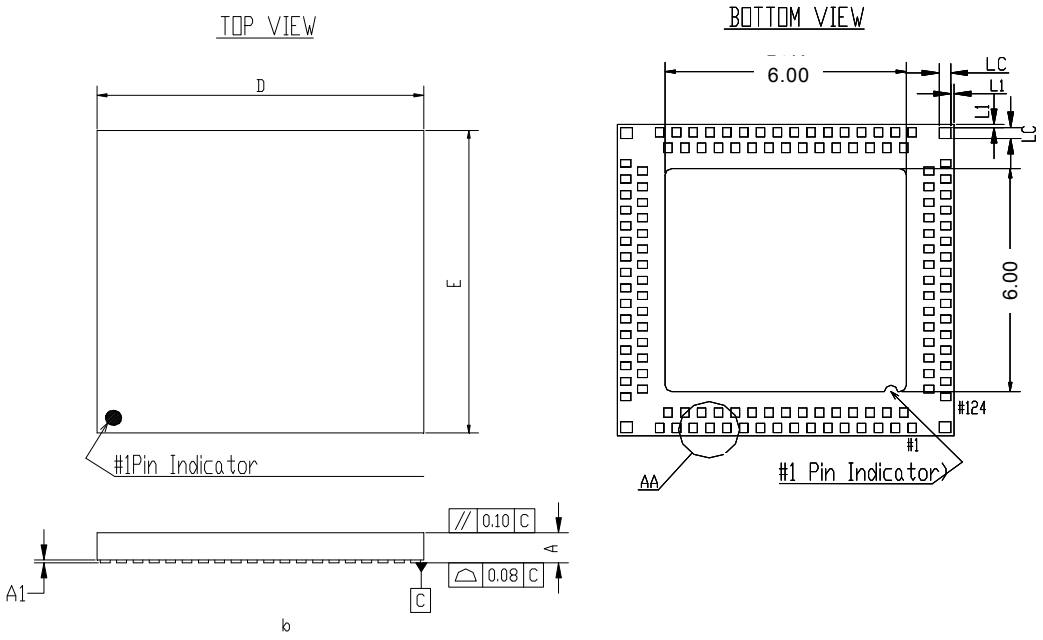
Figure 59. AEL2005 PBGA Package Pinout — Top View

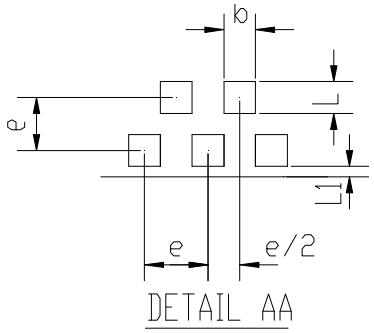
Note: All N/C (No Connect) pins are required to be left as no connect. Do not ground the N/C pins.

17.2 124-Pin QFN Package

The 124-pin QFN package has a 0.5 mm pad spacing. Figure 60 shows a package outline drawing of the AEL2005 device in a QFN package.

- All dimensions are in millimeters (mm)
- All dimensions are in millimeters
- Dimensional tolerance unless otherwise specified +/-0.10
- The surface of the package shall be RZ 4-8um
- Protrusions of package outline shall not exceed 0.10





SYMBOL	COMMON DIMENSIONS		
	MIN	NOM	MAX
D	9.90	10.00	10.10
D1	—	—	—
E	9.90	10.00	10.10
E1	—	—	—
V	—	—	—
A	0.80	0.85	0.90
A1	—	—	0.10
e		0.50	
b	0.25	0.30	0.35
L	0.25	0.30	0.35
L1	0.05	0.10	0.15
LC	0.30	0.35	0.40

Figure 60. AEL2005 124-Pin QFN Package Drawing

Figure 61 shows the package pinout for the AEL2005 when housed in the QFN package.

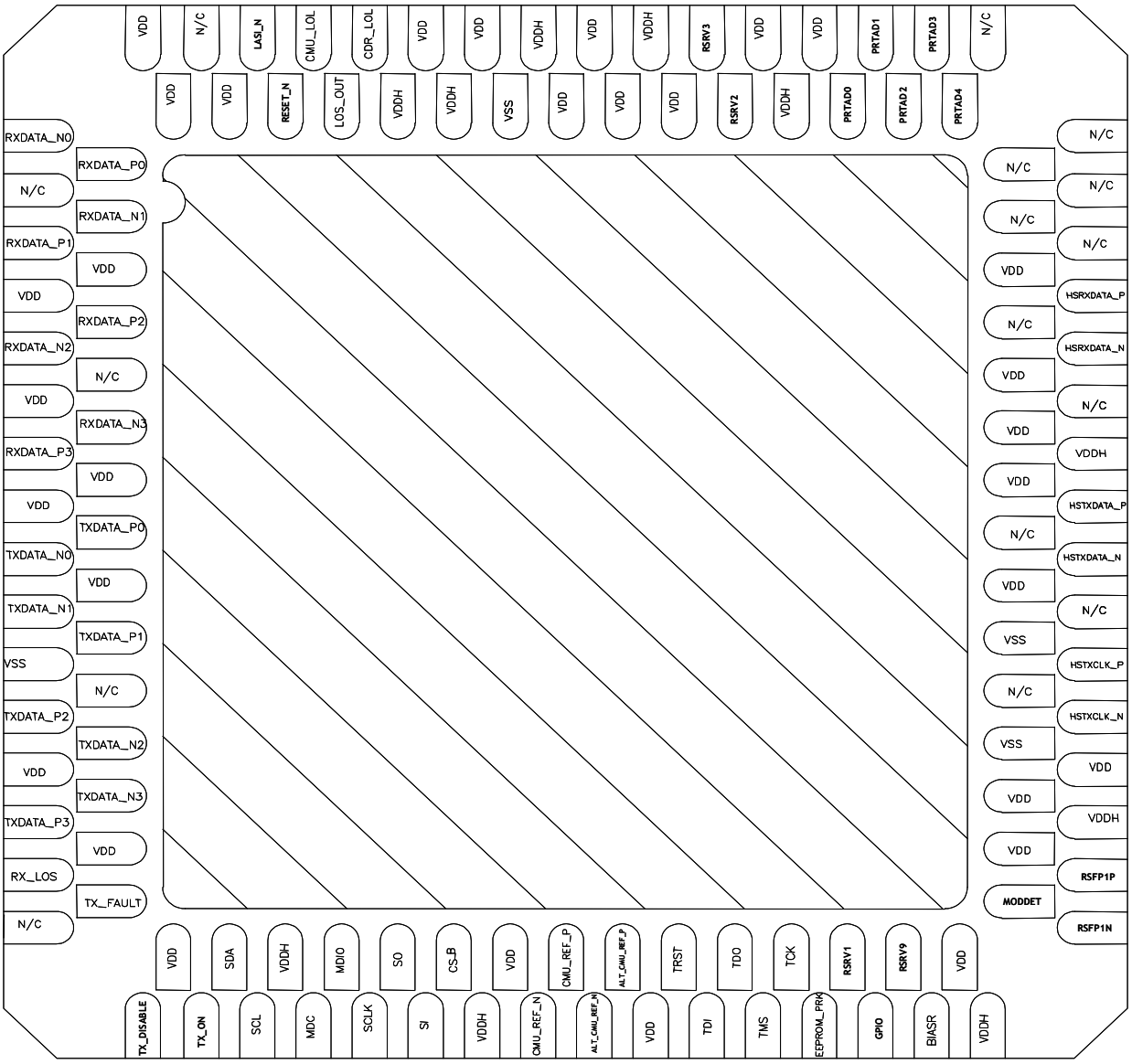


Figure 61. AEL2005 Package Pinout

Note: All N/C (No Connect) pins are required to be left as no connect. Do not ground the N/C pins.

18 Boundary Scan Test Access Port (TAP)

The AEL2005 includes a Test Access Port compatible with the IEEE 1149.1 (JTAG) standard.

The AEL2005 implements the BYPASS, SAMPLE, PRELOAD, and EXTEST commands. The optional INTEST, RUNBIST, CLAMP, and HIGHZ commands are not supported.

The AEL2005 does not include a device identification register, so the IDCODE and USERCODE functions are not implemented. Table 143 shows the AEL2005 boundary scan register order.

As per the JTAG requirements, Register 1 is closest to TDO, while register 25 is closest to TDI.

Table 143. Boundary Scan Register Order

Number	Name	Function
1	TX_DISABLE_data	Output data for TX_DISABLE.
2	CDR_LOL_data	Output data for CDR_LOL.
3	LOS_OUT_data	Output data for LOS_OUT.
4	CMU_LOL_data	Output data for CMU_LOL.
5	LASI_N_data	Output data for LASI_N.
6	LASI_en	Output enable for LASI.
7	MDIO_OUT_data	Output data for MDIO.
8	MDIO_en	Output enable for MDIO.
9	SCL_OUT_data	Output data for SCL.
10	SCL_en	Output enable for SCL.
11	SDA_OUT_data	Output data for SDA.
12	SDA_en	Output enable for SDA.
13	TX_ON_data	Received data on TX_ON.
14	RX_LOS_data	Received data on RX_LOS.
15	TX_FAULT_data	Received data on TX_FAULT.
16	EEPROM_PROTECT_data	Received data on EEPROM_PROTECT.
17	MDC_data	Received data on MDC.
18	MDIO_IN_data	Received data for MDIO.
19	SCL_IN_data	Received data for SCL.
20	SDA_IN_data	Received data for SDA.
21	PRTAD[4]	Received data on PRTAD[4].
22	PRTAD[3]	Received data on PRTAD[3].
23	PRTAD[2]	Received data on PRTAD[2].
24	PRTAD[1]	Received data on PRTAD[1].
25	PRTAD[0]	Received data on PRTAD[0].

19 Ordering Information

Table 144 describes the ordering codes for Puma AEL2005 devices.

Table 144. Puma AEL2005 Ordering Information (PBGA Package)

Ordering Code	Element Type	Element	Description
AEL2005-1B15C	Aeluros Identifier	AEL	
	Device Type	2005	Puma EDC for SFP+ applications
	Speed/Power Grade	1	Standard speed and power
	Package Type	B15	15mm x 15mm BGA package
	Temperature Grade	C	Commercial temperature
AEL2005-1G15C	Aeluros Identifier	AEL	
	Device Type	2005	Puma EDC for SFP+ applications
	Speed/Power Grade	1	Standard speed and power
	Package Type	G15	15mm x 15mm green (lead-free) package
	Temperature Grade	C	Commercial temperature

Table 145. Puma AEL2005 Ordering Information (QFN Package)

Ordering Code	Element Type	Element	Description
AEL2005-1Q10C	Aeluros Identifier	AEL	
	Device Type	2005	Puma EDC for SFP+ applications
	Speed/Power Grade	1	Standard speed and power
	Package Type	Q10	10mm x 10mm QFN package
	Temperature Grade	C	Commercial temperature