AuthenTec, Inc.
Personal Security for the Real World™

EntréPad AES2510 FINGERPRINT SENSOR

Product Family Specification

For Serial or Parallel Interface Applications

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Product Specification for the AES2510 Fingerprint Sensor

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1. Introducing the EntrePad AES2510 Slide Sensor…

…, the latest, lowest cost fingerprint sensor IC. AuthenTec has adapted its patented, award winning TruePrint Technology to read fingerprints while the finger is pulled across the AES2510's rectangular surface. In this manner, the fingerprint images are acquired AND the sensor is substantially reduced in size.

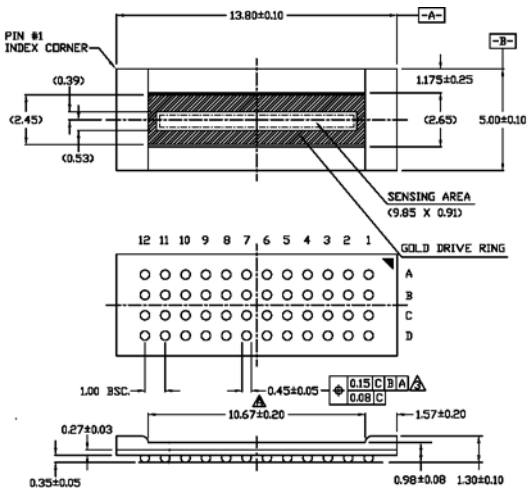
The AES2510 combines both an advanced Master-mode Serial Peripheral Interface with an on-chip DMA engine as well as a convenient easy-to-use 8-bit parallel interface. These interfaces permit easy integration with nearly all of the top baseband and application processors utilized in mobile phones.

1.1 TruePrint Technology is…

…AuthenTec's unique patented fingerprint reading technology. During imaging, a small signal is generated between the IC and the finger's living tissue layer. 3072 individual sensing elements in the slide sensor matrix form a planar antenna array that receives this signal, creating a digital pattern that accurately reproduces the fingerprint's underlying structure.

A powerful utility contained within TruePrint Technology™ is Dynamic Optimization™. This tool analyzes each image, controlling a variety of parameters real-time to optimize the fingerprint image slices, regardless of skin conditions or surface contamination.

1.2 Feature Summary



- ✓ Patented TruePrint Technology for best Ability To Acquire (ATA)
- ✓ High Definition 192 X 16 TruePrint Technology Based Pixel Array
  - o 500 pixels per inch (ppi) native
  - o 9.75mm X 0.81mm array area
- ✓ Compact 48 Ball Grid Array (BGA) Pkg.
  - o 13.8mm X 5mm X (1.3mm or 1.96mm)
- ✓ Extended Operating Voltage Range
  - o 2.4V to 3.6V single supply
- ✓ -20°C to +70°C Mobile Phone Compatible Operating Temperature Range
- ✓ Easy to Integrate System Interfaces
  - o 8-bit Parallel
  - o Synchronous Serial (SPI™ & McBSP™ compatible) Master & Slave mode
  - o On-chip DMA support for simplified image slice transfer during authentication
- ✓ Operation with Crystal, Resonator, or with external clock input
- ✓ Ultra-hard scratch resistance surface coating > 10 Million rubs w/o degradation
- ✓ IEC 61000-4-2 Level 4 ESD Immunity (+/- 15KV)
- ✓ Built-in low power Finger Detection w/system interrupt capability
- ✓ Multiple battery-friendly operating modes @ 2.5V
  - o Imaging @ <38mA typ.
  - o Graphical Cursor Control mode @ < 2 mA typ.

1.3 Conventions

For vectors (groups of bits), ordering will always be from most significant to least significant bit (MSB to LSB, e.g. Pixel_Data[63:0] where bit 63 is the MSB and bit 0 is the LSB).

When vectors that span multiple bytes are transmitted, the lower byte (bits [7:0]) is transmitted first. This applies to pixel data and the authentication word returned after each imaging frame.

Numbers followed by a 'b' are shown in binary. Numbers followed by an 'h' are in hexadecimal.

1.4 Operational Description

The Sensor begins operation in the 'idle' state after a reset. In the idle state, array power is turned off and clocking is disabled (except interface activity). It is then necessary for the system SW to setup the sensor for the desired operation (Imaging or Navigation). The requested operation is enabled by setting the Sensor Mode bits (located in Register 80h:D3-D2). If Imaging is selected, the Sensor enters finger detect mode checks for a finger present at a rate programmed by the Finger Detect Rate setting. The default reset value sets the detect period to ~62 ms.

After finger detection, the sensor will begin the programmed operation and will enter Imaging mode until the finger is removed. Once the finger is removed, the sensor returns to the Low Power Finger Detect mode. When no activity is detected on the system interface bus for approximately 200uS, power is reduced by disabling the internal clocks and the array power is once again turned off.

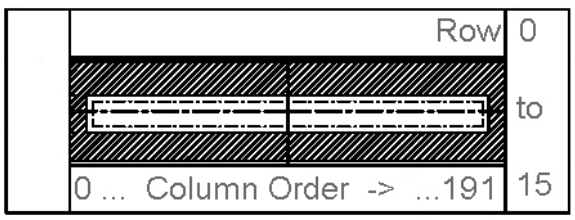


Figure 1-1 Column and Row Numbering

The array consists of 192 columns of 16 pixels each. During imaging, the columns are powered up and the signals from each of the 16 pixels/column are sampled, digitized and returned to the host computer over the selected interface sequentially in order on a per-column basis. The sensor has the capability to utilize only the center 128 columns during imaging mode to facilitate higher finger sliding speeds. During fingerprint enrollment, a 192 pixel wide template is created. Then, optionally, either a 192 pixel wide or 128 pixel wide verify can be performed. This mode is

entirely controlled via software using sensor register settings for start and stop columns.

If the finger detect is not active when it is rechecked at the end of a scan, the array is powered down and the sensor reverts back to checking for a finger at the programmed detect rate.

AuthenTec has application notes to support the integration of the AES2510 for all available interface options. Contact AuthenTec for availability.

1.4.1 Idle Mode

In Idle Mode the Sensor does not perform any finger detect functions since imaging and navigation modes are disabled (analog power remains off and the finger ring is never driven). The sensor will respond to read register commands. Timer 1 and Timer 2 are available to be used as interval timers. They are started by bits in REG80 and return REG9B when complete.

1.4.2 Imaging Mode

The on-chip imaging buffers affect imaging only when slave interfaces are selected. Master interfaces send data when it becomes available.

1.5 Navigation Using the AES2510

There are two navigation modes offered by the AES2510. Mode 1 provides for simple menu scrolling, the typical Left / Right / Up / Down button functionality can be easily emulated on the sensor by statically touching the sensor to indicate desired left or right direction and by sliding the finger at normal finger speeds in the up or down direction to indicate up or down. This mode is identical to the functionality contained within the AES250x products. Mode 2 navigation is a hardware assisted full motion dx/dy system providing functionality similar to a touchpad on a PC. This functionality can be employed for a variety of applications where graphical cursor control is required.

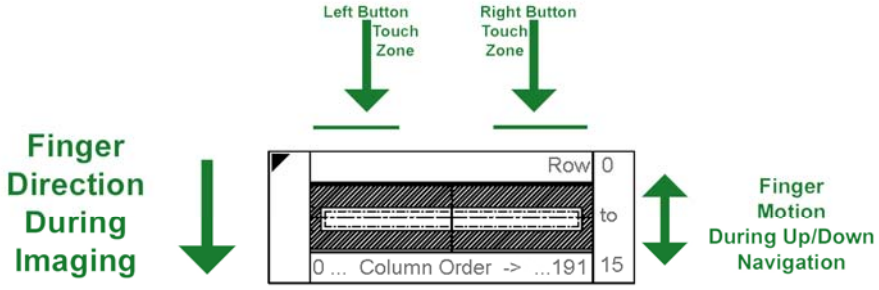
Mode 1 provides for 4 / 5 way navigation (NAV mode), the operations are enabled (via the SENSOR MODE bits as described previously) and Navigation mode is selected, the sensor will provide constant, periodic indications of direction and finger presence by sending a 2-byte message to the selected interface.

Nav Mode 1 (NAV) – cursor control mode

After NAV mode is enabled, the sensor takes 10 samples of the center column approximately every 100 us. After producing an output message, the sensor then enters a low power state for a programmable amount of

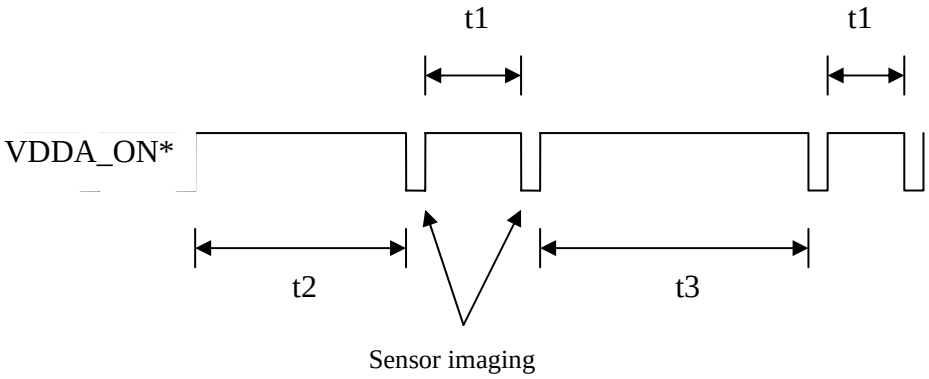
time, and then repeats the above sequence. Output generation rates are programmable and range from 100 Hz down to 26 Hz.

Figure 1-2 Cursor Control Navigation



Nav Mode 2 (NAVI) – graphical navigation mode

For accurate cursor placement the AES2510 has implemented an image-based navigation system supported by on-chip hardware timing of the images. By accurately timing the image capture, accurate dx/dy motions can be calculated. In this mode the sensor takes four images. The figure below shows the profile. The PWR_ON_N pin is low to turn analog power on for finger detect or imaging.



The Nav Mode 2 cycle starts with two image segments separated by a programmable delay t1. The t1 delay is controlled by the GP TIMER 1 value (REGBA and REGBB). The timer has a 14-bit range and 16 us resolution.

The two image segments are followed by a second programmable delay t2. The t2 delay is controlled by the GP TIMER 2 value (REGBC). The timer has a 7-bit range and 1 ms resolution. The t2 delay is followed by another set of two image segments also separated by the t1 delay.

These image segments are followed by a third delay t3. The t3 delay is controlled by the GP TIMER 3 value (REGBD). The timer has a 7-bit range and 1 ms resolution. The cycle then starts over.

If the Ultra Low Power bit (D6 in REG84) is set, the oscillator and PLL are shut off during the t2 and t3 delay periods. When the oscillator and PLL are re-started, there is a delay period where the clock output is blocked. The delay (tdelay) in milliseconds is set by the Osc On Delay field in REG94. The delays between the sets of image segments are extended to (t2 + tdelay) and (t3 + tdelay).

In Nav Mode 2, mode the sensor always behaves as if the column interrupt depth is set to 8. Image headers are disabled, authentication data is disabled, histogram messages are disabled, and register messages are disabled. The sensor now returns only navigation data.

The sensor uses the programmed register settings for gain, drive, frequency, column scan rate, start column, end column, and data format.

For master interfaces, image data is transmitted as it is captured. For slave interfaces, an interrupt (or data available) will be generated after 8 columns of data are available or the four image segment sequence is complete.

2. DC ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

An absolute maximum rating is the maximum value guaranteed by the AuthenTec. The use of a product in violation of these ratings can result in significant loss of device reliability or cause damage to the IC.

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	-0.5	4.3	V
V_I	Input Voltage	-0.5	V_{DD}+0.5	V
V_O	Output Voltage	-0.5	V_{DD}+0.5	V
I_{IK}	Input Clamp Current $V_I < V_{SS}$ of $V_I > V_{DD}$		±20	mA
I_{OK}	Output Clamp Current $V_O < V_{SS}$ of $V_O > V_{DD}$		±20	mA
T_{STG}	Storage Temperature	-65	150	°C
Latch-Up	Latch-Up Immunity	±100		mA
T_{SOL}	Maximum Soldering Temperature (MSL=3)		+240	°C
T_{SOL}	Maximum Soldering Temperature (MSL= TBD)		+260	°C

Figure 2-1 Absolute Maximum Ratings

2.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ	Max.	Units
V_{DD}	Power Supply Voltage	2.4	-	3.6	V
$V_{DDACp-p}$	Power Supply Ripple peak to peak	-50		+50	mV
V_I	Input Voltage	0		V_{DD}	V
V_O	Output Voltage	0		V_{DD}	V
V_{IH}	High Level Input Voltage	70% V_{DD}		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		30% V_{DD}	V
t_t	Digital Input Transition (Rise and Fall) Time	0		3	ns
T_A	Ambient operating temperature	-20		70*	°C

Figure 2-2 Recommended Operating Conditions

***Warning**

The AES2510 remains fully operational at temperatures that are high enough to be uncomfortable for the user.

For reasons of safety and protection, AuthenTec reference designs include circuitry that serves to manage the junction temperature by controlling the supply current. If the hardware developer elects not to use the AuthenTec-provided control circuit design, it will then be essential that an equivalent design be developed and implemented.

2.3 DC Characteristics @ Recommended Operating Conditions

Unless otherwise specified, $V_I = V_{DD}$ or V_{SS}, $T_{Ambient} = 25°C$

Symbol	Parameter	Conditions	Min.	Typ	Max.	Units
V_{OH}	High Level Output Voltage	I_{OH}=2mA	Vdd-0.3			V
V_{OL}	Low Level Output Voltage	I_{OL}=2mA			0.3	V
I_{IL}	Low Level Input Current	$V_I=V_{IL(min.)}$			±1	µA
I_{IH}	High Level Input Current	$V_I=V_{IH(max.}$			±1	µA
I_{OZ}	High Impedance State Output Current				±20	µA
Power Supply Currents						
I_{DDQ}	Supply Current Imaging mode	Vdd=2.5V		38	46	mA
I_{DDQ}	Supply Current Imaging mode	Vdd=2.8V		43	51	mA
I_{DDQ}	Supply Current Imaging mode	Vdd=3.3V		50	60	mA
I_{DDQ}	Supply Current Imaging mode (peak)	Vdd=3.6V		55	65	mA
I_{DDQ}	Supply Current Navigation or Finger Detect	Vdd=2.5V		2.3	2.8	mA
I_{DDQ}	Supply Current Navigation or Finger Detect	Vdd=2.8V		2.5	3.0	mA
I_{DDQ}	Supply Current Navigation or Finger Detect	Vdd=3.3V		3.0	3.6	mA
I_{DDQ}	Supply Current Navigation or Finger Detect	Vdd=3.6V		3.3	4.0	mA

Figure 2-3 DC Characteristics

All I_{DDQ} Currents measured RMS using standard AuthenTec software and drivers. Use of other software or customized register settings may effect actual power consumption.

3. Sensor Operation

3.1 Operation Description

During an imaging event, the RF TruePrint Signal is conducted via the Drive Ring to the users' finger. The TruePrint Signal is then conducted through and modulated by the "live layer" of the finger where the true fingerprint originates. The imaging array (center strip region of the chip) measures the TruePrint signal; the strength of which corresponds to either a ridge or valley region.

The image array of the AES2510 sensor is composed of 16x192 pixels. The array is scanned similarly to a sub-array in AuthenTec's touch sensors. During the imaging process, 16 pixels in a column are powered up, sampled, and converted to 4, 2 or 1-bit values. The high and low reference voltages for the ADC are programmable via 7-bit DACs.

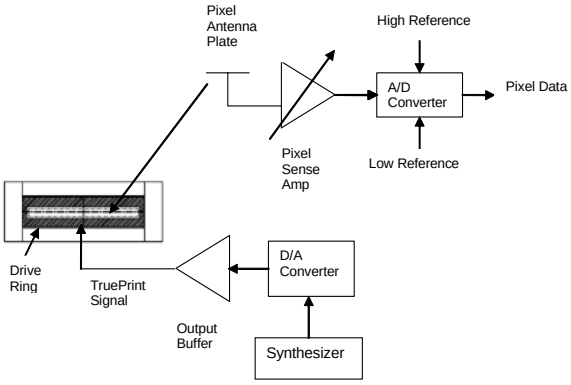


Figure 3-1 AES2510 Functional Diagram

The sensing element of each pixel is an RF sense-amplifier, which picks up the TruePrint (high frequency AC) signal (125 KHz – 2MHz) that is applied to the finger via the Finger Drive Ring located prominently on the top and bottom of the sensor surface. The pixel sense amps receive, amplify, and buffer the signal.

Each pixel output is then converted into a level corresponding to the strength of the received signal. Stronger signals are picked up from ridges than valleys. This output is converted by an A/D converter whose endpoints are adjustable via the Reference High and Reference Low voltages.

The AES2510 device has three selectable interfaces:
1) Asynchronous Serial up to 3Mbps
2) Synchronous Serial – SPI™ compatible (both clock normal and clock opposite) up to 8 Mbps in both slave and master modes
3) 8-bit parallel microprocessor interface running down to 110nS cycle time

4. Pin Definitions

4.1 Packaging Information

The AES2510 sensor is housed in either of two 48 Ball Grid Array packages.

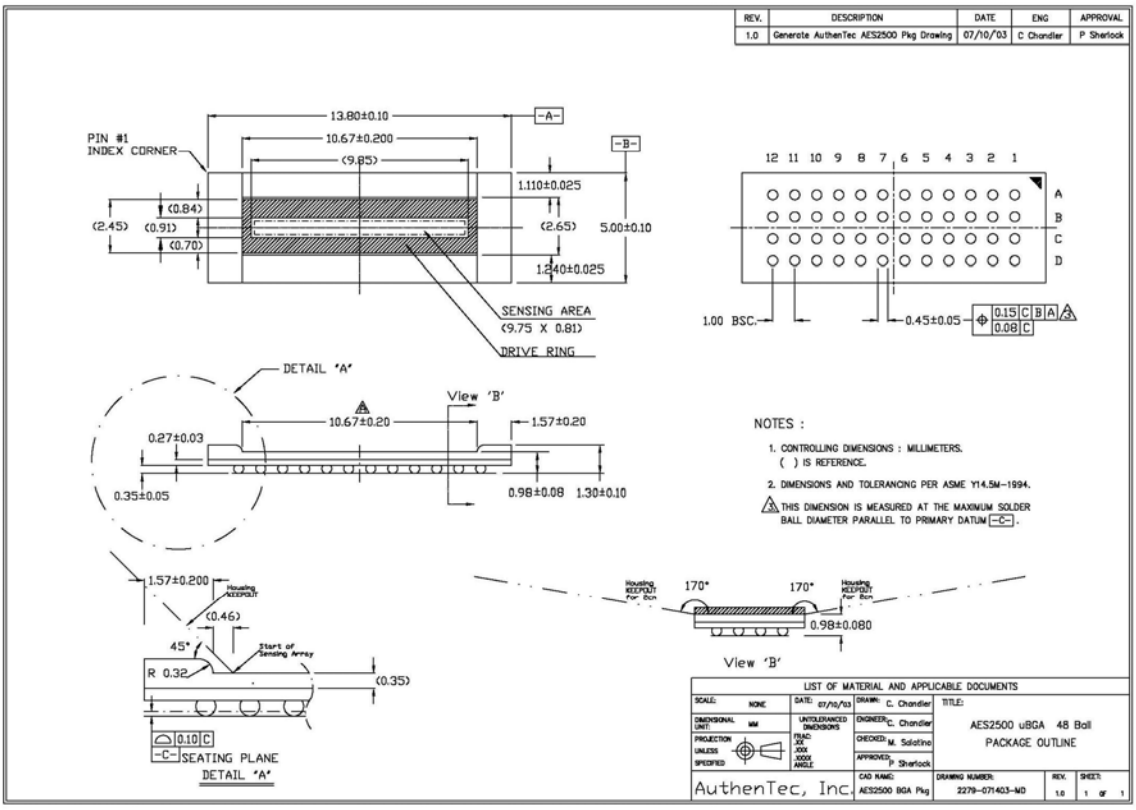


Figure 7 - 48 BGA - Thin Version

The package drawing shows both the mechanical dimensions of the package as well as recommended housing “keep-out” areas and angles of approach to and from the slide surface. For additional information, contact AuthenTec Applications Engineering for more details.

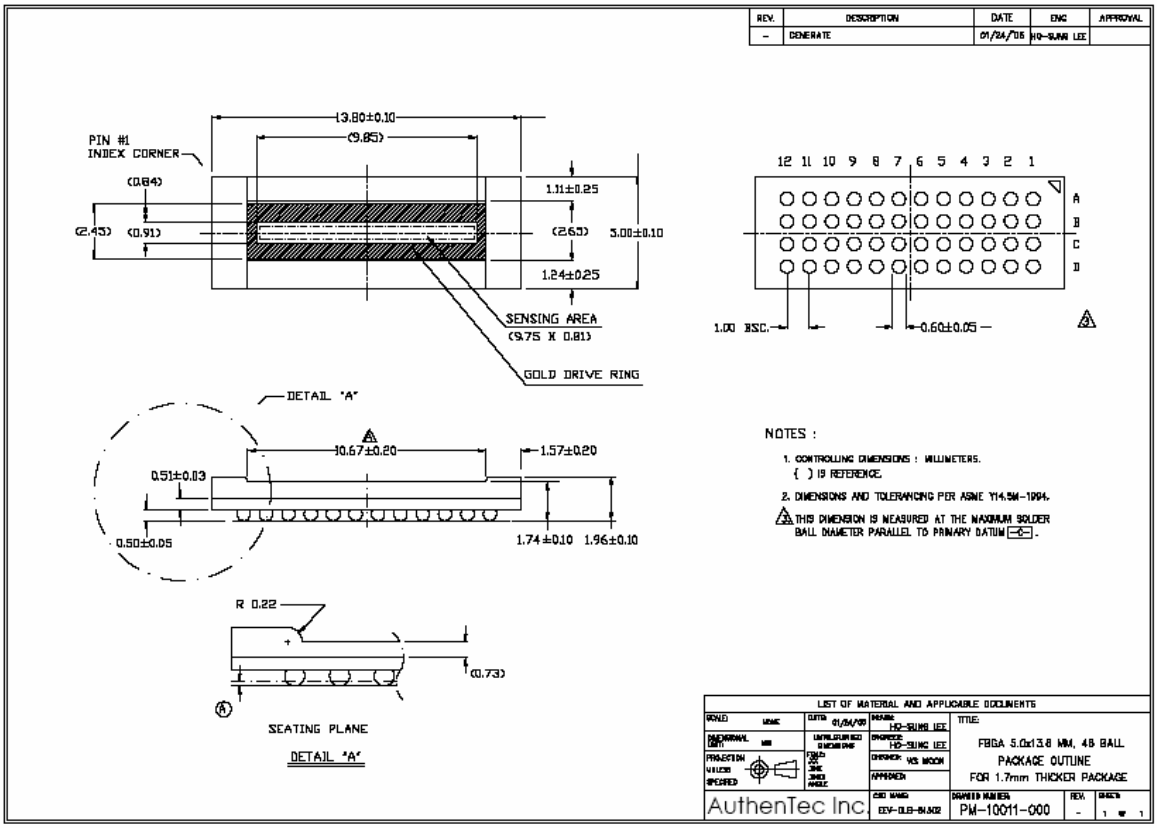


Figure 3 - 48 BGA Thick Style

It is important to note that the solder ball diameter for these two packages are not the same.

Other Information:

	Gold Ring	Nickel Ring
Package Mass:	0.1183g ±0.000388g	0.1159g±0.000877

4.2 Pin List

Interface Specific pin assignments and pin function descriptions of the AES2510 sensor are given below. Shared pin definitions for SIO[13:0] are selected by the state of the IOSEL[1:0] pins. Refer to section 5.1 for the interface-specific SIO definitions. The following pin list matches AuthenTec's certified reference designs. Certain pin functions will be required to change for other implementations.

Pin	Type	Digital Activity	Signal Name (Async Serial)	Signal Name (Sync. Serial)	Signal Name (8-bit Par)
A1	Passive	Static	VREF	VREF	VREF
A2	Passive	Static	CT2	CT2	CT2
A3	Passive	Static	CT1	CT1	CT1
A4	Output	Active	FINGERDRIVE	FINGERDRIVE	FINGERDRIVE
A5	Input	Static	RESET*	RESET*	RESET*
A6	Reserved		N/C	N/C	N/C
A7	Reserved		N/C	N/C	N/C
A8	Power		VDD	VDD	VDD
A9	Power		VSS	VSS	VSS
A10	Power		VDD	VDD	VDD
A11	Input	Active	SYS_CLK	SYS_CLK	SYS_CLK
A12	Output	Active	DRIVE_RING	DRIVE_RING	DRIVE_RING
B1	Input	Static	CLKSEL2	CLKSEL2	CLKSEL2
B2	Power		VSS	VSS	VSS
B3	Power		VDD	VDD	VDD
B4	Input	Static	VDDL	VDDL=Master out VSSL=Slave out	VSSL
B5	Input	Static	VSSL	VDDL	VSSL
B6	Input	Static	CLKSEL1	CLKSEL1	CLKSEL1
B7	I/O	Active	RTR	FS	D1
B8	I/O	Active	RXD	DR	D0
B9	I/O	Active	N/C	N/C	D7
B10	I/O	Active	N/C	SSI_NORM	D6
B11	I/O	Active	BAUD1	A0	D5
B12	I/O	Active	BAUD0	INT	D4
C1	Reserved		N/C	N/C	N/C
C2	Power		VSS	VSS	VSS
C3	Power		VDDA	VDDA	VDDA
C4	Input	Static	VSSL	VSSL	VSSL
C5	Input	Static	CLKSEL0	CLKSEL0	CLKSEL0
C6	Input	Static	VSSL	VSSL	VSSL
C7	I/O	Active	AUTOBAUD_EN	CLK	D2
C8	I/O	Active	TXD	DX	D3
C9	I/O	Active	N/C	N/C	A0
C10	Output	Active	VDDA_ON*	VDDA_ON*	VDDA_ON*
C11	I/O	Active	N/C	N/C	RD*
C12	Power		GPIO0	GPIO0	WR*
D1	Output	Active	DRIVE_RING	DRIVE_RING	DRIVE_RING
D2	Reserved		N/C	N/C	N/C
D3	Reserved		N/C	N/C	N/C
D4	Reserved		N/C	N/C	N/C
D5	Reserved		N/C	N/C	N/C

Pin	Type	Digital Activity	Signal Name (Async Serial)	Signal Name (Sync. Serial)	Signal Name (8-bit Par)
D6	Reserved		N/C	N/C	N/C
D7	Reserved		N/C	N/C	N/C
D8	I/O	Active	GPIO1	GPIO1	CE*
D9	I/O	Active	GPIO2	GPIO2	READY
D10	I/O	Active	GPIO3	GPIO3	INT
D11	Power		VSS	VSS	VSS
D12	Power		VDDA	VDDA	VDDA

Figure 4-4 Pin List by Interface

4.2.1 Pin Type and Activity Definitions

VDD, VSS:	Power Supply Connections
Passive:	Connections to passive components (ex: Filter caps, etc)
Input:	Active Inputs to the sensor
Output:	Active Outputs from the sensor
I/O:	Active I/O's from the sensor (state / configuration dependent)
Reserved:	Do Not Connect anything to these pins
Static:	DC or slowly changing voltages
Active:	Active Signals, Digital or Analog
VDDL:	Fixed Active High Logic Level
VSSL:	Fixed Active Low Logic Level
VDDA:	Pixel Array Power supply pin
N/C:	No Connection externally

4.3 Pin Descriptions (alphabetical listing)

Pin	Signal Name	Function Description
		For pins D8-D12, Refer to the appropriate AuthenTec Reference Design for connection details
C5	CLKSEL0	Clock input option selection. Refer to section 4.4
B6	CLKSEL1	Clock input option selection. Refer to section 4.4
B1	CLKSEL2	Clock input option selection. Refer to section 4.4
A3	CT1	Filter Capacitor - connect to pin A2 through a 0.1uF capacitor, standard bypass type
A2	CT2	Filter Capacitor - connect to pin A3 through a 0.1uF capacitor, standard bypass type
D1	DRIVERING	DriveRing - connection to the metal ring on the sensor surface. No other connections made.
A12	DRIVERING	DriveRing - connection to the metal ring on the sensor surface. No other connections made.
A4	FINGERDRIVE	TruePrint Signal output used to drive radio frequency signal through external circuitry to finger ring pins (A12 and D1). Controlled by internal excitation generator.
B4	IOSEL0	Interface option selection. Refer to Section 5.1
B5	IOSEL1	Interface option selection. Refer to Section 5.1
A5	RESET*	Reset input - 2/3 threshold voltage with hysteretic input. Approximately 57 Kohm pull-up resistor internal, with tolerance of 30%. See section 2.1 for additional definition of a proper reset.
B8	SIO0	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
B7	SIO1	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
C7	SIO2	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
C8	SIO3	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
B12	SIO4	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
B11	SIO5	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
B10	SIO6	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
B9	SIO7	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
C9	SIO8	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
C11	SIO9	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
C12	SIO10	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
D8	SIO11	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
D9	SIO12	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
D10	SIO13	Refer to Figure 5-2 SIO Pin Definitions for each Selected Interface Option
A11	SYS_CLK	Clock input pin - input clock used for all chip functions. See Figure 4-5 and Section 4.4 for input characteristics and requirements.
D12	VDDA	Pixel Array Power Connection
C3	VDDA	Pixel Array Power Connection
C10	VDDA_ON*	External Array Power FET control - If used this pin may drive a high side P-channel FET. See AuthenTec Reference Designs for connection details.
A1, A2, A3		N/C – Refer to AuthenTec reference design for appropriate connections

Figure 4-4 AES2510 Active Pin Functional Description

4.4 Clock Select Control

AES2510 can support a variety of clock sources, ranging in frequency from 6MHz up through 48MHz. The AES2510 uses a single pin crystal/resonator oscillator circuit that can also be overdriven with an external clock source capable of driving >+/-5mA. Clock frequency selection [including clocks driven into the SYS_CLK pin] is done via the CLKSEL[2:0] input pins. The following table shows the CLKSEL[2:0] pin configurations:

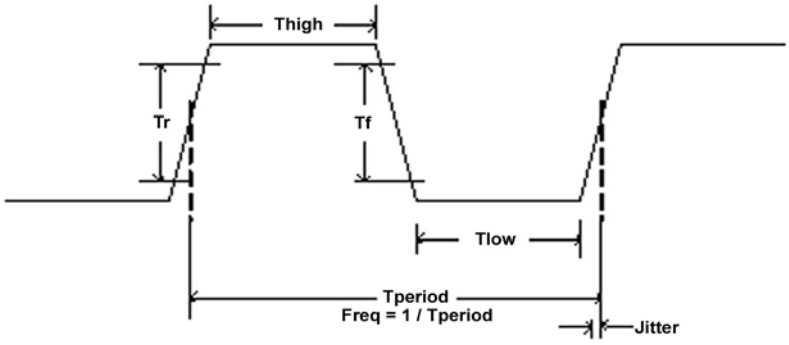
CLKSEL2 Pin B1	CLKSEL1 Pin B6	CLKSEL0 Pin C5	Crystal/Resonator or Clock Frequency Ranges
0	0	0	6 MHz
0	0	1	8 – 9.6 MHz
0	1	0	12 - 13 MHz
0	1	1	18 - 19.5 MHz
1	0	0	24 MHz
1	0	1	Reserved
1	1	0	Reserved
1	1	1	48 – 52 MHz (Direct Clock Input)

Table 4.2.1-1 CLKSEL[2:0] Decode

Frequency related operating parameters (e.g. asynchronous serial baud rates or excitation frequencies) are accurate when the internal clock (MCLK) is 48 MHz. Otherwise these parameters scale appropriately with the actual system clock frequency.

4.4.1 Clock Specification

For the AES2510, there are several different clocking options available: Crystal connection, ceramic resonator connection, and external clock driven. Appropriate application of clock sources is driven the desired circuit application (interface type) and reference design. This section addresses the specification requirements for an externally driven clock. All electrical and environmental conditions from the device specification apply as well. When driving an external clock into the SYSCLK device pin (A11), the following timing diagram applies:



[1]	Parameter	[1]	Minimum	[1]	Maximum
[2]	Freq.(Async. Serial Int.)	[2]	Freq.(nominal) – 1%	[2]	Freq.(nominal) + 1%
[3]	Jitter (Async. Serial Int.)	[3]		[3]	Tperiod*1%
[4]	Freq.(Sync. Serial Int.)	[4]	Freq.(nominal) – 1%	[4]	Freq.(nominal) + 1%
[5]	Jitter (Sync. Serial Int.)	[5]		[5]	Tperiod*1%
[6]	Tr	[6]	-	[6]	3ns
[7]	Tf	[7]	-	[7]	3ns
[8]	Thigh	[8]	45%*[Tperiod]	[8]	55%*[Tperiod]
[9]	Tlow	[9]	45%*[Tperiod]	[9]	55%*[Tperiod]
[10]	VIH (Pin A11)	[10]	70% VDD	[10]	-
[11]	VIL (Pin A11)	[11]	-	[11]	30% VDD
[12]	IIL (Pin A11)	[12]	-1uA	[12]	+1uA
[13]	VOH (Clk Source)	[13]	VDD-0.25V	[13]	-
[14]	VOL (Clock Source)	[14]	-	[14]	VDD+0.25V

Figure 4-5 External Clock Specifications

4.5 Other Timing Information

4.5.1 Imaging Scan Timing / Frame Rates:

Frame rate is highly correlated to maximum finger sweeping speed. The AES2510 column scan timing is 32us per sixteen pixel column and will limit image frame rates to less than [16x192 pixels * 32us/16 pixels = 6.144 ms] or ~162 fps maximum. Transferring register data, histogram data, and authentication data will reduce this frame

rate. When the sensor is utilized in 128 column mode, the frame rate scales proportionally to 244. External system latencies and other external factors beyond the control of the sensor and control software can reduce the maximum effective frame rate to lower values. With appropriate overlap of image slices, the effective generalized finger slide rates are estimated to be 10-11cm/sec in 192 column mode and 14-16 cm/sec in 128 column mode.

4.5.2 Finger Detect Auto-calibration

When using Finger Detect [delay method], the device is automatically calibrated once on power up. Sending a master reset to the device does not affect the setting of the reference delay value used for the finger detect calculation. If desired, the device can be re-calibrated by setting the Recalibrate FD bit [Reg82-D2], which is self-clearing.

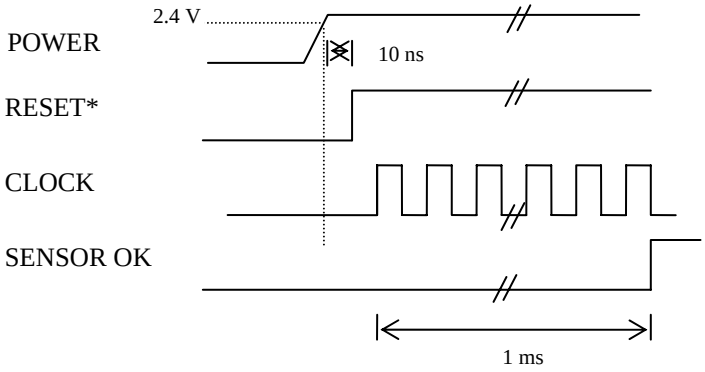
4.6 Reset

4.6.1 2510 Start-up:

The RESET* (and SYS_CLK if the SYS_CLK pin is driven externally) pin should be held in the low state until Vdd reaches at least 2.4V. This prevents powering up the sensor through the input protection network on those pins.

RESET* can be released 10 ns after Vdd reaches 2.4V. The clock may be active or inactive when reset is applied or released. Internally reset does not go inactive until two internal clocks after reset is released.

SYS_CLK can be applied any time after Vdd reaches 2.4V. If using the internal PLL, time is required for it to stabilize before operating the sensor. The PLL lock time is 1 ms worst case. The lock time starts from either clock starting or reset being released, whichever comes last.



5. System Interface Descriptions

5.1 Interface Select Control

Interface selection is done via the IOSEL[1:0] input pins. The following table shows how. See section 4.2 for the IOSEL[1:0] pin assignments.

IOSEL1	IOSEL0	Interface Selection
0	0	8-bit Parallel
0	1	Asynchronous Serial (not recommended)
1	0	SPI-compatible Synchronous Serial
1	1	SPI-compatible Master Out/Slave In Synchronous Serial

Figure 5-1 IOSEL[1:0] Decode

For each interface selection, the following pin assignments apply:

SIO/Pin	Parallel		Async Serial		Sync Serial – Slave SPI		Sync Serial – Master SPI or McBSP	
0/B8	D0	I/O	RXD	I	DR	I	DR	I
1/B7	D1	I/O	RTR	I	FS	I	FSR	I
2/C7	D2	I/O	AUTOBAUD_EN	I	CLK	I	CLKR	I
3/C8	D3	I/O	TXD	O	DX	O	DX	O
4/B12	D4	I/O	BAUD_SEL[0]	I	INT	O	FSX	O
5/B11	D5	I/O	BAUD_SEL[1]	I	A0	I	CLKX [Out when SPI, In when Mcbsp]	I/O
6/B10	D6	I/O	Unused, drives low	O	SPI_NORMAL	I	RTR	I
7/B9	D7	I/O	Unused, drive low	O	Unused, drive low	O	Unused, drive low	O
8/C9	A0	I	Unused, drive low	O	Unused, drive low	O	Frame Per Byte	I
9/C11	IOR_N	I	Unused, drive low	O	Unused, drive low	O	McBsp Mode	I
10/C12	IOW_N	I	GPIO[0]	I/O	GPIO[0]	I/O	GPIO[0]	I/O
11/D8	CE*	I	GPIO[1]	I/O	GPIO[1]	I/O	GPIO[1]	I/O
12/D9	READY	O	GPIO[2]	I/O	GPIO[2]	I/O	GPIO[2]	I/O
13/D10	INT	O	GPIO[3]	I/O	GPIO[3]	I/O	GPIO[3]	I/O

Figure 5-2 SIO Pin Definitions for each Selected Interface Option

5.2 Asynchronous Serial Interface

Asynchronous Serial Connection Diagram

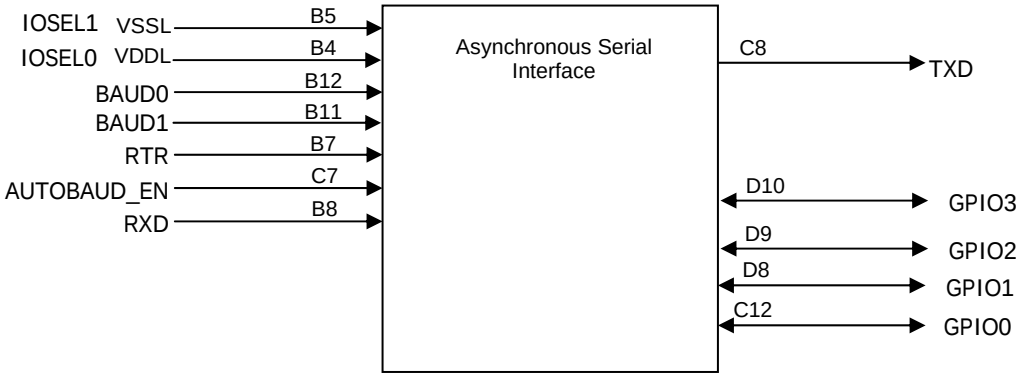


Figure 5-3 Asynchronous Interface diagram

The Asynchronous Serial Interface provides a serial data in and out for communication with the sensor. In addition, the interface has a Ready-To-Receive signal (RTR) that allows the host to throttle data from the sensor. The sensor is always ready to accept input data, so no throttling is necessary for data written to the sensor. Fixed baud rates are provided for test purposes only as the data rates are too slow for use with a slide-type fingerprint sensor.

Async Serial Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
RXD [SIO0]	B8	I	TTL	2	Serial data received from host.
RTR [SIO1]	B7	I	CMOS	N/A	Ready To Receive. High to enable sending serial data to host.
AUTOBAUD_EN [SIO2]	C7	I	CMOS	N/A	Enables autobaud feature of interface when tied high: The first character received after reset must be '0x0F'. When tied low, BAUD[1:0] pins select a fixed bit rate.
TXD [SIO3]	C8	O	CMOS	2	Serial data transmitted to host.
BAUD0 [SIO4]	B12	I	CMOS	N/A	Usage below 2Mbaud not recommend

Async Serial Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
BAUD1 [SIO5]	B11	I	CMOS	N/A	When AUTOBAUD_EN is low [not active], select fixed baud rate according to the table below: BAUD[1:0] Baud Rate 00 115.2k bps 01 460.8k bps 10 750.0k bps 11 921.6k bps In general, the product can only be used in Autobaud mode at bit rates >=2Mbps
GPIO0 [SIO10] GPIO1 [SIO11] GPIO2 [SIO12] GPIO3 [SIO13]	C12, D8, D9 D10	I/O I/O I/O I/O	CMOS CMOS CMOS CMOS	N/A N/A N/A N/A	General Purpose Input/Output – Input/Output definition by register B3h

Figure 5-4 Asynchronous Serial Interface Signal Descriptions

For all data rates and formats, the data is formatted using a standard asynchronous protocol, see section 5.2.2. When autobaud mode is selected, the sensor sends a break character (constant low) after the RESET* pin goes high. The amount of time is selected by the BAUD[1:0] pins.
When Autobaud is enabled, the sensor sends a break character (sets the TXD pin low) after reset goes inactive. TXD is kept low for an amount of time controlled by the BAUD[1,0] select pins.

BAUD[1,0]	TXD low duration
00b	1000 us
01b	500 us
10b	250 us
11b	75 us

Figure 5-5 TXD low duration for Autobaud

After sending the break character, the sensor interprets the next data byte as 0x0F and uses that to determine the bit rate.

After the break character terminates, the sensor interprets the next character received as a 0Fh and sets the bit timing based on that character. Thus, to support automatic baud rate detection after power-on reset, the communication session should begin with the transmission of '0F'h for the sensor to perform a bit time calculation. No further delay in sending data is required after sending the 0Fh byte.

5.2.1 Asynchronous Serial Interface RTR Response

The RTR input can be used to throttle the data output from the chip. Figure 2-2 shows the timing associated with RTR disabling.

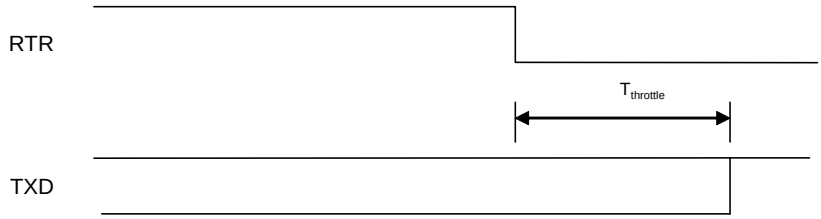


Figure 5-6 RTR Response Timing Diagram

The serial out circuitry in the sensor consists of a one byte buffer feeding an output shift register. The RTR input is sampled whenever the output shift register is empty; the shift register is not loaded until RTR is active. As long as RTR is de-asserted more than 35 ns before the end of the stop bit, data transmission will stop at the end of the current byte.

5.2.2 Asynchronous Protocol

The bit timing for both serial in data and serial out data is shown in Fig. 2-3. Transmit and receive have 1 bit interval for START, 8 data bits and 1 STOP bit with no parity.

The idle state of the TXD line is high. Each data byte sent is preceded by a low start bit and followed by a high stop bit. Each byte is sent LSB first.

The following figure illustrates the asynchronous protocol.

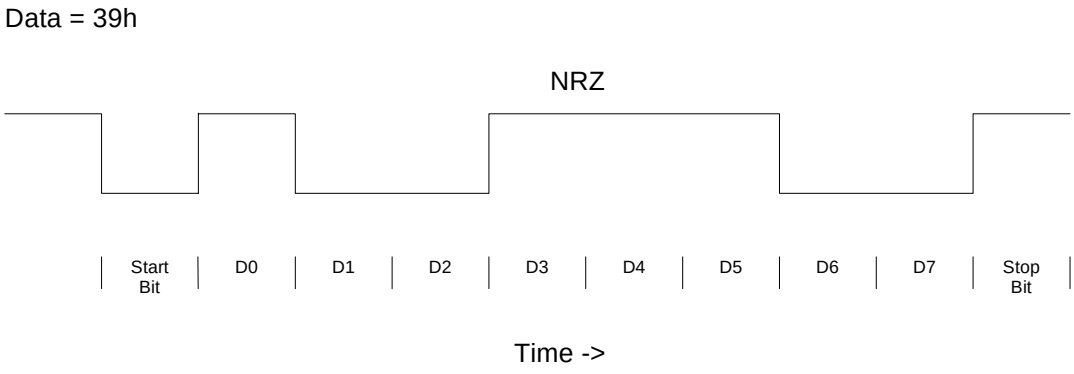


Figure 5-7 Asynchronous Serial Timing Diagram – One Byte

5.3 Synchronous Serial Interface [SSI]

Relevant Registers:
RegBE-bit D4 – Interrupt enable
RegBE-bit D5 – Address control. Selects either the Register Address/Data port (A0 = 0) or the Status port (A0 = 1) for the type of data to be transmitted from the sensor.

NOTE: External signal A0 pin should be held low when using the register control method, register BE bit D5 above. Likewise, the register bit should be kept low when using the A0 pin.

The Synchronous Serial Interface provides serial data in and out for communication with the sensor. This interface acts as a **slave mode** interface only. External data transmit/receive clocks control the data transmission rate. The synchronous serial interface supports 8-bit mode only.

The SSI supports both clock normal and clock opposite phases controlled by the SSI_NORM pin B11. The SPI™-compatible modes support either continuous clock – gated frame protocol or continuous select – gated clock protocol. For all data rates and formats, the data is formatted for a SPI™-compatible synchronous protocol. Each byte is sent most significant bit first. For power cycling/control of these interfaces, please refer to the section of sensor power cycling and application notes supporting the AES2510 sensor.

The usage model of the SSI is similar to other AuthenTec sensors. The host processor has the ability read data when the sensor has no data to provide. For that reason, the transmit data byte source is selectable between both a status register and the sensor data register. In normal operation, the host selects the status register, and reads that until the register indicates data is available. A preferred alternative is to use the INT pin [D10] as a data available indicator.

The host then selects the data register and reads the correct number of bytes from the sensor. The Port Address is set either via an internal register bit or via a package pin (A0) as noted above.

By design the SSI is a full duplex communication scheme, so the host processor (master side of the SSI) must manage the ‘filler’ data produced when reading or writing to the sensor. Inactive filler data should be FFh.

5.3.1 Synchronous Serial Interface Description

SSI Synchronous Serial Connection Diagram

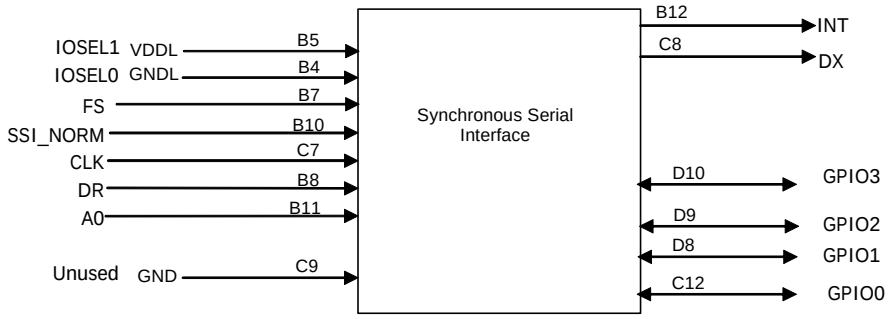


Figure 5-8 SSI-compatible Interface Diagram

SSI Signal Name	Pin	Pin Type	Description
DR [SIO0]	B8	I	Receive Data
FS [SIO1]	B7	I	Frame Sync. Signal
CLK [SIO2]	C7	I	Receive Clock
DX [SIO3]	C8	O	Transmit Data. This signal goes high impedance when FS is high
SSI_NORM [SIO6]	B10	I	Selects Normal phase (non-inverted clock) when high, selects Opposite phase (inverted clock) when low.
INT [SIO4]	B12	O	Interrupt output to indicate data is available when high
A0 [SIO5]	B11	I	Address, when low selects data, when high selects status byte
GPIO0 [SIO10] GPIO1 [SIO11] GPIO2 [SIO12] GPIO3 [SIO13]	C12 D8 D9 D10	I/O I/O I/O I/O	General Purpose Input/Output – Input/Output definition by register B3h

Figure 5-9 SSI Synchronous Serial Interface Signal Descriptions

Port Address Value [A0] either Register bit or A0 Pin	Port Function
0x0	Address/Data port
0x1	Control/Status port Bits [7:4] - 0000 Bits [3:1] - Encoded Data Available bits (valid when Bit 0 is low) 000 or 001 - Row Header(1 byte – data will always be E0h) 010 - Pixel Data(8 bytes) 011 - Histogram Data (33 bytes) 100 - Authentication Data(9 bytes) 101 - Register Data(2 or 64 or 126 bytes; mode dependent. 2 is for Nav or single register mode) Bit 0 - Data available handshake bit for Polled operation, active low

Figure 5-10 Synchronous Serial Interface IO Port Assignment

5.3.2 Synchronous Serial Receive/Transmit Interface Timing

Figure 5-11 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 1 shows timing diagrams for the receive interface in SSI mode with SSI_NORM = 1.

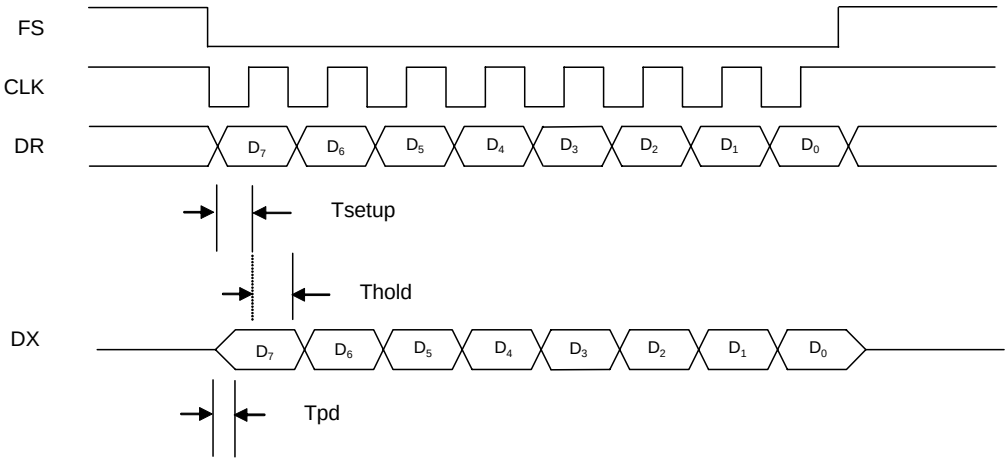


Figure 5-11 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 1

Parameter	Description	Min	Max	Unit
Tsetup	Setup time, data to CLK rising edge	10	-	ns
Thold	Hold time, frame sync or data from CLK rising edge	45	-	ns
Tpd	Propagation delay time, CLK rising edge to DX valid	-	55	ns
	CLK low time	65		ns
	CLK high time	65		ns

Figure 5-12 SSI Receive/Transmit Timing Parameters, SSI_NORM = 1

Figure 5-13 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 0 shows timing diagrams for the receive interface in SSI mode with SSI_NORM = 0.

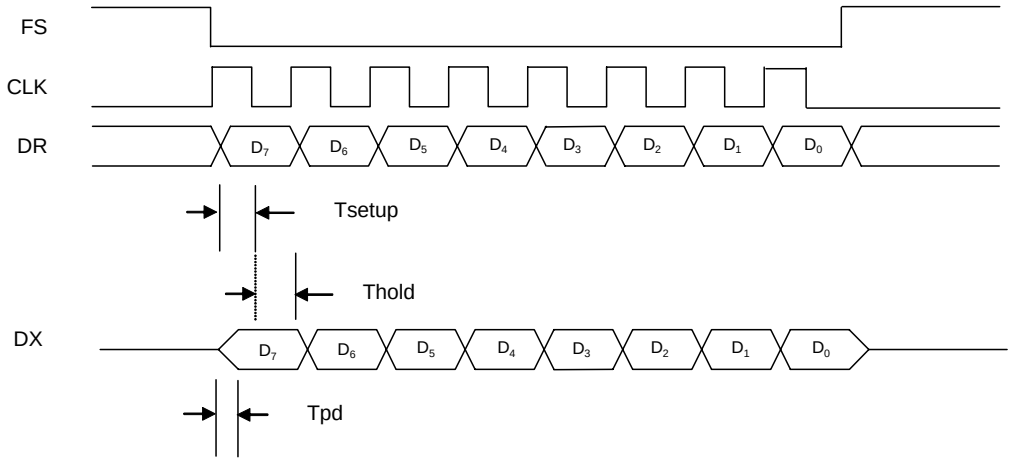


Figure 5-13 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 0

Parameter	Description	Min	Max	Unit
Tsetup	Setup time, data to CLK rising edge	10	-	ns
Thold	Hold time, frame sync or data from CLK rising edge	45	-	ns
Tpd	Propagation delay time, CLK rising edge to DX valid	-	55	ns
	CLK low time	65		ns
	CLK high time	65		ns

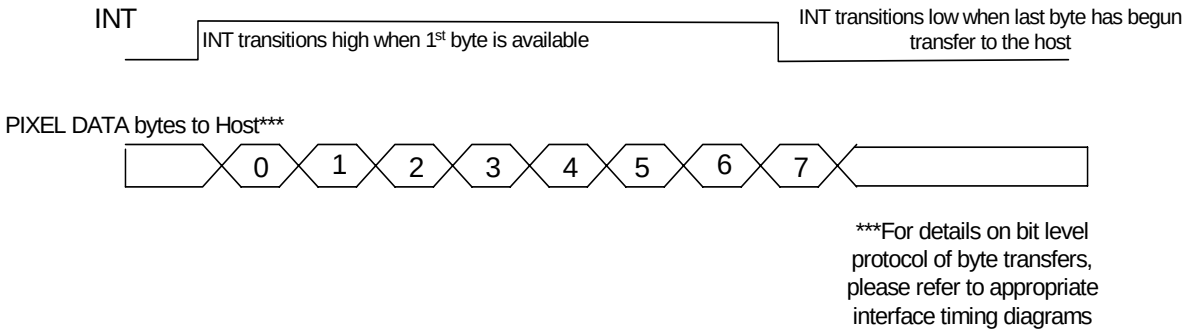
Figure 5-14 SSI Receive/Transmit Timing Parameters, SSI_NORM = 0

5.3.3 Synchronous Serial Interrupt behavior

When employing any of the synchronous serial interfaces, an interrupt signal [INT, active High] is available to support coordination of data transfers. There are two different types of operational modes possible with the sensor, Imaging Mode and Navigation Mode. The following examples will describe the behavior of the INT signal for both operational modes.

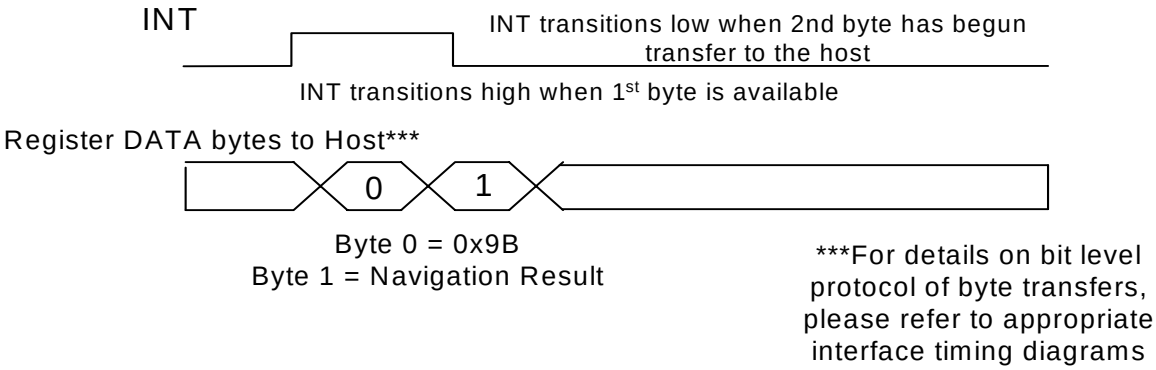
IMAGING MODE
For imaging mode, there are several different types of data packets that can be sourced from the sensor, please refer back to Figure 5-10 Synchronous Serial Interface IO Port Assignment.

An interrupt is generated for each one of these unique data packets and is held active until the beginning of the last data byte is read from the sensor by the host processor. This includes one byte transfers, as in the case of the Row Header packet. In the case of a Pixel Data packet, the following timing would apply:



It is important to note that the INT signal does not transition low until the last data byte of the packet has begun transfer on the selected interface. If there were more data from another source available, the INT would again transition high after being low for ~40nS to let the host know that more data is available from the sensor.

NAVIGATION MODE
When in navigation mode, there is only one possible data source type, Register Data, since the only data produced during Navigation mode is a 2-byte packet consisting of the register address 0x9B and the data value indicating finger presence and direction. So the INT timing for this packet would be as shown in the figure below.



5.3.4 SPI and McBSP Compatible M/S Synchronous Serial Interface Specification

The Master / Slave (M/S) Synchronous Serial Interface shall be capable of the following data transfer:

5.3.4.1 CPU to AES2510 Transfers

- This operation shall utilize AES2510's "Receive" path, and the CPU's "Transmit" path.
- CPU will transfer register data information to the sensor in the following format:

<Register Header> <Register Content>
Register Header has its MSB is set (D7 = 1);
Register Content has its MSB is clear (D7 = 0);
It is possible to send an infinite stream of Register Headers;
Register Content is effective only in the register pointed to by the preceding Register Header;
Sending Register Content without preceding Register Header has no effect;

- A "bit banging" implementation at the CPU side shall be possible to accomplish a register information transfer;
- This interface may be operating at 256Kbps;
- Note absence of the A0 control pin;

This interface shall have the ability to be configured in two modes:

- TI OMAP 15xx, 16xx compatible McBSP Master or Slave mode
- Intel XScale SPI Master or Slave mode

5.3.4.2 AES2510 to CPU Transfers

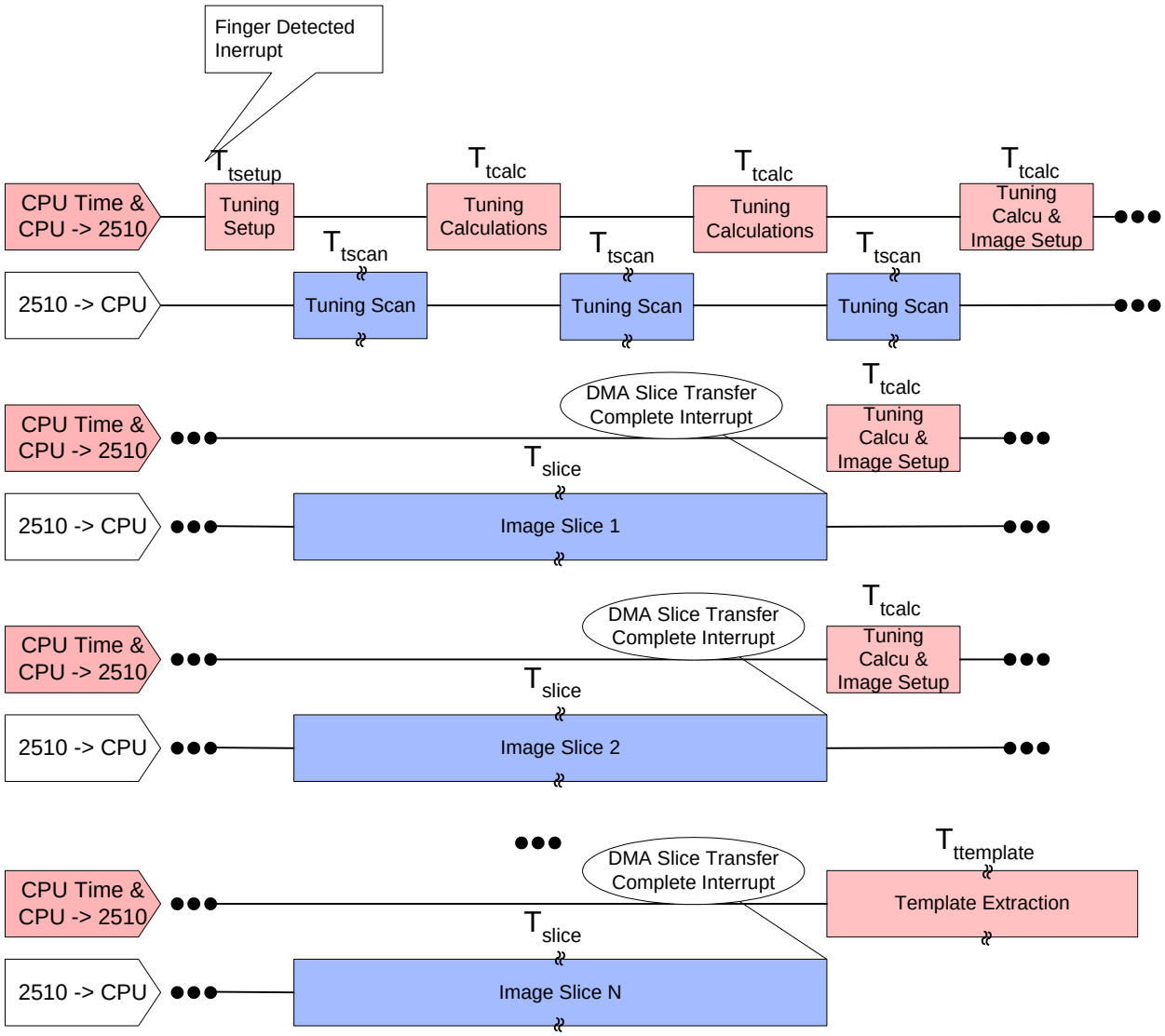
- This operation shall utilize AES2510's "Transmit" path and the CPU's "Receive" path.
- This path will be able to operate at the bit rates up to 8 Mbps; programmable in register 0xBE: D1-D0.
- The data transfers shall have the following format:

<Header> <Data Byte 1>…<Data Byte n>
Header – this value signifies what type of information is transferred (see Sensor Data Types);
Data Bytes – 8 bit values that contain the information for the given data types;

- The Master/Slave architecture allows the AES2510 to be the Master on the Serial Bus. This, coupled with the CPU's port functionality that allows the DMA transfers from the peripheral (serial port) to a memory location (a buffer for the finger print data) allows the off-loading of the CPU processing time.

The M/S Synchronous Serial Interface will allow a high degree of CPU off-loading. The following line diagram illustrates the imaging mode of the AES2510 for this interface. It is assumed that the

CPU can be configured for the DMA transfers from the SPI port peripheral to the memory. Note that the sensor data transfer does not require in-slice processing.



Approximate time durations for the CPU SW executions and the transfer durations are as follows:

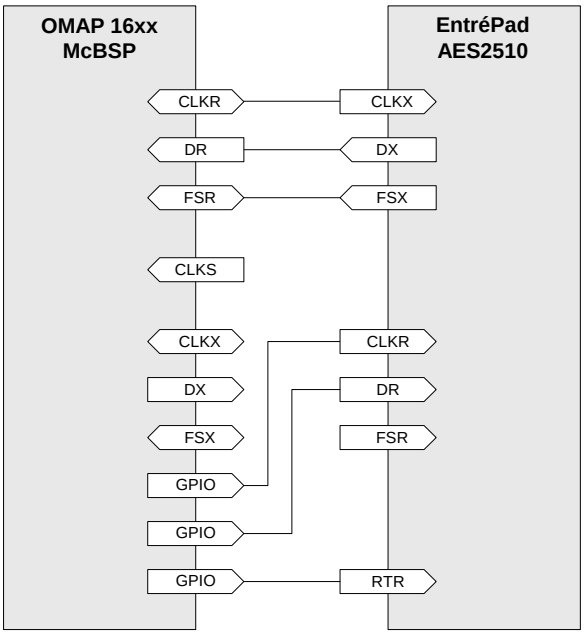
Parameter	Description	Value
T_{tsetup}	Tuning Setup Time	80us
T_{tcalc}	Tuning Calculation Time	150us
T_{tscan}	Tuning Scan Time	750us
T_{slice}	Slice Transfer Time (6.5Mbps)	1374us
$T_{template}$	Template extraction time	Processor dependent

The following table shows the mode selection based on the logic state of the input pins SIO[9:8]:

SIO[9:8]	SPI and MCBSP Compatible M/S Synchronous Serial Mode
00	Intel XScale, SPI Master mode – Frame sync. Active entire message
01	Intel XScale SPI Master mode - Frame sync. Active per byte
10	TI OMAP 15xx, 16xx compatible McBSP Master mode
11	Illegal condition

TI OMAP 16xx Compatible M/S Mode

In this mode the Synch Serial specification shall have the following signal configuration:



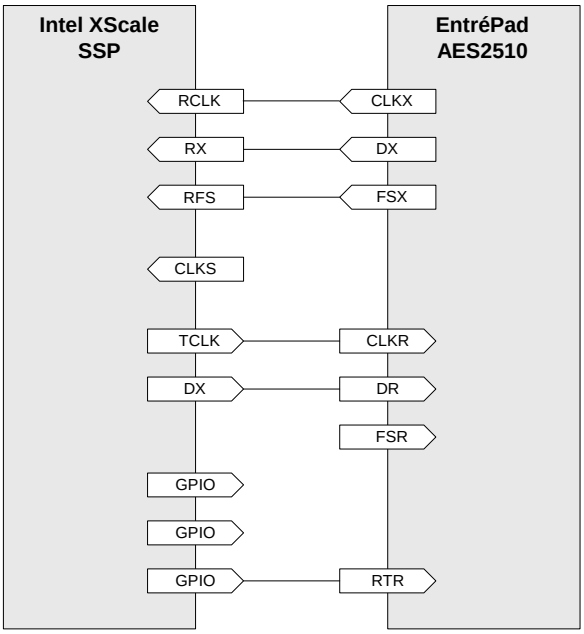
Signal Name	Signal Type	Signal Description
CLKR	I	Receive Clock
DR	I	Receive Serial Data
FSR	I	Receive Frame Synch
CLKX	I	Transmit Clock
DX	O	Transmit Serial Data
FSX	O	Transmit Frame Synch
RTR	I	Ready to Receive (Master / Slave)

In this mode it is possible to exercise the transmit and receive paths asymmetrically: they can send and receive data in different rates (CLKR does not have to be the same CLKX). Note that CLKX (even in the Master mode) is supplied from the OMAP 16xx chip and it is an input.

The Master / Slave control is performed by the RTR pin. When this signal is high (logical 1) the AES2510 can send the data on the transmit interface.

Intel XScale Compatible M/S Mode

In this mode the Synch Serial specification shall have the following signal configuration:



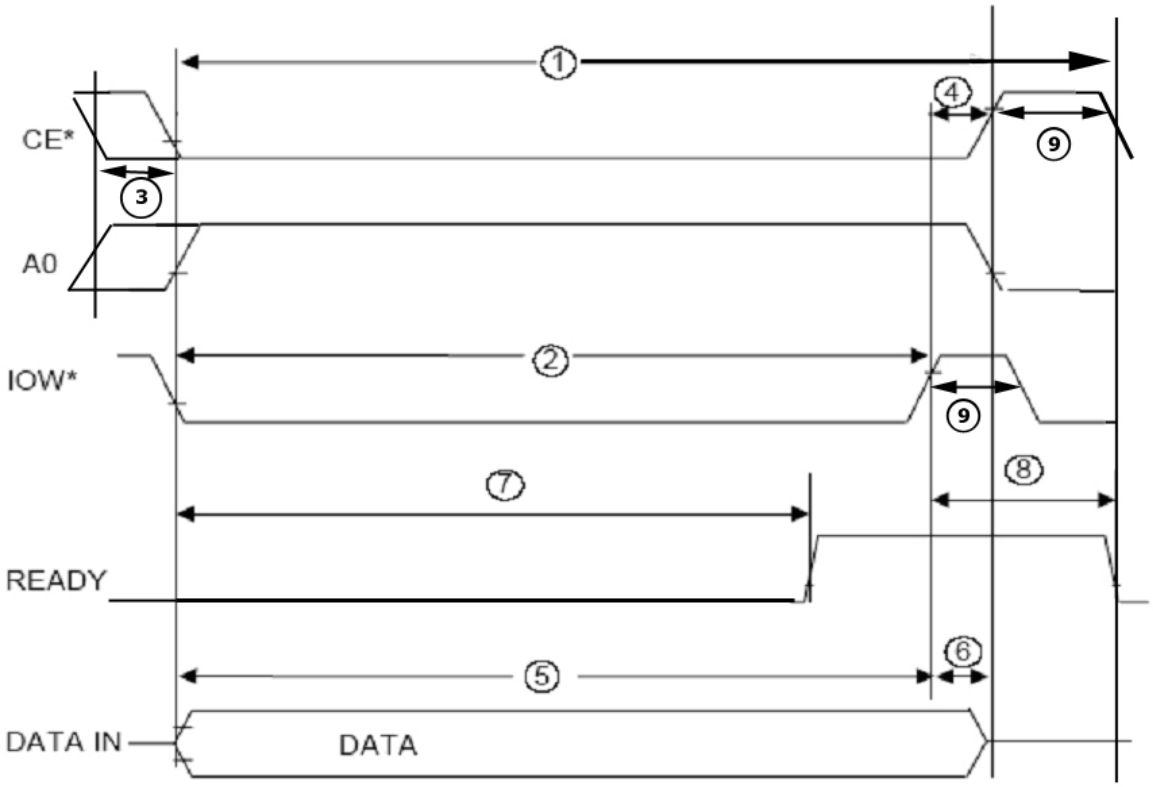
In this mode it is possible to exercise the transmit and receive paths asymmetrically, with different data rates. Note, that in this mode the CLKX is generated by the sensor and it is supplied to the microcontroller for reference.

Signal Name	Signal Type	Signal Description
CLKR	I	Receive Clock
DR	I	Receive Serial Data
FSR	I	Receive Frame Synch
CLKX	O	Transmit Clock
DX	O	Transmit Serial Data
FSX	O	Transmit Frame Synch
RTR	I	Ready to Receive (Master / Slave)

5.4 8-bit Parallel Interface

Table 5-4.1 AC Characteristics of Parallel Write Interface

No.	Parameter	Symbol	Limits		Units
			Min.	Nom	
1	Write cycle time	t_{WC}	110	-	ns
2	IOW* or CE* pulse width	t_{ww}	80	-	ns
3	Setup time, A0 from CE* falling edge	t_{SU}	5	-	ns
4	Hold time, address or chip select from IOW* rising edge	t_h	5	-	ns
5	Data Setup to IOW* rising edge	t_{SUd}	45	-	ns
6	Hold time, IOW* rising edge to data invalid	t_{hd}	5	-	ns
7	IOW* falling edge to READY active	t_{wrm}	65	-	ns
8	IOW* rising edge to READY inactive	t_{rw}	65	-	ns
9	IOW* or CE* time inactive	$t_{inactive}$	30	-	ns



Parallel Interface Write Timing

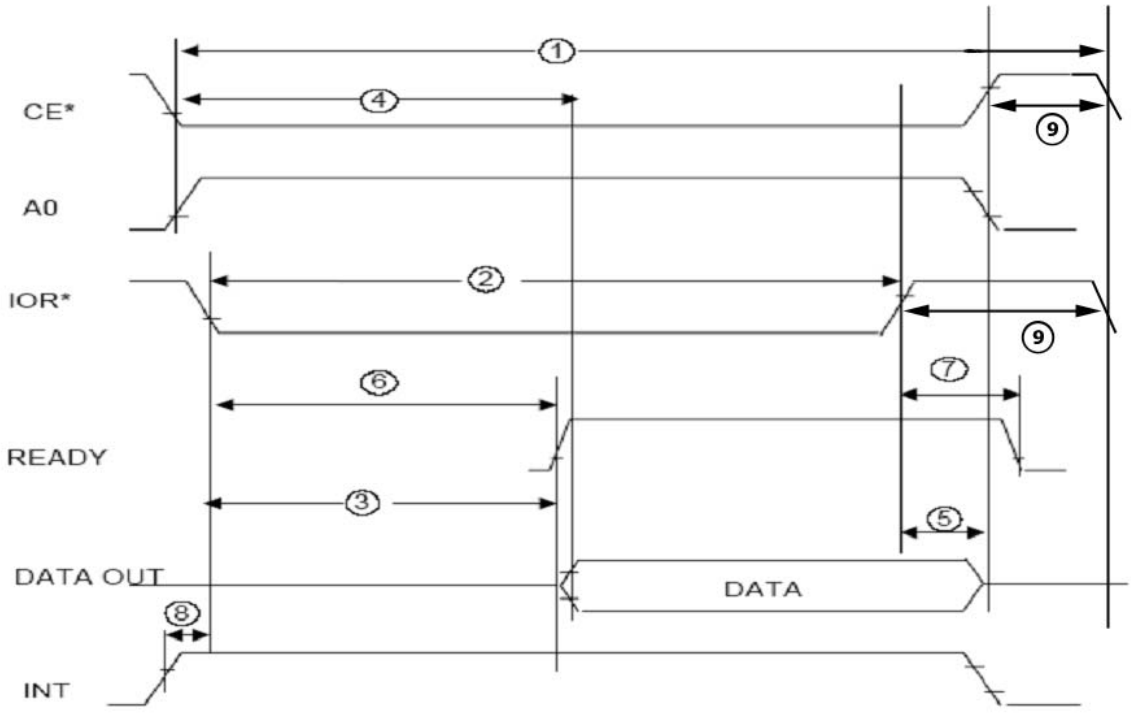
Table 5-4.2 AC Characteristics of Parallel Read Interface

No.	Parameter	Symbol	Limits		Units
			Min	Nom	
1	Read cycle time	t_{rc}	110	-	nS
2	IOR* or CE* Pulse Width	t_{rw}	80	-	nS
3	Access time from IOR* low	t_{accrd}	55	-	nS
4	Access time from address (A0) or chip select (CE*)	t_{acca}	55	-	nS
5	Output high impedance from IOR* or CE*	t_{hz}	5	-	nS
6	IOR* falling edge to READY active	t_{rm}	65	-	nS
7	IOR* rising edge to READY inactive	t_{rr}	65	-	nS
8	INT available time to IOR* falling edge	t_{rw}	0	Note 1	nS
9	IOW* or CE* time inactive	$t_{inactive}$	30	-	nS

Data is read from the parallel interface when IOR* is low and the chip select pim (CE*) is active. The READY sensor output can be used to signal when the interface is ready for cycle completion.

Note 1: To ensure no loss of data, the first read of image data must commence within 256uS of the interrupt going true. Subsequent reads of the same image must commence within 25uS of the corresponding interrupt.

The Figure below shows the timing requirements for read operations

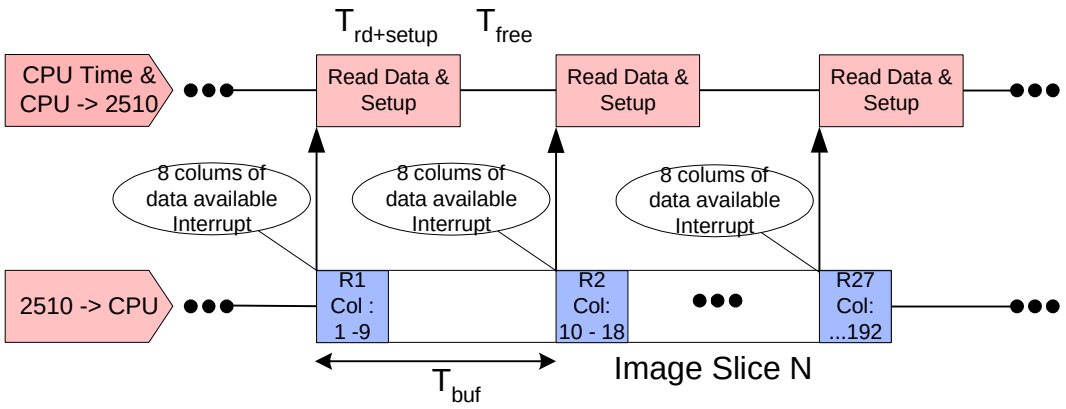


Parallel Interface Read Timing

When the AES2510 is configured for the parallel interface the send buffer is capable of holding up to 10 columns (80 bytes in the standard 4 bits per pixel) of fingerprint data. This buffer is constructed as a FIFO.

The interrupt signal (INT) from the sensor to the processor can be configured to generate an active signal on 1 or 4 or 8 or 9 columns of new data present (configuring a “high water mark”). When a CPU receives the interrupt it can schedule a read of the specified number of bytes from the sensor’s parallel port.

A new byte may be read from a sensor when the data available bit in the Control Port (this is controlled by the A0 pin) is set (D0 = 1).The slice data transfer in the imaging mode that would utilize the sensor’s ability to buffer up to 10 columns of data and interrupt on the 8th full column would have the following characteristic:



Reading 8 columns (64 bytes in the 4bit per pixel configuration) worth of data from the parallel interface would take approximately 7.7us. As the diagram indicates the CPU must be involved in managing this transfer. After the data has been transferred to a memory buffer, the buffer management and the interrupt setup must take place to get the CPU ready for the next 8 columns of data.

Parameter	Description	Value
$T_{rd+setup}$	Read 64 bytes and Setup Time	7.7us + 25us
T_{free}	CPU unencumbered Time	256us - $T_{rd+setup}$
T_{buf}	Time to buffer 8 columns	256us

5.5 Example Hardware Checkout Communication Sequence

The following example illustrates the basic communication with AES2510 via the SSI interface. These examples are intended for illustration and may be helpful in supporting initial integration test and checkout before software test. Utilizing the Register Read operation will enable a hardware designer to verify the SSI interface in the system.

5.5.1 Initialization

For synchronous serial interface operation mode, the following sequence is required for proper operation:

1. Power up the sensor.

2. Release reset or wait until reset is inactive.

5.5.2 Read Registers Sequence

The SSI Master sends the following sequence of bytes to the AES 2510:

0xBE(address: SSI control register)
0x10 (enable SSI interrupts)
0x81 (address: Control Register 2)
0x02 (select: Read Registers command AND enables interrupt)

This sequence requests the registers (63) of the sensor, or 126 bytes in response. The sequence of information received should be in the order of <register number byte, default value byte> repeated for all 126 bytes.

In order to successfully read all the register data from the AES2510 sensor, the SSI Master must write “fill” bytes. The flow diagram illustrates the flow of the SSI bus for the operation of reading of 126 registers from the AES 2510:

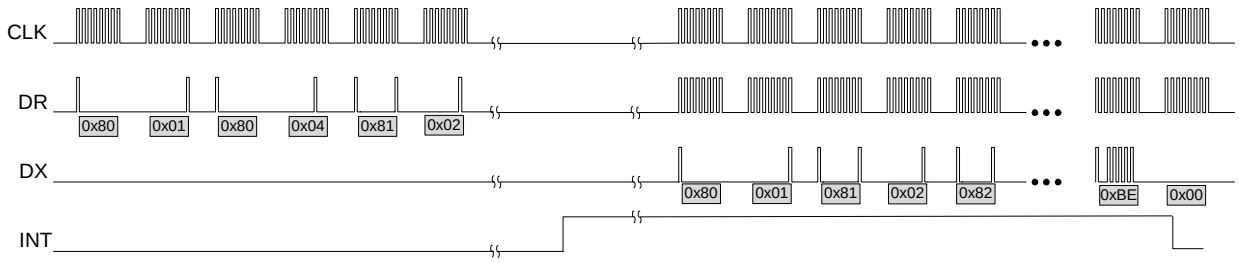


Figure 5-15 Read Register Sequence in SSI Mode

The bytes of information transmitted from the sensor should be, as follows. Dashed line entry indicates the value returned depends upon board configuration or sensor variations. This data is only valid after a power-on reset.

Reg	Default		Reg	Default
80h	00h		A0h	--
81h	00h		A1h	00h
82h	04h		A2h	00h
83h	13h		A3h	00h
84h	07h		A4h	00h
85h	02h		A5h	00h
86h	01h		A6h	00h
87h	01h		A7h	02h
88h	03h		A8h	01h
89h	02h		A9h	00h
8Ah	05h		AAh	00h
8Bh	00h		ABh	00h
8Ch	40h		ACh	20h
8Dh	00h		ADh	00h
8Eh	00h		AEh	--
8Fh	00h		AFh	--
90h	00h		B0h	00h
91h	70h		B1h	00h
92h	20h		B2h	00h
93h	00h		B3h	0Fh
94h	02h		B4h	00h
95h	00h		B5h	00h
96h	7Fh		B6h	26h
97h	08h		B7h	0Dh
98h	20h		B8h	6Ch
99h	--		B9h	00h
9Ah	N/A		BAh	00h
9Bh	00h		BBh	00h
9Ch	--		BCh	00h
9Dh	0Ah		BDh	00h
9Eh	0Xh		BEh	00h
9Fh	--			

6. Data Formats

6.1 Overview

The sensor communicates with the host via data packets. A one-byte header that identifies the message precedes each data packet type. Note that since the pixel data formats use all 8-bits per byte, the header bytes are not unique in the data stream. Software can use the header bytes to verify that it is synchronized with the data stream. They cannot be used as a mechanism to synchronize with the data. If software gets out of synch with the data, it should disable image scanning and issue a scan reset. This will cause the data stream to stop. The following table shows the header byte definitions for each message type.

Header Byte	Definition
80h – BEh	Register headers
BFh – DDh	Reserved.
DEh	Precedes 32 byte histogram message.
DFh	Precedes eight byte authentication value.
E0h	Precedes 500 ppi array data message in gray scale. The array message is 192 columns x 16 pixels per column x ½ byte per pixel = 1536 bytes. In 250 ppi mode, the array message is 96 columns x 8 pixels per column x ½ byte per pixel = 384 bytes. In Extended Precision 250 ppi mode, the array message is 96 columns x 8 bytes per column = 768 bytes.
E1h-EFh	Reserved
F0h	Precedes array data message in binary mode. The array message is 192 columns x 16 pixels per column x 1/8 byte per pixel = 384 bytes. In 250 ppi Mode, the array message is 96 columns x 8 pixels per column x 1/8 byte per pixel = 96 bytes.
F1h –FFh	Reserved.

Table 5.5.2-1 Command Byte Definition

6.1.1 Registers Message Format

When a request to read registers is received (initiated by setting the Read Registers bit in Register 81h-D1, all of the register values are returned preceded by the header for that register.
Registers are written to by writing the register ID followed by the data byte.

6.1.2 Image Data Format – Grey Scale 500 ppi

The following table shows the image data format in this mode.

Byte	Data (D7 – D0)
1	Header (E0h)
2	Column 1 pixel 2[3:0], Column 1 pixel 1[3:0]
3	Column 1 pixel 4[3:0], Column 1 pixel 3[3:0]
4	Column 1 pixel 6[3:0], Column 1 pixel 5[3:0]
5	Column 1 pixel 8[3:0], Column 1 pixel 7[3:0]
6	Column 1 pixel 10[3:0], Column 1 pixel 9[3:0]
7	Column 1 pixel 12[3:0], Column 1 pixel 11[3:0]
8	Column 1 pixel 14[3:0], Column 1 pixel 13[3:0]
9	Column 1 pixel 16[3:0], Column 1 pixel 15[3:0]
10	Column 2 pixel 2[3:0], Column 1 pixel 1[3:0]
|	|
1537	Column 192 pixel 16[3:0], Column 192 pixel 15[3:0]

Table 6.1.2-1 Gray Scale Message Format

The 0xE0h header for the row is sent first, followed by each column vector sent as eight bytes. The 64-bit pixel data also updates the authentication word. After all data for the selected number of rows is sent, the authentication word is sent preceded by the header byte for the authentication message. The authentication data is sent lower byte first. The register values are then returned, with each register preceded by the command byte for the register. The register values are the ones that were in effect during the image.

6.1.3 Image Data Format – 250 ppi

The following table shows the image data format for this mode.

Byte	Data (D7 – D0)
1	Header (E0h)
2	Col 1/Col 2 pixel group 1 [3:0], Col 1/Col 2 pixel group 2 [3:0]
3	Col 1/Col 2 pixel group 3 [3:0], Col 1/Col 2 pixel group 4 [3:0]
4	Col 1/Col 2 pixel group 5 [3:0], Col 1/Col 2 pixel group 6 [3:0]
5	Col 1/Col 2 pixel group 7 [3:0], Col 1/Col 2 pixel group 8 [3:0]
6	Col 3/Col 4 pixel group 1 [3:0], Col 3/Col 4 pixel group 2 [3:0]
|	|
385	Col 191/Col 192 pixel group 7 [3:0], Col 191/Col 192 pixel group 8 [3:0]

Table 6.1.3-1 4 Bit 250 ppi Gray Scale Message Format

The header for the row is sent first, followed by each 2-column vector sent as eight bytes. The difference between this mode and 500 ppi mode is that four adjacent pixels are summed together and returned as a single 4-bit value. The 64-bit pixel data updates the authentication word in the same format as for normal data. After all data for the selected number of columns is sent, the authentication word is sent preceded by the header byte for the authentication message. The authentication data is sent lower byte first. The register values are then returned, with each register preceded by the command byte for the register. The register values are the ones that were in effect during the image.

6.1.4 Image Data Format – Monochrome

The packed monochrome data format sends only a one bit value per pixel but packs the data so all eight bits are used. **Error! Reference source not found.** shows the data format in this mode.

Byte	Data (D7 – D0)
1	Header (F0h)
2	Column 1 pixels 8-1
3	Column 1 pixels 16-9
4	Column 2 pixels 8-1
5	Column 2 pixels 16-9
|	|
385	Column 192 pixels 16-9

Table 6.1.4-1 Monochrome Packed Message Format

The header for the row is sent first, followed by each column sent as two bytes. The 64-bit value from four columns updates the authentication word in the same manner as for normal data. After all data for the selected number of rows is sent, the authentication word and register data are sent as in normal mode.

6.1.5 Histogram Message Format

When the histogram message is enabled, it is sent once per image. When sent once per image, it will be sent after the image data and before the authentication word. The histogram message is preceded by a header byte (0xDE). The header is followed by the counts for each of the bins representing possible pixel values. Bin 0 (the number of pixels whose value is 0) is sent first as two bytes. The first byte has the lower seven bits and the second byte has the upper seven bits. This is followed by the counts for the remaining bins

Byte	Data (D6 – D0)
1	Header (0xDE)
2	Bin0[6:0]
3	Bin0[13:7]
4	Bin1[6:0]
5	Bin1[13:7]
6	Bin2[6:0]
|	|
32	Bin15[6:0]
33	Bin15[13:7]

Table 6.1.5-1 Histogram Message Format

6.1.6 Authentication Word Message Format

The authentication word is sent after an image is complete. The authentication word message is preceded by a header byte (0xDF). The authentication word is used to validate that the transaction is authentic (i.e. that the image data isn't being provided from some storage device containing a valid fingerprint image).

Byte	Data (D6 – D0)
1	Header (0xDF)
2	Authentication Word [7:0]
3	Authentication Word [15:8]
4	Authentication Word [23:16]
5	Authentication Word [31:24]
6	Authentication Word [39:32]
7	Authentication Word [47:40]
8	Authentication Word [55:48]
9	Authentication Word [63:56]

Table 6.1.6-1 Authentication Word Message Format

6.2 Sensor I/O

6.2.1 Control Registers

Control registers are written to by writing the register header (e.g. 0x80 to write REG80) followed by the register contents. All register headers have D7 set, while register contents have D7 cleared (all registers are 7-bits).

Registers that affect imaging are implemented with master registers and local registers. Writing to the sensor writes to master registers, while the local registers are the settings the sensor is using. Local registers are updated from master registers except when imaging.

6.2.2 Sensor ID Message

The Sensor ID register (REG9D) can be read via the Read ID command, initiated by writing a '1' to bit D4 in REG81. The sensor will return two bytes: the register header (0x9D) followed by the contents of that register.

6.2.3 Register Message

The Sensor registers can be read via the Read Registers command, initiated by writing a '1' to bit D1 in REG81. The amount of data that the sensor returns is controlled by register settings.
If Single Reg En (D0 in REGAD) is high, two bytes are returned: the register header and the register specified by REGAD (the register number with D7 cleared) is returned.

If Single Reg En is low and Test Register Enable (D5 in REG98) is high, 126 bytes are returned: the register header and the register contents for each of the sensor registers.

If Single Reg En is low and Test Register Enable is low, 64 bytes are returned: the register header and the register contents for the first 32 registers (REG80-REG9F).

All registers return the local value for the register.

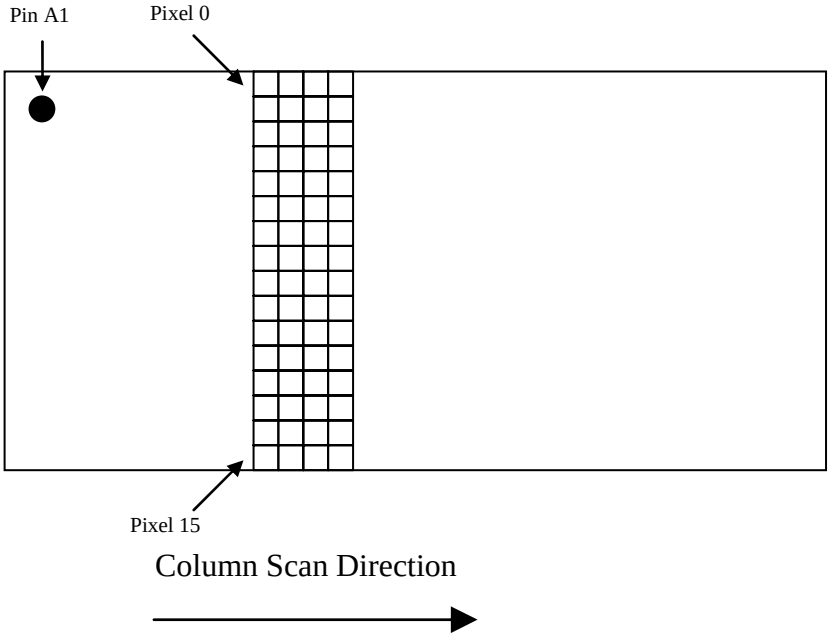
The Read Registers command is ignored when the sensor is imaging.
If One Reg Header (D6 in REG80) is set, the register message begins with the header for the first register sent but no other register headers are sent.

6.2.4 Image Message

The Image message begins with a header. The header is 0xF0 if binary mode is enabled and 0xE0 for all other modes. The Image Header can be disabled by setting bit D6 in REG98.

The output buffer for image data is 8 bytes; it holds one column of pixel data (16 pixels) at the standard resolution of 4-bits per pixel.

The figure below shows column and pixel reference designations. The sensor view is from the top of the sensor looking at the array. Pin A1 is in the upper left corner as shown. Refer to this figure to understand how pixels are packed into bytes for the various data formats.



Columns are scanned from left to right. The region scanned is programmable with a resolution of one column. Pixels are converted in order from Pixel 0 to Pixel 15.

For 4-bit Pixel Depth, pixels are packed into bytes with the first pixel converted going into the lower nibble of the byte and the second pixel going into the upper nibble. The table below shows how one column of data (16 pixels) is packed into 8 bytes.

Byte	Contents
1	PIXEL1[3:0], PIXEL0[3:0]
2	PIXEL3[3:0], PIXEL2[3:0]
3	PIXEL5[3:0], PIXEL4[3:0]
4	PIXEL7[3:0], PIXEL6[3:0]
5	PIXEL9[3:0], PIXEL8[3:0]
6	PIXEL11[3:0], PIXEL10[3:0]
7	PIXEL13[3:0], PIXEL12[3:0]
8	PIXEL15[3:0], PIXEL14[3:0]

Table 6.2.4-1 Column Data – 4-bit Pixel Depth

A Pixel Depth setting of 1-bit per pixel results in two bytes of data per column. The threshold for conversion to binary data is programmable (REG97): if the pixel value is greater than or equal to the programmed threshold, the data returned is a 1, otherwise it is 0.

Byte	Contents
1	PIXEL7, PIXEL6, PIXEL5, PIXEL4, PIXEL3, PIXEL2, PIXEL1, PIXEL0
2	PIXEL15, PIXEL14, PIXEL13, PIXEL12, PIXEL11, PIXEL10, PIXEL9, PIXEL8

Table 6.2.4-2 Column Data – 1-bit Pixel Depth

For 2-bit Pixel Depth, the conversion is performed by taking the upper two bits of each pixel value. This results in each column producing 4 bytes of data.

Byte	Contents
1	PIXEL3[3:2], PIXEL2[3:2], PIXEL1[3:2], PIXEL0[3:2]
2	PIXEL7[3:2], PIXEL6[3:2], PIXEL5[3:2], PIXEL4[3:2]
3	PIXEL11[3:2], PIXEL10[3:2], PIXEL9[3:2], PIXEL8[3:2]
4	PIXEL15[3:2], PIXEL14[3:2], PIXEL13[3:2], PIXEL12[3:2]

Table 6.2.4-3 Column Data – 2-bit Pixel Depth

6.2.5 Authentication Word Message

The Authentication Message is a header (0xDF) followed by 8 bytes of data.

6.2.6 Histogram Message

The Histogram Message is a header (0xDE) followed by 32 bytes of histogram data.

6.2.7 Nav Message

If Nav mode is enabled (SENSOR_MODE is 10b in Register 0x80, D[3:2]), two bytes are returned: the register header for Nav status (0x9B) and the data byte for that register.

6.2.8 Nav2 Message

If Nav2 mode is enabled (SENSOR_MODE is 11b in Register 0x80, D[3:2]), The Nav2 (image based navigation) Message contains only image data, no header or register information is included. See the Image Message section for more details on the format of image messages.

6.2.9 SensorID Message

If the READID command is sent to the sensor (0x81 0x10) two bytes are returned, the register header for Sensor ID register (0x9D) and the data byte indicating the Sensor type.

7. SOFTWARE Interface details

The Register Map and bit level Register Descriptions are contained in this section. Reserved registers are not included in the descriptions section for clarity. Bolded text in the register descriptions indicates default functionality.

7.1 Register Map

Reg	D6	D5	D4	D3	D2	D1	D0	Reset
80h	**One Reg Header**	**Timer2 Start**	**Timer1 Start**	**Sensor Mode[1]**	**Sensor Mode[0]**	Scan Reset[1]	Master Reset[1]	00h
81h			Read IDn[1]	Clear One-Shot[1]	Set One-Shot[1]/ One Shot[2]	Read Registers[1]	Continuous Scan	00h
82h	Disable Auto Update	TMCHARY	Demod Blk Dis	HGC Restart	HGC Enable	Calibrate Finger Det.	Timer Freerun	00h
83h	Read Ref. Delay	Finger Settling Delay [1]	Finger Settling Delay [0]		Detect Rate [2] / Nav Rate [2]	Detect Rate [1] / Nav Rate [1]	Detect Rate [0] / Nav Rate [0]	13h
84h	**Ultra Low Power**	NAV_SEL[1]	NAV_SEL[0]	Nav Corr Range [3][2]	Nav Corr Range [2][2]	Nav Corr Range [1][2]	Nav Corr Range [0][2]	07h
85h		**Use NAV FD**	Nav Fing. Det. Threshold [4]	Nav Fing. Det. Threshold [3]	Nav Fing. Det. Threshold [2]	Nav Fing. Det. Threshold [1]	Nav Fing. Det. Threshold [0]	02h
86h		Nav. Reduce LR	Nav. Debug	Nav. Thresh[3]	Nav. Thresh[2]	Nav. Thresh[1]	Nav. Thresh[0]	01h
87h	**Reserved**	**Reserved**	**Reserved**		Detect Freq [2]	Detect Freq [1]	Detect Freq [0]	01h
88h				Column Scan Rate [3]	Column Scan Rate [2]	Column Scan Rate [1]	Column Scan Rate [0]	03h
89h	VD Clk Inv.	VD 2MHz	**Reserved**	VD Mode [1]	VD Mode [0]	Meas Drive [1]	Meas Drive [0]	02h
8Ah			Meas Freq [4]	Meas Freq [3]	Meas Freq [2]	Meas Freq [1]	Meas Freq [0]	05h
8Bh	Use LP Comp Navigation	Use LP Comp Imaging	LP Comp Capacitor	LP Integ. Vref Low	LP Comp AC coupling	LP Comp Bias [1]	LP Comp Bias [0]	00h
8Ch	Demod Phase[13]	Demod Phase[12]	Demod Phase[11]	Demod Phase[10]	Demod Phase [9]	Demod Phase [8]	Demod Phase [7]	40h
8Dh	**Excitation Mode[1]**	**Excitation Mode[0]**	Pixel High Gain	PulseGen Width[1]	PulseGen Width[0]	Excitation 2X Amp gain	Excitation Warp 9 Enable	00h
8Eh		Gain 2 [1]	Gain 2 [0]			Gain1 [1]	Gain1 [0]	00h
8Fh	Bias2 Unlock	Bias 2 [1]	Bias 2 [0]		Bias1 Unlock	Bias 1 [1]	Bias 1 [0]	00h
90h	Carrier Null En	Carrier Null [5]	Carrier Null [4]	Carrier Null [3]	Carrier Null [2]	Carrier Null [1]	Carrier Null [0]	00h
91h	A/D Reference High [6]	A/D Reference High 5]	A/D Reference High [4]	A/D Reference High [3]	A/D Reference High [2]	A/D Reference High [1]	A/D Reference High [0]	70h
92h	A/D Reference Low [6]	A/D Reference Low [5]	A/D Reference Low [4]	A/D Reference Low [3]	A/D Reference Low [2]	A/D Reference Low [1]	A/D Reference Low [0]	20h
93h	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	**Spare**	00h
94h	**Spare**	**Spare**	**Spare**	Osc. On Delay[3]	Osc. On Delay[2]	Osc. On Delay[1]	Osc. On Delay[0]	02h
95h	Start Col [6]	Start Col [5]	Start Col [4]	Start Col [3]	Start Col [2]	Start Col [1]	Start Col [0]	00h
96h	End Col [6]	End Col [5]	End Col [4]	End Col [3]	End Col [2]	End Col [1]	End Col [0]	7Fh
97h	Low Resolution	Image Res. [1]	Image Res. [0]	Bin. Threshold [3]	Bin. Threshold [2]	Bin. Threshold [1]	Bin. Threshold [0]	08h
98h	**Image Header Disable**	Test Register Enable	Registers First	Histo Full Array	**Auth. Data Disable**	Histo Data Enable	Image Data Disable	20h
99h				GPIO3	GPIO2	GPIO1	GPIO0	00h
9Ah	Power Cycled[2]	Scan Paused[2]	Finger Present - Timer[2]	Scan State [3][2]	Scan State [2][2]	Scan State [1][2]	Scan State [0][2]	N/A
9Bh	**Timer2 Done**	**Timer1 Done**	Finger Present - Navigation[2]	Challenge Word [31][1] / Up[2]	Challenge Word [30][1] / Down[2]	Challenge Word [29][1] / Left[2]	Challenge Word [28][1] / Right[2]	00h
9Ch	Challenge Word [27][1] / FoundryID [6][2]	Challenge Word [26][1] / FoundryID [5][2]	Challenge Word [25][1] / FoundryID [4][2]	Challenge Word [24][1] / FoundryID [3][2]	Challenge Word [23][1] / FoundryID [2][2]	Challenge Word [22][1] / FoundryID [1][2]	Challenge Word [21][1] / FoundryID [0][2]	00h
9Dh	Challenge Word [20][1]/ CHIP_TYPE [6][2]	Challenge Word [19][1]/ CHIP_TYPE [5][2]	Challenge Word [18][1]/ CHIP_TYPE [4][2]	Challenge Word [17][1]/ CHIP_TYPE [3][2]	Challenge Word [16][1]/ CHIP_TYPE [2][2]	Challenge Word [15][1]/ CHIP_TYPE [1][2]	Challenge Word [14][1]/ CHIP_TYPE [0][2]	0Ah
9Eh	Challenge Word [13][1]	Challenge Word [12][1]	Challenge Word [11][1]	Challenge Word [10][1]	Challenge Word [9][1] /	Challenge Word [8][1] / IO_SEL [1][2]	Challenge Word [7][1] / IO_SEL [0][2]	0Xh
9Fh	Challenge Word [6][1] / MASK_REV [6][2]	Challenge Word [5][1]/ MASK_REV [5][2]	Challenge Word [4][1]/ MASK_REV [4][2]	Challenge Word [3][1]/ MASK_REV [3][2]	Challenge Word [2][1]/ MASK_REV [2][2]	Challenge Word [1][1]/ MASK_REV [1][2]	Challenge Word [0][1]/ MASK_REV [0][2]	00h

Reg	D6	D5	D4	D3	D2	D1	D0	Reset
A0h	Full Bit Integr [6] [2]	Full Bit Integr [5] [2]	Full Bit Integr [4] [2]	Full Bit Integr [3] [2]	Full Bit Integr [2] [2]	Full Bit Integr [1] [2]	Full Bit Integr [0] [2]	--
A1h	Excit Bias Unlock	Manual Excit Bias [1]	Manual Excit Bias [0]		Sense Amp Bias Unlock	Sense Amp Bias [1]	Sense Amp Bias [0]	00h
A2h	BIT DEMOD OFF	**BIT CLKON**	BIT MEASURE	**BIT ANCHON**	BIT EXCIT ON	BIT FGR DET	BIT DCRST	00h
A3h		Blanking	Channel Null Enable	**Reserved**	Channel Null Width [2]	Channel Null Width [1]	Channel Null Width [0]	00h
A4h	Analog Test Enable	Analog Test Mode [1]	Analog Test Mode [0]	Ref. BIT Enable	ANCH BIT Enable	A/D BIT Enable	Pixel BIT Enable	00h
A5h		**Excit. Test Enable**	**Excit. Data [4]**	**Achan Addr [3] / Excit. Data [3]**	**Achan Addr [2] / Excit. Data [2]**	**Achan Addr [1] / Excit. Data [1]**	**Achan Addr [0] / Excit. Data [0]**	00h
A6h		Dig. Mux. Sel.[1]	Dig. Mux. Sel.[0]	Ref Mux Sel [3]	Ref Mux Sel [2]	Ref Mux Sel [1]	Ref Mux Sel [0]	00h
A7h	Negedge Disable	Alt. Synth Mode	Samp Stretch		Hi Ref Bias	Array Float	Peek	02h
A8h	Decrease Rdet	Triggered Excit.	**Spare**	FD Threshold [3]	FD Threshold [2]	FD Threshold [1]	FD Threshold [0]	01h
A9h	Dig Mux Enable	Dig Mux Sel [5]	Dig Mux Sel [4]	Dig Mux Sel [3]	Dig Mux Sel [2]	Dig Mux Sel [1]	Dig Mux Sel [0]	00h
AAh	Invert BIT Data	Fixed BIT Data	Dig BIT Enable	BIT Data [3]	BIT Data [2]	BIT Data [1]	BIT Data [0]	00h
ABh	Loopback	Analog Reset	Fast Count	Cont. Update		**Par/SSI Int Depth [1]**	**Par/SSI Int Depth [0]**	00h
ACh		Orig Embd Word	Test Embd Word				Single Reg En	20h
ADh	Single Reg ID [6]	Single Reg ID [5]	Single Reg ID [4]	Single Reg ID [3]	Single Reg ID [2]	Single Reg ID [1]	Single Reg ID [0]	00h
AEh					FDRV X [9]	FDRV X [8]	FDRV X [7]	--
AFh	FDRV X [6]	FDRV X [5]	FDRV X [4]	FDRV X [3]	FDRV X [2]	FDRV X [1]	FDRV X [0]	--
B0h			**Frame Pad Length[4]**	**Frame Pad Length[3]**	**Frame Pad Length[2]**	**Frame Pad Length[1]**	**Frame Pad Length[0]**	00h
B1h		Column Advance	Stop On Column			Stop_Col [8]	Stop_Col [7]	00h
B2h	Stop_Col [6]	Stop_Col [5]	Stop_Col [4]	Stop_Col [3]	Stop_Col [2]	Stop_Col [1]	Stop_Col [0]	00h
B3h	**Spare**	Delay Image Off	**Reserved**	GPO Disable[3]	GPO Disable[2]	GPO Disable[1]	GPO Disable[0]	0Fh
B4h	HGC High Delta	HGC High Step	HGC Disable Track		HGC Max. Gain		HGC Frame Type	00h
B5h	HGC Debug	HGC Disable 1/8 Bins	HGC Disable A/D	**Reserved**	HGC Disable Phase	HGC Disable Gain	HGC Disable Init	00h
B6h	HGC Blk Target [6]	HGC Blk Target [5]	HGC Blk Target [4]	HGC Blk Target [3]	HGC Blk Target [2]	HGC Blk Target [1]	HGC Blk Target [0]	26h
B7h	HGC Wht Target [6]	HGC Wht Target [5]	HGC Wht Target [4]	HGC Wht Target [3]	HGC Wht Target [2]	HGC Wht Target [1]	HGC Wht Target [0]	0Dh
B8h	HGC Phase Offset [6]	HGC Phase Offset [5]	HGC Phase Offset [4]	HGC Phase Offset [3]	HGC Phase Offset [2]	HGC Phase Offset [1]	HGC Phase Offset [0]	6Ch
B9h	HGC State [6] [2]	HGC State [5] [2]	HGC State [4] [2]	HGC State [3] [2]	HGC State [2] [2]	HGC State [1] [2]	HGC State [0] [2]	00h
BAh	**SOF Time[13] / GP Timer 1 [13]**	**SOF Time[12] / GP Timer 1 [12]**	**SOF Time[11] / GP Timer 1 [11]**	**SOF Time[10] / GP Timer 1 [10]**	**SOF Time[9] / GP Timer 1 [9]**	**SOF Time[8] / GP Timer 1 [8]**	**SOF Time[7] / GP Timer 1 [7]**	00h
BBh	**SOF Time[6] / GP Timer 1 [6]**	**SOF Time[5] / GP Timer 1 [5]**	**SOF Time[4] / GP Timer 1 [4]**	**SOF Time[3] / GP Timer 1 [3]**	**SOF Time[2] / GP Timer 1 [2]**	**SOF Time[1] / GP Timer 1 [1]**	**SOF Time[0] / GP Timer 1 [0]**	00h
BCh	**EOF Time[13] / GP Timer 2 [6]**	**EOF Time[12] / GP Timer 2 [5]**	**EOF Time[11] / GP Timer 2 [4]**	**EOF Time[10] / GP Timer 2 [3]**	**EOF Time[9] / GP Timer 2 [2]**	**EOF Time[8] / GP Timer 2 [1]**	**EOF Time[7] / GP Timer 2 [0]**	00h
BDh	**EOF Time[6] / GP Timer 3 [6]**	**EOF Time[5] / GP Timer 3 [5]**	**EOF Time[4] / GP Timer 3 [4]**	**EOF Time[3] / GP Timer 3 [3]**	**EOF Time[2] / GP Timer 3 [2]**	**EOF Time[1] / GP Timer 3 [1]**	**EOF Time[0] / GP Timer 3 [0]**	00h
BEh		**SSI A0**	**SSI Int. Enable**			**SSI Master Clk Select[1]**	**SSI Master Clk Select[0]**	00h

[1] Write Only
[2] Read Only

Table 6.2.9-1 Registers Summary

8. Part Numbering Scheme

AES2510 – I – PP – CC – DDEE

I = Temperature Range
I = Extended temperature range = -20C to 70C

PP = Packaging Options
GA = 48 BGA with std. Leaded Balls
GF = 48 BGA with lead free Balls

CC = Carrier Options
CA = Plastic Carrier Trays 240 sensors per tray
TR = Tape & Reel w/ 3500 sensors per reel

DD = Drive Ring Options:
GO = Gold
NI = Nickel

EE = Options
00 = Silicon revision code in 2510 series*

* Contact AuthenTec Sales for current revision code.

Example: AES2510 with Gold ring, Lead-free solder balls, shipped as tape reels:
AES2510-I-GF-TR-GO00

8 Character Backside Laser Part Marking

1 2 3 4 5 6 7 8

1:
Q for Leaded AES2510
D for Lead-free AES2510

2345:
WWYY = date of manufacture in numerical week and year format
WW = 01 – 52, YY = 04 for 2004, etc.

678:
Foundry specific wafer lot code – contact AuthenTec for specific information.

9. Revision History

Version	Date	Person	Reason
Review Version	26 Mar 2004	Lee	Release Date of Public Specification 2510 for Wireless / Mobile Serial I/F applications
Updates	7 April 2004	Lee	Updates from Brandt/Minteer/Schenk/Heilpern
Final	04/26/04	Various	Final Edits
1.1	6/1/04	Lee	External Clock specifications added, A0 and Int pin assignments corrected (1 changed each)
1.2	12 Aug 2004	Lee	Added packaging & part numbering information
1.3	6 Sep 2005	Lee	Added thick package, package weights, corrections