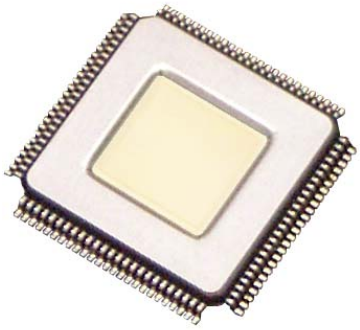
AuthenTec, Inc.
Personal Security for the Real World™

EntréPad AES3400 FINGERPRINT SENSOR
Product Family Specification

Hardware Reference



Sensor Shown 4X Actual Size

2257 Rev 1.1
May 12, 2004

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Product Specification for the AES3400 Fingerprint Sensor
2257 Rev 1.0(21OCT03)

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1. EntrePad AES3400 Fingerprint Sensor

Introducing…

…the AuthenTec EntréPad™ AES3400™; AuthenTec's 3rd generation low power, small form-factor fingerprint identification sensor IC. This product combines silicon-based image capture with proprietary sensor control and matching algorithms to deliver the best Ability-To-Acquire (ATA) fingerprint images in the biometrics industry.

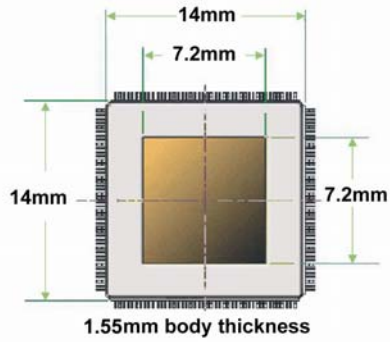
AuthenTec's EntréPad AES3400 utilizes TruePrint® Technology, allowing the sensor to look past the easily obscured outer surface of the skin to the living layer below where the unique ridge and valley patterns of the fingerprint originate.

TruePrint® is…

…AuthenTec's unique patented imaging technology. During imaging, a small near-field signal is generated between the IC and the finger's living tissue layer. 16,384 individual elements in the sensor matrix form a planar antenna array that receives this signal, creating a digital pattern that accurately reproduces the fingerprint's underlying structure.
A powerful utility contained within TruePrint® Technology™ is Dynamic Optimization™. This tool analyzes each image, controlling up to 15 sensor parameters to optimize the fingerprint image, regardless of unusual skin conditions or surface contamination.

Feature Summary

- ✓ Patented TruePrint® Technology for best Ability To Acquire (ATA)
- ✓ Compact Industry Standard 100-Pin LQFP Package
- ✓ High Definition 128 X 128 TruePrint® Technology Based Pixel Array
  - o 500 pixels per inch (ppi)
- ✓ Extended Range 2.7V to 3.6V single power supply
- ✓ 0°C to +70°C operating temperature range
- ✓ Easy to Integrate USB 2.0 Full Speed, Synchronous & Asynchronous Serial, & 8-bit Parallel System Interfaces
- ✓ 6 or 12MHz Operation with Crystal or supplied clock input
- ✓ USB Selective Suspend Support
- ✓ Ultra-hard surface coating
  - o > 1 Million rubs w/o degradation
  - o Highly scratch resistant
- ✓ IEC 61000-4-2 Level 3 ESD Capability (+/- 8KV)
- ✓ Built-in low power Finger Detection w/system interrupt capability
- ✓ Low power operation; <6mW / imaging event



The form factor of the EntréPad AES3400 is 100-pin JEDEC-standard Low-profile Quad Flat Package (LQFP)

2. INTRODUCTION

The *AES3400 Product Specification* is a hardware reference manual. It describes in detail the physical organization, operation, interfaces, and internal functionality of the AuthenTec EntréPad™ AES3400™ fingerprint sensor integrated circuit.

The AES3400 sensor uses state-of-the-art techniques to capture and transmit a fingerprint from a user to a host computer. Reference Design Kits are available that can assist the developer in producing designs that take advantage of the powerful features of this chip.

> **Note:** Users should be aware that information on AuthenTec's products, the Company, and other matters (including software updates) are available on the AuthenTec web site at www.authentec.com.
>
> For further information or guidance, contact AuthenTec Application Engineering at mailto:apps@authentec.com for the latest product information.

2.1 Scope

This hardware specification is intended for the use of hardware designers, software designers, and others who require detailed information about the functionality and operation of the AES3400 sensor.

2.2 Applicability

This edition of the *AES3400 Product Specification* is the production release version 1.0. It replaces all preliminary versions with various changes. The material in this document applies only to the AuthenTec AES3400 sensor.

2.3 Conventions

2.3.1 Vector Presentation

For vectors (groups of bits), ordering will always be from MSB to LSB (for example, Pixel_Data[47:0] where bit 47 is the MSB and bit 0 is the LSB).

When vectors that span multiple bytes are transmitted, the lower byte (bits [7:0]) is transmitted first. This applies to pixel data and the authentication word returned after each imaging frame.

2.3.2 Typography and Related Information

Numbers followed by a "b" are in binary notation. Numbers followed by an "h" are in hexadecimal.

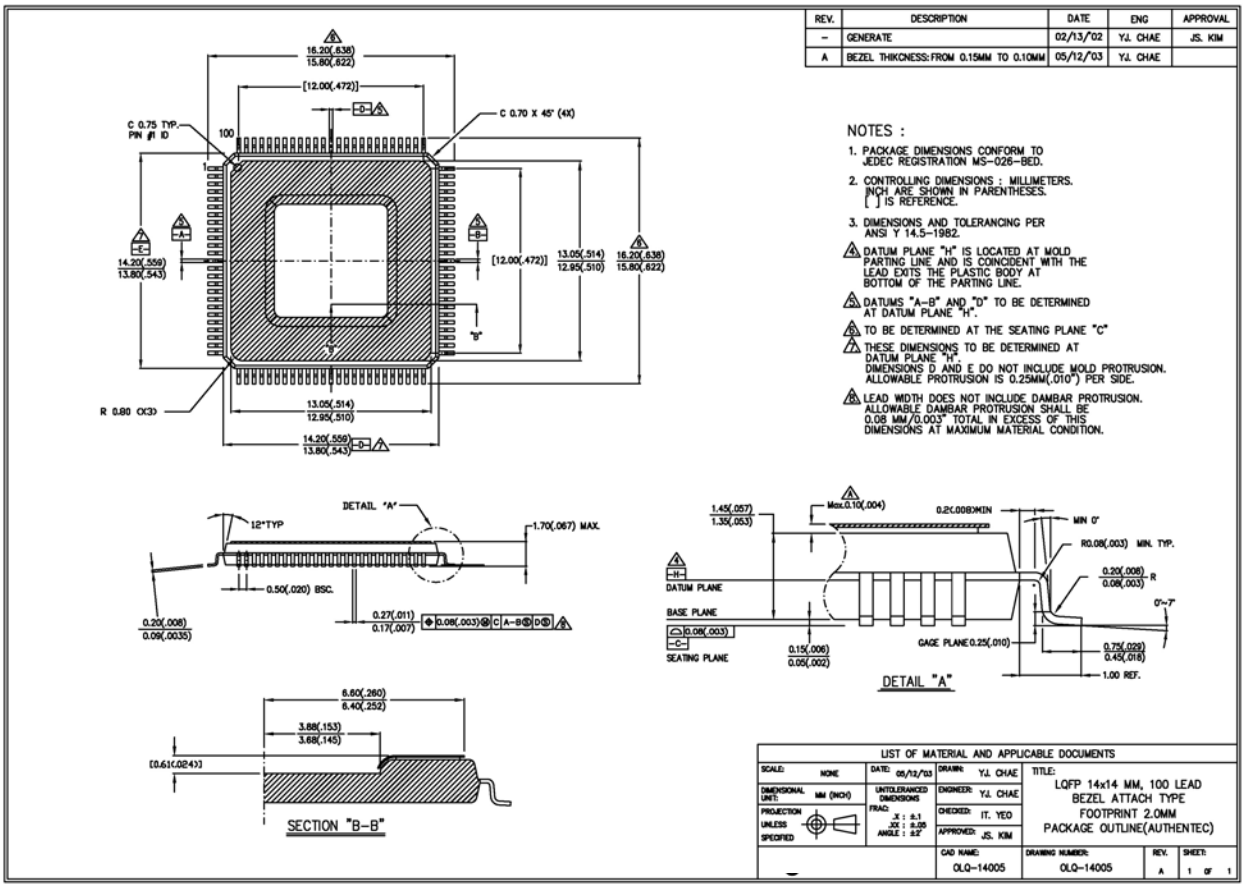
Reference

This publication is prepared and presented in accordance with the guidelines and conventions of the *Microsoft Manual of Style for Technical Publications*, Microsoft Press, Redmond WA USA. Other reference material includes the *Chicago Manual of Style*, University of Chicago Press, Chicago IL, and the *IBM Dictionary of Computing*, Information Development, Poughkeepsie NY.

3. AES3400 SPECIFICATIONS

3.1 AES3400 Package Drawing

The AES3400 sensor is packaged in a JEDEC-standard 100-pin LQFP (Low-profile Quad Flat Package). A nickel plated stainless steel bezel is attached to the top of the package to provide the necessary TruePrint® drive signal to the finger. The most current package drawing can always be found on the AuthenTec website at www.authentec.com.



3.2 Functional Summary

The AES3400 sensor is comprised of a **sensor matrix**, a nickel plated stainless steel **drive bezel**, and supporting electronics. The purpose of these elements is to detect the presence of a finger placed on the surface of the sensor matrix, and to reliably produce a digital image of the fingerprint. This image must be suitable for processing through AuthenTec, AuthenTec Solution Provider, or third-party software for the purpose of identifying (authenticating) the person associated with the image.

3.2.1 The Sensor Matrix

A fingerprint imaging platen, the *sensor matrix*, occupies the center of the chip. This opening in the package is 7.2mm square, with the actual array occupying an area of 6.5mm square, and is the actual surface of the integrated circuit die.

The surface of the *sensor matrix* is treated with a proprietary, advanced ceramic coating, having a Mohs hardness rating of 7+. The purpose of this layer is to protect the exposed IC and to generally resist abrasion, scratches, and wear.

The *sensor matrix* is comprised of 16,384 individual elements arranged in a 128 x 128 square pattern. It is further organized into eight rectangular rows or “sub-arrays” (numbered 0 through 7), each containing 128 columns of 16 pixels (1,536 elements). With the notched corner of the IC on the lower right (when viewed from the *sensor matrix* side) the 128X16 pixel rows are oriented in horizontal bands across the surface with row 0 at the bottom proceeding to row 7 at the top.

Each element in the *sensor matrix* is provided with an under-pixel amplifier, a synchronous demodulator, and a spatial filter node. Scanning each column within an enabled row digitizes the image. In sequence, each of the 16 pixels in the column of the enabled row is sampled and digitized.

The AES3400 has three pin-selectable interfaces: Parallel, Asynchronous Serial, Synchronous Serial and USB. For each configuration, the designer must be careful to appropriately tie unused inputs on the package.

3.2.2 The Drive Ring

A square annular drive ring bezel surrounds the sensor matrix. The *drive ring* is excited by on-chip direct digital synthesis components that typically generate a sinusoidal signal. As part of Dynamic Optimization™ the phase, frequency, and amplitude of this signal is programmatically controlled by the sensor control registers.

3.3 Functional Block Diagram

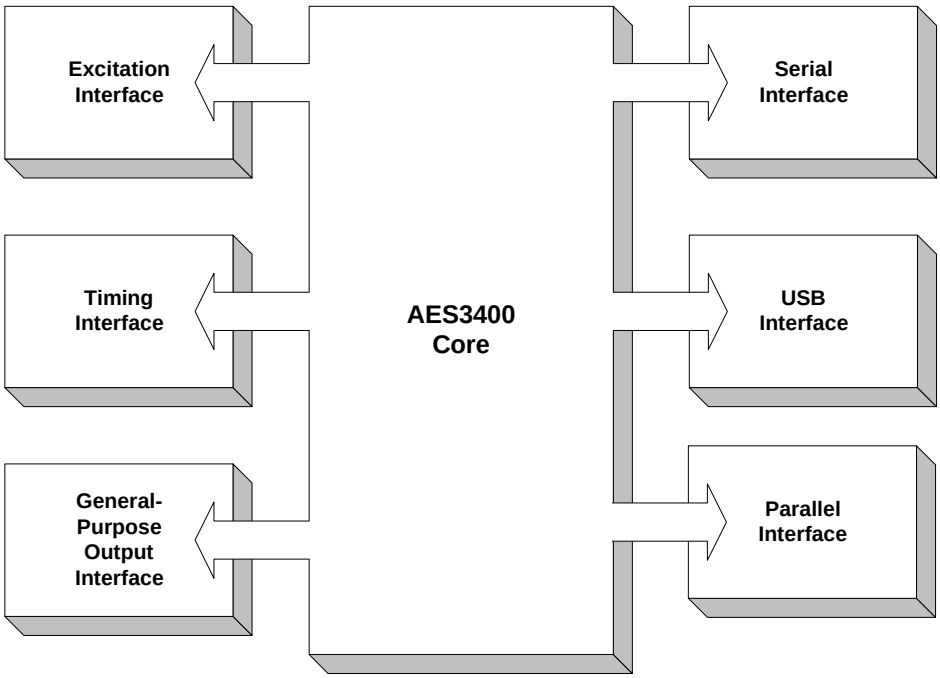


Figure 3-2 Top-level Sensor Block Diagram

3.4 Interface Descriptions

Interface	Description
Serial Interface	When selected, provides asynchronous Serial control for the Sensor IC and serial response including pixel data and current register settings. The data rate and format is selectable.
Analog Interface	Provides interfaces for analog signals requiring off-chip components. These include the PLL charge pump filter and filtering for the finger ring drive signal.
GPIO Interface	Four general purpose Input/Output pins for user convenience.
System Interface	Clock and reset signals.
USB Interface	When selected, provides control and data interface to USB 2.0 compliant host controller using the Full Speed (12Mbps) option.
Parallel Interface	When selected, provides control and data interface for a generic parallel bus. Includes address, data, select, control, and interrupt signals.

3.5 PIN LIST – USB Configuration

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	GND	26	GND	51	VDD	76	GND
2	OVC_VDDA	27	RESERVED	52	GND	77	M2PLATE
3	OVC_DET	28	RESERVED	53	D+	78	M2PLATE
4	VSSL	29	RESERVED	54	D-	79	M2PLATE
5	OVC_VDDD	30	RESERVED	55	PID0	80	M2PLATE
6	VSSL	31	DRIVE_RING	56	GPIO0	81	DRIVE_RING
7	ENUM	32	DRIVE_RING	57	GPIO1	82	DRIVE_RING
8	VDDL	33	DRIVE_RING	58	PID1	83	DRIVE_RING
9	VSSL	34	DRIVE_RING	59	PLL_FILTER	84	DRIVE_RING
10	GND	35	DRIVE_RING	60	XTAL_IN	85	DRIVE_RING
11	VDDA	36	DRIVE_RING	61	PID4	86	DRIVE_RING
12	GND	37	DRIVE_RING	62	GND	87	DRIVE_RING
13	VDDA	38	DRIVE_RING	63	VDD	88	DRIVE_RING
14	M2PLATE	39	DRIVE_RING	64	GND	89	DRIVE_RING
15	RESERVED	40	DRIVE_RING	65	FINGERDRIVE	90	DRIVE_RING
16	RESERVED	41	DRIVE_RING	66	VDDA	91	DRIVE_RING
17	RESERVED	42	DRIVE_RING	67	GPIO2	92	DRIVE_RING
18	RESERVED	43	DRIVE_RING	68	GPIO3	93	DRIVE_RING
19	6/12MHz	44	DRIVE_RING	69	PID2	94	DRIVE_RING
20	VSSL	45	DRIVE_RING	70	PID3	95	DRIVE_RING
21	VDDL	46	M2PLATE	71	GND	96	RESERVED
22	VDDL	47	M2PLATE	72	VDD	97	RESERVED
23	PLL_ENABLE*	48	M2PLATE	73	SUSPEND	98	RESERVED
24	VDD_ON*	49	M2PLATE	74	USB_OE*	99	RESERVED
25	VDDA	50	RESET*	75	VDDA	100	OVC_SENSE

USB Implementation Notes:

Reserved PIDs are listed below for specific sensor orientations

- 4h = 0 degrees
- 5h = 90 degrees
- 6h = 180 degrees
- 7h = 270 degrees

Other PID's are available upon request. Contact mailto:apps@authentec.com

3.6 PIN LIST – Asynchronous & Synchronous Serial

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	GND	26	GND	51	RESERVED	76	GND
2	OVC_VDDA	27	RESERVED	52	GND	77	M2PLATE
3	OVC_DET	28	RESERVED	53	NU/A0	78	M2PLATE
4	VSSL	29	RESERVED	54	NU/INT	79	M2PLATE
5	OVC_VDDD	30	RESERVED	55	BAUD1/NU	80	M2PLATE
6	VSSL	31	DRIVE_RING	56	GPIO0/GPIO0	81	DRIVE_RING
7	NU/SSI_NORM	32	DRIVE_RING	57	GPIO1/GPIO1	82	DRIVE_RING
8	VDDL	33	DRIVE_RING	58	BAUD0/NU	83	DRIVE_RING
9	VSSL	34	DRIVE_RING	59	PLL_FILTER	84	DRIVE_RING
10	GND	35	DRIVE_RING	60	XTAL_IN	85	DRIVE_RING
11	VDDA	36	DRIVE_RING	61	NU/NU	86	DRIVE_RING
12	GND	37	DRIVE_RING	62	GND	87	DRIVE_RING
13	VDDA	38	DRIVE_RING	63	VDD	88	DRIVE_RING
14	M2PLATE	39	DRIVE_RING	64	GND	89	DRIVE_RING
15	RESERVED	40	DRIVE_RING	65	FINGERDRIVE	90	DRIVE_RING
16	RESERVED	41	DRIVE_RING	66	VDDA	91	DRIVE_RING
17	RESERVED	42	DRIVE_RING	67	GPIO2/GPIO2	92	DRIVE_RING
18	RESERVED	43	DRIVE_RING	68	GPIO3/GPIO3	93	DRIVE_RING
19	6/12MHz	44	DRIVE_RING	69	TX/DX	94	DRIVE_RING
20	VSSL	45	DRIVE_RING	70	AUTOBAUD_EN/CLK	95	DRIVE_RING
21	IO_SEL1	46	M2PLATE	71	GND	96	RESERVED
22	IO_SEL0	47	M2PLATE	72	VDD	97	RESERVED
23	PLL_ENABLE*	48	M2PLATE	73	RTR/FS	98	RESERVED
24	VDD_ON*	49	M2PLATE	74	RXD/DR	99	RESERVED
25	VDDA	50	RESET*	75	VDDA	100	OVC_SENSE

3.7 PIN LIST – 8-bit Parallel

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	GND	26	GND	51	RESERVED	76	GND
2	OVC_VDDA	27	RESERVED	52	GND	77	M2PLATE
3	OVC_DET	28	RESERVED	53	D7	78	M2PLATE
4	VSSL	29	RESERVED	54	D6	79	M2PLATE
5	OVC_VDDD	30	RESERVED	55	D5	80	M2PLATE
6	VSSL	31	DRIVE_RING	56	A0	81	DRIVE_RING
7	INT	32	DRIVE_RING	57	IOR*	82	DRIVE_RING
8	VDDL	33	DRIVE_RING	58	D4	83	DRIVE_RING
9	VSSL	34	DRIVE_RING	59	PLL_FILTER	84	DRIVE_RING
10	GND	35	DRIVE_RING	60	XTAL_IN	85	DRIVE_RING
11	VDDA	36	DRIVE_RING	61	READY	86	DRIVE_RING
12	GND	37	DRIVE_RING	62	GND	87	DRIVE_RING
13	VDDA	38	DRIVE_RING	63	VDD	88	DRIVE_RING
14	M2PLATE	39	DRIVE_RING	64	GND	89	DRIVE_RING
15	RESERVED	40	DRIVE_RING	65	FINGERDRIVE	90	DRIVE_RING
16	RESERVED	41	DRIVE_RING	66	VDDA	91	DRIVE_RING
17	RESERVED	42	DRIVE_RING	67	IOW*	92	DRIVE_RING
18	RESERVED	43	DRIVE_RING	68	CE*	93	DRIVE_RING
19	6/12MHz	44	DRIVE_RING	69	D3	94	DRIVE_RING
20	VSSL	45	DRIVE_RING	70	D2	95	DRIVE_RING
21	VSSL	46	M2PLATE	71	GND	96	RESERVED
22	VSSL	47	M2PLATE	72	VDD	97	RESERVED
23	PLL_ENABLE*	48	M2PLATE	73	D1	98	RESERVED
24	VDD_ON*	49	M2PLATE	74	D0	99	RESERVED
25	VDDA	50	RESET*	75	VDDA	100	OVC_SENSE

3.8 Device Level Pin Descriptions & Specifications

Grouped in relevant categories by interface

3.8.1 System Interface

Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
XTAL_IN	60	I	CMOS	12	Input from crystal or external clock source.
RESET*	50	I	CMOS	N/A	Active low reset. This pin has an internal pull-up ~57K with ±20% tolerances such that a capacitor to ground can be added to implement a power on reset.
IO_SEL1	21	I	CMOS	N/A	Along with IO_SEL0, selects the active interface as follows: IOSEL[10] 00 Parallel I/O 01 Asynchronous Serial I/O 10 Synchronous Serial I/O 11 USB I/O Note: there are no internal pull-ups on IO_SEL1 or IO_SEL0
IO_SEL0	22	I	CMOS	N/A	Along with IO_SEL1, selects the active interface.
6/12MHZ	19	I	CMOS	N/A	When high, requires 6MHz clock input

3.8.2 SIO Definitions by Interface Type

For each interface selection, the following pin assignments will apply:

PIN	Parallel		Async. Serial		Sync. Serial		USB	
7	INT	O	reserved	O	SPI_NORMAL	O/I	ENUM	O
53	D7	B	Not Used	O	A0	I	D+	B
54	D6	B	Not Used	O	INT	O	D-	B
55	D5	B	BAUD1	I	CLKX	I	PID0	O/I
56	A0	I	GPIO0	B	GPIO0	B	GPIO0	B
57	IOR*	I	GPIO1	B	GPIO1	B	GPIO1	B
58	D4	B	BAUD0	I	FSX	I	PID1	O/I
61	READY	O	Not Used		Not Used		PID4	O/I
67	IOW*	I	GPIO2	B	GPIO2	B	GPIO2	B
68	CE*	I	GPIO3	B	GPIO3	B	GPIO3	B
69	D3	B	TX	O	DX	O	PID2	O/I
70	D2	B	AUTOBAUD_EN	I	CLK	I	PID3	O/I
73	D1	B	RTR	I	FS	I	SUSPEND	O
74	D0	B	RXD	I	DR	I	USB_OE*	O

Figure 3-3 SIO Definition for each Interface

3.8.3 USB Interface

Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
D+	53	I/O	USB	12	D+ USB internal transceiver pin
D-	54	I/O	USB	12	D- USB internal transceiver pin
SUSPEND	73	O	CMOS	N/A	SUSPEND goes active when the host controller issues a *SUSPEND* command to the AES3400
USB_OE*	74	O	CMOS	N/A	USB_OE goes active when the AES3400 is in USB transmit mode.
PID0	55	I	CMOS	2	USB Product ID
PID1	58	I	CMOS	2	USB Product ID
PID2	69	I	CMOS	2	USB Product ID
PID3	70	I	CMOS	2	USB Product ID
PID4	61	I	CMOS	2	USB Product ID

3.8.4 Asynchronous Serial Interface

Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
BAUD0	58	I	CMOS	N/A	
BAUD1	55	I	CMOS	N/A	Used to select fixed baud rate according to the table below: BAUD[1:0] Baud Rate 00 - 115k bps (do not use) 01 - 460k bps (do not use) 10 - 750k bps Recommended 11 - 921k bps Recommended
RTR	73	I	CMOS	N/A	Ready To Receive. High to enable sending serial data to host
RXD	74	I	TTL	2	Serial data received from host
TX	69	O	CMOS	2	Serial data transmitted to host

The data is formatted using a standard asynchronous protocol. The idle state of the line is high. Each data byte sent is preceded by a low start bit and followed by a high stop bit. Each byte is sent LSB first.

3.8.5 Parallel Interface

Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
CE*	68	I	CMOS	8	Active low chip enable
READY	61	O	CMOS	8	Active high request for wait state
IOR*	57	I	CMOS	8	Active low read enable
IOW*	67	I	CMOS	8	Active low write enable
INT	7	O	CMOS	8	Active high interrupt
D7	53	B	CMOS	8	MSB of parallel data
D6	54	B	CMOS	8	Parallel data bit
D5	55	B	CMOS	8	Parallel data bit
D4	58	B	CMOS	8	Parallel data bit
D3	69	B	CMOS	8	Parallel data bit
D2	70	B	CMOS	8	Parallel data bit
D1	73	B	CMOS	8	Parallel data bit
D0	74	B	CMOS	8	LSB of parallel data
A0	56	I	CMOS	8	Address input

3.8.6 Latch-up Circumvention Function

The Latch-up Circumvention Circuit is a totally self-contained function that is included to deal with ESD induced latch-up. The basic circuit functionality is as follows: Powered off of its own independent power pins (OVC_VDDD – GND and OVC_VDDA - VSSL), the circuit senses voltage on an external current sense resistor via OVC_VDDA and OVC_SENSE and uses this information to control power to the rest of the sensor using OVC_DET.

Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
GND	1	GND	N/A	N/A	Independent ground pad for Latch-up recovery circuit
OVC_VDDD	5	PWR	N/A	N/A	Independent power pad for Latch-up recovery circuit
OVC_DET	3	O	CMOS	N/A	Power control, designed to drive P-channel FET to switch power off if latch-up condition is detected
OVC_SENSE	100	I	Analog	N/A	Least positive sense voltage on sense resistor, “load side”
OVC_VDDA	2	I/ PWR	Analog	N/A	Most positive sense voltage on sense resistor as well as supply pin for analog portion of OVC circuit.
VSSL	4	I	CMOS	N/A	Reserved

Table 3-1 Latch-up Circumvention Signal Description

4. OPERATING CONDITIONS

4.1 Absolute Maximum Ratings

An absolute maximum rating is the maximum value guaranteed by ASIC manufacturer. The use of a product in violation of these ratings can result in significant loss of device reliability or even damage to the IC.

Symbol	Parameter	Min.	Max.	Units
V_{CC}	Supply Voltage	-0.5	3.9	V
V_I	Input Voltage	-0.5	V_{CC}	V
V_O	Output Voltage	-0.5	V_{CC}	V
I_{IK}	Input Clamp Current $V_I < V_{SS}$ of $V_I > V_{CC}$		±20	mA
I_{OK}	Output Clamp Current $V_O < V_{SS}$ of $V_O > V_{CC}$		±20	mA
T_{STG}	Storage Temperature	-65	150	°C
Latch-Up	I/O Latch-Up Immunity	±100		mA

Absolute Maximum Ratings

4.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ	Max.	Units
V_{cc}	Supply Voltage	2.7	3.3	3.6	V
V_I	Input Voltage	0		V_{CC}	V
V_O	Output Voltage (IOH=0mA)	0		V_{CC}	V
V_{IH}	High Level Input Voltage	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage	0		0.8	V
T_t	Input Transition (Rise and Fall) Time	0		3	ns
T_a	Ambient Operating Temperature	0		70	°C

Recommended Operating Conditions

4.3 Electrical DC Characteristics

Symbol	Parameter	Conditions	Min.	Typ	Max.	Units
V_{OH}	High Level Output Voltage	I_{OH}=2mA	V_{CC}-0.3			V
V_{OL}	Low Level Output Voltage	I_{OL}=-2mA			0.3	V
I_{IL}	Low Level Input Current	$V_I=V_{IL}$(min.)			±1	µA
I_{IH}	High Level Input Current	$V_I=V_{IH}$(max.)			±1	µA
I_{OZ}	High Impedance State Output Current				±20	µA
I_{ccq}	Quiescent Supply Current (deselected, using Overcurrent protection circuit, non-USB)	$V_{IN}=V_{cc}$ OR $V_{IN}=V_{ss}$ Vcc=Max.			150	uA
I_{ccq}	Deselected Supply Current USB	$V_{IN}=V_{cc}$ OR $V_{IN}=V_{ss}$ Vcc=Max.			400	uA
I_{ccq}	Low Power Finger Detect Supply Current (Based upon 1, detect / second)	$V_{IN}=V_{cc}$ OR $V_{IN}=V_{ss}$ Vcc = Typ		250	1000	uA
I_{ccq}	Active Supply Current (not imaging) w/8 detects/second.	$V_{IN}=V_{cc}$ OR $V_{IN}=V_{ss}$ Vcc = Typ		4		mA
I_{ccq}	Imaging Supply Current (imaging, sense amp bias = max)	$V_{IN}=V_{cc}$ OR $V_{IN}=V_{ss}$ Vcc = Max.		55	65	mA

Electrical DC Characteristics

Power Dissipation Notes

- ✓ In the imaging state, the sensor current depends on various bias current settings and the kernel (cloud) size. Imaging currents can range from 35mA to 65mA typically depending on these settings. Using standard AuthenTec SW settings, the typical Iccq currents are valid.
- ✓ Imaging takes place over a very short ¼ to ½ second. Thus, average power consumption and energy usage of the sensor from the system perspective is extremely low.

4.4 ELECTRICAL INTERFACES

4.4.1 Asynchronous Serial Interface

The Serial Interface provides a serial data in and out for communication with the sensor. In addition, the interface has two signals that select the baud rate (BAUD1-BAUD0) and a Ready-To-Receive signal (RTR) that allows the host to throttle data from the sensor. The sensor is always ready to accept input data, so no throttling is necessary for data written to the sensor.

4.4.2 USB Interface

The USB interface is compliant with version 2.0 of the USB specification for full speed devices. AES3400 is a USB low power device. The implementation will utilize 3 endpoints in one interface and will support dual 64 byte ping-pong buffers for transmission of image data from the sensor to the host.

Endpoint 0 will support control read and write transactions, including String Descriptor support for the device identification function in Windows, Endpoint 1 will be a BULKIN endpoint for data going from the Sensor to the Host, and Endpoint 2 will be a BULKOUT endpoint for Sensor commands from the Host.

On chip pull-ups will not be used in AES3400 in order to meet the USB suspend current specification. The upper 8 bits of the Product ID field are set to 34h. The AuthenTec Product ID will be 34nn(hex), requiring the eight PID data package pins to be tied to appropriate VDD/GND levels external to the package to program the lower byte of the ID to the desired value.

4.4.3 Parallel Interface

The Parallel Interface is microprocessor bus compatible, and provides a high-speed parallel data and control bus port into the sensor. The interface also provides a selectable interrupt signal to the processor to signal data availability (INT) or can be used in a polled fashion. The parallel interface utilizes two I/O ports to minimize resource requirements in the IO port address space of the PC architecture. The system hardware, external to the sensor, must provide an external decode signal (Chip Enable, CE_N, active low) to indicate that the address decode of the other 9 I/O address lines is satisfied.

The parallel interface is also only active when the USB interface and serial interfaces are inactive, as selected with IO_SEL[1:0] input pins, with parallel bus outputs held in the tri-stated condition when inactive. The Address/Data port, Address 0, will function essentially like a byte wide version of the serial interface. The host software will write commands and data or write commands and read streams of parallel data by sending register addresses followed by update values or commands. Parallel port status is available on Address 1.

When the parallel port interrupt is enabled, an interrupt will be generated on the INT pin whenever data from any of the potential internal data sources is ready to be read from the sensor, including the 2 byte message generated during low power finger detect activation. The interrupt will go inactive at the end of each group read. The parallel bus is asynchronous to the internal sensor clock and

will be synchronized to transitions on the IOR_N (I/O Read) and IOW_N (I/O Write) control lines, which are conditioned with Schmitt input buffers for noise immunity.

Standard processor bus timing will be supported on this bus along with high drive, tri-state output buffers. The logical model for the two ports is shown in table below. The parallel interface will require1 pins: 4 inputs, 8 bi-directs, and 2 outputs.

When the USB interface is selected, the 8 data lines will define the low byte of the Product ID in the USB configuration space and must not be left floating. These pins must also be tied to either power or ground when using the Serial interface.

At power up, the interface will be in Polled mode (interrupts disabled) – Control Byte, Bit 7 = '0'. Also, the master reset control will not change the Interrupt/Polled state configuration. The INT pin goes active when the chip has data to output. The INT pin will stay active until it is explicitly cleared by writing address 0x1 with a '1' in the D6 position. If the interrupt is cleared before all the data associated with the interrupt is read, it will not get set again for the remaining bytes. If there is "stacked" data (e.g. at the end of an image frame when the chip has authentication data and register to be sent), the interrupt could get set immediately after the last byte of the current message is read.

The parallel bus will also support bus cycle time stretching via the 'READY' pin. This pin must be low before an access cycle can start. This output will be driven active high by the sensor to indicate when the sensor is ready for either a read or write cycle to complete, providing a means to use the sensor with processors that have faster bus cycles than the sensor can normally support.

Port Address Value [SA0]	Port Function [Default State]
0x0	**Address/Data port [DFh]**
0x1	**Control/Status port [0000_0000]** Bit 7- Interrupt Enable/Polled Enable#[0] Bit 6- Interrupt Clear[0] Bit 5- 0 Bit 4- 0 Bits [3:1]- Encoded Data Available bits 000-No Data [default] 001-Row Header (1 byte) 010-Pixel Data (8 bytes) 011-Histogram Data (33 bytes) 100-Authentication Data (9 bytes) 101-Register Data (114 bytes) 110-Single Register (2 bytes) Bit 0- Data available handshake bit for Polled operation, active low [0]

Parallel Interface IO Port Assignment

4.5 USB Device Descriptor Information

Configuration 2 Descriptor

Offset	Field	Index(dec)	Value	Meaning
91	bLength	0	09h	Length of this descriptor = 9 bytes
92	bDescriptorType	1	02h	Type = Configuration
93	wTotalLength(L)	2	20h	Total Length(L) including Interface and Endpoint descriptors
94	wTotalLength(H)	3	00h	
95	bNumInterfaces	4	01h	Number of interfaces in this configuration
96	bConfigurationValue	5	02h	Configuration value used by Set_Configuration to select this interface
97	iConfiguration	6	00h	00h = no string reference
98	bmAttributes	7	A0h	A0h, Attributes: bus-powered, remote wake-up supported for low power finger detect
99	MaxPower	8	32h	Max current =100mA

Configuration 2, Interface 0, Alternate Setting 0 Descriptor

Offset	Field	Index(dec)	Value	Meaning
100	bLength	0	09h	Length of the Interface descriptor = 9 bytes
101	bDescriptorType	1	04h	Descriptor type = interface
102	bInterfaceNumber	2	00h	Zero based index of this interface = 0
103	bAlternateSetting	3	00h	Alternate setting =0
104	bNumEndpoints	4	02h	Number of endpoints in this interface (not counting endpoint0)
105	bInterfaceClass	5	FFh	Interface Class = vendor specific
106	bInterfaceSubClass	6	FFh	Interface Sub Class = vendor specific
107	bInterfaceProtocol	7	FFh	Interface Protocol = vendor specific
108	iInterface	8	00h	Index to string descriptor = none

Configuration 2, Interface 0, Alternate Setting 0, Bulk Endpoint Descriptors

Offset	Field	Index(dec)	Value	Meaning
109	bLength	0	07h	Descriptor length = 7 bytes long
110	bDescriptorType	1	05h	ENDPOINT descriptor
111	bEndpointAddress	2	81h	In endpoint, endpoint #1
112	bmAttributes	3	02	xfr type = Bulk
113	wMaxPacketSize(L)	4	20h	Max Packet Size = 32 bytes
114	wMaxPacketSize(H)	5	00h	
115	bInterval	6	00h	Polling interval in milliseconds
Offset	**Field**	**Index(dec)**	**Value**	**Meaning**
116	bLength	0	07h	Descriptor length = 7 bytes long
117	bDescriptorType	1	05h	ENDPOINT descriptor
118	bEndpointAddress	2	02h	Out endpoint, endpoint #2
119	bmAttributes	3	02	xfr type = Bulk
120	wMaxPacketSize(L)	4	08h	Max Packet Size = 8 bytes
121	wMaxPacketSize(H)	5	00h	
122	bInterval	6	00h	Polling interval in milliseconds

String 0 Descriptor

Field	Index	Value	Meaning
bLength	0	04h	String Index 0
bDescriptorType	1	03h	String descriptor type
wLANGID(0)(L)	2	09h	Language ID for English (L)
wLANGID(1)(H)	3	04h	Language ID for English (H)

String 2 Descriptor

Field	Index	Value	Meaning
bLength	0	26h	String Index 1
bDescriptorType	1	03h	String descriptor type
bString	2	4600h	“Fingerprint Sensor” – in UNICODE format “F”
	4	6900h	“i”, 00
	6	6E00h	“n”, 00
	8	6700h	“g”, 00
	10	6500h	“e”, 00
	12	7200h	“r”, 00
	14	7000h	“p”, 00
	16	7200h	“r”, 00
	18	6900h	“i”, 00
	20	6E00h	“n”, 00
	22	7400h	“t”, 00
	24	2000h	“ “, 00
	26	5300h	“S”, 00
	28	6500h	“e”, 00
	30	6E00h	“n”, 00
	32	7300h	“s”, 00
	34	6F00h	“o”, 00
	36	7200h	“r”, 00

4.6 Clock Generation and Distribution Notes

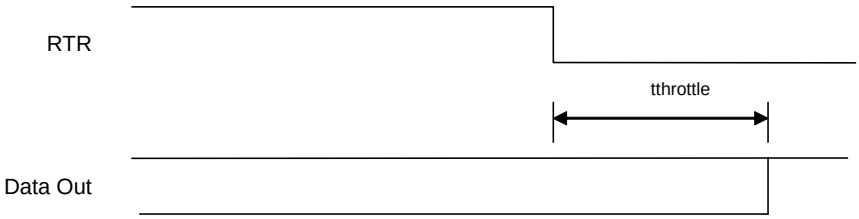
The input clock is 12 MHz when generated from a crystal. When using an on-board oscillator or driven from an external source, the clock source may be 12 MHz or 6 MHz. The 6/12MHZ pin (19) selects the frequency.

An internal PLL multiplies the input frequency to generate an internal 48 MHz clock used for the USB interface. Other than the USB input data sampling and input data sampling on the parallel bus, all logic runs off the input clock.

Use of the PLL_BYPASS control allows driving the MCLKIN pin with an externally generated clock for test purposes or when a clock frequency other than 48MHz is desired.

4.7 Asynchronous Serial Interface

The RTR input can be used to throttle the data output from the chip. The following diagram shows the timing associated with RTR disabling.



RTR Response Timing Diagram

The serial out circuitry in the sensor consists of a one-byte buffer feeding an output shift register. The RTR input is sampled whenever the output shift register is empty; the shift register is not loaded until RTR is active. As long as RTR is de-asserted more than 35 ns before the end of the stop bit, data transmission will stop at the end of the current byte.

As mentioned earlier, RTR will also pause the scan if the internal buffers are not ready to send data. This feature can be disabled so that column scan timing is not altered and these conditions instead cause loss of image data. The amount of time that RTR can be de-asserted will then be limited by the column scan period setting and the baud rate. If RTR is de-asserted for more than the difference between the two column scan periods and the time to send 16 bytes serially, image data will be lost. For example, 21.7 us are required to send each byte at 460.8 Kbps. For a column scan period setting of 256 us, RTR should not be de-asserted for more than 164.8 us every two column periods (512 – 348.8).

4.8 Synchronous Serial Interface [SSI]

Relevant Registers:
Reg81-bit D6 – Interrupt enable
Reg81-bit D5 – Address control. Selects either the Register Address/Data port (A0 = 0) or the Status port (A0 = 1) for the type of data to be transmitted from the sensor.

NOTE: External signal A0 pin [B9] should be held low when using the register control method, register 81 bit D5 above.

Reg81 – bit D6 – Interrupt Enable. Setting bit D6 in Register 81 enables interrupts.

The Synchronous Serial Interface provides serial data in and out for communication with the sensor. This interface acts as a **slave mode** interface only. External data transmit/receive clocks, with a maximum bit rate of 6Mbps, control the data transmission rate. The synchronous serial interface supports 8-bit mode only.

The SSI supports both clock normal and clock opposite phases controlled by the SSI_NORM pin B11. The SPI™-compatible modes support either continuous clock – gated frame protocol or continuous select – gated clock protocol. For all data rates and formats, the data is formatted for a SPI™-compatible synchronous protocol. Each byte is sent most significant bit first. For power cycling/control of these interfaces, please refer to the section of sensor power cycling and application notes supporting the AES3400 sensor.

The usage model of the SSI is similar to other AuthenTec sensors. The host processor has the ability read data when the sensor has no data to provide. For that reason, the transmit data byte source is selectable between both a status register and the sensor data register. In normal operation, the host selects the status register, and reads that until the register indicates data is available. An alternative is to use the INT pin [B10] as a data available indicator.

The host then selects the data register and reads the correct number of bytes from the sensor. The Port Address is set either via an internal register bit or via a package pin (A0) as noted above.

By design the SSI is a full duplex communication scheme, so the host processor (master side of the SSI) must manage the ‘filler’ data produced when reading or writing to the sensor. Inactive filler data should be FFh.

4.8.1 Synchronous Serial Interface Description

SSI Synchronous Serial Connection Diagram

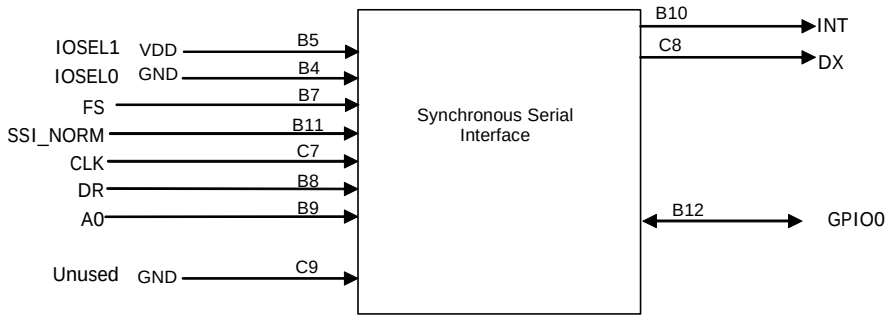


Figure 4-1 SSI-compatible Interface Diagram

SSI Signal Name	Pin	Pin Type	Description
DR	74	I	Receive Data
FS	73	I	Frame Sync. Signal
CLK	70	I	Receive Clock
DX	69	O	Transmit Data. This signal goes high impedance when FS is high
GPIO0 – GPIO3	56, 57, 67, 68	I/O	General Purpose Input/Output
SSI_NORM	7	I	Selects Normal phase (non-inverted clock) when high, selects Opposite phase (inverted clock) when low.
INT	54	O	Interrupt output to indicate data is available when high
A0 [SIO7]	53	I	Address, when low selects data, when high selects status byte
Unused	61	I	Tie this pin Low.

Figure 4-2 SSI Synchronous Serial Interface Signal Descriptions

Port Address Value [A0] either Register bit or A0 Pin	Port Function
0x0	Address/Data port
0x1	Control/Status port Bits [7:4] - 0000 Bits [3:1] - Encoded Data Available bits (valid when Bit 0 is low) 00X - Row Header(1 byte – data will always be E0h) 010 - Pixel Data(8 bytes) 011 - Histogram Data (33 bytes) 100 - Authentication Data(9 bytes) 101 - Register Data(2 or 64 or 126 bytes; mode dependent. 2 is for Nav or single register mode) Bit 0 - Data available handshake bit for Polled operation, active low

Figure 4-3 Synchronous Serial Interface IO Port Assignment

4.8.2 Synchronous Serial Receive/Transmit Interface Timing

Figure 4-4 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 1 shows timing diagrams for the receive interface in SSI mode with SSI_NORM = 1.

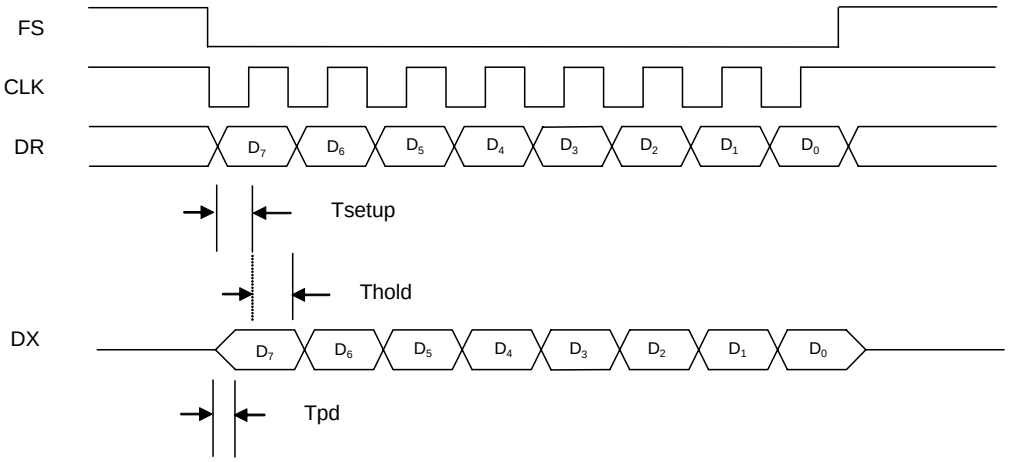


Figure 4-4 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 1

Parameter	Description	Min	Max	Unit
Tsetup	Setup time, data to CLK rising edge	10	-	ns
Thold	Hold time, frame sync or data from CLK rising edge	45	-	ns
Tpd	Propagation delay time, CLK rising edge to DX valid	-	55	ns
	CLK low time	65		ns
	CLK high time	65		ns

Table 1 SSI Receive/Transmit Timing Parameters, SSI_NORM = 1

Figure 4-5 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 0 shows timing diagrams for the receive interface in SSI mode with SSI_NORM = 0.

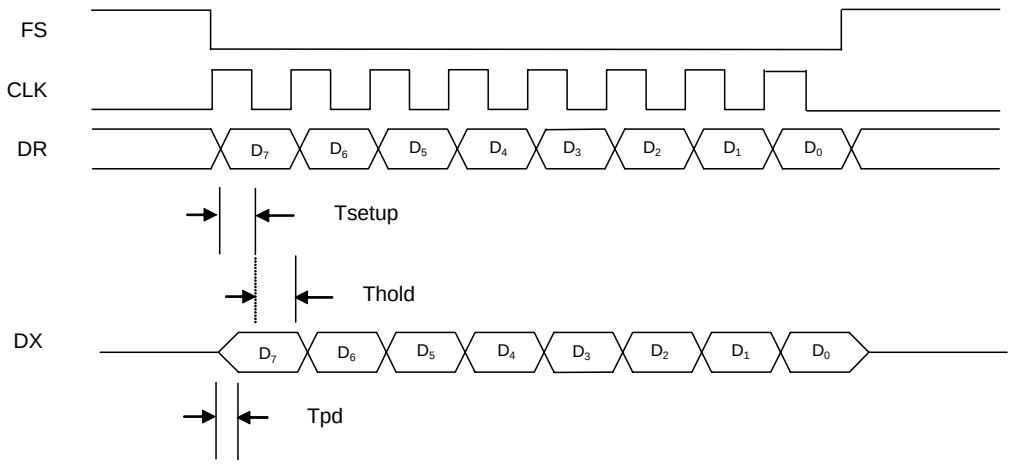


Figure 4-5 Receive/Transmit Interface, SPI-compatible mode, SSI_NORM = 0

Parameter	Description	Min	Max	Unit
Tsetup	Setup time, data to CLK rising edge	10	-	ns
Thold	Hold time, frame sync or data from CLK rising edge	45	-	ns
Tpd	Propagation delay time, CLK rising edge to DX valid	-	55	ns
	CLK low time	65		ns
	CLK high time	65		ns

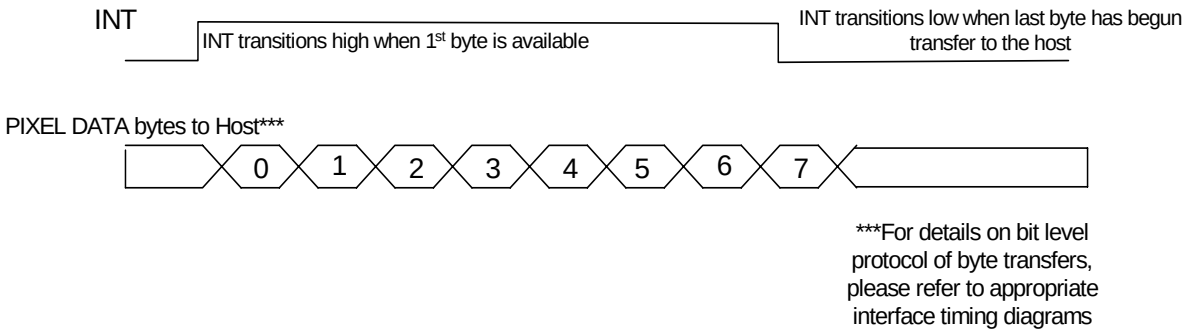
Figure 4-6 SSI Receive/Transmit Timing Parameters, SSI_NORM = 0

4.8.3 Synchronous Serial Interrupt behavior

When employing any of the synchronous serial interfaces, an interrupt signal [INT, active High] is available to support coordination of data transfers. The following example describes the behavior of the INT signal for imaging mode:

IMAGING MODE
For imaging mode, there are several different types of data packets that can be sourced from the sensor, please refer back to Figure 4-3 Synchronous Serial Interface IO Port Assignment.

An interrupt is generated for each one of these unique data packets and is held active until the beginning of the last data byte is read from the sensor by the host processor. This includes one byte transfers, as in the case of the Row Header packet. In the case of a Pixel Data packet, the following timing would apply:



It is important to note that the INT signal does not transition low until the last data byte of the packet has begun transfer on the selected interface. If there were more data from another source available, the INT would again transition high after being low for ~40nS to let the host know that more data is available from the sensor.

4.9 Example Hardware Checkout Communication Sequence

The following example illustrates the basic communication with AES3400 via the SSI interface. They are intended for illustration and may be helpful in supporting initial integration test and checkout before software test.. Utilizing the Register Read operation will enable a hardware designer to verify the SSI interface in the system.

4.9.1 Initialization

For synchronous serial interface operation mode, the following sequence is required for proper operation:

1. Power up the sensor.
2. Release reset or wait until reset is inactive.

4.9.2 Read Registers Sequence

The SSI Master sends the following sequence of bytes to the AES 3400:

0x80 (address: register Control Register 1)
0x01 (select: Master Reset)
0x81 (address: Control Register 2)
0x42 (select: Read Registers command AND enables interrupt)

This sequence requests the registers (62) of the sensor, or 124 bytes in response. The sequence of information received should be in the order of <register number byte, default value byte> repeated for all 124 bytes.

In order to successfully read all the register data from the AES3400 sensor, the SSI Master must write “fill” bytes. The flow diagram illustrates the flow of the SSI bus for the operation of reading of 124 registers from the AES 3400:

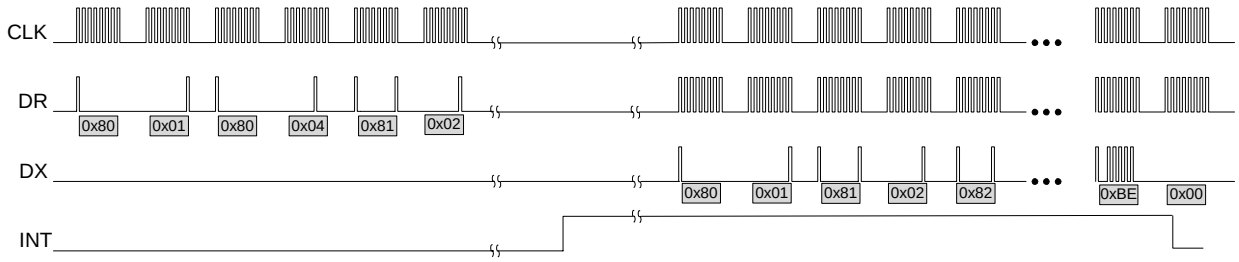


Figure 4-7 Read Register Sequence in SSI Mode

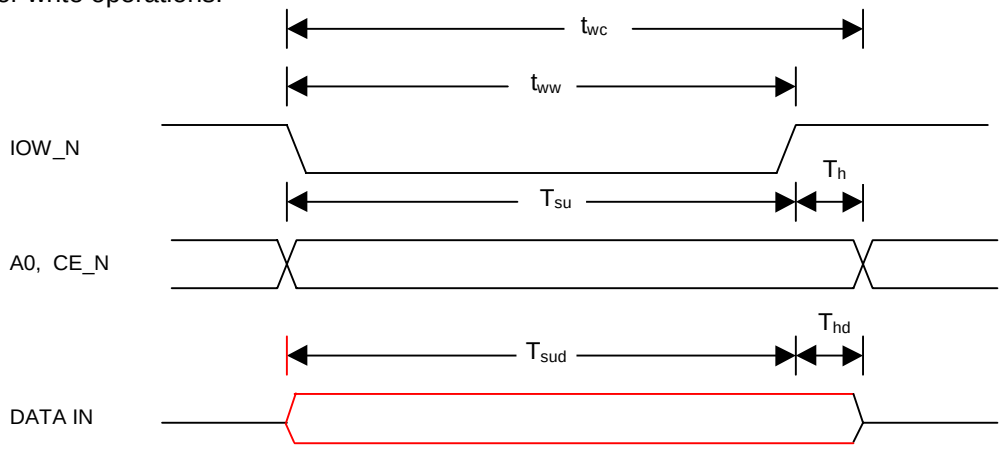
The bytes of information transmitted from the sensor should be, as follows. Dashed line entry indicates the value returned depends upon board configuration or sensor variations. This data is only valid after a power-on reset.

Reg	Default		Reg	Default
80h	00h		A0h	00h
81h	00h		A1h	00h
82h	04h		A2h	00h
83h	13h		A3h	00h
84h	04h		A4h	00h
85h	00h		A5h	00h
86h	63h		A6h	00h
87h	01h		A7h	00h
88h	01h		A8h	08h
89h	02h		A9h	01h
8Ah	05h		AAh	00h
8Bh	00h		ABh	00h
8Ch	38h		ACh	00h
8Dh	00h		ADh	20h
8Eh	02h		AEh	--h
8Fh	00h		AFh	--h
90h	00h		B0h	01h
91h	70h		B1h	00h
92h	0Ch		B2h	00h
93h	00h		B3h	00h
94h	0Fh		B4h	0Fh
95h	00h		B5h	00h
96h	7Fh		B6h	0Ch
97h	08h		B7h	26h
98h	20h		B8h	0Dh
99h	--h		B9h	6Ch
9Ah	N/A		BAh	00h
9Bh	N/A		BBh	00h
9Ch	--h		BCh	00h
9Dh	05h		BDh	00h
9Eh	00h		BEh	00h
9Fh	20h			

4.10 Parallel Interface

4.10.1 Write Timing

Data is written to the parallel interface at the rising edge of IOW_N if the chip select (CE_N) pin is active. The following figure shows the timing requirements for write operations.



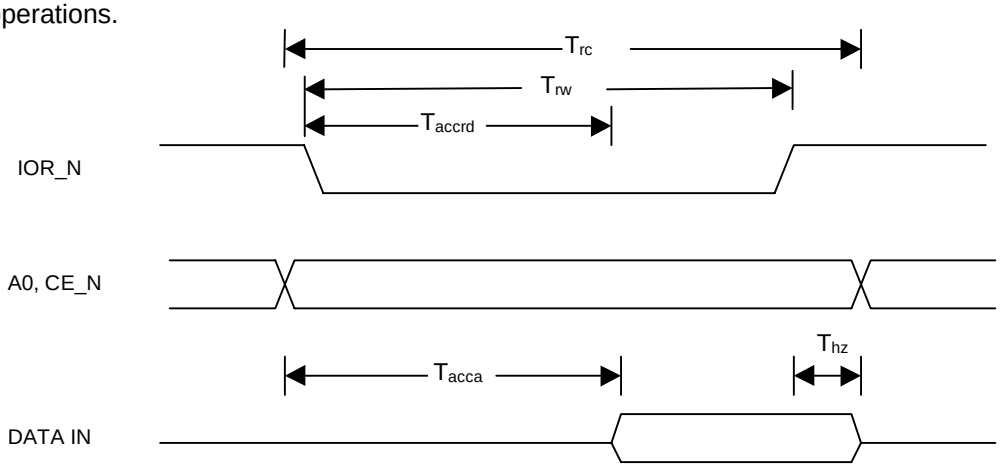
Parallel Interface Write Timing Diagram

PARAMETER	DESCRIPTION			
twc	WRITE CYCLE TIME	80	-	ns
tww	Write Pulse Width	50	-	ns
tsu	Setup time, address or chip select to IOW_N rising edge	25	-	ns
th	Hold time, address or chip select from IOW_N rising edge	5	-	ns
tsud	Setup time, data to IOW_N rising edge	25	-	ns
thd	Hold time, data from IOW_N rising edge	5	-	ns

Parallel Interface Write Timing Parameters

4.10.2 Read Timing

Data is read from the parallel interface when IOR_N is low and the chip select pin (CE_N) is active. The following figure shows the timing requirements for write operations.



Parallel Interface Read Timing Diagram

Parameter	Description	Min	Max	Unit
trc	Read Cycle time	80	-	ns
trw	Read Pulse width	50	-	ns
taccrd	Access time from read low	45	-	ns
tacca	Access time from address or chip select	55	-	ns
thz	Output high impedance from IOR_N or chip select	5	-	ns

Parallel Interface Read Timing Parameters

4.10.3 Finger Detect Auto-calibration

The selectable auto-calibration function will permit users to replace software finger detect calibration with a hardware based calibration. Once the auto-calibration bit is set in REG82, the sensor will search through the available capacitor settings (with the resistor setting remaining fixed) to find the optimum finger-detect sensitivity setting. Using worst-case finger detect frequency settings, this operation will take approximately 1 millisecond to complete (7 'binary search' detect cycles at 128 us per cycle).

At the completion of the auto-calibration cycle, the sensor will generate an appropriate interrupt based on the interface selected and will send out the address (0x82) and value of the capacitor setting value. A value of REG_A8h [if detect was not active the last cycle] or (REG_A8-1) [if detect was active the last cycle] will be added to the capacitor value to provide finger detection noise immunity. If adding the noise immunity offset would cause an overflow, the capacitor register value will be clamped at the upper limit of 7Fh. Auto-calibration will not function properly with the finger detect rate set to "continuous" or 16.7 millisecond detect rate settings.

5. SOFTWARE Interface details

5.1 Register Map

Register Map

Reg	D6	D5	D4	D3	D2	D1	D0	Reset
80h	Reserved	Reserved	Reserved	Reserved	Register Update	Scan Reset[1]	Master Reset[1]	00h
81h	SSI Int. Enable	SSI A0	Read Idn[1]	Clear One-Shot[1]	Set One-Shot[1]/ One Shot[2]	Read Registers[1]	Continuous Scan	00h
82h	Reserved	Reserved	Reserved	HGC Restart	HGC Enable	Auto Cal	Sleep Detect	04h
83h	Reserved	Finger Settling Delay [1]	Finger Settling Delay [0]	Reserved	Detect Rate [2]	Detect Rate [1]	Detect Rate [0]	13h
84h	Reserved	Reserved	Reserved	Reserved	Ref Resistor [2]	Ref Resistor [1]	Ref Resistor [0]	04h
85h	Cap	Cap	Cap	Cap	Cap	Cap	Cap	00h
86h	Reserved	Reserved	Reserved	Reserved	Reserved	Detect Drive [1]	Detect Drive [0]	63h
87h	Reserved	Reserved	Reserved	Reserved	Detect Freq [2]	Detect Freq [1]	Detect Freq [0]	01h
88h	Reserved	Reserved	Reserved	Column Scan Rate [3]	Column Scan Rate [2]	Column Scan Rate [1]	Column Scan Rate [0]	01h
89h	Reserved	Reserved	Reserved	Reserved	Reserved	Meas Drive [1]	Meas Drive [0]	02h
8Ah	Meas_Mult[2]	Meas_Mult[1]	Meas_Mult[0]	Reserved	Meas Freq [2]	Meas Freq [1]	Meas Freq [0]	05h
8Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
8Ch	Demod Phase [13]	Demod Phase [12]	Demod Phase [11]	Demod Phase [10]	Demod Phase [9]	Demod Phase [8]	Demod Phase [7]	38h
8Dh	Demod Phase [6]	Demod Phase [5]	Demod Phase [4]	Demod Phase [3]	Demod Phase [2]	Demod Phase [1]	Demod Phase [0]	00h
8Eh	Reserved	Gain 2 [1]	Gain 2 [0]	Reserved	Reserved	Gain1 [1]	Gain1 [0]	02h
8Fh	Bias2 Unlock	Bias 2 [1]	Bias 2 [0]	Reserved	Bias1 Unlock	Bias 1 [1]	Bias 1 [0]	00h
90h	Reserved	Carrier Null En	Carrier Null [4]	Carrier Null [3]	Carrier Null [2]	Carrier Null [1]	Carrier Null [0]	00h
91h	A/D Reference High [6]	A/D Reference High 5]	A/D Reference High [4]	A/D Reference High [3]	A/D Reference High [2]	A/D Reference High [1]	A/D Reference High [0]	70h
92h	A/D Reference Low [6]	A/D Reference Low [5]	A/D Reference Low [4]	A/D Reference Low [3]	A/D Reference Low [2]	A/D Reference Low [1]	A/D Reference Low [0]	0Ch
93h	Reserved	Reserved	Reserved	Start Row[3]	Start Row [2]	Start Row [1]	Start Row [0]	00h
94h	Reserved	Reserved	Reserved	End Row[3]	End Row [2]	End Row [1]	End Row [0]	0Fh
95h	Start Col [6]	Start Col [5]	Start Col [4]	Start Col [3]	Start Col [2]	Start Col [1]	Start Col [0]	00h
96h	End Col [6]	End Col [5]	End Col [4]	End Col [3]	End Col [2]	End Col [1]	End Col [0]	7Fh
97h	Eight Bit	Low Res	Binarize	Threshold [3]	Threshold [2]	Threshold [1]	Threshold [0]	08h
98h	Reserved	Test Register Enable	Registers First	Histo Full Array	Histo Each Row	Histo Data Enable	Image Data Disable	20h
99h	Reserved	Reserved	Reserved	GPIO3	GPIO2	GPIO1	GPIO0	00h
9Ah	Power Cycled[2]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	N/A
9Bh	Reserved	Reserved	Reserved / AD Idle	Challenge Word [31][1]	Challenge Word [30][1]	Challenge Word [29][1]	Challenge Word [28][1]/ Finger Present[2]	N/A
9Ch	Challenge Word [27][1] / FoundryID[6][2]	Challenge Word [26][1] / FoundryID[5][2]	Challenge Word [25][1] / FoundryID[4][2]	Challenge Word [24][1] / FoundryID[3][2]	Challenge Word [23][1] / FoundryID[2][2]	Challenge Word [22][1] / FoundryID[1][2]	Challenge Word [21][1] / FoundryID[0][2]	00h
9Dh	Challenge Word [20][1]/ CHIP_TYPE[6][2]	Challenge Word [19][1]/ CHIP_TYPE[5][2]	Challenge Word [18][1]/ CHIP_TYPE[4][2]	Challenge Word [17][1]/ CHIP_TYPE[3][2]	Challenge Word [16][1]/ CHIP_TYPE[2][2]	Challenge Word [15][1]/ CHIP_TYPE[1][2]	Challenge Word [14][1]/ CHIP_TYPE[0][2]	05h
9Eh	Challenge Word [13][1]	Challenge Word [12][1] / Reserved	Challenge Word [11][1] / Reserved	Challenge Word [10][1]	Challenge Word [9][1] /	Challenge Word [8][1] / IO_SEL[1][2]	Challenge Word [7][1] / IO_SEL[0][2]	00h
9Fh	Challenge Word [6][1] / Reserved	Challenge Word [5][1]/ Reserved	Challenge Word [4][1]/ Reserved	Challenge Word [3][1]/ Reserved	Challenge Word [2][1]/ Reserved	Challenge Word [1][1]/ Reserved	Challenge Word [0][1]/ Reserved	20h

Reg	D6	D5	D4	D3	D2	D1	D0	Reset
A0h	Reserved	Reserved	Excitation Bias Unlock	Reserved	Reserved	Excitation Bias [1]	Excitation Bias [0]	00h
A1h	Reserved	Reserved	Sense Amp Bias Unlock	Reserved	Reserved	Sense Amp Bias [1]	Sense Amp Bias [0]	00h
A2h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A3h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A4h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A5h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A6h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A7h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	08h
A8h	Reserved	Triggered Excit.	Enable Rdet	AutoCal Offset[3]	AutoCal Offset[2]	AutoCal Offset[1]	AutoCal Offset[0]	01h
A9h	LowPwr Enable	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
AAh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
ABh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
ACh	Reserved	Orig Embd Word	Set Test EMBW	Reserved	Reserved	Reserved	Single Reg En	20h
ADh	Single Reg ID [6]	Single Reg ID [5]	Single Reg ID [4]	Single Reg ID [3]	Single Reg ID [2]	Single Reg ID [1]	Single Reg ID [0]	00h
AEh	Reserved	Reserved	Watchdog Enable	Reserved	Watchdog time[2]	Watchdog time[1]	Watchdog time[0]	00h
AFh	Reserved	Reserved	OSC On Delay[4]	OSC On Delay[3]	OSC On Delay[2]	OSC On Delay[1]	OSC On Delay[0]	01h
B0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B1h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B2h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B3h	Reserved	Reserved	Reserved	GPO disable[3]	GPO disable[2]	GPO disable[1]	GPO disable[0]	0Fh
B4h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B5h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0Ch
B6h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	26h
B7h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0Dh
B8h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	6Ch
B9h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
BAh	Full Bit Int [6] [2]	Full Bit Int [5] [2]	Full Bit Int [4] [2]	Full Bit Int [3] [2]	Full Bit Int [2] [2]	Full Bit Int [1] [2]	Full Bit Int [0] [2]	00h
BBh	FDRV Delay [6] [2]	FDRV Delay [5] [2]	FDRV Delay [4] [2]	FDRV Delay [3] [2]	FDRV Delay [2] [2]	FDRV Delay [1] [2]	FDRV Delay [0] [2]	00h
BCh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
BDh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h

Table Registers Summary

[1]Write Only
[2]Read Only

6. Revision History

Version	Date	Person	Reason
Released	12/29/03	Lee	Release Date of Public Specification
Updated	5/12/04	Lee	Changed Pin 51 to Reserved for Serial & Parallel pinouts, added revision table, updated TOC, minor editing, etc.

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