晶采光電科技股份有限公司
AMPIRE CO., LTD.

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	HAREX
CUSTOMER PART NO.	
AMPIRE PART NO.	AF-12880BFI-00H
APPROVED BY	
DATE	

☑ Approved For Specifications
☐ Approved For Specifications & Sample

AMPIRE CO., LTD.
TOWER A, 4F, No.114, Sec. 1, HSIN-TAI 5th RD., HIS-CHIH,
TAIPEI HSIEN, TAIWAN(R.O.C.)
台北縣汐止鎮新台五路一段114號4樓(東方科學園區A棟)
TEL:886-2-26967269, FAX:886-2-26967196 or 886-2-26967270

APPROVED BY	CHECKED BY	ORGANIZED BY

RECORD OF REVISION

Revision Date	Contents
2001/11/29	New Release

1 FEATURES

(1) Display format : 128×80 dots, 1/80 duty, 1/10 bias.

(2) Construction : LCD panel and COF.

(3) Display type : FSTN, Transflective, Positive , 6 o'clock view

(4) Driver LSI : HD66741

(5) Interface for 68 series family MPU

(6) Internal oscillation circuit.

(7) Extend temperature type.

2 MECHANICAL DATA

Parameter	Stand Value	Unit
Dot size	0.20(W) × 0.23(H)	mm
Dot pitch	0.22(W) × 0.25(H)	mm
Active area	28.14(W) ×19.98(H)	mm
Viewing area	30.5(W) ×24.0 (H)	mm
Module size	34.5(W) ×57.2(H) × 1.7 Max. (T)	mm

3 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Logic Circuit Supply Voltage	VDD-VSS	-0.3	+7.0	V
LCD Driving Voltage	VLCD	-0.3	+17.0	V
Input Voltage	V_I	-0.3	VDD+0.3	V
Operating Temp.	T_{OP}	-20	70	°C
Storage Temp.	T_{STG}	-30	85	°C

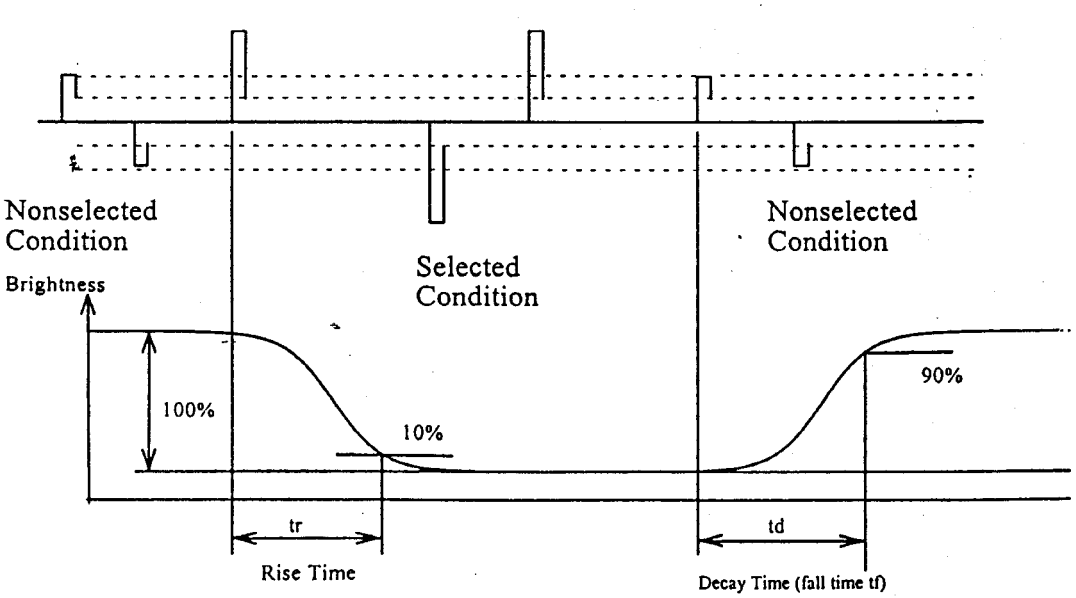
4 ELECTRO-OPTICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	Note
----- Electronic Characteristics -----							
Logic Circuit Supply Voltage	VDD-VSS	--	2.9	3.0	3.1	V	
LCD Driving Voltage (FSTN)	VLCD	-20 °C	--	--	--	V	* The LCD driving should be decided by real design.
		25 °C	--	10.5*	--		
		70 °C					
Input Voltage	VIH	--	0.7VDD	--	VDD	V	
	VIL	--	-0.3	--	0.15 VDD	V	
Logic Supply Current	IDD	VDD=3.0V	--	0.05	0.15	mA	
----- Optical Characteristics (FSTN) -----							
Contrast	CR	25°C	8.2	13.7	--		Note 1
Rise Time	Tr	25°C	--	200	--	ms	Note 2
Fall Time	Tf	25°C	--	200	--	ms	
Viewing Angle Range	θ f	25°C & CR≥2	--	51	--	Deg.	Note 3
	θ b		--	30	--		
	θ l		--	31	--		
	θ r		--	33	--		
Frame Frequency	FF	25°C	--	82.0	--	Hz	

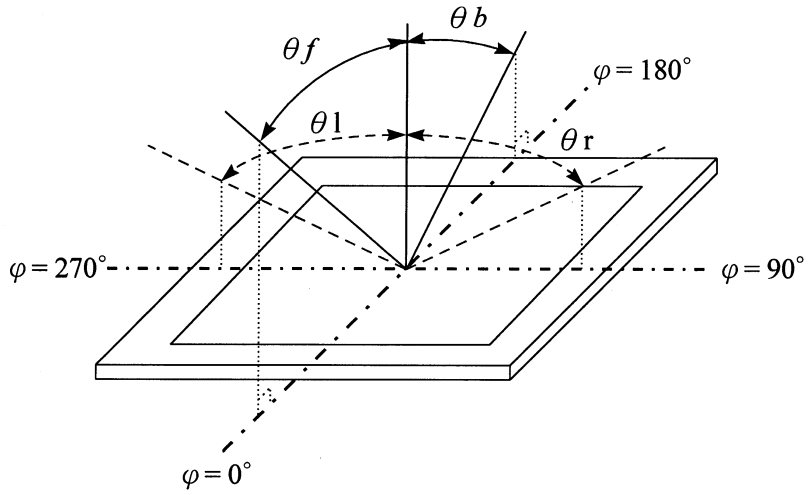
(NOTE 1) Contrast ratio :

CR = (Brightness in OFF state) / (Brightness in ON state)

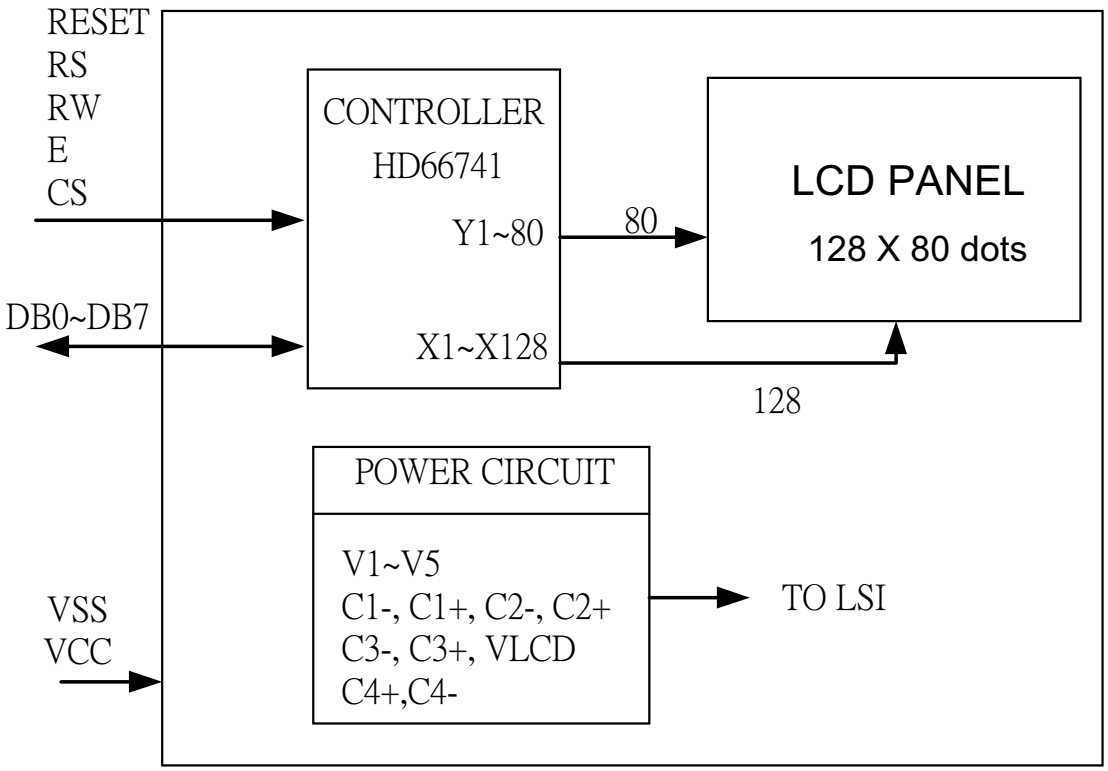
(NOTE 2) Response time :



(NOTE 3) Viewing angle



5 BLOCK DIAGRAM & POWER SUPPLY



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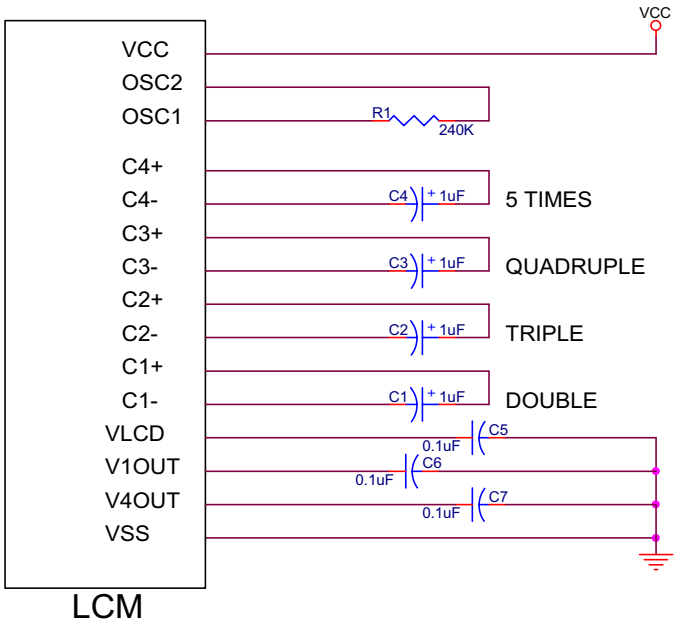


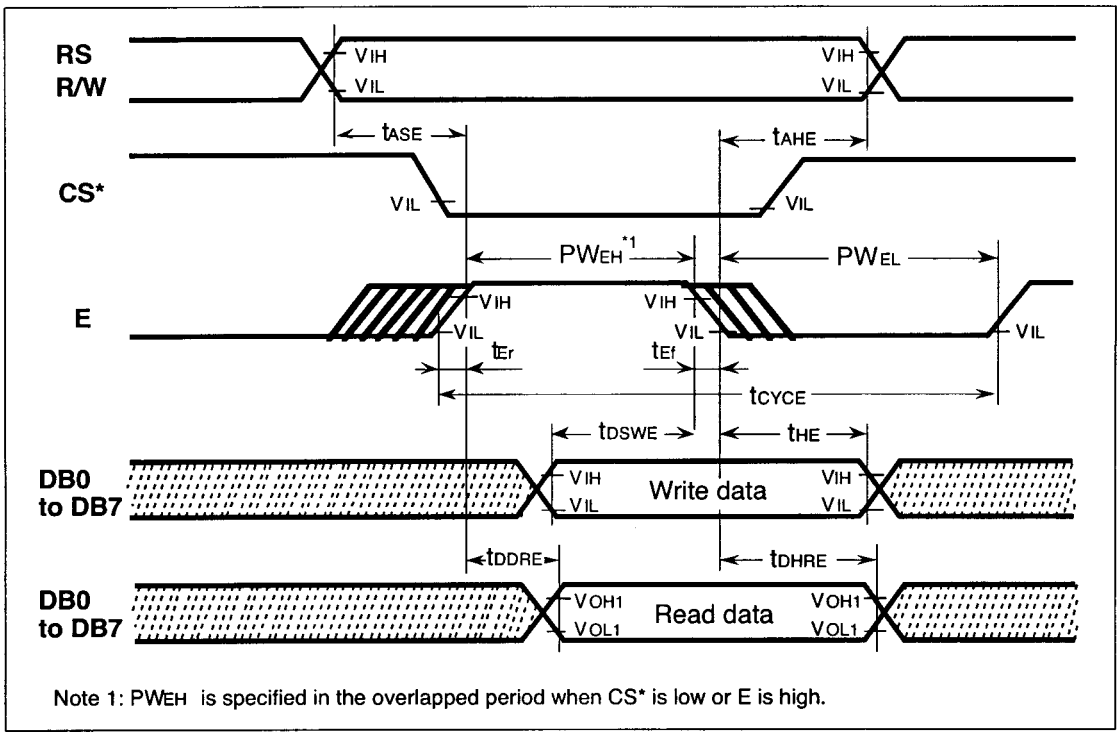
6 INTERFACE

No.	Symbol	Function
1	VSS	Ground (0V)
2	RW	68 system : Serves as a signal to select data read / write operation. (L: write, H: read)
3	E	68 system : serves as a enable signal to activate data read / write operation
4	RS	Register select input. (L: instruction, H: RAM access)
5	CS	Select HD66741 at low, or fix to GND
6	/RESET	Reset input pin at low
7	DB0	Parallel data bus for 68 system
8	DB1	
9	DB2	
10	DB3	
11	DB4	
12	DB5	
13	DB6	
14	DB7	
15	VDD	Power supply for logic (3.0V)

7 TIMING CHARACTERISTICS

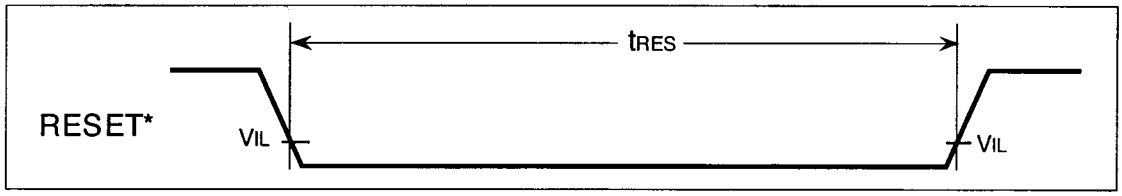
68-SYSTEM

Item	Symbol	VDD=1.8to2.7V		VDD=2.7to5.5V		Unit
		Min	Max	Min	Max	
Enable cycle time	t_{CYCE}	**Write** 600	--	380	--	ns
	t_{CYCE}	**Read** 800		500		
Enable High-level plus width	PW_{EH}	**Write**120	--	70	--	
	PW_{EH}	**Read** 350		250		
Enable Lo-level pulse width	PW_{EL}	**Write**300	--	150	--	
	PW_{EL}	**Read** 300		150		
Enable rise/fall time	t_{Er}, t_{Ef}	--	25	--	25	
Setup time (RS,R/W to E,CS*)	t_{ASE}	50	--	50	--	
Address hold time	t_{AHE}	20	--	20	--	
Write Data set-up time	t_{DSWE}	60	--	60	--	
Write Data hold time	t_{HE}	20	--	20	--	
Read Data delay time	t_{DDRE}	--	300	--	200	
Read Data hold time	t_{DHRE}	5	--	5	--	



68 System BUS

RESET OPERATION:



8 INSTRUCTION DESCRIPTION

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Start oscillation	0	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW) or upper contrast adjustment bits (CT4-3).	0
									BT1	BT0	Sets the register selection (SW) or boost level (BT1/0).	0
Contrast control 2	0	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0).	0
								BS2	BS1	BS0	Sets the LCD bias value (BS2-0).	0
Entry mode set	0	0	0	0	1	0	0	REV	I/D	1	Sets the black-and-white reversal (REV) or address update direction after RAM access (I/D).	0
								CT5	RDM	0	Sets the higher contrast adjustment bit (CT5) or read, modify, write (RDM).	0
Display on/off control	0	0	0	0	1	1	0	D	DL10	0	Sets display on (D) or double-height display line (DL10).	0
								DL9	DL8	DL7	Specifies double-height display lines (DL9–DL7).	0
Display line control	0	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (NL2-0).	0
								CN1	CN0	NL3	Specifies centering (CN1–0) or the number of display lines (NL3).	0
Double-height display control	0	0	0	1	0	0	0	DL3	DL2	DL1	Specifies double-height display lines (DL3-1).	0
								DL6	DL5	DL4	Specifies double-height display lines (DL6–4).	0

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle
Vertical scroll control 1	0	0	0	1	0	0	1	SN2	SN1	SN0	Sets the display-start line (SN2-0).	0
								<0>	<0>	SN3	Sets the display-start line (SN3).	0
Vertical scroll control 2	0	0	0	1	0	1	0	SL2	SL1	SL0	Sets the display-start raster-row (SL2-0).	0
								<0>	PS1	PS0	Sets the partial scroll (PS1–0).	0
Port control	0	0	0	1	1	1	0	PT2	PT1	PT0	Sets the general port output (PT2-0).	0
								<0>	DCC	BC	Selects the boosting cycle (DCC) or LCD drive AC waveform (B/C).	0
LCD-driving-waveform control	0	0	0	1	1	1	1	NW2	NW1	NW0	Sets the number of n-raster-rows (NW2–0) in C-pattern AC drive.	0
								EOR	NW4	NW3	Sets the EOR output (EOR) or the number of n-raster-rows (NW4–3) in C-pattern AC drive.	0
RAM address set (upper bits)	0	0	1	0	1			AD10–6 (upper bits)			Initially sets the upper addresses of the CGRAM to the address counter (AC).	0
RAM address set (lower bits)	0	0	1	1				AD5-0 (lower bits)			Initially sets the lower addresses of the CGRAM to the AC.	0
Write data to RAM	0	1				Write data					Writes data to CGRAM.	0
Read data from RAM	1	1				Read data					Reads data from CGRAM.	0

Note: The upper column of each register can be set when SW = 0. The lower column can be set when SW = 1.

Bit definition:

CMS = 0: COM1/80 => COM1

SGS = 0: SEG1/128 => SEG1

AMP = 1: Operational amplifier and booster circuit on

SLP = 1: Sleep mode

STB = 1: Standby mode

SW = 0: Upper register setting

SW = 1: Lower register setting

CT5-0: Contrast adjustment

BT1/0: Boost level selection (00: Triple, 01: Quadruple, 10: Five-times)

BS2-0: LCD drive bias selection

REV = 0: Normal display

REV = 1: Black-and-white reversed display of the graphics display

ID = 1: Address increment

ID = 0: Address decrement

RDM = 1: Read, modify, and write mode (Not automatically update the address counter after reading)

D = 1: Display on

NL3-0: Display line setting (0000: 1/8 duty ratio, 0001: 1/16 duty ratio, 0010: 1/24 duty ratio, 0011: 1/32 duty ratio, 0100: 1/40 duty ratio, 0101: 1/48 duty ratio, 0110: 1/56 duty ratio, 0111: 1/64 duty ratio, 1000: 1/72 duty ratio, 1001: 1/80 duty ratio)

DL1-10: Double-height line specifications (DL1: 1st line, DL2: 2nd line, DL3: 3rd line, DL4: 4th line, DL5: 5th line, DL6: 6th line, DL7: 7th line, DL8: 8th line, DL9: 9th line, DL10: 10th line)

SN3-0: Display-start line (0000: 1st line, 0001: 2nd line, 0010: 3rd line, 0011: 4th line, 0100: 5th line, 0101: 6th line, 0110: 7th line, 0111: 8th line, 1000: 9th line, 1001: 10th line)

SL2-0: Display-start raster-row specifications (000: 1st raster-row...111: 8th raster-row)

CN1–0 Centering specifications (00: no centering, 01: 16-dot shift below, 10: 8-dot shift above)

PT2-0: Port output control (PT2 = 1: PORT2 = Vcc, PT1 = 1: PORT1 = Vcc, PT0 = 1: PORT0 = Vcc)

B/C = 0: B-pattern waveform drive

B/C = 1: C-pattern waveform drive

EOR = 1: EOR alternating drive at C-pattern waveform

NW4–0: Reversed number of n raster-rows at C-pattern waveform drive (alternating with the set value + one raster-row)

DCC = 0: Boosted at 1/64-divided clock

DCC = 1: Boosted at 1/32-divided clock

ADD10-0: CGRAM address set (000H-4FFH)

9 QUALITY AND RELIABILITY

9.1 TEST CONDITIONS

Tests should be conducted under the following conditions :

Ambient temperature : 25 ± 3°C

Humidity : 65 ± 20% RH.

9.2 SAMPLING PLAN

Sampling method shall be in accordance with MIL-STD-105E , level II, normal single sampling plan .

9.3 ACCEPTABLE QUALITY LEVEL

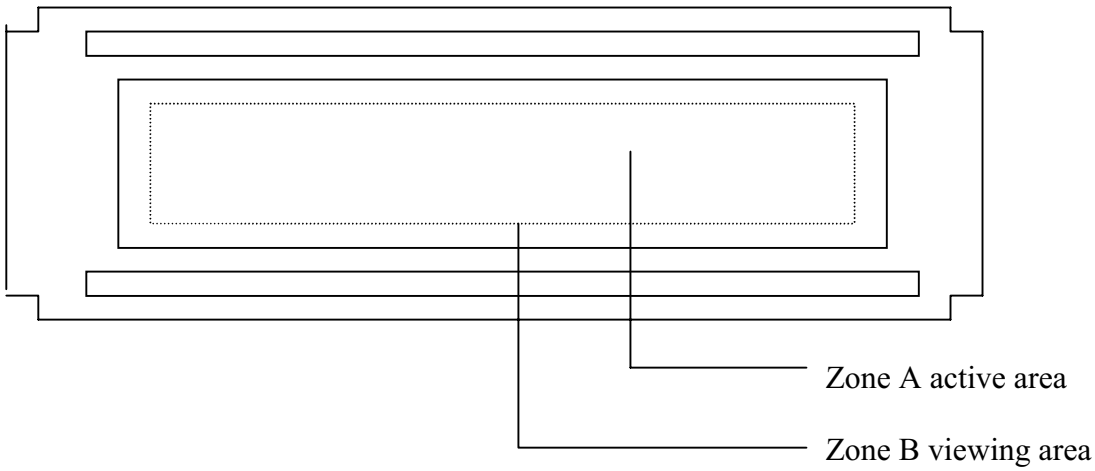
A major defect is defined as one that could cause failure to or materially reduce the usability of the unit for its intended purpose. A minor defect is one that does not materially reduce the usability of the unit for its intended purpose or is an infringement from established standards and has no significant bearing on its effective use or operation.

9.4 APPEARANCE

An appearance test should be conducted by human sight at approximately 30 cm distance from the LCD module under flourescent light. The inspection area of LCD panel shall be within the range of following limits.

9.5 INSPECTION QUALITY CRITERIA

Item	Description of defects			Class of Defects	Acceptable level (%)
Function	Short circuit or Pattern cut			Major	0.65
Dimension	Deviation from drawings			Major	1.5
Black spots	Ave . dia . D	area A	area B	Minor	2.5
	D≤0.2	Disregard			
	0.2<D≤0.3	3	4		
	0.3<D≤0.4	2	3		
	0.4<D	0	1		
Black lines	Width W, Length L	A	B	Minor	2.5
	W≤0.03	disregard			
	0.03<W≤0.05	3	4		
	0.05<W≤0.07 , L≤3.0	1	1		
	See line criteria				
Bubbles in polarizer	Average diameter D 0.2 < D < 0.5 mm for N = 4 , D > 0.5 for N = 1			Minor	2.5
Color uniformity	Rainbow color or newton ring.			Minor	2.5
Glass Scratches	Obvious visible damage.			Minor	2.5
Contrast ratio	See note 1			Minor	2.5
Response time	See note 2			Minor	2.5
Viewing angle	See note 3			Minor	2.5



9.6 RELIABILITY

Test Item	Test Conditions	Note
	Extend Temp. type	
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	85±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Thermal Shock Test	-30°C ~ 25°C ~ 85°C 60 m in. 5 min. 60 min. (1 cycle) Total 24 cycle	1,2
Humidity Test	70 °C, Humidity 90%, 240 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

10 HANDLING PRECAUTIONS

(1) A LCD module is a fragile item and should not be subjected to strong mechanical shocks.

(2) Avoid applying pressure to the module surface. This will distort the glass and cause a change in color.

(3) Under no circumstances should the position of the bezel tabs or their shape be modified.

(4) Do not modify the display PCB in either shape or positioning of components.

(5) Do not modify or move location of the zebra or heat seal connectors.

(6) The device should only be soldered to during interfacing. Modification to other areas of the board should not be carried out.

(7) In the event of LCD breakage and resultant leakage of fluid do not inhale, ingest or make contact with the skin. If contact is made rinse immediately.

(8) When cleaning the module use a soft damp cloth with a mild solvent, such as Isopropyl or Ethyl alcohol. The use of water, ketone or aromatic is not permitted.

(9) Prior to initial power up input signals should not be applied.

(10) Protect the module against static electricity and observe appropriate anti-static precautions.

11 OUTLINE DIMENSION