AF2302N

20V N-Channel Enhancement Mode MOSFET

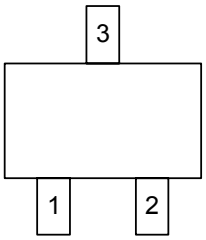
■ Features

- Advanced trench process technology
- High density cell design for ultra low on-resistance
- Excellent thermal and electrical capabilities
- Compact and low profile SOT-23 package

■ Product Summary

V_{DS} = 20V
$R_{DS\ (on)}$, V_{GS}@4.5V, I_{DS}@3.6A =65mΩ.
$R_{DS\ (on)}$, V_{GS}@2.5V, I_{DS}@3.1A =95mΩ.

■ Pin Assignments



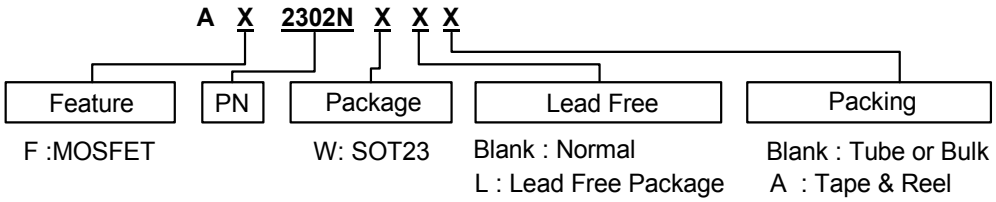
(Top View)

1. G
2. S
3. D

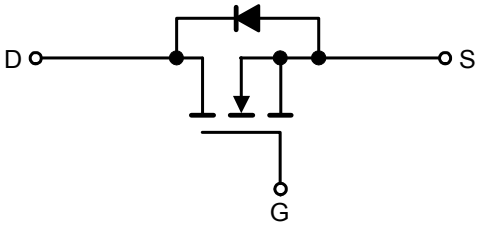
■ Pin Descriptions

Pin No.	Pin Name	Description
1	G	Gate
2	S	Source
3	D	Drain

■ Ordering information



■ Block Diagram



■ Absolute Maximum Ratings (T_A=25ºC unless otherwise noted)

Symbol	Parameter		Rating	Units
V_{DS}	Drain-Source Voltage		20	V
V_{GS}	Gate-Source Voltage		±8	V
I_D	Continuous Drain Current		2.4	A
I_{DM}	Pulsed Drain Current		10	A
P_D	Maximum Power Dissipation	T_A=25ºC	1.25	W
		T_A=70ºC	0.8	
T_J	Operating Junction Temperature		+150	ºC
T_J, T_{STG}	Operating Junction and Storage Temperature Range		-55 to +150	ºC

■ Thermal Performance

Symbol	Parameter	Limit	Units
T_L	Lead Temperature (1/8" from case)	5	S
$R_{\theta JA}$	Junction to Ambient Thermal Resistance (PCB mounted)	100	ºC/W

Note: Surface mounted on FR4 board t ≤ 5 sec.

■ Electrical Characteristics Rate I_D=2.4A, (T_A=25ºC unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
Static						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=250uA	20	-	-	V
$R_{DS(ON)}$	Drain-Source On-State Resistance	V_{GS}=4.5V, I_D=3.6A	-	50	65	mΩ
		V_{GS}=2.5V, I_D=3.1A	-	75	95	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D=250uA	0.45	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=20V, V_{GS}=0V	-	-	1.0	uA
I_{GSS}	Gate Body Leakage	V_{GS}=±8V, V_{DS}=0V	-	-	±100	nA
$I_{D(ON)}$	On-State Drain Current	V_{DS}=5V, V_{GS}=4.5V	6	-	-	A
g_{fs}	Forward Tranconductance	V_{DS}=5V, I_D=3.6A	-	10	-	S
Dynamic						
Q_g	Total Gate Charge	V_{DS}=10V, I_D=3.6A, V_{GS}=4.5V	-	5.2	10	nC
Q_{gs}	Gate-Source Charge		-	0.65	-	
Q_{gd}	Gate-Drain Charge		-	1.5	-	
$t_{d(on)}$	Turn-On Delay Time	V_{DD}=10V, R_L=10Ω, I_D=1A, V_{GEN}=4.5V, R_G=6Ω	-	7	15	nS
t_r	Turn-On Rise Time		-	55	80	
$t_{d(off)}$	Turn-Off Delay Time		-	16	60	
t_f	Turn-Off Fall-Time		-	10	25	
C_{iss}	Input Capacitance	V_{DS}=10V, V_{GS}=0V, f=1.0MHz	-	450	-	pF
C_{oss}	Output Capacitance		-	70	-	
C_{rss}	Reverse Transfer Capacitance		-	43	-	
Source-Drain Diode						
I_S	Max. Diode Forward Current		-	-	1.6	A
V_{SD}	Diode Forward Voltage	I_S=1.0A, V_{GS}=0V	-	0.75	1.2	V

Note: Pulse test: pulse width ≤ 300uS, duty cycle ≤ 2%

■ Marking Information

(Top View)

SOT23

XX YW

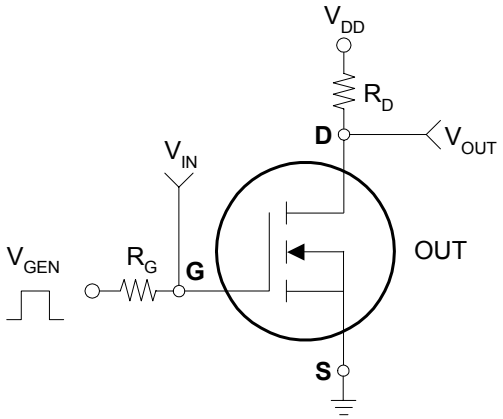
→ XX: Device Code
(See Appendix)

→ Date code
Y : Year
W : Week(A~Z)

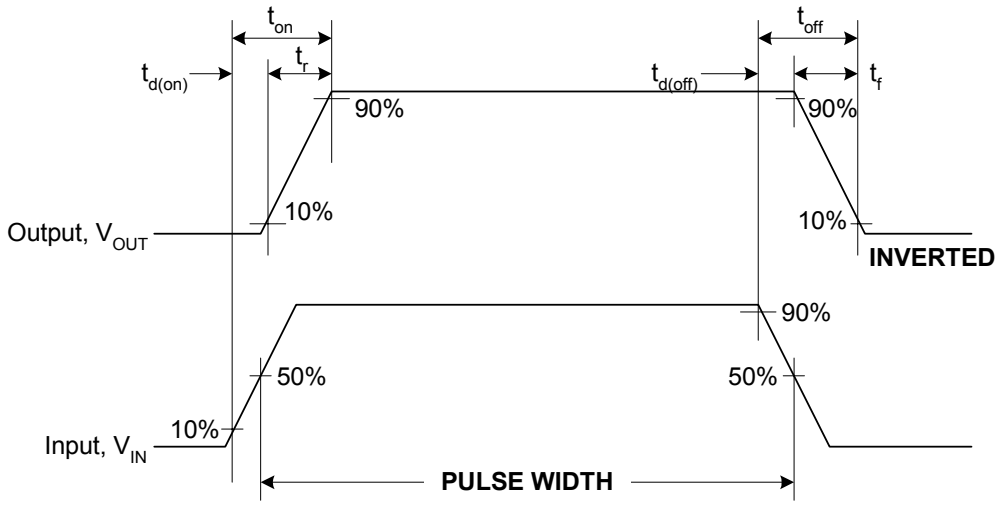
Appendix

Part Number	Package	Device Code
AF2302N	SOT23-3	02

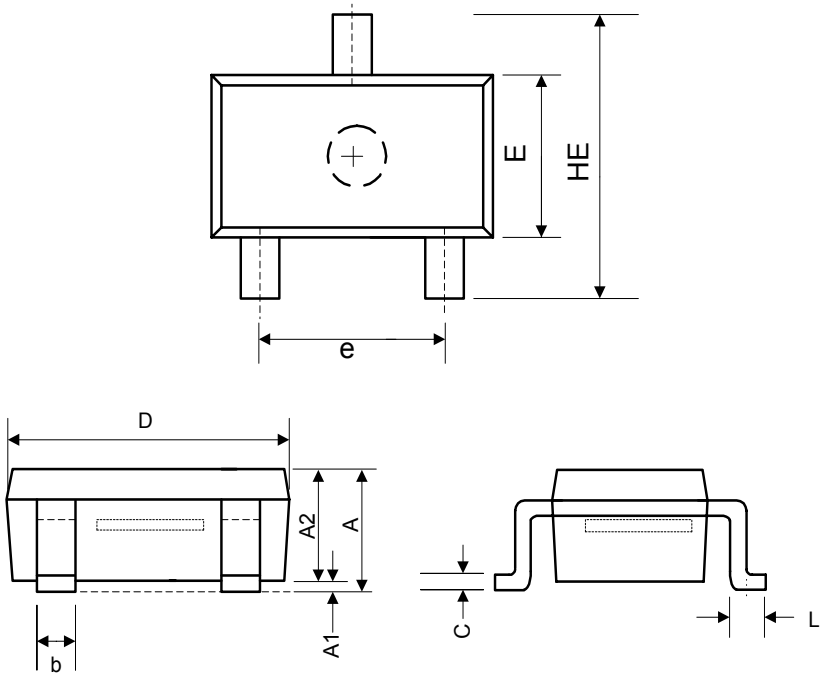
■ Switching Test Circuit



■ Switching Waveforms



■ Package Information



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.00	1.20	1.40	0.039	0.047	0.055
A1	0.00	-	0.10	0.000	-	0.004
A2	1.00	1.15	1.30	0.039	0.045	0.051
b	0.35	-	0.50	0.014	-	0.020
C	0.10	0.175	0.25	0.004	0.007	0.010
D	2.70	2.90	3.10	0.106	0.114	0.122
E	1.40	1.60	1.80	0.055	0.063	0.071
e	1.70	2.00	2.30	0.067	0.079	0.091
HE	2.40	2.70	3.00	0.094	0.106	0.118
L	0.30	-	0.55	0.012	-	0.022