1.5A Synchronous Step-Down Converter

DESCRIPTION

The AF5030S is a monolithic synchronous buck regulator. The device can provides 1.5A of continuous load current over a wide input voltage of 4.75V to 23V. Current mode control provides fast transient response and cycle-by-cycle current limit.
An adjustable soft-start prevents inrush current at turn-on, and in shutdown mode the supply current drops to 0.3μA.

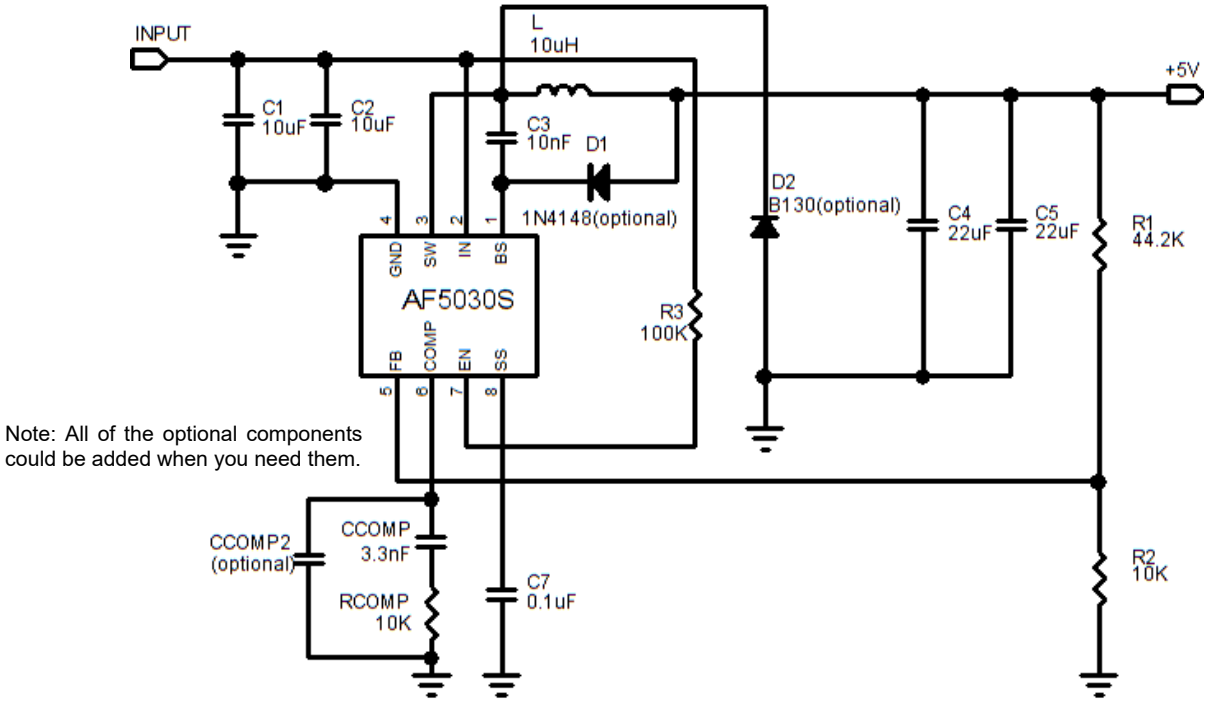
FEATURES

- 1.5A Output Current
- Wide 4.75V to 23V Operating Voltage
- Integrated 130mΩ Power MOSFET Switches
- Output Adjustable from 0.925V to 0.8*VIN
- Up to 95% Efficiency
- Programmable Soft-Start
- SOP-8 Package

APPLICATIONS

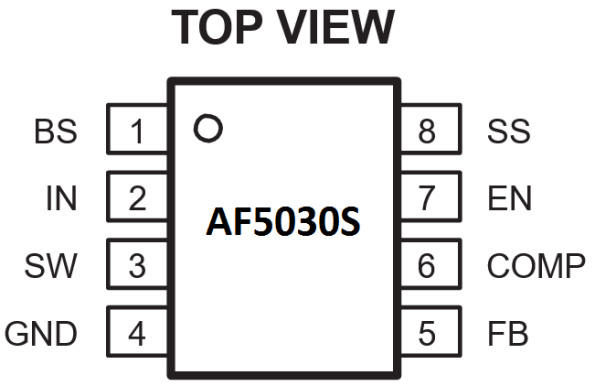
- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

TYPICAL APPLICATION



Note: All of the optional components could be added when you need them.

PACKAGE REFERENCE



PIN FUNCTIONS

PIN NO.	Name	Description
1	BS	High-Side Gate Drive Boost Input. BS supplies the drive for the high-side N-Channel MOSFET switch. Connect a 0.01μF or greater capacitor from SW to BS to power the high side switch.
2	IN	Power Input. Drive IN with a 4.75V to 23V power source. Bypass IN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3	SW	Power Switching Output. SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
4	GND	Ground.
5	FB	Feedback Input. FB senses the output voltage to regulate that voltage. Drive FB with a resistive voltage divider from the output voltage. The feedback threshold is 0.925V.
6	COMP	Compensation Node. COMP is used to compensate the regulation control loop. Connect a series RC network from COMP to GND to compensate the regulation control loop. In some cases, an additional capacitor from COMP to GND is required.
7	EN	Enable Input. EN is a digital input that turns the regulator on or off. Drive EN high to turn on the regulator, drive it low to turn it off. Pull up with 100kΩ resistor for automatic startup.
8	SS	Soft-Start Control Input. SS controls the soft start period. Connect a capacitor from SS to GND to set the soft-start period. A 0.1μF capacitor sets the soft-start period to 15ms. To disable the soft-start feature, SS unconnected the Capacitor.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage VIN .....-0.3V to +26V
Switch Node Voltage VSW 27V
Boost Voltage VBS .....VSW–0.3V to VSW + 6V
All Other Pins.....-0.3V to +6V
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C/10s
Storage Temperature ..... –65°C to + 150°C

RECOMMENDED OPERATING CONDITIONS

Input Voltage (VIN) ..... 4.75V to 23V
Output Voltage (VSW) ..... 0.925 to 20V
Operating Temperature.....–40°C to +85°C

ELECTRICAL CHARACTERISTICS

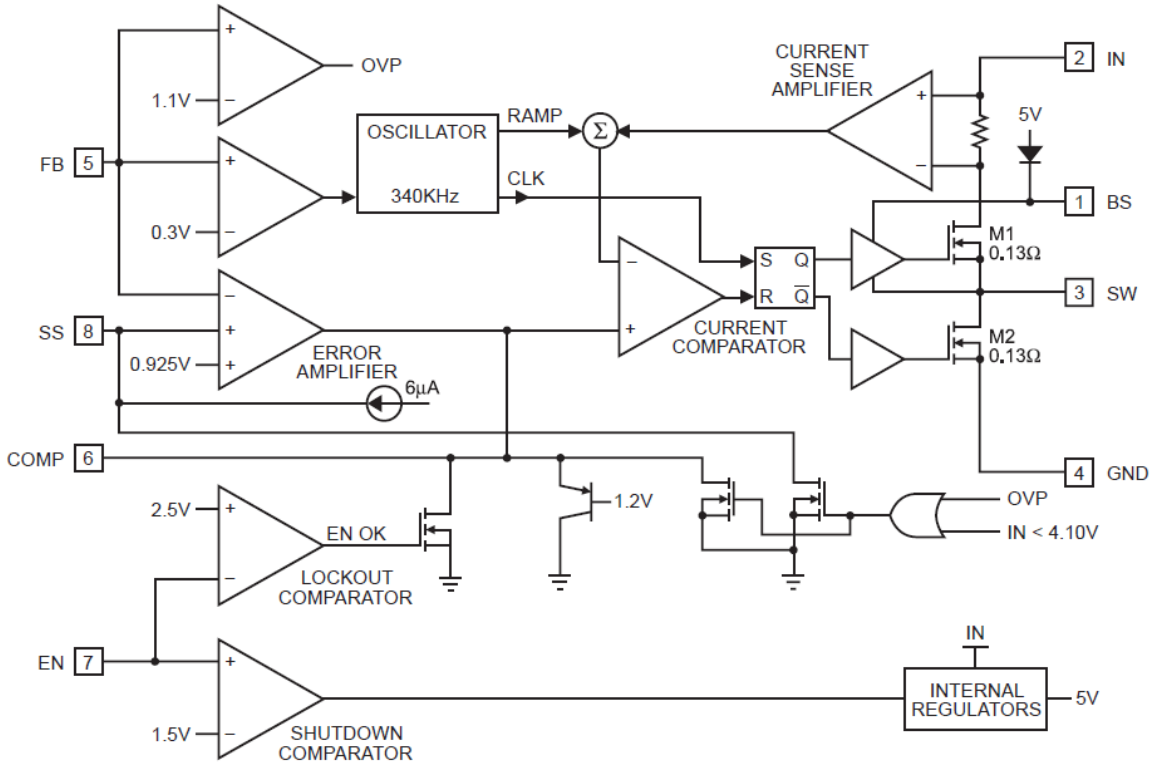
(V_{IN} = 12V, T_A = +25°C, unless otherwise noted.)

Parameter	Symbol	Condition	MIN	TYP	MAX	Units
Shutdown Supply Current	ISD	VEN ≤ 0.3V		0.3	3.0	uA
Supply Current	IQ	VEN ≥ 2.6V, VFB = 1.0V		1.3	1.5	mA
Feedback Voltage	VFB	4.75V ≤ VIN ≤ 23V	0.900	0.925	0.950	V
Feedback Overvoltage Threshold	VFB_OVP			1.1		V
Error Amplifier Voltage	AEA			400		V/V
Error Amplifier Transconductance	GEA	ΔIC = ±10μA		820		uA/V
High-Side Switch On Resistance	RDS(ON)-1			130		mΩ
Low-Side Switch On Resistance	RDS(ON)-2			130		mΩ
High-Side Switch Leakage Current		VEN = 0V, VSW = 0V			10	uA
Upper Switch Current Limit		Minimum Duty Cycle	2.4	3.4	--	A
Lower Switch Current Limit		From Drain to Source		1.1		A
COMP to Current Sense Transconductance	GCOMP			3.5		A/V
Oscillation Frequency	Fsw		350	400	450	Khz
Short Circuit Oscillation Frequency	Fosc2	VFB = 0V		140		Khz
Maximum Duty Cycle	DMAX	VFB = 1.0V		90		%
EN Shutdown Threshold Voltage		VEN Rising	1.1	1.5	2.0	V
EN Shutdown Threshold Voltage Hysteresis				210		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Hysterisis				210		mV
Input Under Voltage Lockout Threshold		VIN Rising	3.80	4.20	4.40	V
Input Under Voltage Lockout Threshold Hysteresis				210		mV

Soft-Start Current		VSS = 0V		6		uA
Soft-Start Period		CSS = 0.1μF		15		mS
Thermal Shutdown(1)				160		°C

Note1: Guaranteed by design, not tested.

FUNCTIONAL BLOCK DIAGRAM

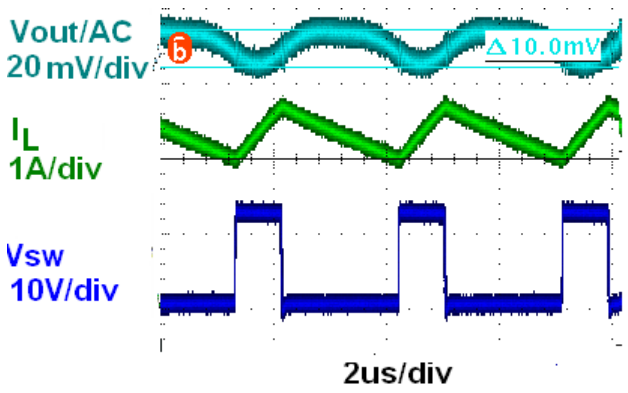


TYPICAL PERFORMANCE CHARACTERISTICS

(Vin=12V, Io=0 mA, Temperature = 25 degree C, unless otherwise specified)

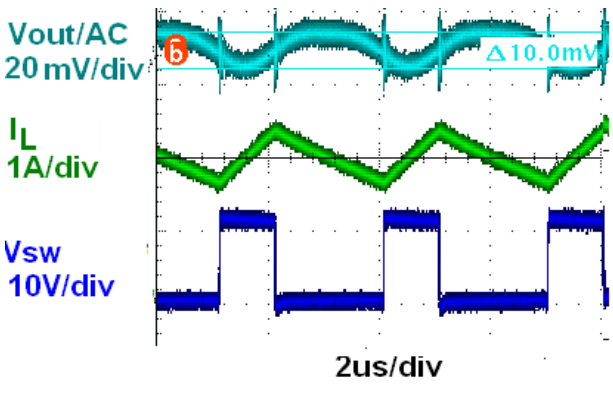
Light Load Operation (No load)

Vin=12V, Iin=8.2 mA, Vout=3.3V



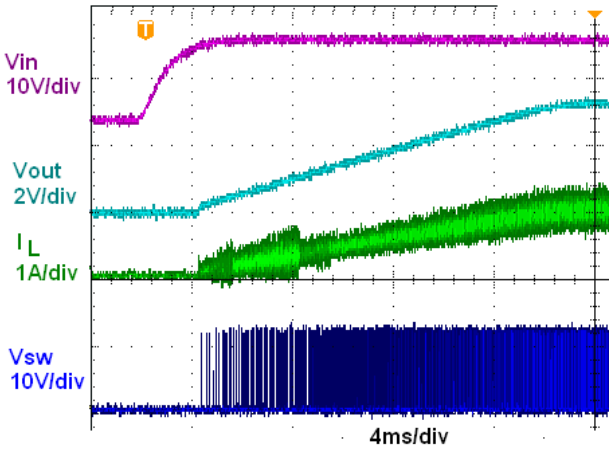
Heavy Load Operation (1.5A Load)

Vin=12V, Vout=3.3V

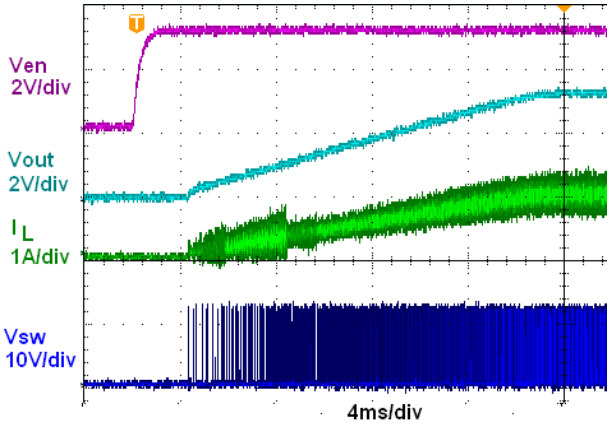


Startup Vin=12V, Vout=3.3V, Iout=1A

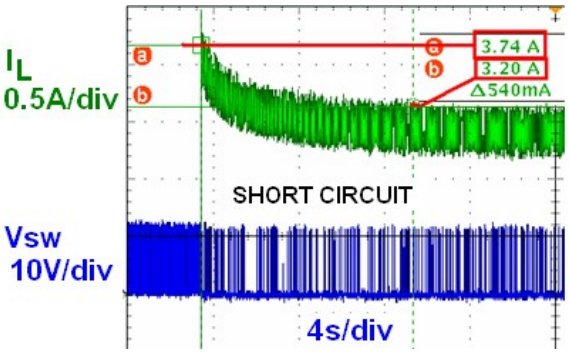
through Vin.

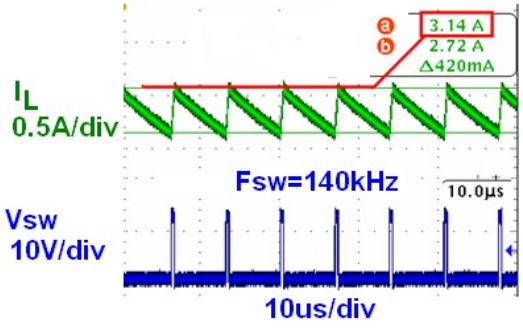


through Enable.



Short Circuit Protection Vin=12V





OPERATION FUNCTIONAL DESCRIPTION

The AF5030S is a synchronous rectified, current-mode, step-down regulator. It regulates input voltages from 4.75V to 23V down to an output voltage as low as 0.925V, and supplies up to 1.5A of load current.

The AF5030S uses current-mode control to regulate the output voltage. The output voltage is measured at FB through a resistive voltage divider and amplified through the internal trans-conductance error amplifier. The voltage at the COMP pin is compared to the switch current measured internally to control the output voltage.

The converter uses internal N-Channel MOSFET switches to step-down the input voltage to the regulated output voltage. Since the high side MOSFET requires a gate voltage greater than the input voltage, a boost capacitor connected between SW and BS is needed to drive the high side gate. The boost capacitor is charged from the internal 5V rail when SW is low.

When the AF5030S FB pin exceeds 20% of the nominal regulation voltage of 0.925V, the over voltage comparator is tripped and the COMP pin and the SS pin are discharged to GND, forcing the high-side switch off.

APPLICATIONS INFORMATION

COMPONENT SELECTION

SETTING THE OUTPUT VOLTAGE

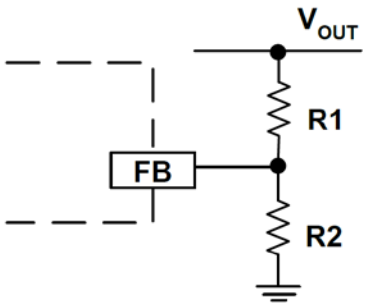


Figure1. Output Voltage Setting

The output voltage is set using a resistive voltage divider from the output voltage to FB pin.The voltage divider divides the output voltage down to the feedback voltage by the ratio:

$$V_{FB} = \frac{R_2}{R_1 + R_2} \cdot V_{OUT}$$

Where VFB is the feedback voltage and VOUT is the output voltage. Thus the output voltage is:

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \cdot 0.925$$

INDUCTOR

The inductor is required to supply constant current to the output load while being driven by the switched input voltage. A larger value inductor will result in less ripple current that will result in lower output ripple voltage. However, the larger value inductor will have a larger physical size, higher series resistance, and/or lower saturation current. A good rule for determining the inductance to use is to allow the peak-to-peak ripple current in the inductor to be approximately 30% of the maximum switch current limit. Also, make sure that the peak inductor current is below the maximum switch current limit. The inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_L} \cdot (1 - D)$$

$$\text{Where } D = \frac{V_{OUT}}{V_{IN}},$$

VOUT is the output voltage, VIN is the input voltage, FSW is the switching frequency, and ΔIL is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The

peak inductor current can be calculate

$$I_{LP} = I_{LOAD} + \frac{V_{OUT}}{2 \cdot F_{SW} \cdot L} \cdot (1 - D)$$

Where ILOAD is the load current.
The choice of which style inductor to use mainly depends on the price vs. Size Requirements and any EMI requirements.

OPTIONAL SCHOTTKY DIODE

During the transition between high-side switch and low-side switch, the body diode of the low side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.Table 1 lists Schottky diode and their manufacturers.

TABLE 1--Diode Selection Guide

VIN	Part Number	Voltage/Current Rating
<20V	B130	30V,1A
<20V	SK13	30V,1A

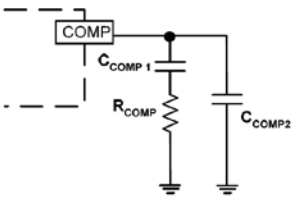
INPUT CAPACITOR

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter.A low ESR electrolytic capacitor is highly recommended.Since large current flows in and out of this capacitor during switching,its ESR also affects efficiency.
When EC cap is used, the input capacitance needs to be equal to or higher than 68uF.The RMS ripple current rating needs to be higher than 50% of the output current.The input capacitor should be placed close to the VIN and GND pins of the AF5030S,with the shortest traces possible.The input capacitor can be placed a little bit away if a small parallel 0.1uF ceramic capacitor is placed right next to the AF5030S.
When VIN above 15V,pure ceramic CIN is not recommended,This is because the ESR of a ceramic cap is often too small,pure ceramic CIN will work with the parasite inductance of the input trace and forms a Vin resonant tank.When Vin is hot plug in/out.this resonant tank will boost the Vin spike to a very high voltage and damage the AF5030S.

OUTPUT CAPACITOR

The output capacitor also needs to have a low ESR to keep low output ripple voltage .In the case of ceramic output ceramic output capacitors,RESR is very small and does not contribute to the ripple.Therefore,a lower capacitance value can be used for ceramic capacitors.In the case of tantalum or electrolytic capacitors,the ripple is dominated by RESR multiplied by the ripple current.In that case,the output capacitor is chosen to have sufficiently low ESR.
For ceramic output capacitors,typically choose two capacitors of about 22uF.For tantalum or electrolytic capacitors,choose a capacitor with less than 50mΩ ESR.

COMPENSATION COMPONENTS



C_{COMP2} is needed only for high ESR output capacitor

Figure 2. Stability Compensation

The feedback loop of the AF5030S is stabilized by the components at the COMP pin,as shown in figure 2.The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = G_{COMP} \cdot A_{EA} \cdot \frac{V_{FB}}{I_{OUT}}$$

The dominant pole P1 is due to Ccomp：

$$F_{P1} = \frac{G_{EA}}{2\pi \cdot A_{EA} \cdot C_{COMP}}$$

The second pole P2 is the output pole:

$$F_{P2} = \frac{I_{OUT}}{2\pi \cdot C_{OUT} \cdot V_{OUT}}$$

The first zero Z1 is due to Rcomp and Ccomp:

$$F_{Z1} = \frac{1}{2\pi \cdot C_{COMP} \cdot R_{COMP}}$$

The system may have another zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$F_{ESR} = \frac{1}{2\pi \cdot C_{OUT} \cdot R_{ESRCOUT}}$$

And finally ,the third pole is due to Rcomp and Ccomp(if Ccomp2 is used)：

$$F_{P3} = \frac{1}{2\pi \cdot C_{COMP2} \cdot R_{COMP}}$$

The following steps should be used to compensate the IC:

STEP1. Set the crossover frequency at 1/10 of the switching frequency via Rcomp:

$$R_{COMP} = \frac{2\pi \cdot V_{OUT} \cdot C_{OUT} \cdot F_{SW}}{10 \cdot G_{EA} \cdot C_{COMP} \cdot V_{FB}}$$

But limit Rcomp to 10KΩ maximum.

STEP2. Set the zero fZ1 at 1/4 of the crossover frequency. If Rcomp is less than 10KΩ,the equation for Ccomp is:

$$C_{COMP} = \frac{0.637}{R_{COMP} \cdot F_C}$$

The value unit is F.

STEP3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the crossover frequency,an additional compensation capacitor Ccomp2 is required.The condition for using Ccomp2 is:

$$\pi \cdot C_{OUT} \cdot R_{ESRCOUT} \cdot F_{SW} \geq 1$$

And the proper value for Ccomp2 is:

$$C_{COMP2} = \frac{C_{OUT} \cdot R_{ESRCOUT}}{R_{COMP}}$$

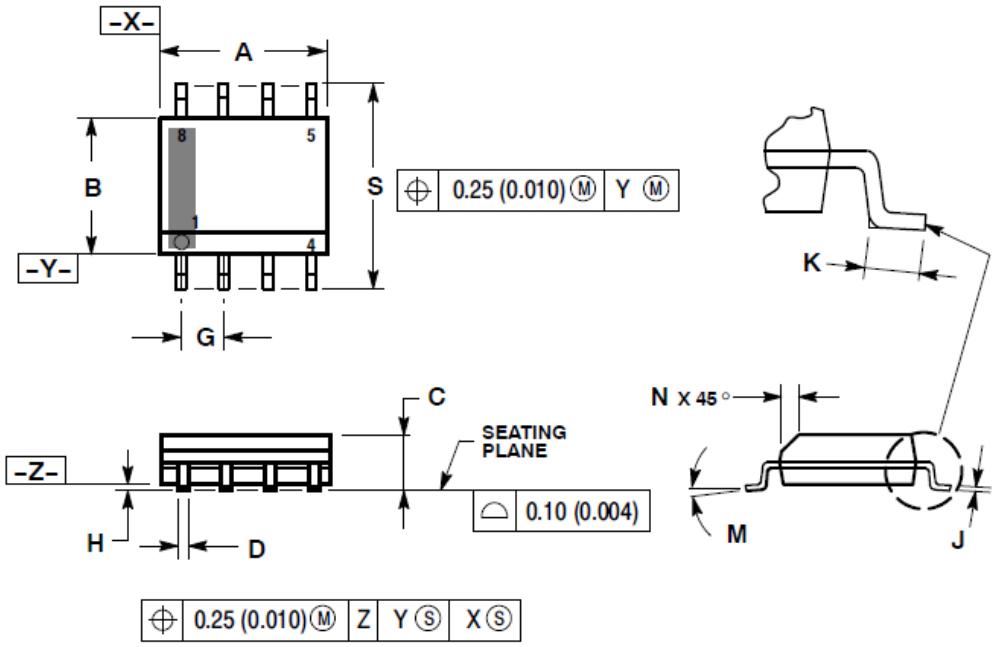
Though Ccomp2 is unnecessary when the output capacitor has sufficiently low ESR,a small value Ccomp2 such as 100pF may improve stability against PCB layout parasitic effects.

TABLE 2-- Component Selection Guide for Stability Compensation

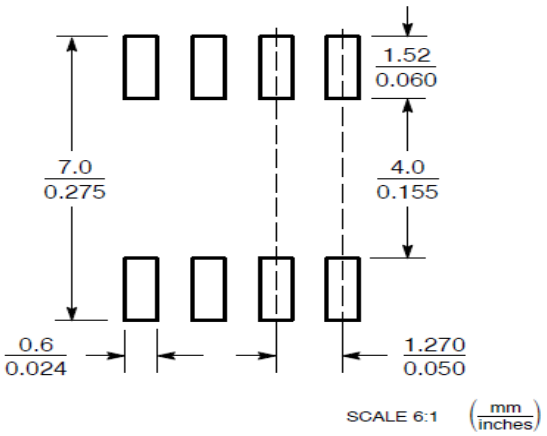
VIN Range (V)	VOUT (V)	COUT (uF)	Rcomp (kΩ)	Ccomp (nF)	Ccomp2 (pF)	Inductor (uH)
5--15	1.0	22uF×2	3.3	5.6	none	4.7
5--15	1.2		3.9	4.7		4.7
5--15	1.8		5.6	3.3		10
5--15	2.5		8.2	2.2		
5--15	3.3		10	2		
5--15	5.0		10	3.3		

PACKAGE DIMENSIONS

SOP-8



SOLDERING FOOTPRINT*



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

DISCLAIMER

AFSEMI RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. AFEMI DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICIENCE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

THE GRAPHS PROVIDED IN THIS DOCUMENT ARE STATISTICAL SUMMARIES BASED ON A LIMITED NUMBER OF SAMPLES AND ARE PROVIDED FOR INFORMATIONAL PURPOSE ONLY. THE PERFORMANCE CHARACTERISTICS LISTED IN THEM ARE NOT TESTED OR GUARANTEED. IN SOME GRAPHS, THE DATA PRESENTED MAY BE OUTSIDE THE SPECIFIED OPERATING RANGE (E.G,. OUTSIDE SPECIFIED POWER SUPPLY RANGE.) AND THEREFORE OUTSIDE THE WARRANTED RANGE.