



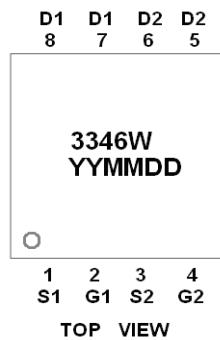
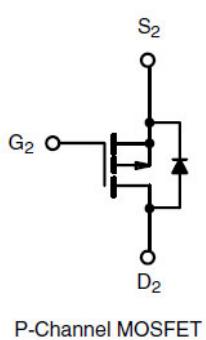
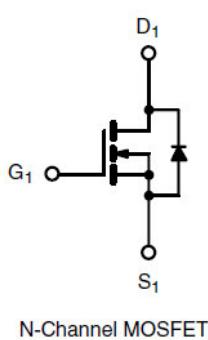
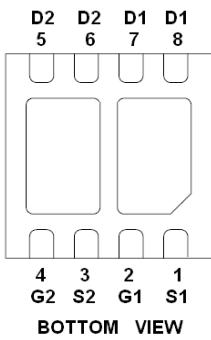
**Alfa-MOS
Technology**

**AFC3346W
40V N & P Pair
Enhancement Mode MOSFET**

General Description

AFC3346W, N & P Pair enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent RDS(ON), low gate charge. These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

Pin Description (DFN3X3-8L)



Application

- DC/DC Conversion
- Load Switch
- DC FAN

Pin Define

Pin	Symbol	Description
1	S1	Source 1
2	G1	Gate 1
3	S2	Source 2
4	G2	Gate 2
5	D2	Drain 2
6	D2	Drain 2
7	D1	Drain 1
8	D1	Drain 1

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFC3346WFN338RG	3346W YYMMDD	DFN3X3-8L	Tape & Reel	5000 EA

※ YY year code

※ MM month code

※ DD date code

※ AFC3346WFN338RG : 13" Tape & Reel ; Pb- Free ; Halogen- Free



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Absolute Maximum Ratings (N-Channel)

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	15	A
$T_A=70^\circ\text{C}$		12	
Pulsed Drain Current	I_{DM}	40	A
Continuous Source Current(Diode Conduction)	I_S	10	A
Power Dissipation	P_D	2	W
$T_A=70^\circ\text{C}$		1.5	
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	56	$^\circ\text{C}/\text{W}$

Electrical Characteristics (N-Channel)

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0		3.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$			1	uA
$T_J=85^\circ\text{C}$		$V_{DS}=32\text{V}, V_{GS}=0\text{V}$			10	
On-State Drain Current	$I_{D(\text{on})}$	$V_{DS} \geq 5\text{V}, V_{GS}=10\text{V}$	20			A
Drain-Source On-Resistance	$R_{DS(\text{on})}$	$V_{GS}=10\text{V}, I_D=15\text{A}$		20	28	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=12\text{A}$		30	38	
Forward Transconductance	g_{FS}	$V_{DS}=15\text{V}, I_D=5.0\text{A}$		25		S
Diode Forward Voltage	V_{SD}	$I_S=2\text{A}, V_{GS}=0\text{V}$		0.85	1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=20\text{V}, V_{GS}=4.5\text{V}$ $I_D= 5\text{A}$		10	14	nC
Gate-Source Charge	Q_{gs}			2.8		
Gate-Drain Charge	Q_{gd}			3.2		
Input Capacitance	C_{iss}	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		850		pF
Output Capacitance	C_{oss}			110		
Reverse Transfer Capacitance	C_{rss}			75		
Turn-On Time	$t_{d(\text{on})}$	$V_{DD}=20\text{V}, R_L=4\Omega$ $I_D=5.0\text{A}, V_{GEN}=10\text{V}$ $R_G=1\Omega$		6	12	ns
	t_r			10	20	
Turn-Off Time	$t_{d(\text{off})}$			20	36	
	t_f			6	12	



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Absolute Maximum Ratings (P-Channel)

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	-40	V
Gate -Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	-12.0	A
		-10.0	
Pulsed Drain Current	I_{DM}	-40	A
Continuous Source Current(Diode Conduction)	I_S	-10	A
Power Dissipation	P_D	1.8	W
		1.2	
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$

Electrical Characteristics (P-Channel)

($T_A=25^\circ\text{C}$ Unless otherwise noted)

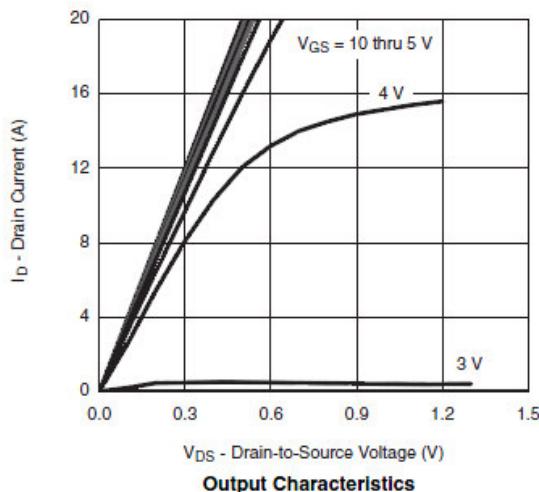
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D = -250\mu\text{A}$	-40			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D = -250\mu\text{A}$	-1.0		-3.0	
Gate Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS} = \pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -32\text{V}, V_{GS}=0\text{V}$			-1	uA
		$V_{DS} = -32\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$			-20	
On-State Drain Current	$I_{D(on)}$	$V_{DS} \geq -5\text{V}, V_{GS} = -10\text{V}$	-20			A
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{V}, I_D = -12\text{A}$		34	45	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -10\text{A}$		48	62	
Forward Transconductance	g_{FS}	$V_{DS} = -15\text{V}, I_D = -5\text{A}$		20		S
Diode Forward Voltage	V_{SD}	$I_S = -2\text{A}, V_{GS}=0\text{V}$		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=-20\text{V}, V_{GS}=-4.5\text{V}$ $I_D = -5.0\text{A}$		13	20	nC
Gate-Source Charge	Q_{gs}			4.5		
Gate-Drain Charge	Q_{gd}			6.5		
Input Capacitance	C_{iss}	$V_{DS}=-20\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		1100		pF
Output Capacitance	C_{oss}			145		
Reverse Transfer Capacitance	C_{rss}			115		
Turn-On Time	$t_{d(on)}$	$V_{DD}=-20\text{V}, R_L=4\Omega$ $I_D=-5.0\text{A}, V_{GEN}=-4.5\text{V}$		40	80	ns
	t_r			55	100	
Turn-Off Time	$t_{d(off)}$			30	60	
	t_f			12	20	



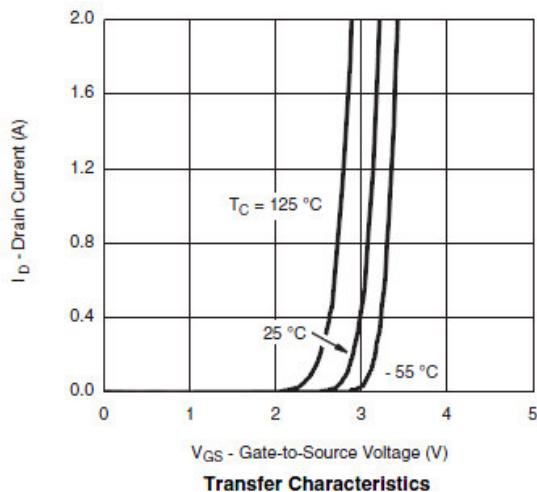
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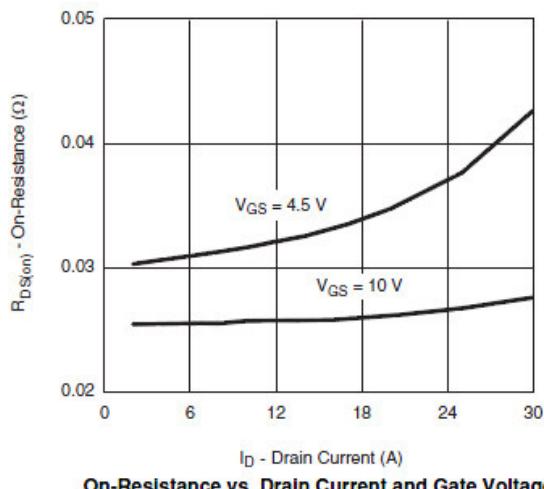
Typical Characteristics (N-Channel)



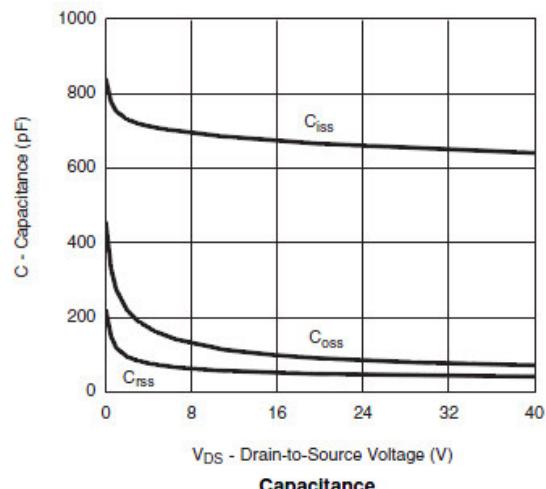
Output Characteristics



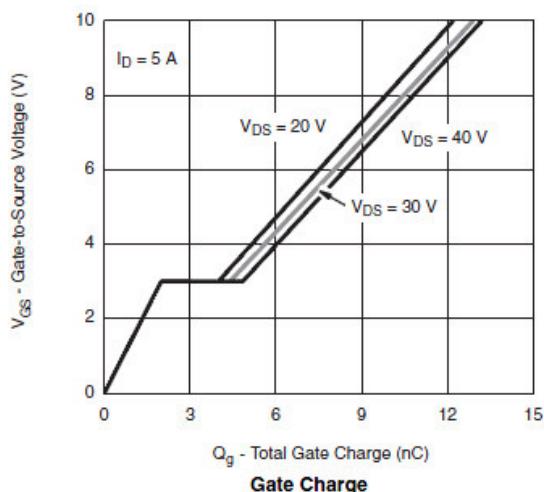
Transfer Characteristics



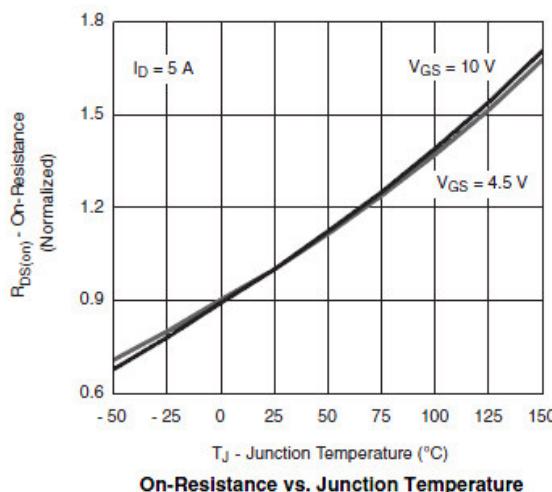
On-Resistance vs. Drain Current and Gate Voltage



Capacitance



Gate Charge



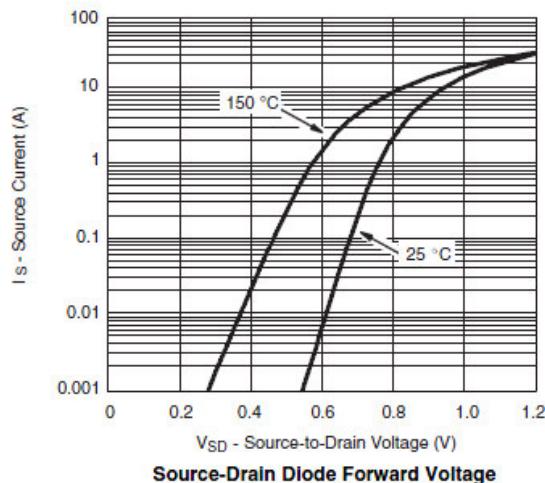
On-Resistance vs. Junction Temperature



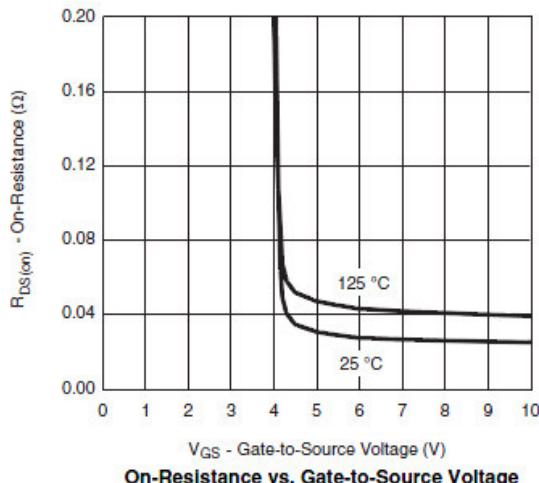
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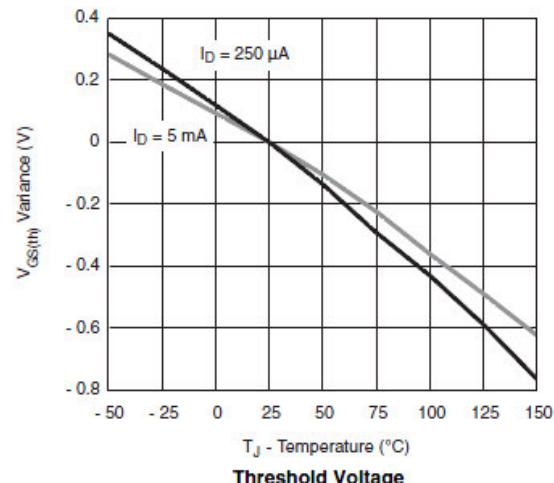
Typical Characteristics (N-Channel)



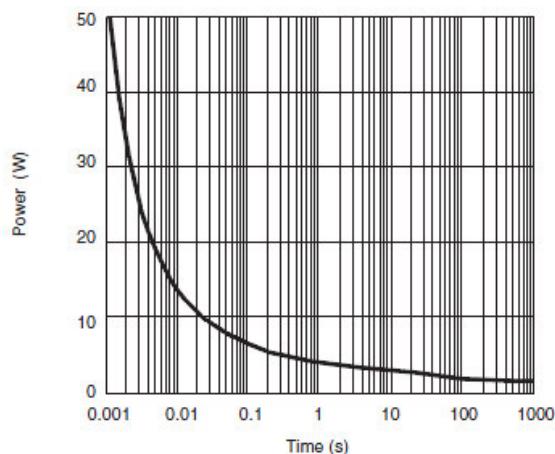
Source-Drain Diode Forward Voltage



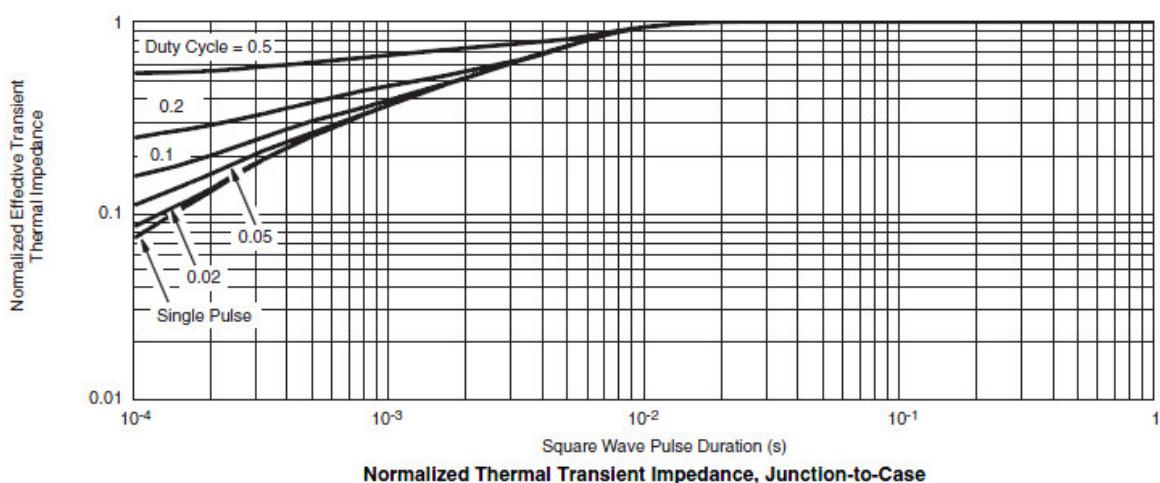
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



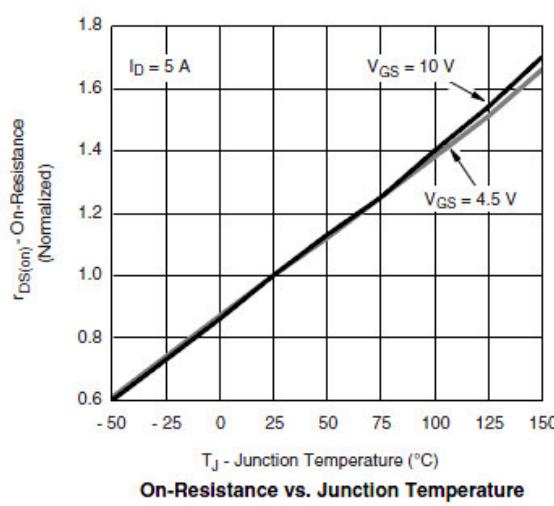
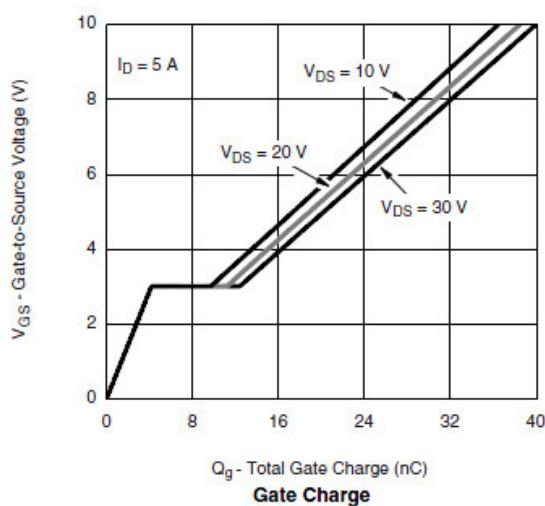
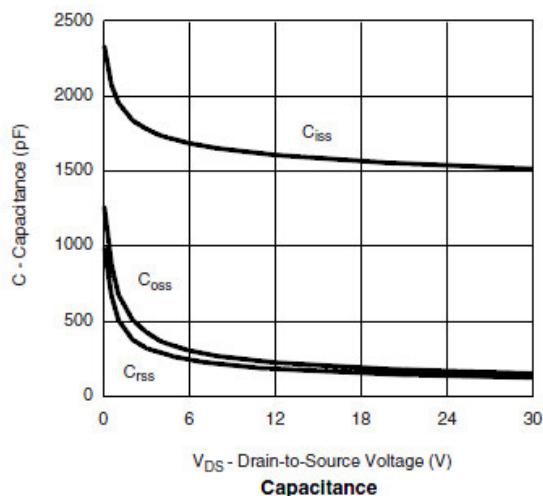
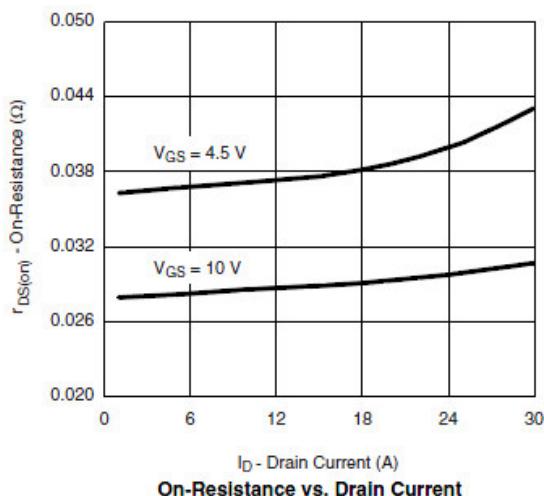
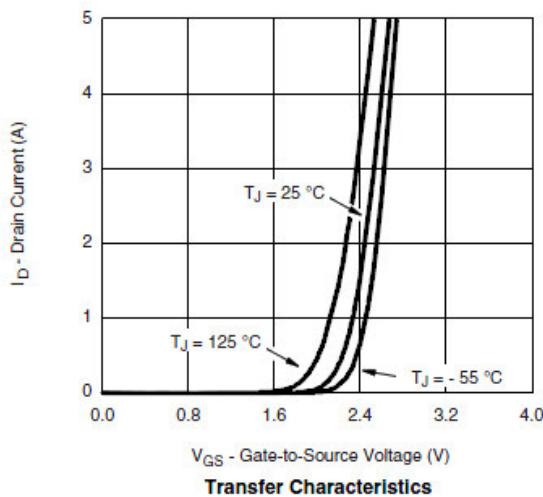
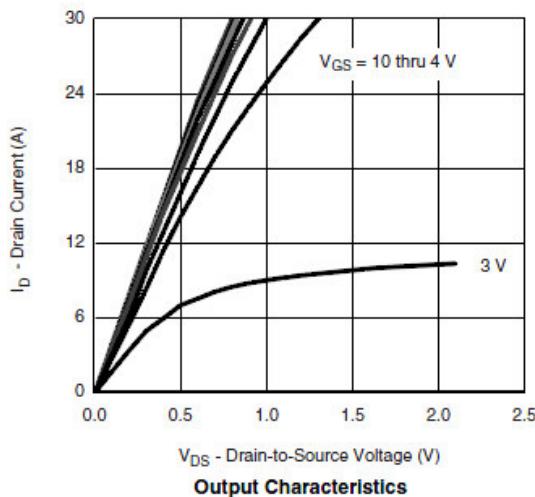
Normalized Thermal Transient Impedance, Junction-to-Case



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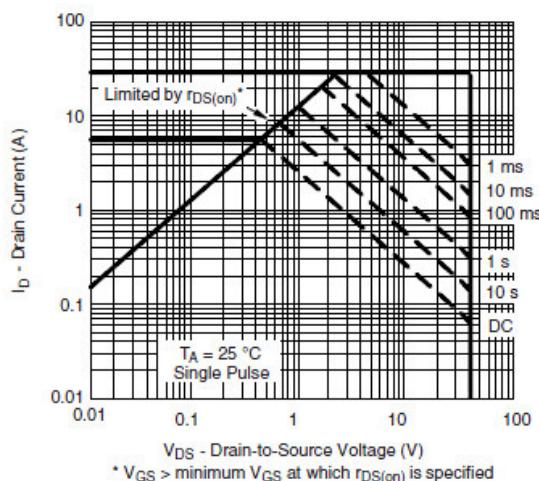
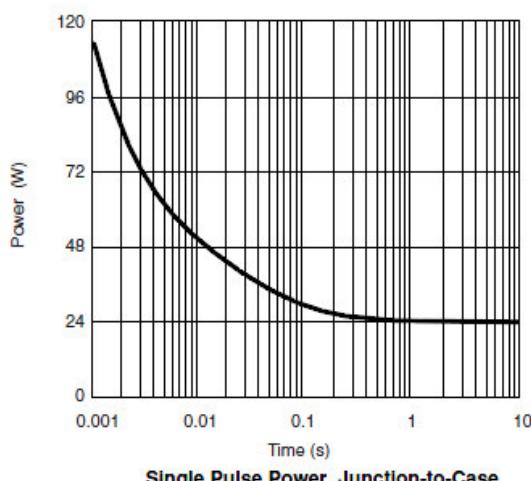
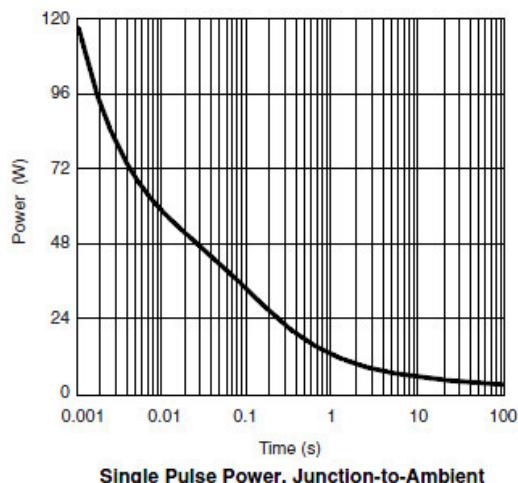
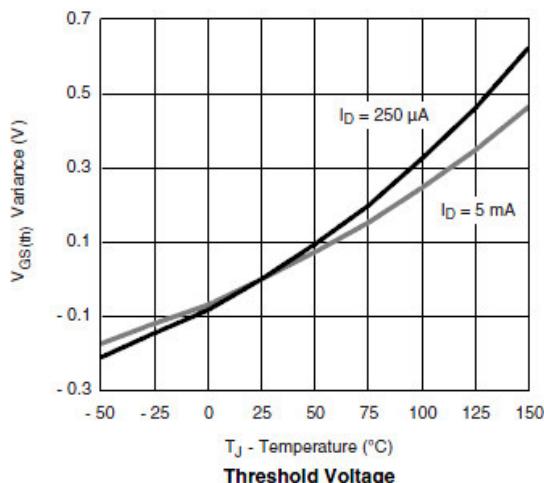
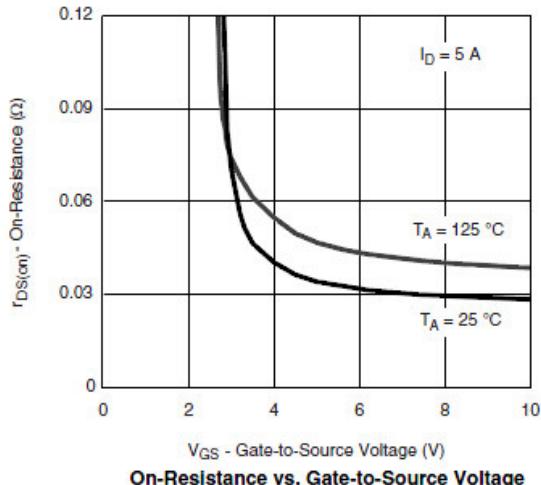
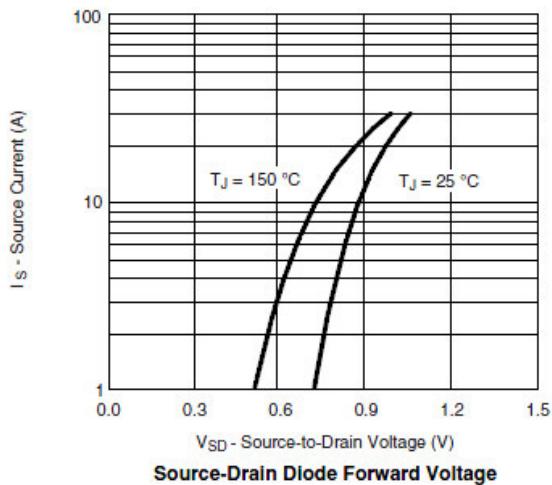




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Typical Characteristics (P-Channel)



* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient

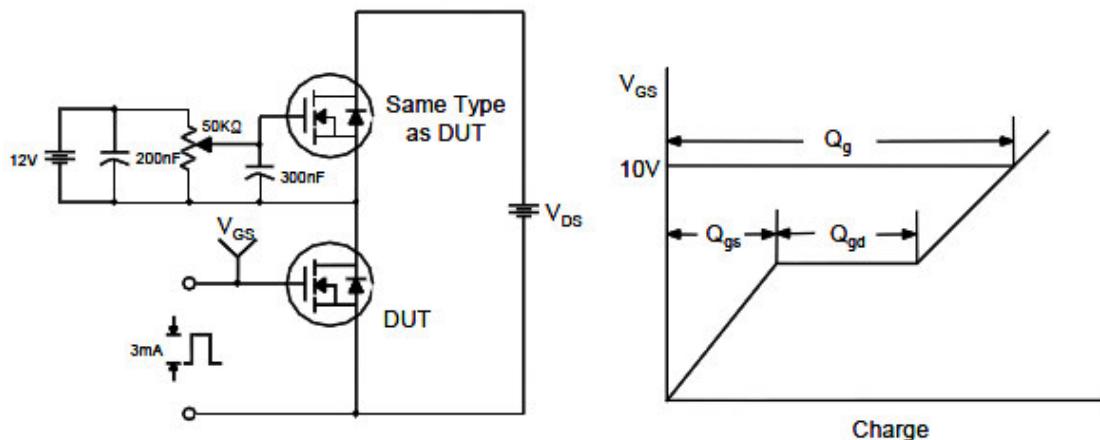


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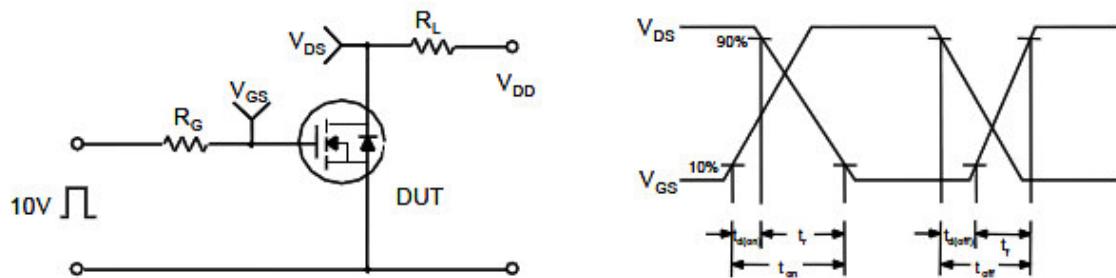
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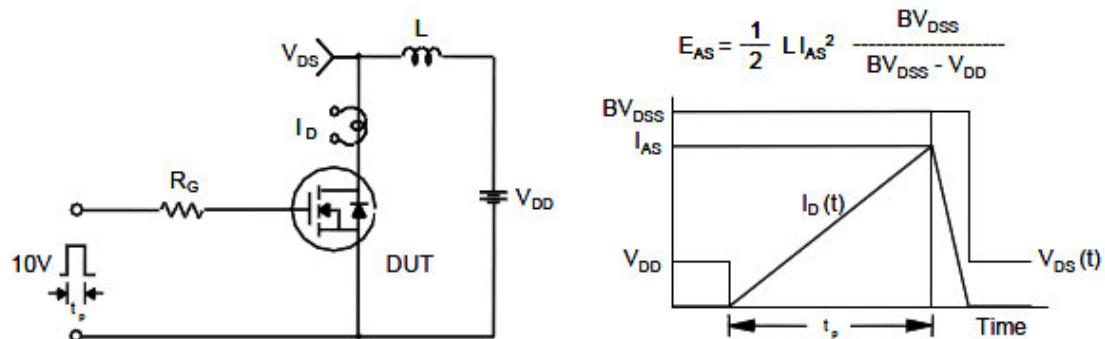
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

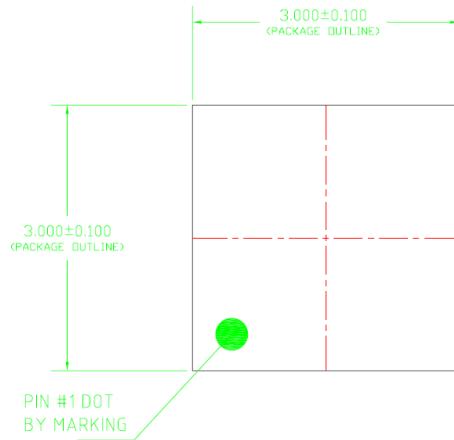




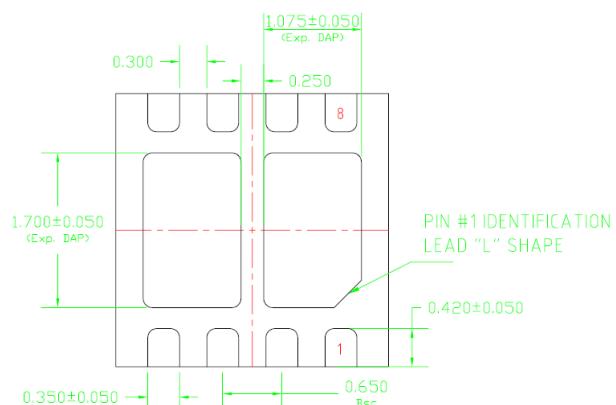
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Package Information (DFN3X3-8L)



TOP VIEW



BOTTOM VIEW



SIDE VIEW

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2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)
Tel : 886 2) 2651 3928
Fax : 886 2) 2786 8483
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