Alfa-MOS Technology

AFE0514

4-Line ESD Protection
Low Capacitance Bi-direction TVS

General Description

AFE0514 are designed by bi-direction TVS diode, to protect high speed data interfaces. This product has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).The TVS diode prevents over-voltage on the power line, protecting any downstream components. The low capacitance configuration allows the user to protect high-speed data or transmission lines. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

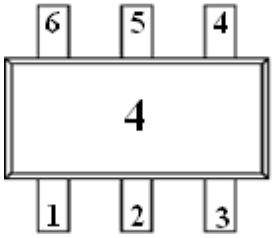
Features

- Transient protection for high-speed data lines to IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact) IEC 61000-4-4 (EFT) 40A (5/50ns)
- Small package saves board space
- Protects up to four I/O lines & power line
- Low capacitance (<3pF) for high-speed interfaces
- Low leakage current and clamping voltage
- Low operating voltage: 5.0V
- Solid-state silicon-avalanche technology

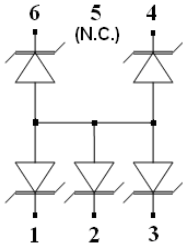
Application

- USB 2.0 Power and Data Line Protection
- Monitors and Flat Panel Displays
- Digital Visual Interface (DVI)
- 10/100/1000 Ethernet
- Notebook Computer
- SIM Ports
- ATM Interface
- IEEE 1394 Firewire Ports
- Cellular Handsets & Accessories
- Portable Instrumentation
- Digital Cameras
- MP3 Players
- Video Graphics Cards

Pin Description (SOT-563)



Schematic & PIN Configuration(SOT-563)



Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFE0514S56RG	4	SOT-563	Tape & Reel	3000 EA

※ AFE0514S56RG : 7" Tape & Reel ; Pb- Free ; Halogen- Free

ABSOULTE MAXIMUM RATINGS

(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Peak Pulse Power (t_p = 8/20 μs)	P_{pk}	100	W
Maximum Peak Pulse Current (t_p = 8/20 μs)	I_{PP}	6	A
ESD per IEC 61000 – 4 – 2 (Air)	V_{PP}	±15	KV
ESD per IEC 61000 – 4 – 2 (Contact)	V_{PP}	±8	KV
Operating Junction Temperature	T_J	-55 ~ 125	℃
Storage Temperature Range	T_{STG}	-55 ~ 150	℃
Lead Soldering Temperature	T_L	260 (10sec)	℃

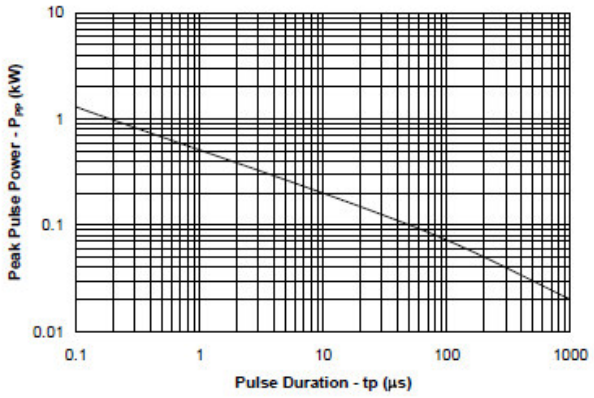
ELECTRICAL CHARACTERISTICS

(T_A=25℃ Unless otherwise noted)

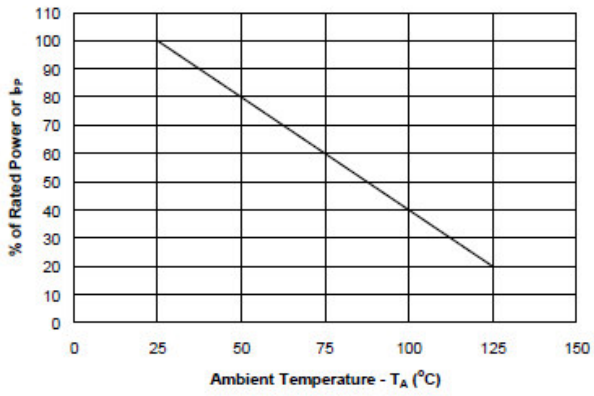
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Stand – Off Voltage	V_{RWM}	Any Pin to Pin2			5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Any Pin to Pin2	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V , T=25℃ Any Pin to Pin2		0.5	1	μA
Clamping Voltage	V_C	I_{PP} = 1A , tp = 8/20 μs Any Pin to Pin2			13	V
Clamping Voltage	V_C	I_{PP} = 6A , tp = 8/20 μs Any Pin to Pin2			15	V
Junction Capacitance	C_j	V_R = 0V , f = 1MHz Any Pin to Pin2		2	3	pF

Typical Characteristics

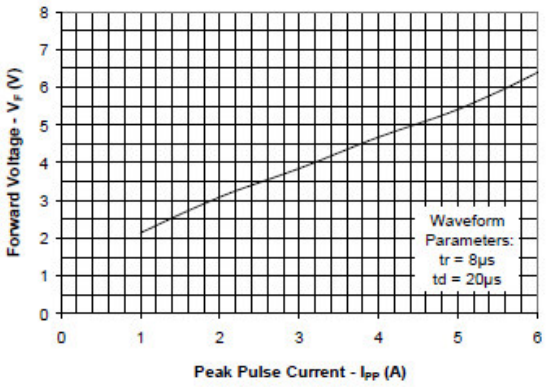
Non-Repetitive Peak Pulse Power vs. Pulse Time



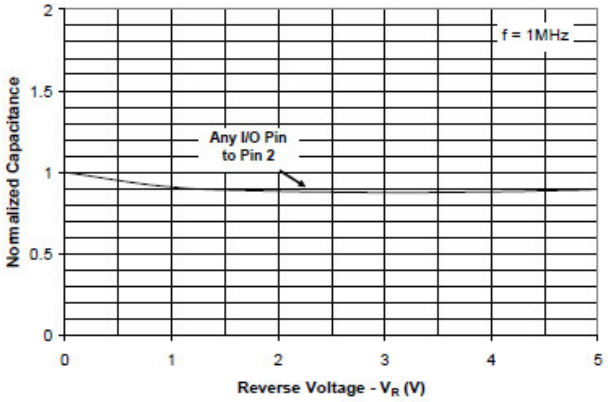
Power Derating Curve



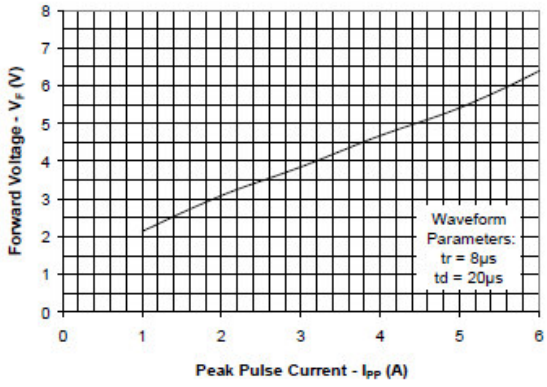
Forward Voltage vs. peak Pulse Current



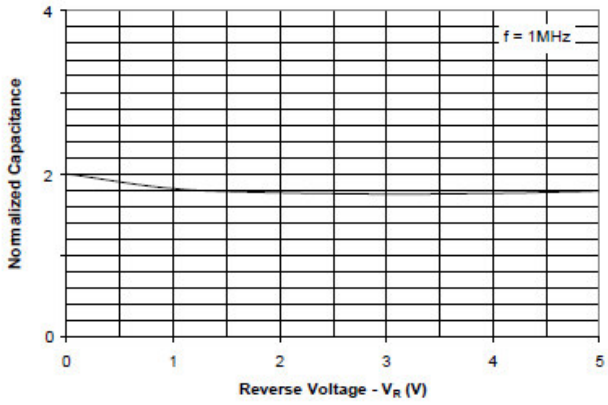
Capacitance vs. Reverse Voltage (Normalized to 0V)



Forward Voltage vs. peak Pulse Current



Capacitance vs. Reverse Voltage (Normalized to 0V)

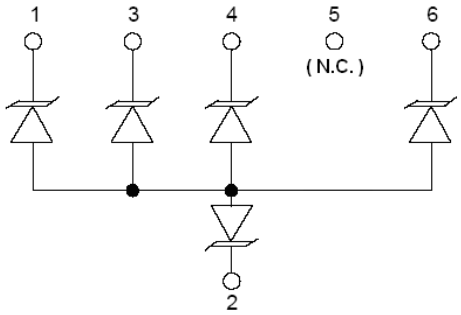


Application Information

Device Connection for Protection of Five Data Lines

AFE0514 is designed to protect up to five bidirectional data lines. The device is connected as follows:

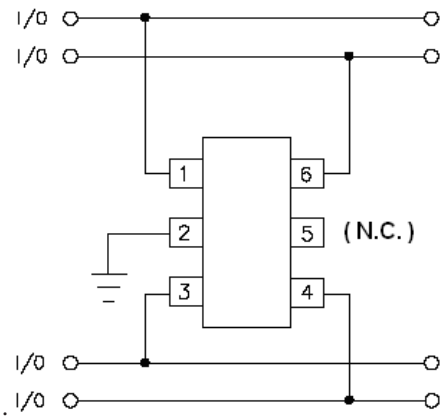
1. Bidirectional protection of five I/O lines is achieved by connecting pins 1, 3, 4, 5, and 6 to the data lines. Pin 2 is connected to ground. The ground connection should be made directly to the ground plane for best results. The path length is kept as short as possible to reduce the effects of parasitic inductance in the board traces.



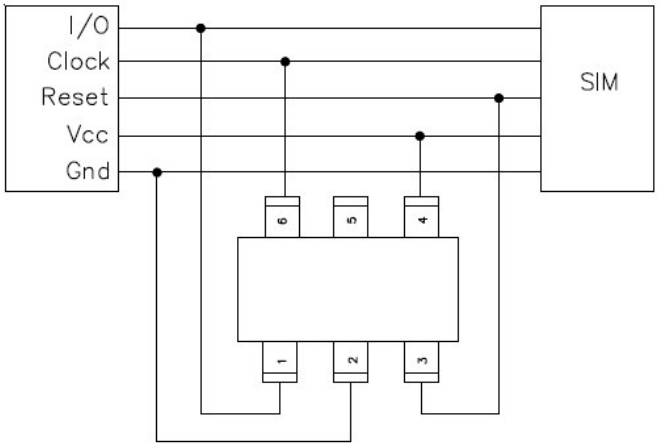
Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

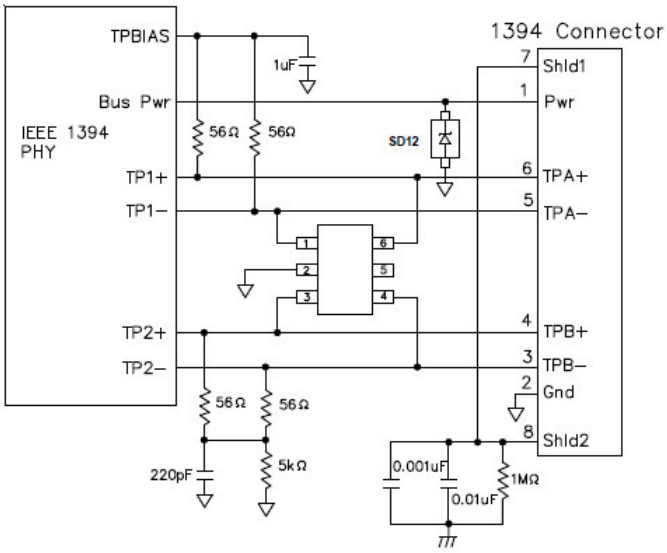
1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible.



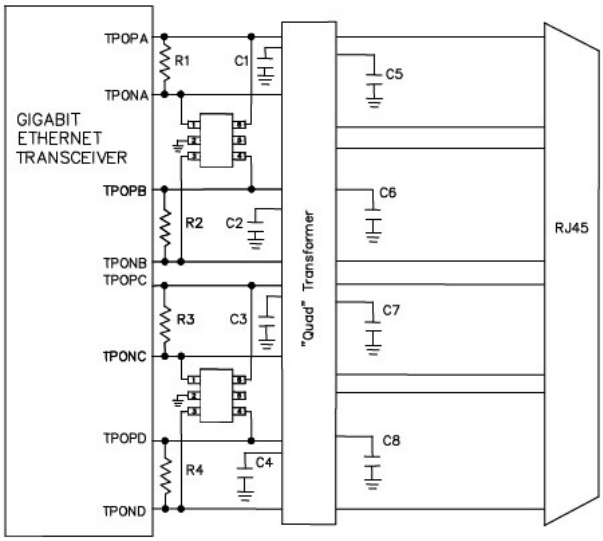
Application Information



SIM Port - Protection of Three Data Lines and VCC

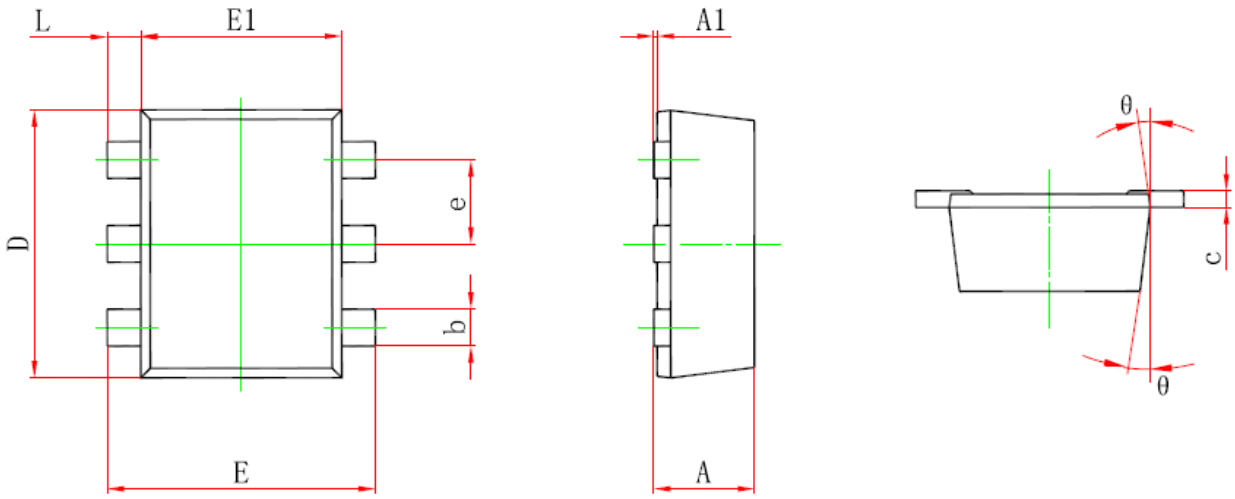


IEEE 1394 Firewire Protection



Gigabit Ethernet Protection

Package Information (SOT-563)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.525	0.600	0.021	0.024
A1	0.000	0.050	0.000	0.002
e	0.450	0.550	0.018	0.022
c	0.090	0.160	0.004	0.006
D	1.500	1.700	0.059	0.067
b	0.170	0.270	0.007	0.011
E1	1.100	1.300	0.043	0.051
E	1.500	1.700	0.059	0.067
L	0.100	0.300	0.004	0.012
θ	7 °REF.		7 °REF.	

©2010 Alfa-MOS Technology Corp.
2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)
Tel : 886 2) 2651 3928
Fax : 886 2) 2786 8483
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