Alfa-MOS Technology

AFE4114P

Ultra Low Capacitance 5-Channel ESD Protection Array

General Description

The AFE4114P is a 5-channel ultra low capacitance rail clamp ESD protection diodes array. Each channel consists of a pair of ESD diodes that steer positive or negative ESD current to either the positive or negative rail. A zener diode is integrated in to the array between the positive and negative supply rails.

In the typical applications, the negative rail pin (assigned as GND) is connected with system ground. The Positive ESD current is steered to the ground through an ESD diode and Zener diode and the positive ESD voltage is clamped to the zener voltage. The AFE4114P is idea to protect high speed data lines.

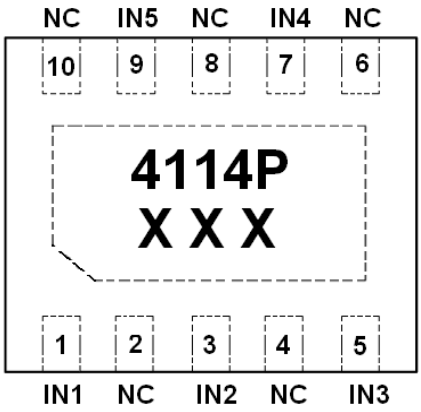
Features

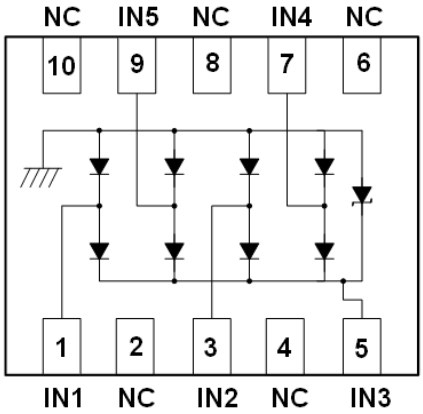
- 5 channels of ESD protection
- Provides ESD protection to IEC61000-4-2 level 4
- ±17kV air discharge
- ±12kV contact discharge
- Input to GND capacitance: 3.0pF(Max)
- Channel I/O to I/O capacitance: 1.5pF(Max)
- Low clamping voltage
- Low operating voltage (5V)
- Improved zener structure
- Optimized package for easy high speed data lines PCB layout.

Application

- High Definition Multi-Media Interface Protection
- DVI port
- 10 / 100/ 1000M Ethernet interface
- USB2.0 interface
- Flat panel monitors
- Set-top box
- VGA interface.

Pin Description Top View (TQFN-10 (2.6X2.6X0.55-0.5))





Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFE4114PTQFN10RG	4114P	TQFN-10-2.6X2.6X0.55-0.5	Tape & Reel	3000 EA

※ 4114P Device Code
※ XXX Date Code
※ AFE4114PTQFN10RG : 7" Tape & Reel ; Pb- Free ; Halogen- Free

Absolute Maximum Ratings

(T_A=25℃ Unless otherwise noted)

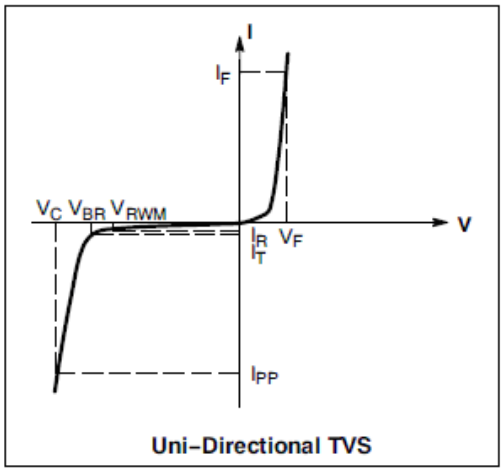
Parameter	Symbol	Typical	Unit
Peak Pulse Power (t_p = 8/20 μs)	P_{pk}	150	W
Peak Pulse Current (t_p = 8/20 μs)	I_{PP}	10	A
ESD per IEC 61000 – 4 – 2 (Air)	V_{ESD1}	±17	KV
ESD per IEC 61000 – 4 – 2 (Contact)	V_{ESD2}	±12	KV
Operating Junction Temperature	T_J	-55 ~ 125	℃
Storage Temperature Range	T_{STG}	-55 ~ 150	℃

Electrical Characteristics

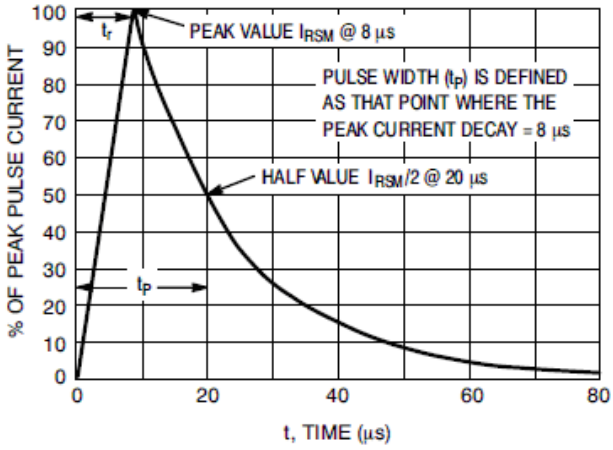
(T_A=25℃ Unless otherwise noted)

Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Reverse Working Voltage	V_{RWM}	Any Pin to GND			5	V
Forward Voltage	V_F	I_F =10mA	0.4	0.8	1.5	V
Reverse Breakdown Voltage	V_{BR}	I_t = 1mA Any Pin to GND	6			V
Reverse Leakage Current	I_R	V_{RWM} = 5V , T=25℃ Any Pin to GND			1	μA
Positive Clamping Voltage	V_{C1}	I_{PP} = 1A , tp = 8/20 μs Positive pulse Any Pin to GND		8.5	12	V
Negative Clamping Voltage	V_{C2}	I_{PP} = 1A , tp = 8/20 μs Negative pulse Any Pin to GND		1.8		V
Junction Capacitance Between Channel	C_{j1}	V_R = 0V , f = 1MHz Between I/O Pin		1.3	1.5	pF
Junction Capacitance Between I/O to GND	C_{j2}	V_R = 0V , f = 1MHz Any Pin to GND			3.0	pF

Electrical Parameter



Uni-Directional TVS



8 X 20 µs Pulse Waveform

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
I_T	Test Current
V_{BR}	Breakdown Voltage @ I_T
I_F	Forward Current
V_F	Forward Voltage @ I_F

Typical Characteristics

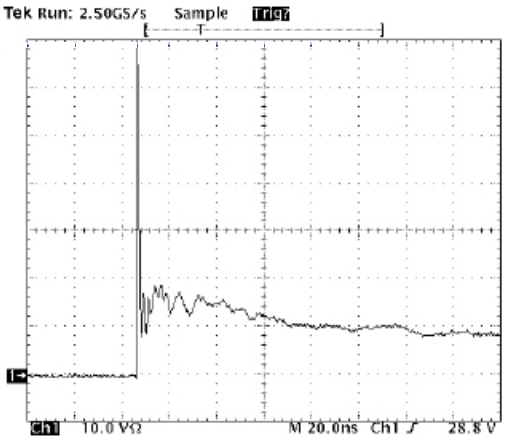


Figure 1 ESD clamping voltage screenshot
(Forward 8kv contact IEC 61000-4-2 standard)

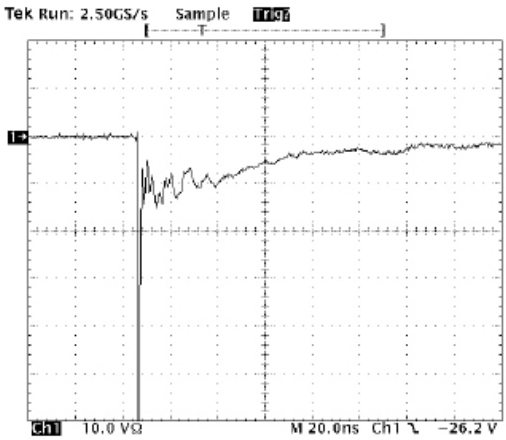


Figure 2 ESD clamping voltage screenshot
(Reverse 8kv contact IEC 61000-4-2 standard)

Application Information

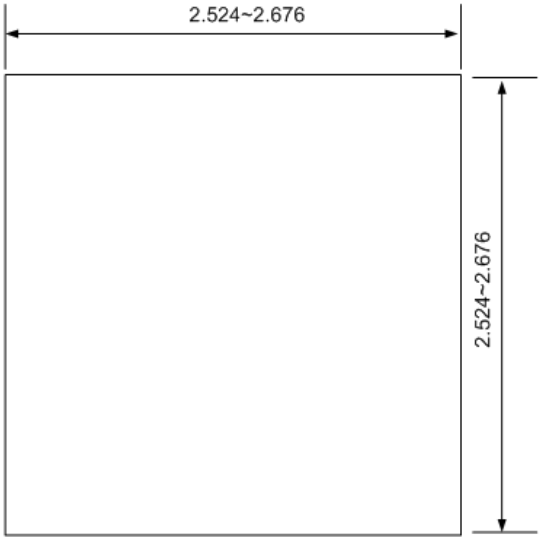
(Gigabit Ethernet GR-1089 Intra-Building Protection)

These devices are designed to protect low voltage date lines operating at 5.0 volts. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 1, 3, 7 and 9. The center pin should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. Pins 2,4,6,8 and 10 are not connected. Note that pin5 is connected internally to the cathode of the low voltage TVS. It is not recommended that these pins be directly connected to a DC source greater than the breakdown voltage (VB) as the device can latch on as described below.

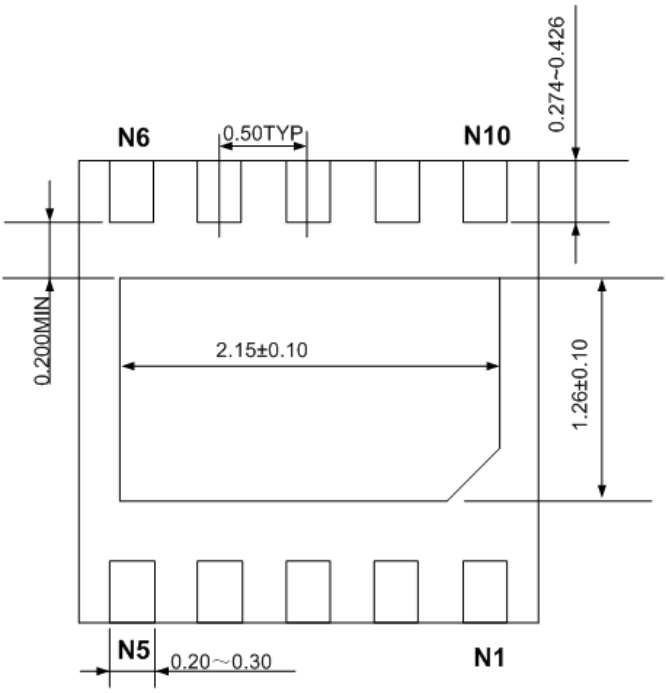
(Gigabit Ethernet ESD Protection)

The TVS employs a complex N-P-P-N structure in contrast to the P-N structure normally found in traditional silicon-avalanche TVS diodes. Since the TVS devices use a 6-layer structure, they exhibit a slightly different IV characteristic curve when compared to conventional devices. During normal operation, the device represents a high-impedance to the circuit up to the device working voltage (VRWM).During an ESD event, the device will begin to conduct and will enter a low impedance state when the punch through voltage is exceeded. Unlike a conventional device, the low voltage TVS will exhibit a slight negative resistance characteristic as it conducts current. This characteristic aids in lowering the clamping voltage of the device, but must be considered in applications where DC voltages are present.

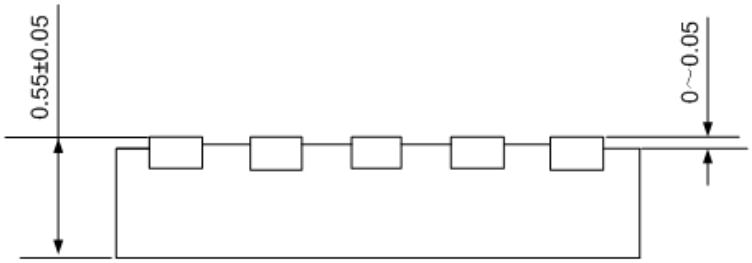
Package Information (TQFN-10 (2.6X2.6X0.55-0.5))



Top View



Bottom View



Side View

©2010 Alfa-MOS Technology Corp.
2F, No.80, Sec.1, Cheng Kung Rd., Nan Kang Dist., Taipei City 115, Taiwan (R.O.C.)
Tel : 886 2) 2651 3928
Fax : 886 2) 2786 8483
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