24-Bit, 3-Channel, 2KSPS, Low Noise, Low Power ΣΔADC

Features

- 2.5V to 3.6V operation voltage range
- Up to 21 bits ENOB
- RMS noise
  - 784nV RMS noise @ 250Hz, PGA = x1
  - 74nV RMS noise @ 250Hz, PGA = x128
- 300μA ultra-low current consumption
- 6uA (typ.) standby-mode current
- Input Channels
  - Three fully differential signal input channels
  - Two fully differential reference input channels
- Embedded temperatures sensor
- Built-in power supply monitor
- Sensors burn-out diagnostic
- Internal precision clock oscillator
- 2-stages programmable signal gain amplifier
  - x1 ~ x128 1st stage gain
  - x1 ~ x16 2nd stage gain

  2 programmable IDAC current sources
- -40 ~ 85°C operation temperature
- 250Hz to 2KHz output data rates
- QFN16-3x3 package
- A build-in moving-average digital filter

Applications

- Instrumentation
- Direct RTD, thermistor measurements
- IR thermopile sensor measurements
- Gas detectors
- Pressure sensor acquisition
- Wheatstone bridge sensor measurement
- Liquid chromatography
- PH sensor analysis
- Smart Home sensor analog front-end

Description

The AFE6160A is a 3-channel, low-noise and ultra-low power 24-bit Sigma-Delta Analog-to-Digital Converter (SDADC) with an integrated decimation filter. The device supports output data rates of 250Hz, 500Hz, 1kHz or 2kHz and communicates with a host MCU through standard I²C interface.

The AFE6160A provides three independent differential signal input channels and two independent reference input channels. Two precision current sources (IDACx) and one voltage source (AVDD) are available for direct sensor excitation.

The device incorporates two-stage Programmable Gain Amplifiers (PGA) for signal inputs and one programmable gain amplifier for reference inputs. The 1st stage signal amplifier, PGAGN, offers gain setting from x1 to x128, while the 2nd stage signal amplifier, ADCGN, supports gain setting from x1 to x16. The reference amplifier, REFGN, provides gain attenuation from x1 to x0.25.

Embedding with well-calibrated temperature sensor and a precision 1.024MHz internal oscillator, the AFE6160A is a cost-effective solution for the applications of high precision measurement.

Pin Function Description

Pin Name	Pin No.	I/O	Description
VCM	1	I/O	Common-mode voltage regulation
AVSS	2	P	Analog ground
AVDD	3	I/O	Analog power
VSS	4	P	Digital ground
SDA	5	I/O	I^{2}C digital interface data I/O
EOC	6	O	Interrupt I/O for end of data conversion
SCL	7	I	I^{2}C digital interface clock input
VDD	8	P	Digital power
AIN0+, AIN0-	9,10	I	CH0 differential analog signal input
AIN1+, AIN1-	11,12	I	CH1 differential analog signal input
AIN2+, AIN2-	13,14	I	CH2 differential analog signal input
RIN1+, RIN1-	13,14	I	CH1 differential reference voltage input
RIN0+, RIN0-	15,16	I	CH0 differential reference voltage input

Pin Configuration and Functions

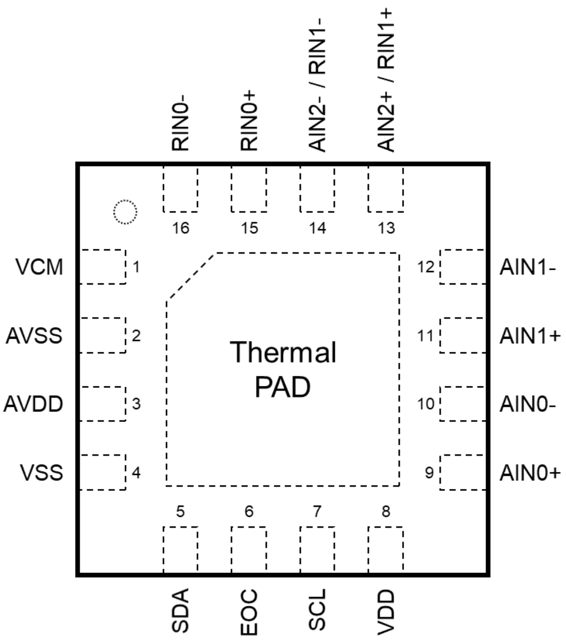


Figure 1 Top view of AFE6160A

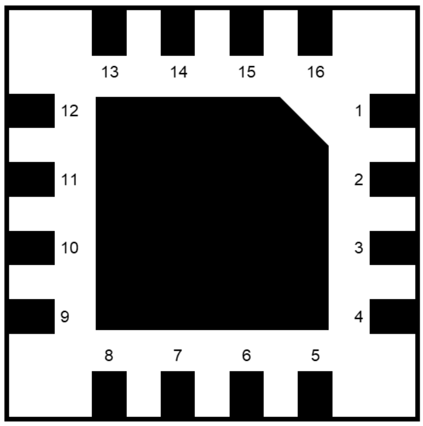


Figure 2 Bottom view of AFE6160A

Ordering Information

Product ID	Package Type	Packing	Comments
AFE6160A-NQ16NNR	QFN16-3x3	3000 Units/Reel	Green

Marking Information

ESMT

Line 1: Production Name

Line 2: Date Code

Functional Block Diagram

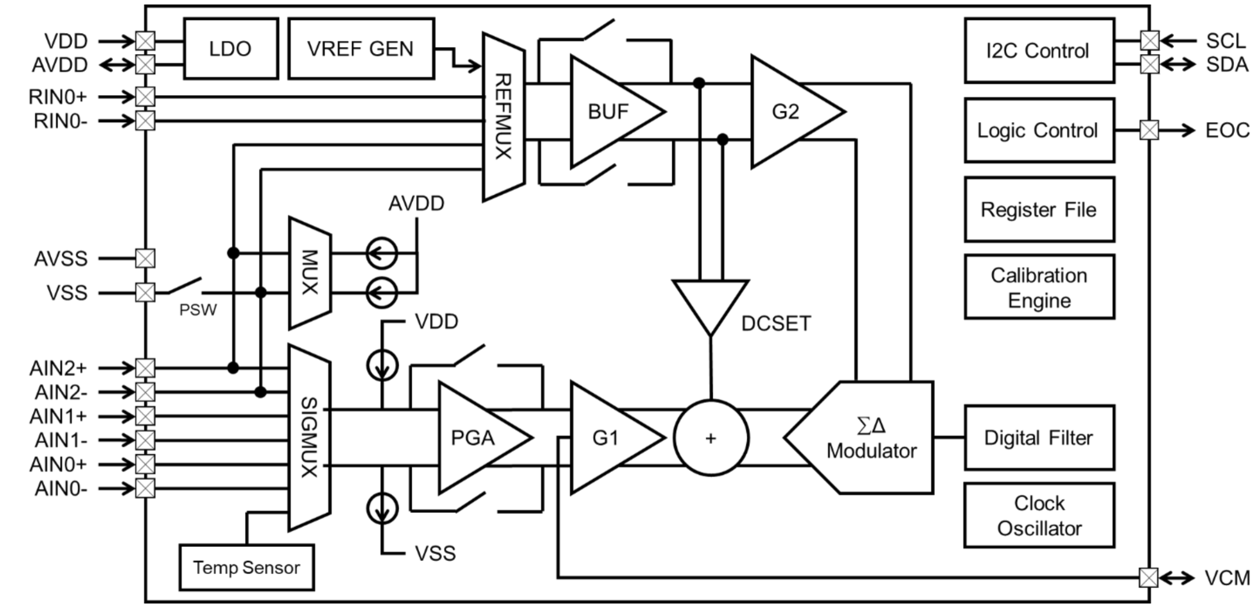


Figure 3 Function block diagram of AFE6160A

Table of Contents

Specifications

Absolute Maximum Rating

Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device.

Symbol	Description	Conditions	Min	Max	Unit
VDD	Supply Voltage	VDD	-0.3	4.0	V
AVDD	Analog Voltage	AVDD	-0.3	4.0	V
V_{IN}	Input Pin Voltage	AINx+, AINx-, RINx+, RINx-, VCM	-0.3	4.0	V
V_{IO}	Digital I/O ports	EOC, SDA, SCL	-0.3	4.0	V
T_A	Operation Temperature Range		-40	85	°C
T_{stg}	Storage Temperature Range		-55	150	°C
ESD	Human Body Mode	AINx+, AINx-, RINx+, RINx-, SDA, SCL, EOC	±2000		V
		AVDD, VCM	±1000		V
	Charged Device Model		±500		V

(1) Operation Stresses beyond the Absolute Maximum Ratings may cause permanent damage. Operation within the Absolute Maximum Ratings but outside the Recommended Operating Conditions may result in degraded functionality, reduced performance, reliability issues, or shortened device lifetime.

(2) All voltage values are with respect to network ground terminal.

(3) Power dissipation and thermal limits must be observed

Recommended Operating Condition

Symbol	Description	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VDD	System power supply	VDD to VSS	2.5	3.3	3.6	V
AVDD	Analog power suppl (*1)	AVDD to AVSS	AVDD	2.8	3.6	V
VCM	Common mode voltage (*1)	VCM to AVSS	0.6	(AVDD-0.3) / 2 (±5%)	AVDD - 1.0	V
ANALOG INPUTS						
V_{AINx}	Absolute input voltage	INBUF = 1	AVSS	—	AVDD - 0.6	V
		INBUF = 0	AVSS	—	AVDD	V
V_{IN}	Differential input voltage	$V_{IN} = V_{AINx+} - V_{AINx-}$	—	$\pm V_{REF}$/Gain	—	V
REFERENCE INPUTS						
V_{REF}	Differential reference voltage	$V_{REF} = V_{RINx+} - V_{RINx-}$	0.3	—	AVDD - AVSS	V
V_{RINx+}	Positive reference voltage	VRBUF = 0	$V_{RINx-} + 0.3$	—	AVDD	V
		VRBUF = 1	$V_{RINx-} + 0.3$	—	AVDD - 0.6	
V_{RINx-}	Negative reference voltage		AVSS	—	$V_{RINx+} - 0.3$	V
DIGITAL INPUTS/OUTPUTS						
IO	GPIO ports	SDA, SCL, EOC	VSS	—	VDD	V
OPERATION TEMPERATURE						
T_A	Operating ambient temperature		-40	—	85	°C

(*1) The typical value of AVDD and VCM is generated by AFE6160A internally. The minimum and maximum value are the recommended operation range when an external voltage is supplied on those two voltages (Figure 19).

Electrical Characteristics

All specifications are at Ta = 25℃, VDD = 3.3V, internal AVDD and VCM, VSS = AVSS = 0V, PGA, PGA chopper and ADC chopper are enabled, PGAGN = ADCGN = REFGN = x1, reference buffer is enabled (unless otherwise noticed).

Symbol	Description	Conditions	Min	Typ	Max	Unit
POWER SUPPLY						
VDD	System power supply	VDD to VSS	2.5	3.3	3.6	V
I_Q	Quiescent current	INBUF = 0	–	300	350	μA
			–	350	400	μA
		Stand-by Mode	–	6	9	μA
PGA						
PGAGN	PGA Gain Ratio	PGAGN [2:0] = 000	–	1	–	V/V
		PGAGN [2:0] = 001	–	2	–	V/V
		PGAGN [2:0] = 010	–	4	–	V/V
		PGAGN [2:0] = 011	–	8	–	V/V
		PGAGN [2:0] = 100	–	16	–	V/V
		PGAGN [2:0] = 101	–	32	–	V/V
		PGAGN [2:0] = 110	–	64	–	V/V
		PGAGN [2:0] = 111	–	128	–	V/V
	RFI filter 3dB frequency	Design guaranteed	–	12.8	–	MHz
VCM_{PGA}	Input common-mode voltage	PGAGN [2:0] ≠ 000	0.3	–	–	V
$PGAGN_{TC}$	Temperature drift of PGAGN	PGAGN [2:0] = 001	–	-100	–	ppm/°C
		PGAGN [2:0] = 111	–	-400	–	
Sigma-Delta ADC PERFORMANCE						
ENOB	Effective Resolution	VRBUF = 0	–	21	–	LSB
ODR	Output data rate	OSR [1:0] = 00	–	500	–	SPS
		OSR [1:0] = 01	–	1000	–	
		OSR [1:0] = 10	–	2000	–	
		OSR [1:0] = 11	–	250	–	
V_{OS}	Offset voltage		–	10	–	LSB
V_{OS_TC}	Temperature drift of V_{OS}		–	-10	–	LSB/°C
GE	Gain error	±0.8FSR	-1.0	±0.25	+1.0	%
INL	Integral non-linearity		–	±30	–	ppm
CMRR	common-mode rejection ratio	ODR=500SPS@60Hz	–	80	–	dB
PSRR	power-supply rejection ratio	VDD to VSS	–	90	–	dB
R_{PSW}	Sensor switch	I_{PSW} =1mA	7	10	13	Ω
ADCGN	ADC Gain Ratio	ADCGN [3:0] = 0000	–	1	–	V/V
		ADCGN [3:0] = 0001	–	2	–	V/V
		ADCGN [3:0] = 0010	–	3	–	V/V
		ADCGN [3:0] = 0011	–	4	–	V/V

		ADCGN [3:0] = 0100	—	5	—	V/V
		ADCGN [3:0] = 0101	—	6	—	V/V
		ADCGN [3:0] = 0110	—	7	—	V/V
		ADCGN [3:0] = 0111	—	8	—	V/V
		ADCGN [3:0] = 1000	—	9	—	V/V
		ADCGN [3:0] = 1001	—	10	—	V/V
		ADCGN [3:0] = 1010	—	11	—	V/V
		ADCGN [3:0] = 1011	—	12	—	V/V
		ADCGN [3:0] = 1100	—	13	—	V/V
		ADCGN [3:0] = 1101	—	14	—	V/V
		ADCGN [3:0] = 1110	—	15	—	V/V
		ADCGN [3:0] = 1111	—	16	—	V/V
$ADCGN_{TC}$	Temperature drift of ADCGN	ADCGN [3:0] = 1111	—	-70	—	ppm/°C
ANALOG INPUTS/OUTPUTS						
V_{AINx}	Absolute input voltage	INBUF = 1	AVSS	—	AVDD - 0.6	V
		INBUF = 0	AVSS	—	AVDD	V
V_{IN}	Differential input voltage	$V_{IN} = V_{AINx+} - V_{AINx-}$	—	$\pm V_{REF}$/Gain	—	V
AVDD	Analog power supply	AVDD to AVSS	AVDD	2.8	3.6	V
LR_{AVDD}	AVDD load regulation	IOUT = 30mA	-1%	—	+1%	
$AVDD_{TC}$	Temperature drift of AVDD		—	500	—	ppm/°C
VCM	Common mode voltage	VCM to AVSS	0.6	(AVDD-0.3) / 2 (±5%)	AVDD - 1.0	V
VCM_{TC}	Temperature drift of VCM		—	300	—	ppm/°C
REFERENCE INPUTS						
V_{REF}	Differential reference voltage	$V_{REF} = V_{RINx+} - V_{RINx-}$	0.3	—	AVDD - AVSS	V
V_{RINx+}	Positive reference voltage	VRBUF = 0	V_{RINx-} + 0.3	—	AVDD	V
		VRBUF = 1	V_{RINx-} + 0.3	—	AVDD - 0.6	
V_{RINx-}	Negative reference voltage		AVSS	—	V_{RINx+} - 0.3	V
REFGN	Reference Gain Ratio	VRGN [1:0] = 00	—	1	—	V/V
		VRGN [1:0] = 01	—	0.5	—	V/V
		VRGN [1:0] = 10	—	0.75	—	V/V
		VRGN [1:0] = 11	—	0.25	—	V/V
$REFGN_{TC}$	Temperature drift of REFGN	VRGN [1:0] = 11	—	±10	—	ppm/°C
$VREF_{IN1}$	VREF1 from internal bandgap		—	1.2	—	V
$VREF_{IN2}$	VREF2 from internal bandgap		—	0.8	—	V
DC INPUT OFFSET						
DCSET	Input DC offset adjustment	DCSET [2:0] = 000	—	0	—	V
		DCSET [2:0] = 001	—	1/12.5VREF	—	V
		DCSET [2:0] = 010	—	2/12.5VREF	—	V
		DCSET [2:0] = 011	—	3/12.5VREF	—	V
		DCSET [2:0] = 100	—	4/12.5VREF	—	V

		DCSET [2:0] = 101	—	5/12.5VREF	—	V
		DCSET [2:0] = 110	—	6/12.5VREF	—	V
		DCSET [2:0] = 111	—	7/12.5VREF	—	V
$DCSET_{TC}$	Temperature drift of DCSET	+1/12.5VREF	—	10	—	ppm/°C
IDAC CURRENT SOURCES (IDAC1, IDAC2)						
IDACx	V_{comp} = 1.6V±0.02V	IDACx [6:0] = 0000000	—	8.0	—	µA
		IDACx [6:0] = 0000001	—	16.0	—	µA
		IDACx [6:0] = 0000010	—	25.0	—	µA
		IDACx [6:0] = 0000100	—	45.0	—	µA
		IDACx [6:0] = 0001000	-1%	80.0	+1%	µA
		IDACx [6:0] = 0010000	—	150.0	—	µA
		IDACx [6:0] = 0100000	—	300.0	—	µA
		IDACx [6:0] = 1000000	—	590.0	—	µA
		IDACx [6:0] = 1111111	—	1150.0	—	µA
V_{comp}	Compliance voltage		1.0	—	AVDD - 0.3	V
$IDAC_{TC}$	Temperature drift of IDAC	IDACx[6:0]_0001000	—	-60	—	ppm/°C
$IDAC_{Vcomp}$	Compliance voltage vs. IDAC		—	-2	—	%/V
BURN-OUT CURRENT						
I_{BODP}	Burn-out source current		4	5	6	µA
I_{BODN}	Burn-out sink current		3.5	4.5	5.5	µA
DIGITAL INPUTS/OUTPUTS (SDA, SCL, EOC)						
V_{OL}	Low-level output voltage	I_{SINK} = 4mA	—	—	0.4	V
V_{IL}	Low-level input voltage	SDA, SCL	0.7VDD	—	—	V
V_{IH}	Low-level output voltage	SDA, SCL	—	—	0.3VDD	V
I_{LEAK}	Input leakage current	SDA, SCL	—	—	1	µA
INTERNAL CLOCK OSCILLATOR						
F_{CLK}	Master clock frequency		-2%	1.024	+2%	MHz
T_{SUP}	Clock start-up time		1	—	—	ms
INTERNAL TEMPERATURE SENSOR						
	Temperature accuracy	-40 to 85℃	—	± 3	—	°C
	Current consumption		—	35	—	µA
DIGITAL VOLTAGE MONITOR						
	VDD DIVIDER		0.2	0.25	0.3	V/V
OPERATION TEMPERATURE						
T_A	Ambient temperature		-40	—	85	°C

I²C Digital Communication Timing Diagrams

Symbol	Conditions	Min	Max	Unit
f_{SCL}	SCL operating frequency	2.5	100	μs
f_{BUF}	Bus free time between STOP and START	1.3	—	us
t_{HDSTA}	Hold time after repeated START condition.	600	—	ns
t_{SUSTA}	Repeated START condition setup time	600	—	ns
t_{SUSTO}	STOP condition setup time	600	—	ns
t_{HDDAT}	Data hold time (*3)	0	—	ns
t_{HSUDAT}	Data setup time	100	—	ns
t_{LOW}	SCL clock low period	1300	—	ns
t_{HIGH}	SCL clock high period	600	—	ns
t_{VDAT}	Data valid time (*4)	—	900	ns
t_{FDA}	Data fall time	—	300	ns
t_R	Clock rise time	—	300	ns
t_F	Clock fall time	—	300	ns
Time out	Clock fall time	100	—	ms
$t_{RCClock/data}$	rise time for SCL=100KHz	—	1	μs

(*2) The host and device have the same VDD voltage. The voltages are based on statisctical analysis of samples tested during initial release.

(*3) The maximum t_{HDDAT} can be 0.9us for fast mode, and is less than the maximum t_{VDAT} by a transition time.

(*4) t_{VDAT}=time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worst). = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

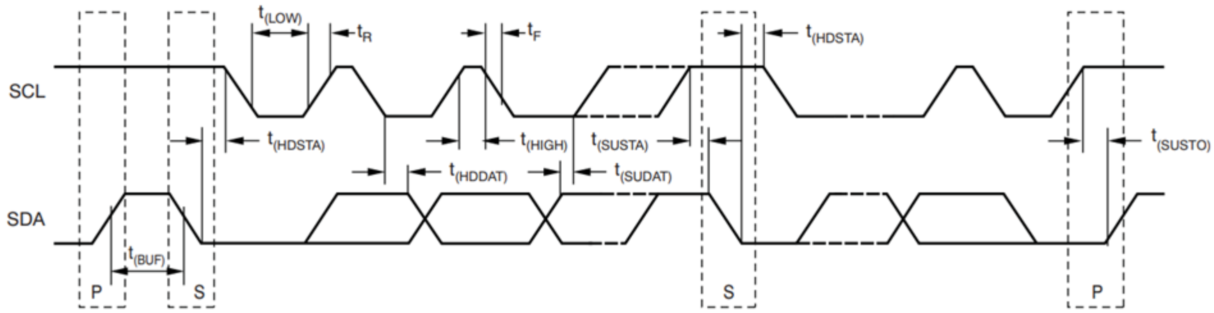


Figure 4 Time diagram of I²C protocol

Performance Characteristics

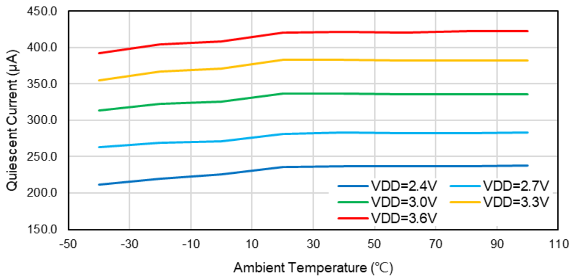


Figure 5 Current consumption vs. Temperature

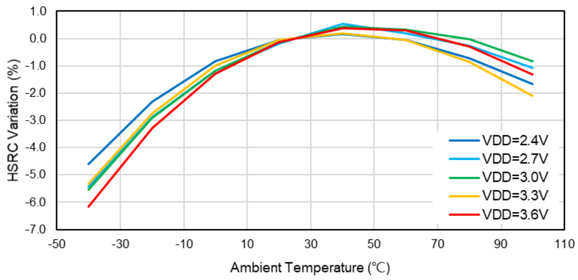


Figure 6 RC oscillator frequency vs. Temperature

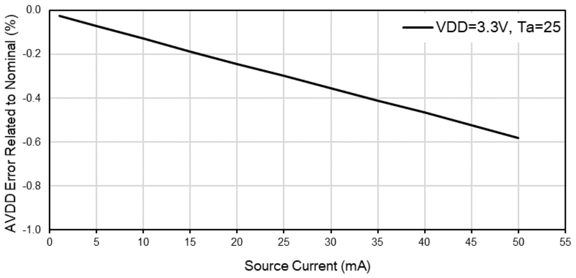


Figure 7 AVDD variation vs. Load current

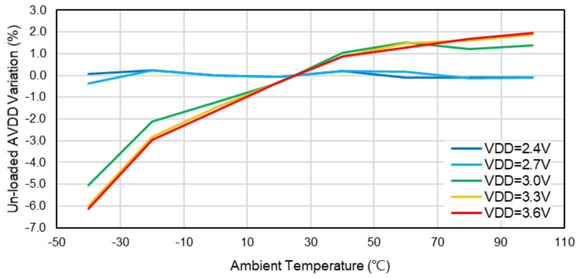


Figure 8 AVDD variation vs. Temperature

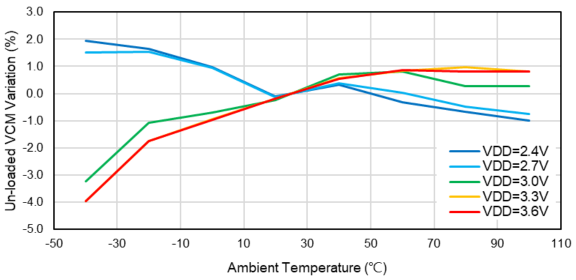


Figure 9 VCM variation vs. Temperature

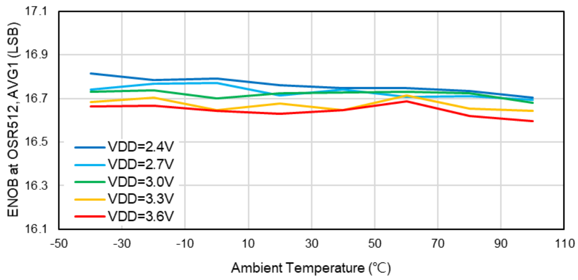


Figure 10 ENOB vs. Temperature

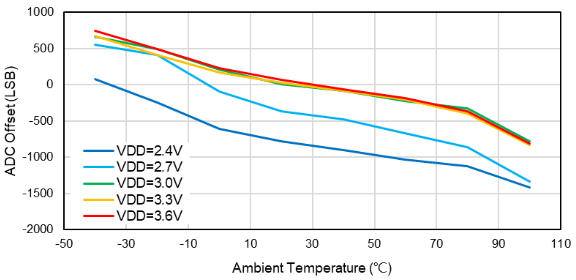


Figure 11 ADC Offset vs. Temperature

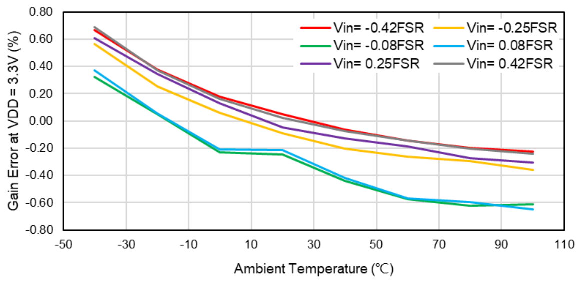


Figure 12 Gain Error vs. Temperature

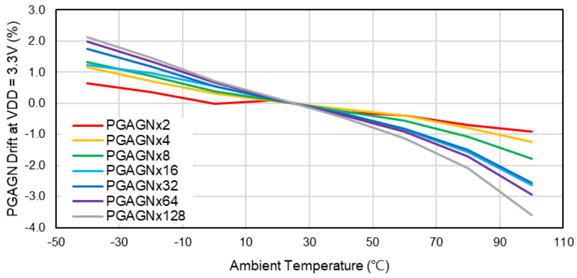


Figure 13 PGAGN vs. Temperature

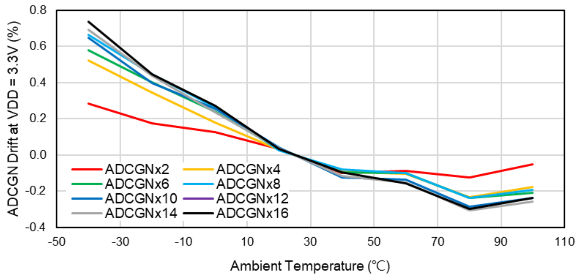


Figure 14 ADCGN vs. Temperature

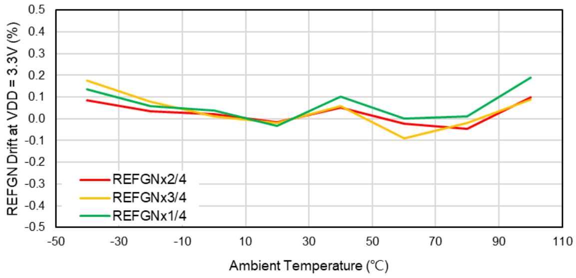


Figure 15 REFGN vs. Temperature

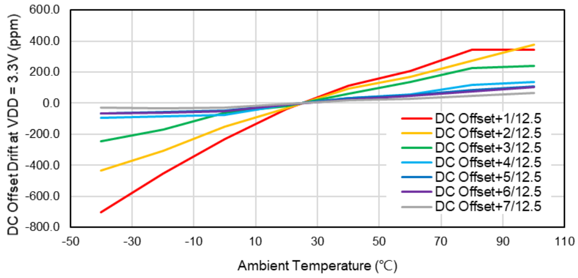


Figure 16 DC Offset vs. Temperature

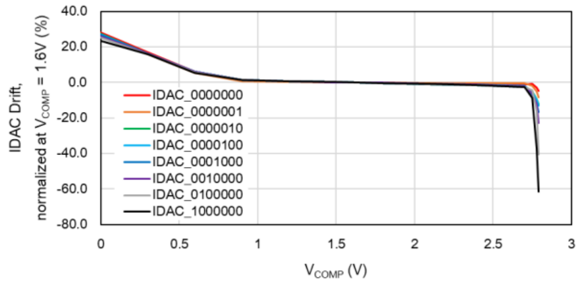


Figure 17 IDAC vs. V_{COMP}

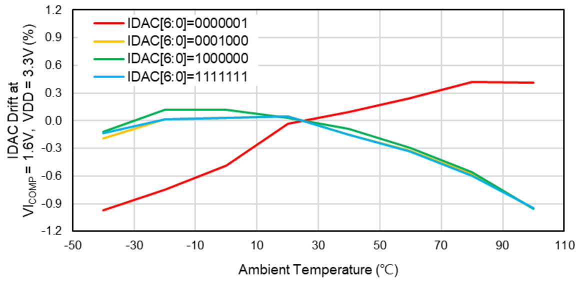


Figure 18 IDAC vs. Temperature

Multiplexer Connection Network

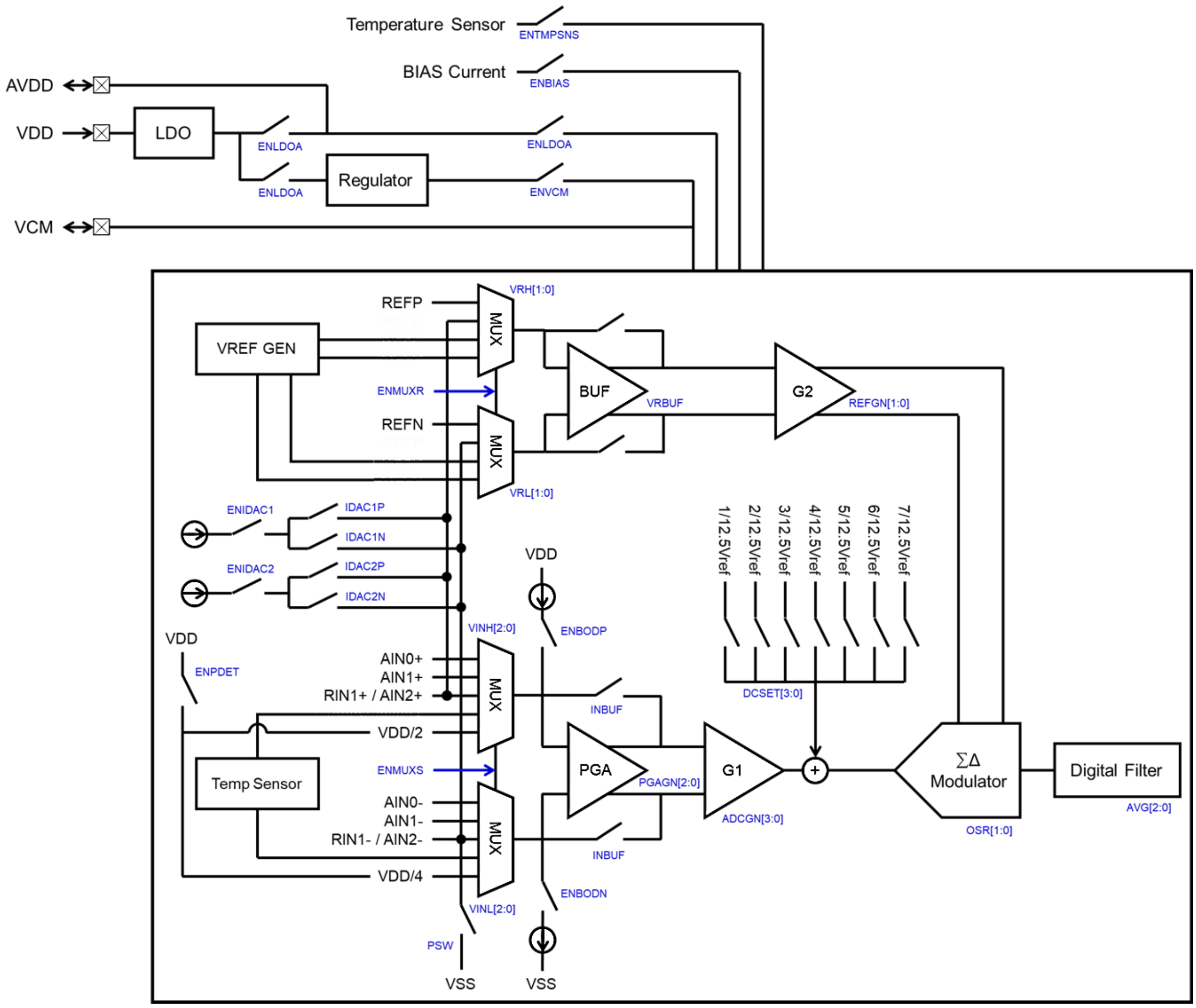


Figure 19 Multiplexer diagram of AFE6160A

Noise and Resolution

The performance of a sigma-delta ADC is typically specified in two forms: Root-Mean-Square (RMS) and Peal-to-Pead (PP) noise. Noise level decreases with longer oversampling intervals and lower gain setting. In practical, system designer requires a trade-off between Signal-to-Noise-Ratio (SNR) and Output Data Rate (ODR) to meet the application requirement.

The RMS noise can be expressed in term of Effective Number of Bits (ENOB), while and the PP noise is commonly specified as Noise-Free Bits resolution (NFB). The following equations illustrate the calculation of ENOB and NFB from the measured ADC.

$$RMS\ noise = \frac{FSR \times \sqrt{\frac{\sum_{i=0}^{N}(X_i - X_{avg})^2}{N}}}{2^n}, \qquad ENOB = Log_2\left(\frac{FSR}{RMS\ noise}\right)$$

$$PP\ noise = \frac{FSR \times (X_{max} - X_{min})}{2^n}, \qquad NFB = Log_2\left(\frac{FSR}{PP\ noise}\right)$$

The n represents the ADC resolution, X represents the ADC data and N is the amount of ADC data (recommend N > 1024). The AFE6160A is a differential, bipolar analog input sigma-delta converter with 24 bits 2's complements digital output, so the n = 24 and FSR is 2 x V_{REF}.

Table 1 to Table 4 summarize the ADC noise performance across different gain setting and ODR. Table 1 and Table 2 show the RMS noise (ENOB) and PP noise (NFB) using internal bandgap voltage, $VREF_{IN1}$, while Table 3 and Table 4 show the data using ratiometric measurement. With ratiometric measurement, the noise from supply of Device Under Test (DUT) can be effectively canceled. Moreover, the noise of internal reference and reference buffer are eliminated too, resulting in an improvement of ENOB by 1.5LSB. The AFE6160A also integrates a moving average digital filter, which further enhances noise performance without compromising the output data rate (ODR).

The 2nd gain amplifier, ADCGN, also amplifies the noise contributed from 1st gain amplifier, PGAGN. Therefore, ADCGN should primarily be used to increase the signal level when the maximum PGAGN setting is insufficient. Power consumption can be reduced without degrading the performance by enabling ADCGN while keeping PGAGN disabled. In this case, the RMS noise of PGAGN x16 (PGA enabled) and ADCGN x16 (PGA disabled) is the equivalent.

The recorded ADC amount is 2000 points, due to the statistical nature of noise, repeated noise measurements may yield higher or lower noise performance results.

Table 1 RMS noise in nV (ENOB).

VDD = 3.3V, Ta = 25°C, AINx+ = 1.654V, AINx- = 1.646V, Vref = $VREF_{IN1}$
ADCCH=1, VRBUF=1, PGACH=1, INBUF=1

OSR	AVG	SPS	PGAGN							
			x1	x2	x4	x8	x16	x32	x64	x128
128	1	2000	61702 (15.25)	31611 (15.21)	15850 (15.21)	8400 (15.12)	4950 (14.89)	3432 (14.42)	2577 (13.83)	2527 (12.86)
256	1	1000	42691 (15.78)	21474 (15.77)	10860 (15.75)	5936 (15.63)	3548 (15.37)	2482 (14.88)	2097 (14.13)	1936 (13.24)
512	1	500	29283 (16.32)	15082 (16.28)	8031 (16.19)	4482 (16.03)	2607 (15.81)	1858 (15.30)	1576 (14.55)	1781 (13.36)
1024	1	250	21030 (16.80)	10698 (16.78)	5693 (16.69)	3027 (16.60)	1962 (16.22)	1504 (15.61)	1317 (14.80)	1299 (13.82)
	2		16794 (17.12)	8833 (17.05)	4707 (16.96)	2545 (16.85)	1682 (16.44)	1281 (15.84)	1173 (14.96)	1216 (13.91)
	4		13176 (17.47)	6860 (17.42)	3590 (17.35)	2111 (17.12)	1350 (16.76)	1055 (16.12)	1027 (15.16)	929 (14.30)
	8		9924 (17.88)	5057 (17.86)	2787 (17.72)	1515 (17.60)	1019 (17.17)	880 (16.38)	859 (15.41)	741 (14.63)
	16		6683 (18.75)	3636 (18.33)	1926 (18.25)	1185 (17.95)	782 (17.55)	779 (16.56)	628 (15.87)	556 (15.04)
	32		5114 (18.84)	2326 (18.98)	1431 (18.68)	921 (18.31)	679 (17.75)	610 (16.91)	520 (16.14)	571 (15.00)
	64		3327 (19.46)	1921 (19.25)	949 (19.27)	775 (18.56)	889 (17.36)	475 (17.27)	459 (16.32)	552 (15.05)
	128		2182 (20.07)	1855 (19.30)	790 (19.53)	896 (18.35)	641 (17.84)	840 (16.45)	327 (16.81)	285 (16.01)

VDD = 3.3V, Ta = 25°C, AINx+ = 1.654V, AINx- = 1.646V, Vref = $VREF_{IN1}$
ADCCH=1, VRBUF=1, PGACH=1, INBUF=1, PGAGN=[000]

OSR	AVG	SPS	ADCGN				REFGN			
			x1	x4	x8	x16	x1	x0.75	x0.5	x0.25
128	1	2000	59340 (15.30)	19261 (14.93)	13454 (14.44)	9373 (13.97)	61704 (15.25)	51772 (15.09)	41681 (14.81)	27110 (14.43)
256	1	1000	41591 (15.82)	13610 (15.43)	9469 (14.95)	6873 (14.41)	42572 (15.78)	34063 (15.69)	25610 (15.52)	18157 (15.01)
512	1	500	29222 (16.63)	9727 (15.91)	6575 (15.48)	4789 (14.93)	30771 (16.25)	23805 (16.21)	17766 (16.04)	12438 (15.56)
1024	1	250	21321 (16.78)	6930 (16.40)	4664 (15.97)	3476 (15.40)	21105 (16.80)	16319 (16.75)	12177 (16.59)	8720 (16.07)
	2		17061 (17.10)	5799 (16.66)	3984 (16.20)	2967 (15.63)	18272 (17.00)	15158 (16.86)	10773 (16.77)	7569 (16.27)
	4		12484 (17.55)	4405 (17.06)	3193 (16.52)	2289 (16.00)	13292 (17.46)	10663 (17.37)	8243 (17.15)	5799 (16.66)
	8		9008 (18.02)	3560 (17.36)	2291 (17.00)	1975 (16.21)	9651 (17.92)	8129 (17.76)	6039 (17.60)	4192 (17.13)
	16		6307 (18.54)	2172 (18.08)	1709 (17.42)	1246 (16.88)	6967 (18.39)	5531 (18.31)	3852 (18.25)	2727 (17.75)
	32		4913 (18.90)	1592 (18.52)	1203 (17.93)	1022 (17.16)	4871 (18.91)	3999 (18.78)	2741 (18.74)	1837 (18.32)
	64		3450 (19.41)	1388 (18.72)	781 (18.55)	669 (17.77)	3161 (19.53)	3110 (19.14)	2220 (19.04)	1418 (18.69)
	128		2346 (19.96)	698 (19.71)	706 (18.70)	634 (17.85)	2460 (19.90)	2840 (19.27)	1457 (19.65)	974 (19.23)

Table 2 PP noise in nV (NFB).

VDD = 3.3V, Ta = 25°C, AINx+ = 1.654V, AINx- = 1.646V, Vref = $VREF_{IN1}$
ADCCH=1, VRBUF=1, PGACH=1, INBUF=1

OSR	AVG	SPS	PGAGN							
			x1	**x2**	**x4**	**x8**	**x16**	**x32**	**x64**	**x128**
128	1	2000	413132 (12.50)	205421 (12.51)	109577 (12.42)	67091 (12.13)	33045 (12.15)	26965 (11.44)	18185 (11.01)	16066 (10.19)
256	1	1000	298834 (12.97)	152206 (12.94)	73063 (13.00)	36657 (13.00)	23532 (12.64)	14667 (12.32)	13749 (11.41)	13251 (10.47)
512	1	500	199699 (13.55)	104856 (13.48)	60260 (13.28)	29933 (13.29)	16791 (13.13)	12937 (12.50)	10834 (11.76)	10974 (10.74)
1024	1	250	139475 (14.07)	67663 (14.11)	35906 (14.03)	22119 (13.73)	11677 (13.65)	10657 (12.78)	9059 (12.02)	8316 (11.14)
	2		113010 (14.37)	60010 (14.29)	30327 (14.27)	18185 (14.01)	12168 (13.59)	8681 (13.08)	7921 (12.21)	8250 (11.15)
	4		101566 (14.53)	43344 (14.76)	24712 (14.57)	15092 (14.28)	8628 (14.09)	6321 (13.53)	6706 (12.45)	6172 (11.57)
	8		60511 (15.28)	31829 (15.20)	19741 (14.89)	10282 (14.83)	5883 (14.64)	5320 (13.78)	4949 (12.89)	5803 (11.66)
	16		38767 (15.92)	26965 (15.44)	11587 (15.66)	7135 (15.36)	4622 (14.99)	4886 (13.91)	3507 (13.38)	3039 (12.59)
	32		26608 (16.46)	13375 (16.45)	8225 (16.15)	4381 (16.06)	4274 (15.10)	3317 (14.46)	2642 (13.79)	2482 (12.88)
	64		18597 (16.98)	9584 (16.93)	5651 (16.70)	3970 (16.21)	3988 (15.20)	2383 (14.94)	2740 (13.74)	2788 (12.72)
	128		10872 (17.75)	9012 (17.02)	3684 (17.31)	3541 (16.37)	2950 (15.63)	2803 (14.71)	1826 (14.33)	1272 (13.85)

VDD = 3.3V, Ta = 25°C, AINx+ = 1.654V, AINx- = 1.646V, Vref = $VREF_{IN1}$
ADCCH=1, VRBUF=1, PGACH=1, INBUF=1, PGAGN=[000]

OSR	AVG	SPS	ADCGN				REFGN			
			x1	**x4**	**x8**	**x16**	**x1**	**x0.75**	**x0.5**	**x0.25**
128	1	2000	373077 (12.65)	131607 (12.15)	96273 (11.61)	73528 (10.99)	389099 (12.59)	360489 (12.29)	278664 (12.07)	186253 (11.65)
256	1	1000	299549 (12.97)	99564 (12.56)	59777 (12.29)	51588 (11.51)	296688 (12.98)	234962 (12.90)	154853 (12.92)	114906 (12.35)
512	1	500	205135 (13.51)	61798 (13.25)	44954 (12.70)	33313 (12.14)	222731 (13.40)	175524 (13.32)	125027 (13.23)	84829 (12.79)
1024	1	250	144339 (14.02)	47314 (13.63)	31954 (13.20)	23568 (12.64)	155354 (13.92)	98491 (14.16)	89979 (13.70)	58544 (13.32)
	2		116158 (14.33)	40734 (13.85)	28914 (13.34)	20447 (12.84)	130033 (14.17)	107718 (14.03)	73385 (14.00)	55969 (13.39)
	4		88692 (14.72)	32651 (14.17)	19294 (13.92)	15485 (13.24)	83113 (14.82)	69845 (14.65)	58150 (14.33)	41270 (13.83)
	8		55361 (15.40)	21493 (14.77)	13983 (14.39)	12463 (13.55)	57364 (15.35)	48280 (15.19)	42915 (14.77)	29683 (14.30)
	16		39768 (15.88)	16022 (15.19)	9727 (14.91)	8458 (14.11)	43917 (15.74)	34869 (15.66)	25392 (15.53)	17667 (15.05)
	32		27895 (16.39)	9191 (15.99)	6974 (15.39)	4962 (14.88)	29182 (16.33)	26071 (16.08)	16952 (16.11)	12338 (15.57)
	64		18883 (16.96)	7153 (16.36)	4256 (16.11)	4318 (15.08)	17595 (17.06)	16415 (16.74)	11730 (16.64)	7904 (16.21)
	128		10586 (17.79)	3541 (17.37)	3076 (16.57)	3469 (15.40)	11301 (17.70)	11802 (17.22)	6509 (17.49)	4756 (16.94)

Table 3 RMS noise in nV (ENOB).

VDD = 3.3V, Ta = 25°C, Ratiometric Measurement ADCCH=1, VRBUF=0, PGACH=1, INBUF=1										
OSR	**AVG**	**SPS**	**PGAGN**							
			x1	**x2**	**x4**	**x8**	**x16**	**x32**	**x64**	**x128**
128	1	2000	36793 (15.99)	15016 (16.29)	8085 (16.18)	4178 (16.13)	2358 (15.96)	1674 (15.45)	1367 (14.74)	1296 (13.82)
256	1	1000	14596 (17.23)	7562 (17.28)	4069 (17.17)	2238 (17.03)	1505 (16.60)	1127 (16.02)	1060 (15.11)	915 (14.32)
512	1	500	9278 (17.98)	5108 (17.84)	2780 (17.72)	1613 (17.50)	1060 (17.11)	781 (16.55)	671 (15.77)	636 (14.85)
1024	1	250	6489 (18.50)	3487 (18.39)	1923 (18.25)	1133 (18.01)	757 (17.60)	569 (17.01)	487 (16.23)	454 (15.33)
	2		5618 (18.70)	2944 (18.64)	1629 (18.49)	982| (18.22)	606 (17.92)	484 (17.24)	414 (16.47)	392 (15.55)
	4		4267 (19.10)	2206 (19.05)	1243 (18.88)	726 (18.66)	496 (18.21)	336 (17.77)	304 (16.91)	280 (16.03)
	8		2941 (19.64)	1602 (19.51)	921 (19.31)	541 (19.08)	349 (18.71)	263 (18.12)	236 (17.28)	217 (16.40)
	16		2187 (20.07)	1233 (19.89)	649 (19.82)	389 (19.56)	249 (19.20)	192 (18.57)	177 (17.69)	170 (16.75)
	32		1508 (20.60)	789 (20.54)	399 (20.52)	247 (20.21)	156 (19.88)	151 (18.92)	122 (18.23)	137 (17.06)
	64		998 (21.20)	474 (21.27)	313 (20.87)	193 (20.57)	143 (20.00)	102 (19.49)	85 (18.75)	94 (17.61)
	128		784 (21.55)	472 (21.28)	180 (21.67)	133 (21.11)	100 (20.52)	95 (19.58)	88 (18.71)	74 (17.96)

VDD = 3.3V, Ta = 25°C, Ratiometric Measurement ADCCH=1, VRBUF=0, PGACH=1, INBUF=1, PGAGN=[000]										
OSR	**AVG**	**SPS**	**ADCGN**				**REFGN**			
			x1	**x4**	**x8**	**x16**	**x1**	**x0.75**	**x0.5**	**x0.25**
128	1	2000	36143 (16.02)	11022 (15.73)	7367 (15.31)	5567 (14.72)	34647 (16.08)	25225 (16.12)	38779 (14.92)	16422 (15.16)
256	1	1000	14144 (17.37)	6417 (16.51)	4828 (15.92)	3728 (15.30)	14507 (17.34)	11522 (17.25)	9962 (16.88)	8931 (16.04)
512	1	500	9082 (18.01)	4476 (17.03)	3420 (16.42)	2656 (15.79)	9448 (17.95)	8094 (17.76)	6686 (17.45)	6171 (16.57)
1024	1	250	6796 (18.43)	3163 (17.53)	2527 (16.86)	1856 (16.30)	6432 (18.51)	5412 (18.34)	4819 (17.93)	4187 (17.13)
	2		5392 (18.76)	2615 (17.81)	2042 (17.16)	1608 (16.51)	5512 (18.73)	4634 (18.57)	3945 (18.21)	3609 (17.34)
	4		4247 (19.11)	1974 (18.21)	1541 (17.57)	1259 (16.86)	4201 (19.12)	3546 (18.95)	3231 (18.50)	2732 (17.74)
	8		3053 (19.58)	1479 (18.63)	1148 (18.00)	891 (17.36)	2873 (19.67)	2447 (19.49)	2194 (19.06)	1920 (18.25)
	16		2472 (19.89)	1013 (19.18)	820 (18.48)	606 (17.92)	2033 (20.17)	2004 (19.78)	1517 (19.59)	1400 (18.71)
	32		2063 (20.15)	1068 (19.10)	797 (18.52)	609 (17.91)	1604 (20.51)	1241 (20.47)	1243 (19.88)	1136 (19.01)
	64		1067 (21.10)	545 (20.07)	454 (19.33)	308 (18.90)	1125 (21.02)	927 (20.89)	859 (20.41)	724 (19.66)
	128		893 (21.36)	334 (20.78)	281 (20.03)	223 (19.36)	734 (21.64)	767 (21.16)	513 (21.16)	440 (20.38)

Table 4 PP noise in nV (NFB).

VDD = 3.3V, Ta = 25°C, Ratiometric Measurement
ADCCH=1, VRBUF=0, PGACH=1, INBUF=1

OSR	AVG	SPS	PGAGN							
			x1	x2	x4	x8	x16	x32	x64	x128
128	1	2000	215149 (13.45)	102425 (13.52)	57220 (13.36)	28467 (13.36)	16522 (13.15)	12589 (12.54)	8494 (12.11)	9361 (10.97)
256	1	1000	103712 (14.50)	52357 (14.48)	25213 (14.54)	17810 (14.04)	10148 (13.85)	8163 (13.17)	8603 (12.09)	5799 (11.66)
512	1	500	66376 (15.14)	35262 (15.05)	18811 (14.96)	11784 (14.64)	7010 (14.39)	6679 (13.46)	5069 (12.85)	4416 (12.05)
1024S	1	250	40054 (15.87)	22459 (15.71)	13733 (15.42)	7921 (15.21)	5695 (14.68)	3549 (14.37)	3688 (13.31)	2965 (12.63)
	2		38338 (15.93)	19598 (15.90)	10693 (15.78)	6330 (15.53)	3970 (15.21)	3143 (14.54)	3138 (13.54)	2971 (12.62)
	4		27895 (16.39)	14949 (16.29)	8225 (16.15)	4435 (16.05)	3228 (15.50)	1962 (15.22)	2025 (14.18)	1988 (13.20)
	8		20456 (16.84)	9084 (17.01)	5293 (16.79)	3219 (16.51)	2387 (15.94)	1739 (15.40)	1498 (14.61)	1243 (13.88)
	16		13590 (17.43)	6866 (17.42)	4005 (17.19)	2342 (16.97)	1591 (16.52)	1198 (15.93)	1100 (15.06)	980 (14.22)
	32		9298 (17.98)	4220 (18.12)	2468 (17.89)	1448 (17.66)	1055 (17.12)	894 (16.36)	729 (15.65)	895 (14.35)
	64		6008 (18.61)	2789 (18.71)	1824 (18.33)	1073 (18.09)	706 (17.70)	519 (17.14)	393 (16.54)	477 (15.26)
	128		3719 (19.30)	2217 (19.05)	1037 (19.14)	679 (18.75)	510 (18.17)	380 (17.59)	418 (16.45)	358 (15.68)

VDD = 3.3V, Ta = 25°C, Ratiometric Measurement
ADCCH=1, VRBUF=0, PGACH=1, INBUF=1, PGAGN=[000]

OSR	AVG	SPS	ADCGN				REFGN			
			x1	x4	x8	x16	x1	x0.75	x0.5	x0.25
128	1	2000	231171 (13.34)	73814 (12.99)	52929 (12.47)	38767 (11.92)	258636 (13.18)	167370 (13.39)	225449 (12.38)	94414 (12.63)
256	1	1000	92983 (14.66)	40126 (13.87)	33242 (13.13)	25517 (12.52)	86546 (14.76)	81861 (14.42)	70667 (14.05)	57364 (13.35)
512	1	500	57220 (15.36)	29576 (14.31)	21440 (13.77)	17801 (13.04)	62227 (15.24)	56863 (14.95)	43416 (14.75)	44882 (13.71)
1024	1	250	41914 (15.81)	23210 (14.66)	17005 (14.11)	14314 (13.36)	47636 (15.62)	35512 (15.63)	35477 (15.05)	30148 (14.28)
	2		35620 (16.04)	18847 (14.96)	14162 (14.37)	11659 (13.65)	42343 (15.79)	33474 (15.71)	32258 (15.18)	20885 (14.81)
	4		26321 (16.48)	15271 (15.26)	11122 (14.72)	8377 (14.13)	29182 (16.33)	25105 (16.13)	20814 (15.82)	18418 (14.99)
	8		21029 (16.80)	11158 (15.71)	7975 (15.20)	5686 (14.69)	20027 (16.87)	19097 (16.52)	13661 (16.42)	12660 (15.53)
	16		16165 (17.18)	6187 (16.57)	4631 (15.98)	3514 (15.38)	15163 (17.27)	10407 (17.40)	9155 (17.00)	8047 (16.19)
	32		11730 (17.64)	7081 (16.37)	4900 (15.90)	3666 (15.32)	10157 (17.85)	7617 (17.85)	7081 (17.37)	6258 (16.55)
	64		6008 (18.61)	3290 (17.48)	2289 (17.00)	1681 (16.45)	6294 (18.54)	4292 (18.68)	4363 (18.07)	3648 (17.33)
	128		4578 (19.00)	1681 (18.45)	1341 (17.77)	1082 (17.08)	3433 (19.42)	3755 (18.87)	2789 (18.71)	2253 (18.02)

System Description

Overview

The AFE6160A is a low-noise, low power 24-bit sigma-delta ADC integrating many features to reduce Bill of Material (BOM) cost of the system for sensor signal measurement. An on-chip temperature sensor and power supply monitor record the condition of environment without extra sensors.

The device provides two precision current sources and one voltage source for sensor excitation, and a built-in open/short diagnostic function. Three differential signal input channels and two differential reference input channels give flexible measurement configuration.

A two-stage signal amplifier allows signal amplification up to x2048, while a reference gain amplifier can shrink the Full-Scale Range (FSR) of signa-delta ADC, effectively achieving x8192 overall signal amplification. A Built-in DC offset ensure that the input signal is at the proper level of FSR for ADC acquisition.

The AFE6160A supports four configurable ODR and a moving-average digital filter, the digital filter can enhance the performance of SDADC without reducing ODR. Two conversion mode are available: one-shot conversion and continuous conversion mode. To access the valid and latest data, reading should be performed through standard I²C interface after the EOC signal is asserted.

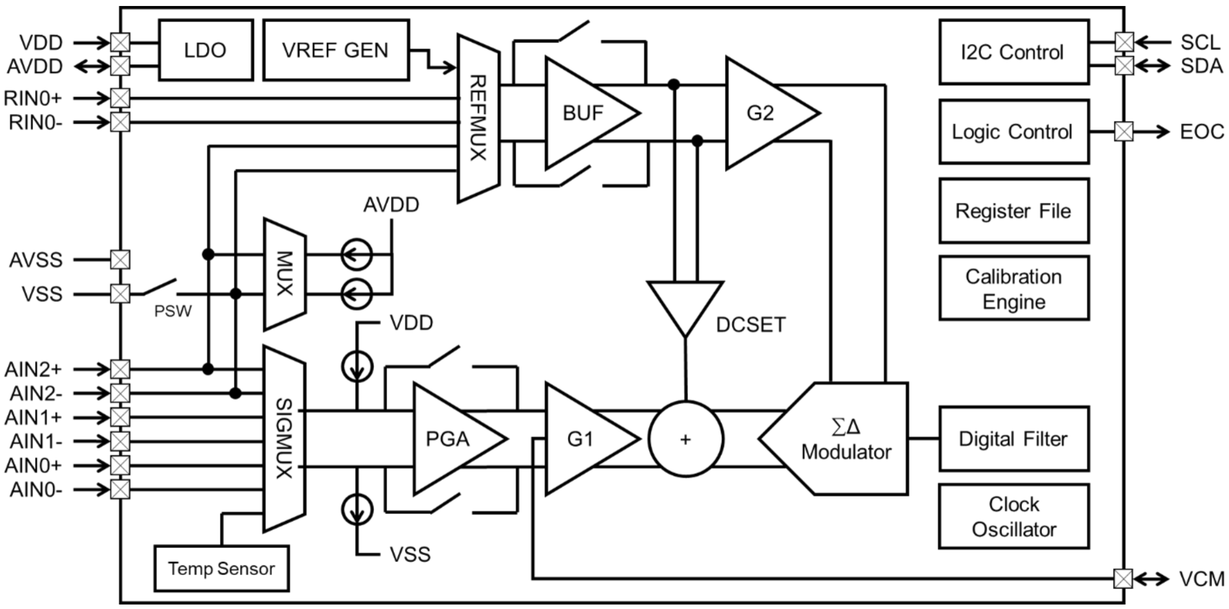


Figure 20 Function block diagram of AFE6160A

Power Supplies and Monitor

The AFE6160A has one digital power supply input, VDD, one analog power supply, AVDD, and one common mode voltage supply, VCM. VDD regulates the AVDD and powers the digital section of the AFE6160A, including clock generator and digital processing circuits AVDD regulates the VCM and powers other analog section of AFE6160A such as PGA and sigma-delta ADC. In addition, AVDD can be used as a voltage source for external sensor excitation, the loading ability is about 30mA.

An external voltage power can be applied to AVDD, according to the Figure 19, the external AVDD must be greater than internal AVDD, the rail range of PGAGN, ADCGN and the input range of external reference could be benefited.

AFE6160A builds-in a supply voltage monitor function, the VDD voltage will be attenuated internally by one-fourth and applied to the channel 4 of signal multiplexer. This function can monitor the voltage variation from power supply during the measurement.

Reset

The AFE6160 only supports software reset, the device could be reset by sending a fixed I^2C pattern. The device responds to the two-wire general call address (0000 000) if the LSB bit is 0. The device acknowledges the general call address and responds to commands in the 2^{nd} byte. If the 2^{nd} byte is 0000 0110, the AFE6160A resets the internal registers to default values.

Digital Communication Interface

The communication interface of AFE6160A is compatible with standard I^2C, the speed of SCL supports up to 1MHz fast mode (SDA and SCL timing requirements are followed the standard). AFE6160A operates as a slave device, a controller or master device could access the register data via I^2C protocol.

Both SDA and SCL lines use open-drain I/O mode, requiring an external pull-up resistor to read the right status. Schmitt triggers are implemented on both SDA and SCL input to minimize the effects of signal fluctuations caused by noisy environment.

If the SCL line is held at low level by the master more than 16ms (typ.) after a START condition, the AFE6160A reset its internal I^2C state machine to prevent the bus hang-up. After reset, the SDA would be released and the device waits for the next START condition.

I^2C communication becomes available 5ms after Power on Reset (POR) or software reset. During the 5ms period, if the level of AVDD is exceed 0.5V, the I^2C interface enters the protection mode and address matching would always NACK. To exit protection mode, hold the level of AVDD below 0.5V for at least 5ms.

Register File

The built-in register file can be configured to control the functions of AFE6160A. After POR or software reset, the registers will be set to default value.

Time Diagram & Slave Address

In accordance with standard I²C protocol, a slave device requires a 7-bit I²C address to be recognized on the I²C bus. During communication, the 8th bit of slave address indicates the transfer direction (read or write). The AFE6160A uses a fixed 7-bit I²C address 1001000 (or 0x48H) and Figure 21 and Figure 22 illustrate the time diagram of I²C timing diagrams for read and write operations.

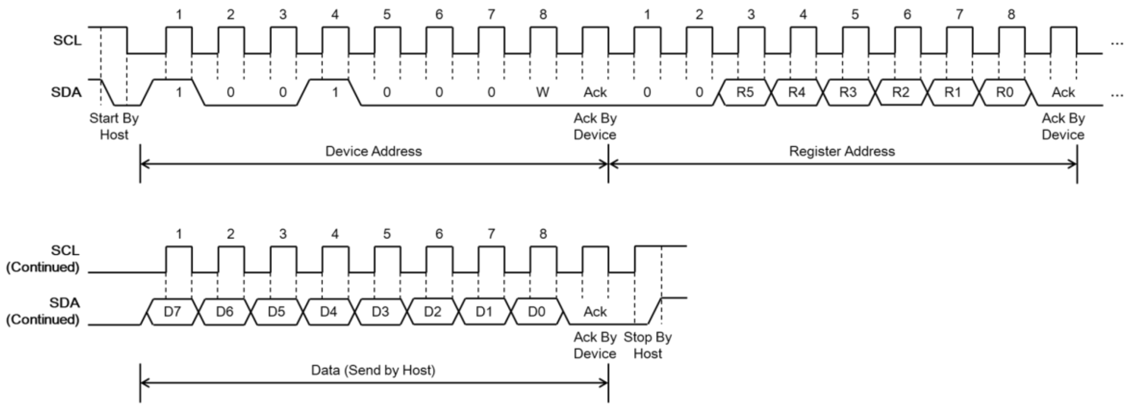


Figure 21 Two-wire timing diagram for Write Single Byte format

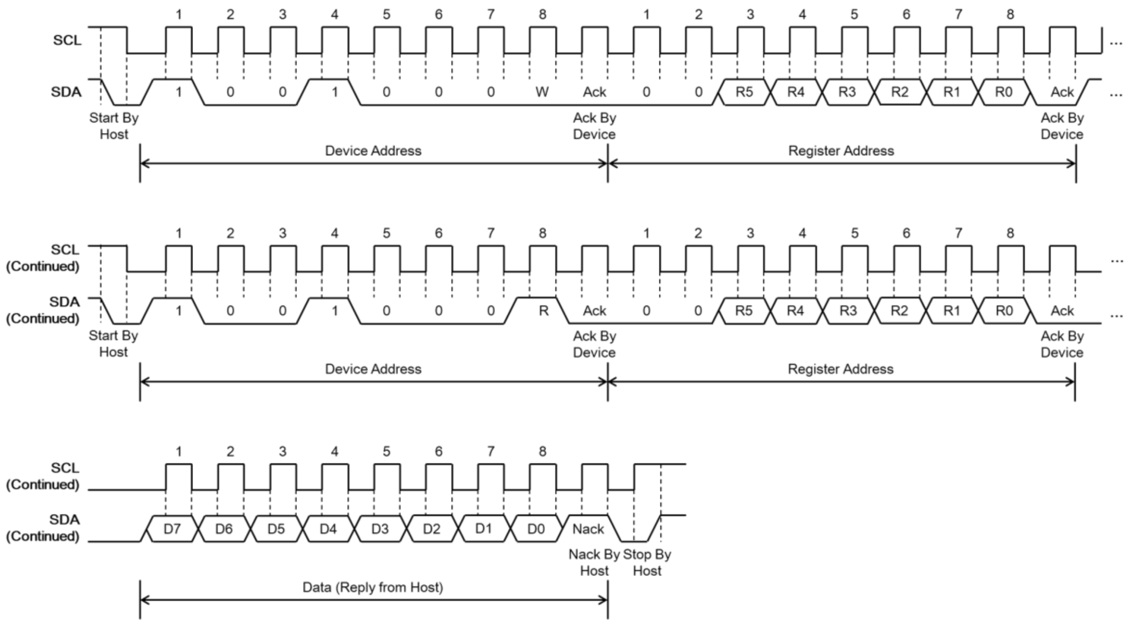


Figure 22 Two-wire timing diagram for Read Single Byte format

Signal and Reference Multiplexer

Signal Multiplexer

The AFE6160A is 3-channel data acquisition system suitable for applications requiring high channel density such as industrial process control, portable medical devices and automated test equipment. By multiplexer, multiple sensors signal can be measured with a single sigma-delta ADC, reducing the system cost.

Setting bit ENMUXS to 1 enables the signal multiplexer. There're two signal multiplexers, one for the positive analog input, VINH, and one for the negative analog input, VINL. Channel 0, 1 and 2 represent input of AIN0, AIN1 and AIN2 respectively. Channel 3 is input of internal temperature sensor and channel 4 is power monitor input. Differential input between AIN0+ and AIN1- is configurable by proper setting, however, such configuration isn't recommended.

The AIN2 analog input has multiple functions, 1. signal input channel 2 (AIN2+, AIN2-), 2. reference input channel 1 (RIN1+, RIN1-) and 3. IDAC output. Moreover, the compliance voltage of IDAC can be configured as signal or reference input.

Reference Multiplexer

The reference voltage can be select from two external reference inputs and two internal reference sources, providing flexibility for data acquisition. For example, an AVDD-excited sensor can be measured ratiometrically, while other sensor can be measured through internal reference voltage – all with a single AFE6160A.

Setting bit ENMUXR to 1 enables the reference multiplexer. There're two reference multiplexers, one for the analog input, VRH, and one for the negative analog input, VRL. Channel 0 (RIN0+, RIN0-) is a dedicated external reference input, while channel 1 (RIN1+, RIN1-) is a multi-function external reference input. Channel 3 and 4 are internal bandgap reference supply $VREF_{IN1}$ and $VREF_{IN2}$ respectively. When the internal reference voltage is selected, it is recommended to connect the external reference pins to analog ground to minimize the multiplexer-coupled noise.

A reference buffer (bit VRBUF) is provided to prevent the distortion when a unknow or high impedance external reference input is applied. Enabling the buffer would decrease ENOB by ~0.5 LSB due to buffer-induced noise, moreover, the rail range of reference buffer is limited to AVDD-0.6V to AVSS.

When using the internal reference, enabling reference buffer improves the performance of sigma-delta ADC by filtering high-frequency noise from bandgap voltage. For the external reference, if the output impedance of source input is negligible compared to the input impedance of AFE6160A reference (2MΩ), the buffer can be disabled to achieve optimal sigma-delta ADC performance, and the limitation of rail range is from AVDD to AVSS.

Signal Amplification and DC Offset Adjustment

Instrumentation Amplifier

The 1st stage gain amplifier of AFE6160A is a programmable instrumentation amplifier, PGAGN. This function can be enabled by setting bit INBUF to 1 and an unknown or high impedance signal input would not be distorted.

The maximum input voltage (V_{AINx}) is AVDD-0.6V and the common mode voltage of differential input must be greater than 0.3V. The differential signal input can be amplified by the low-noise PGA with eight programmable gain values, x1, x2, x4, x8, x16, x32, x64 and x128. A simplified PGAGN diagram is shown in Figure 23, the amplified signal should remain within the output rail range: AVDD-0.1V (non-inverting output) and AVSS (inverting output).

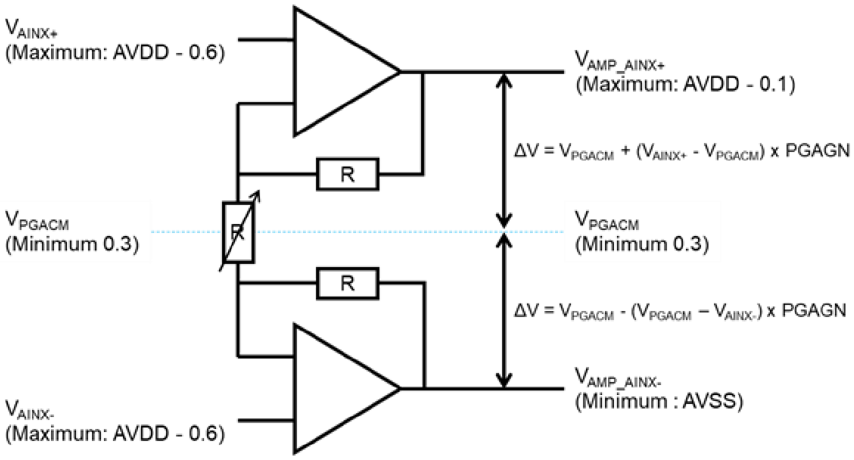


Figure 23 Simplified diagram of instrumentation amplifier, PGAGN.

Operational Amplifier

The 2nd stage gain amplifier of AFE6160A is a programmable operational amplifier, ADCGN. This amplifier is always enabled and the default gain is x1. Moreover, the differential signal can be enhanced up to x16 with lower power consumption by disable PGA.

The input rail range of ADCGN is from AVDD to AVSS and is connected to the output of PGA. The differential signal input can be amplified with sixteen programmable gain values, x1~x16. A simplified ADCGN diagram is shown in Figure 24, the amplified signal should remain within the output rail range: AVDD-0.6V (non-inverting output) and AVSS+0.4V (inverting output).

Another programmable operational amplifier, REFGN, is used to effectively amplified the signal by scaling the reference input. The differential reference input can be amplified with four programmable gain values x1, x0.75, x0.5 and x0.25, therefore, the signal can be amplified up to x8192 effectively. However, if required effective gain setting exceeds x1024, an external operation amplifier is recommended to pre-amplify the signal before AFE6160A to achieve optimal performance of sigma-delta ADC.

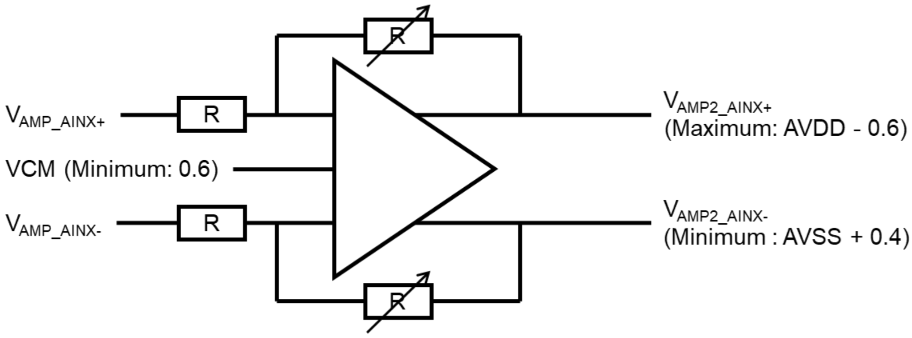


Figure 24 Simplified diagram of operational amplifier, ADCGN.

DC Offset

The AFE6160A offers a programmable DC offset voltage to shift differential input to properly level of FSR (Typical 0.8FSR). This function is enabled when the bit DCSET is not 0, Seven offset voltage are available (1/12.5VREF to 7/12.5VERF) and the VREF is determined by reference multiplexer.

Figure 25 shows the simplified diagram of DC offset, the non-inverting input is increased by half of DC offset while inverting input is decreased by half of DC offset. The output rail range is AVDD-0.3V (non-inverting output) to AVSS+0.3V (inverting output), if the DC offset is disabled, the output rail range would be the same as ADCGN.

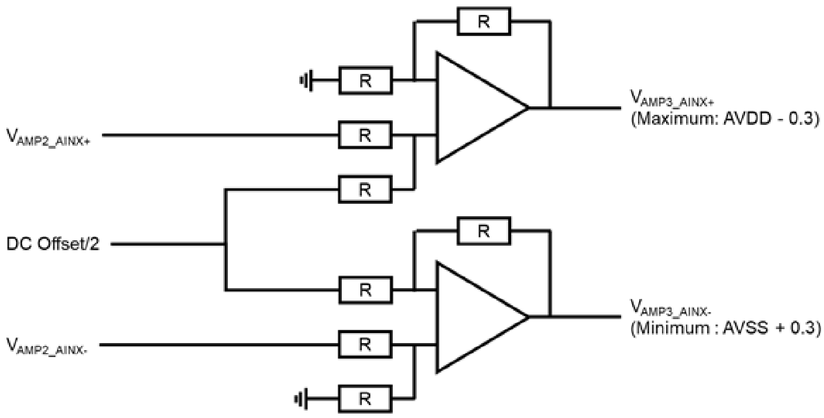


Figure 25 Simplified diagram of DC offset.

Input Impedance

The input impedance of AFE6160A has strong dependent on gain setting, as summarized in Table 5. As mentioned before, enabling PGA can significantly increase the input impedance, providing better tolerance to unknow impedance. The input impedance decreases as the PGAGN or ADCGN increases, in particular, the reduction in input impedance can be roughly estimated from the gain setting of ADCGN.

Table 5 Input impedance of different gain setting

PGAGN	ADCGN	Impedance (MΩ)	PGAGN	ADCGN	Impedance (MΩ)
X	x1	2.72	x1	x1	1500
X	x4	0.68	x2	x1	450
X	x8	0.34	x4	x1	150
X	x16	0.17	x8	x1	40
			x16	x1	15
			x32	x1	4
			x64	x1	1
			x128	x1	0.5

Clock Oscillator

A well-calibrated (±2%) 1.024MHz internal oscillator, HSRC, serving as the primary clock source of AFE6160A. The clock of sigma-delta ADC is fixed at HSRC/4, and an additional programmable divider (2, 4, 8, 16, 32) is available to further reduce clock of sigma-delta ADC. Usually, for a given ODR, the large Over Sampling Rate (OSR) with a faster clock has better performance than small OSR with slower clock.

ADC Conversion

ADC Output Format

Since the sigma-delta ADC is an oversampling analog input, the requirement of transition band of anti-aliasing filter is more relax than brick-wall stop band filter in Nyquist-rate data converters. In most applications, a simple single-pole RC filter is sufficient at the input pins, AIN0, AIN1 and AIN2.

The AFE6160A provides a 24-bit, 2's complements digital output. An ideal ADC code for a given differential signal input within the FSR can be calculated by the equation shown in Figure 26. When the input signal is less than or equal to -VERF, the ADC code will be 0x800000H. When the input signal is greater than or equal to +VERF, the ADC code will be 0x000000H rather than 0x7FFFFFH.

It should be noticed that the ADC code described here and Figure 26 refer to the uncalibrated ADC (DATA_R) rather than calibrated ADC (DATA). Moreover, an abnormal ADC output might occur when the amplified signal is exceeded the output rail range of PGAGN, ADCGN or DC Offset.

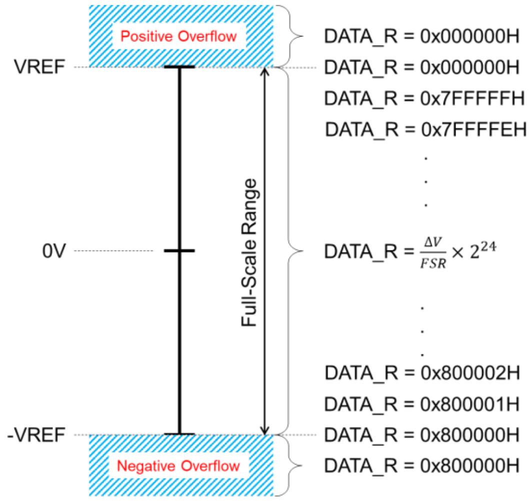


Figure 26 Illustration of ADC output.

End Of Conversion

The EOC pin is an open-drain output I/O and requires an external pull-up resistor to read the right status. When an ADC conversion is complete, EOC would be pulled-low by AFE6160A. EOC will remain low level even if after the next conversion is complete, only an "EOC Clear" operation can release low level of EOC.

Several operations automatically perform an "EOC Clear", such as,

- Disabling or enabling ADC (bit ENADC)
- Change OSR
- Change input or reference channel
- Change size of moving average buffer
- Disabling or enabling sensor fault detection (bit ENBODP, ENBODN)
- Read register "INSTA"

Among this, only reading register "INSTA" clears EOC without re-initializing the sigma-delta ADC (Don't need the ADC settling time) so, the "EOC Clear" is mainly using this command.

Output Data Rate

The AFE6160A supports four Over Sampling Rate (OSR) setting: 128, 256, 512 and 1024. With a 256kHz sigma-delta ADC clock, the ODR can be programmed to 2kHz, 1kHz, 500Hz and 250Hz respectively.

$$Conversion\ Period\ (ms) = \frac{OSR}{Speed\ of\ SDADC}, \quad ODR\ (kHz) = \frac{1}{Conversion\ Period}$$

Due to the nature of sigma-delta ADC, the first conversion after re-configuring the AFE6160A requires longer period compared to subsequent conversions. This additional period is called ADC settling time, the settling time can be estimated by following equation.

$$ADC\ Settling\ Time\ (ms) = \frac{256 + 3 \times OSR}{Speed\ of\ SDADC} + \frac{OSR}{Speed\ of\ SDADC} \times (AVG - 1)$$

The constant 256 represents pre-setting time of AFE6160A. The AFE6160A requires three times the OSR to get the first valid converted result. When a moving-average filter is enabled, the first converted data would be updated (EOC is pulled-low) after the buffer is filled.

Moving-Average Filters

Besides the decimation filter built-in the sigma-delta ADC, the AFE6160A incorporates a moving-average filter to improve the performance without reducing the ODR. Eight moving average buffer sizes are programmable: 1, 2, 4, 8, 16, 32, 64 and 128.

For example, if the ODR is 2kHz, setting size of moving-average buffer to 128 can enhance the performance of sigma-delta ADC (ENOB) by 4bits LSB.

Factory Calibration

During manufacturing, the AFE6160A is factory-calibrated to minimize the offset error and gain error at room temperature. The calibration parameters are stored in One-Time Programmable (OTP) memory, so the re-calibration of AFE6160A is not possible. If a measurement system experiences higher input impedance mis-match or system offset from temperature or environment variations, please contact ESMT if requiring the cus-tomized calibration.

Operation Mode

Continuous conversion mode

In continuous conversion mode, the AFE6160A would convert the ADC continuously under proper setting of register file. In this mode, only the first converted ADC requires ADC settling time, the subsequent conversion follow the ODR.

One-shot conversion mode

In One-Show Conversion Mode (OSM), the AFE6160A stops converting after current ADC conversion is com-plete. This function can be implemented by setting ENADC to 0 after an EOC interrupt. The next conversion should be triggered by setting the ENADC to 1, each conversion period corresponds to ADC settling time.

Standby mode

The standby mode provides lowest current consumption, in this mode, all the analog circuit blocks including HSRC, sigma-delta ADC, PGA, LDOA, VCM and TMPSNS are disabled. In addition, the level of communica-tion pin SDA, SCL and EOC should be held at high. The device can be woken up by writing proper setting of register file via I^2C.

IDAC Excitation Current Sources

The AFE6160A includes two independent, grounded-available current sources, IDAC1 and IDAC2, to excite an external sensor such as resistive bridge, thermistor and RTD. Each IDAC output can be programmed form 8μA to 1.150mA via the register setting. Each IDAC output can be routed to pin AIN2+ or AIN2-, so the maximum output current at pin AIN2+ or AIN2 is 2.3mA.

The compliance voltage strongly affects IDAC output. Due to the IDACs are driven by AVDD, if the compliance voltage is close to AVDD, the output current decrease significantly. Moreover, if the compliance voltage is less than 1V, the output of IDAC would increase due to the characteristics of MOS. The IDACs are factory-calibrated at 1.6V compliance voltage and it is recommended to operate the IDACs within 1.0V ~ AVDD-0.4V.

Sensor Diagnostic

For harsh application environment, safety is the highest priority and an internal diagnostic becomes important part of the industry requirements. The AFE6160A integrates a DUT open/short diagnostic function without extra components, helping save BOM cost.

Open-circuit detection

The AFE6160A provides a weak burn-out source current from VDD to pin AIN0+, AIN1+ or AIN2+ depending on the setting of signal multiplexer. If the DUT is in an open-circuit condition, the positive node of analog signal is pulled-up to VDD, while the negative node is floating. As the result, ADC output would become larger than normal value or even overflow. By proper setting of register file, the bit SNSH would be set to 1 to indicate sensor open-circuit situation.

Short-circuit detection

The AFE6160A provides a weak burn-out sink current from pin AIN0-, AIN1- or AIN2- to VSS depending on the setting of signal multiplexer. If the DUT is in a short-circuit condition, the voltage difference between positive and negative analog signal input would approach 0, so the ADC output would smaller than normal value. By proper setting of register file, the bit SNSL would be set to 1 to indicate a sensor short-circuit situation.

The diagnostics function make system more robust. The ADC readings of the functional sensor may be affected when the burnout currents sources are enabled. For precision measurement, disable the burn-out current and only enable them while sensor fault condition testing.

Local Temperature Sensor

The AFE6160A integrates an internal temperature sensor for environment conditioning. The temperature sensor consists of multiple on-chip diodes, the difference in current density between diodes generates a voltage that is proportional to absolute temperature (PTAT).

The calibrated temperature data can be readout through register DATA, the format is shown in temperature_format. There are 1 sign-bit and 12 temperature bits to represent 1 temperature, the resolution of 1 LSB is 0.0625°C, for example, if the temperature is 25.25°C, the DATA output would be 0x001940H.

For best performance of temperature sensor, the AFE6160A should be configured as the same condition as calibration, i.e., VDD=3.3V, OSR512, INBUF=1, BUFCH=1, VRBUF=1, ADCCH=1, SNSCH=1, PGAGNx1, ADCGNx1 and REFGNx1. Other configuration would cause a larger error in temperature.

On-Chip Sensor Switch

In most of the case, a higher the excitation current on the sensor generates larger the output voltage. However, the high excitation current result in higher power consumption and stronger self-heating effect, that might lead to measurement fault or even permanent damage to sensor. To reduce the self-heating, a common approach is to power the sensor only when ADC conversion period, but not every measurement system can support this flexibility.

The AFE6160A integrates a power-saving switch, PSW, connecting from pin AIN2- to VSS to address a greater flexibility of measurement system. The PSW can be switched on during ADC conversion period while switching off at idle time for power saving. It should be noticed that the voltage variation due to the switch-on resistance (10Ω).

Layout Note and Grounding Guidelines

As mention before, the AFE6160A has three power supplies, VDD, AVDD and VCM, power decoupling capacitors are critical for high resolution data conversion. A dual-capacitor consisting of a 2.2µF in parallel with 0.1µF should be placed between VDD-VSS, AVDD-AVSS and VCM-AVSS. In addition, the power trace should be as wider as possible to minimize the path impedance and reduce the voltage drop and glitch.

The communication pin SCL, SDA and EOC are open-drain I/O mode, an external 4.7kΩ pull-up resistor is recommended.

The differential signal and reference are referenced to its common-mode voltage. A 0.1µF capacitor can be used to filter the high frequency noise of common-mode voltage. Moreover, implementation of an anti-aliasing filter helps suppress the high frequency noise due to the lower sampling rate of sigma-delta ADC.

The analog ground plane should be paved underneath the AFE6160A to prevent coupling of digital signal into device. Routing digital signals under the device or parallel to the sensitive signals should be avoid, because these traces might couple the noise into the device, signal or reference.

The ground and power traces around AFE6160A should be separated to minimize any switching noise. Using large ground planes with multiple vias and ensuring short return path to reduce the ground impedance and minimize the disturbance voltage. In addition, shielding technique should be considered to protect the sensitive analog input and reference input signals from noisy environment. Since digital interface is fast switching signal, ground shielding can prevent the radiating noise. Digital signals should never be touted close to the analog or reference signals. A double-sided PCB with solid ground plane is preferred to achieve the best performance.

The PCB layout must ensure that the return current path are as close as possible to the paths the currents took to reach their destinations.

Application Information

Power Saving and Ratiometric Measurement for Bridge Sensors

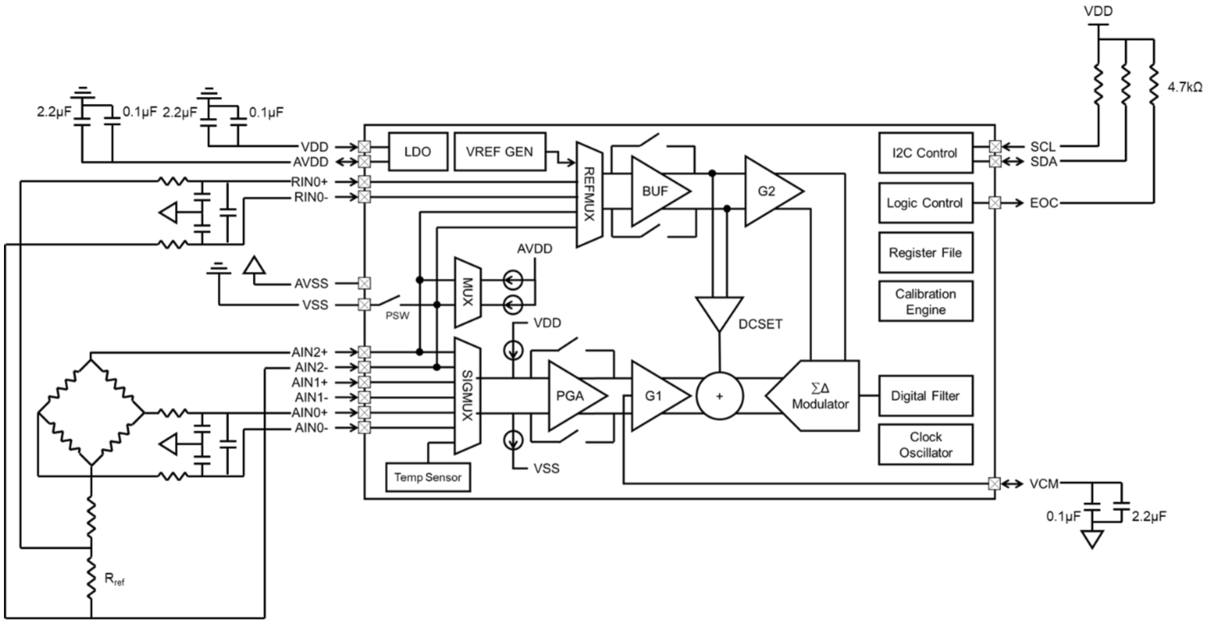


Figure 27 Power Saving and Ratiometric Measurement for Bridge Sensors

Ratiometric Measurement for IR Thermopile

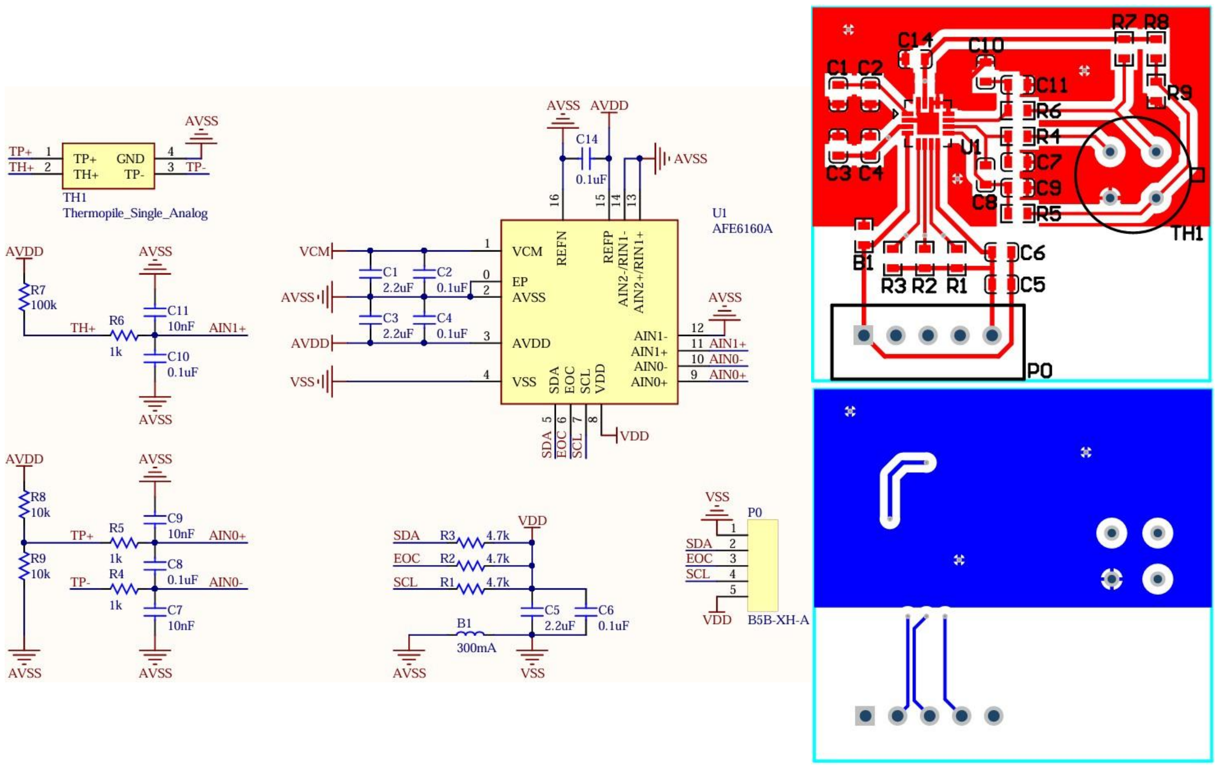


Figure 28 Ratiometric Measurement for IR Thermopile

Register Summary

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
DATA_RH	0x00	R	DATA_R [23:16]								0x00
DATA_RM	0x01	R	DATA_R [15:8]								0x00
DATA_RL	0x02	R	DATA_R [7:0]								0x00
DATA_H	0x03	R	DATA [23:16]								0x00
DATA_M	0x04	R	DATA [15:8]								0x00
DATA_L	0x05	R	DATA [7:0]								0x00
OSR	0x18	R/W	–	–	–	OSR [1:0]		AVG [2:0]			0x00
ENCFG	0x19	R/W	–	–	ENBODN	ENBODP	ENPDET	ENVCM	ENLDOA	ENBIAS	0x00
SIGMUX	0x1A	R/W	–	–	–	–	–	INCH1	INCH0	–	0x00
SIGCFG	0x1B	R/W	ENMUXS	–	VINL [2:0]			VINH [2:0]			0x00
REFCFG	0x1C	R/W	ENMUXR	–	–	–	VRL [1:0]		VRH [1:0]		0x00
IDACCFG	0x1D	R/W	–	–	PSW	–	DAC2N	DAC1N	DAC2P	DAC1P	0x00
PGACFG	0x1E	R/W	–	VRBUF	PGACH	INBUF	–	PGAGN [2:0]			0x00
ADCCFG	0x1F	R/W	ENADC	ADCCH	REFGN [1:0]		ADCGN [3:0]				0x00
DCSET	0x20	R/W	–	–	–	–	–	DCSET [2:0]			0x00
TSNS	0x21	R/W	–	–	–	–	–	–	SNSCH	TMPSNS	0x00
IDAC1	0x22	R/W	ENIDAC1	IDAC1 [6:0]							0x00
IDAC2	0x23	R/W	ENIDAC2	IDAC2 [6:0]							0x00
SYSCLK	0x24	R/W	–	CLKDIV [2:0]			–	–	–	ENHSRC	0x01
INSTA	0x25	R/W	INTF	SNSL	SNSH	–	–	–	–	INTEN	0x00
SNSTH_HH	0x26	R/W	SNSTH_H [23:16]								0x00
SNSTH_HM	0x27	R/W	SNSTH_H [15:8]								0x00
SNSTH_HL	0x28	R/W	SNSTH_H [7:0]								0x00
SNSTH_LH	0x29	R/W	SNSTH_L [23:16]								0x00
SNSTH_LM	0x2A	R/W	SNSTH_L [15:8]								0x00
SNSTH_LL	0x2B	R/W	SNSTH_L [7:0]								0x00

Register Description

Raw Data Register

The three registers store 24-bit uncalibrated ADC data.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
DATA_RH	0x00	R	DATA_R [23:16]								0x00
DATA_RM	0x01	R	DATA_R [15:8]								0x00
DATA_RL	0x02	R	DATA_R [7:0]								0x00

Data Register

The three registers store 24-bit uncalibrated ADC data.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
DATA_H	0x03	R	DATA [23:16]								0x00
DATA_M	0x04	R	DATA [15:8]								0x00
DATA_L	0x05	R	DATA [7:0]								0x00

When the signal multiplexer is switched to internal temperature, DATA register shows the calibrated temperature data in following format.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
DATA_H	0x03	R	–								0x00
DATA_M	0x04	R	TEMP [11:4]								0x00
DATA_L	0x05	R	TEMP [3:0]				0	0	0	0	0x00

Bits	Bits Name	Description
[23:16]	Reserved	–
[15:4]	TEMP [11:0]	TEMP [11]: Sign bit TEMP [10]: 64°C TEMP [9]: 32°C TEMP [8]: 16°C TEMP [7]: 8°C TEMP [6]: 4°C TEMP [5]: 2°C TEMP [4]: 1°C TEMP [3]: 0.5°C TEMP [2]: 0.25°C TEMP [1]: 0.125°C TEMP [0]: 0.0625°C
[3:0]	Reserved	Fixed at 0

Oversampling Rate Register

This register controls the over sampling rate and moving average buffer size

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
OSR	0x18	R/W	–	–	–	OSR [1:0]		AVG [2:0]			0x00

Bits	Bits Name	Description
[7:6]	Reserved	–
[4:3]	OSR [1:0]	00: OSR = 512 (500sps if CLKDIV [6:4] = 000) 01: OSR = 256 (1000sps if CLKDIV [6:4] = 000) 10: OSR = 128 (2000sps if CLKDIV [6:4] = 000) 11: OSR = 1024 (250sps if CLKDIV [6:4] = 000)
[2:0]	AVG [2:0]	000: Buffer size of moving average is 1 001: Buffer size of moving average is 2 010: Buffer size of moving average is 4 011: Buffer size of moving average is 8 100: Buffer size of moving average is 16 101: Buffer size of moving average is 32 110: Buffer size of moving average is 64 111: Buffer size of moving average is 128

ENCFG Register

This register controls the power and sensor diagnostic function.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
ENCFG	0x19	R/W	–	–	ENBODN	ENBODP	ENPDET	ENVCM	ENLDOA	ENBIAS	0x00

Bits	Bits Name	Description
[7:6]	Reserved	–
[5]	ENBODN	0: Disable burn-out sink current 1: Enable burn-out sink current
[4]	ENBODP	0: Disable burn-out source current 1: Enable burn-out source current
[3]	ENPDET	0: Disable power supply monitor 1: Enable power supply monitor
[2]	ENVCM	0: Disable common-mode voltage generator 1: Enable common-mode voltage generator
[1]	ENLDOA	0: Disable analog voltage regulator 1: Enable analog voltage regulator
[0]	ENBIAS	0: Disable bias current 1: Enable bias current

Input Routing Register

This register controls the input routing.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
SIGMUX	0x1A	R/W	–	–	–	–	–	INCH1	INCH0	–	0x00

Bits	Bits Name	Description
[7:3]	Reserved	–
[2:1]	INCH	00：Differential analog input signals go-through 01：Differential signals connect to positive terminal input 10：Differential signals connect to negative terminal input 11：Reserved
[0]	Reserved	–

Input Signal Multiplexer Register

This register controls the signal multiplexer.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
SIGCFG	0x1B	R/W	ENMUXS	–	VINL [2:0]			VINH [2:0]			0x00

Bits	Bits Name	Description
[7]	ENMUXS	0: Disable signal multiplexer 1: Enable signal multiplexer
[6]	Reserved	–
[5:3]	VINL [2:0]	Negative multiplexer input of differential signal is 000: AIN0- 001: AIN1- 010: AIN2- 011: Negative input of internal temperature sensor 100: VDD/4 (Power monitor) 101~111: AVSS
[2:0]	VINH [2:0]	Positive multiplexer input of differential signal is 000: AIN0+ 001: AIN1+ 010: AIN2+ 011: Positive input of internal temperature sensor 100: VDD/2 (Power monitor) 101~111: AVSS

Reference Voltage Input Multiplexer Register

This register controls the reference multiplexer.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
REFCFG	0x1C	R/W	ENMUXR	–	–	–	VRL [1:0]		VRH [1:0]		0x00

Bits	Bits Name	Description
[7]	ENMUXR	0: Disable reference multiplexer 1: Enable reference multiplexer
[6:4]	Reserved	–
[3:2]	VRL [1:0]	Negative multiplexer input of differential reference is 00: RIN0- 01: RIN1- 10: AVSS (Negative input of REF_{IN1}) 11: 0.2V (Negative input of REF_{IN2})
[1:0]	VRH [1:0]	Positive multiplexer input of differential reference is 00: RIN0+ 01: RIN1+ 10: 1.2V (Positive input of REF_{IN1}) 11: 1.0V (Positive input of REF_{IN2})

IDAC Configuration Register

This register controls the routing of IDAC and power switch.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
IDACCFG	0x1D	R/W	–	–	PSW	–	DAC2N	DAC1N	DAC2P	DAC1P	0x00

Bits	Bits Name	Description
[7:6]	Reserved	–
[5]	PSW	0: Disable power saving switch 1: Enable power saving switch
[4]	Reserved	–
[3]	DAC2N	0: Output of IDAC2 toward AIN2- is disabled 1: Output of IDAC2 is AIN2-
[2]	DAC1N	0: Output of IDAC1 toward AIN2- is disabled 1: Output of IDAC1 is AIN2-
[1]	DAC2P	0: Output of IDAC2 toward AIN2+ is disabled 1: Output of IDAC2 is AIN2+
[0]	DAC1P	0: Output of IDAC1 toward AIN2+ is disabled 1: Output of IDAC1 is AIN2+

PGACFG Register

This register controls the PGA and the reference buffer.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
PGACFG	0x1E	R/W	–	VRBUF	PGACH	INBUF	–	PGAGN [2:0]			0x00

Bits	Bits Name	Description
[7]	Reserved	–
[6]	VRBUF	0: Disable reference buffer 1: Enable reference buffer
[5]	PGACH	0: Disable PGA chopper 1: Enable PGA chopper
[4]	INBUF	0: Disable PGA 1: Enable PGA
[3]	Reserved	–
[2:0]	PGAGN [2:0]	000: PGAGN x1 001: PGAGN x2 010: PGAGN x4 011: PGAGN x8 100: PGAGN x16 101: PGAGN x32 110: PGAGN x64 111: PGAGN x128

ADC Configuration Register

This register controls the sigma-delta ADC module and reference gain

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
ADCCFG	0x1F	R/W	ENADC	ADCCH	REFGN [1:0]		ADCGN [3:0]				0x00

Bits	Bits Name	Description
[7]	ENADC	0: Disable sigma-delta ADC 1: Enable sigma-delta ADC
[6]	ADCCH	0: Disable ADC chopper 1: Enable ADC chopper
[5:4]	REFGN [1:0]	00: REFGN x1 01: REFGN x0.5 10: REFGN x0.75 11: REFGN x0.25
[3:0]	ADCGN [3:0]	0000: ADCGN x1 0001: ADCGN x2 0010: ADCGN x3 0011: ADCGN x4

		0100: ADCGN x5 0101: ADCGN x6 0110: ADCGN x7 0111: ADCGN x8 1000: ADCGN x9 1001: ADCGN x10 1010: ADCGN x11 1011: ADCGN x12 1100: ADCGN x13 1101: ADCGN x14 1110: ADCGN x15 1111: ADCGN x16

DC Offset Register

This register controls the DC offset.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
DCSET	0x20	R/W	–	–	–	–	–	DCSET [2:0]			0x00

Bits	Bits Name	Description
[7:3]	Reserved	–
[2:0]	DCSET [2:0]	000: DC Offset is 0/12.5VREF 001: DC Offset is 1/12.5VREF 010: DC Offset is 2/12.5VREF 011: DC Offset is 3/12.5VREF 100: DC Offset is 4/12.5VREF 101: DC Offset is 5/12.5VREF 110: DC Offset is 6/12.5VREF 111: DC Offset is 7/12.5VREF

Temperature Sensor Register

This register controls the internal temperature sensor

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
TSNS	0x21	R/W	–	–	–	–	–	–	SNSCH	TMPSNS	0x00

Bits	Bits Name	Description
[7:2]	Reserved	–
[1]	SNSCH	0: Disable chopper of internal temperature sensor 1: Enable chopper of internal temperature sensor
[0]	TMPSNS	0: Disable internal temperature sensor and sigma-delta ADC module 1: Enable internal temperature sensor and sigma-delta ADC module

IDAC1 Register

This register controls the output of IDAC1.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
IDAC1	0x22	R/W	ENIDAC1	IDAC1 [6:0]							0x00

Bits	Bits Name	Description
[7]	ENIDAC1	0: Disable IDAC1 1: Enable IDAC1
[6:0]	IDAC1 [6:0]	Level of IDAC1 output is 0000000: 8μA 0000001: 16μA 0000010: 25μA 0000100: 45μA 0001000: 80μA 0010000: 150μA 0100000: 300μA 1000000: 590μA 1111111: 1150μA

IDAC2 Register

This register controls the output of IDAC2.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
IDAC2	0x23	R/W	ENIDAC2	IDAC2 [6:0]							0x00

Bits	Bits Name	Description
[7]	ENIDAC2	0: Disable IDAC2 1: Enable IDAC2
[6:0]	IDAC2 [6:0]	Level of IDAC2 output is 0000000: 8μA 0000001: 16μA 0000010: 25μA 0000100: 45μA 0001000: 80μA 0010000: 150μA 0100000: 300μA 1000000: 590μA 1111111: 1150μA

System Clock Register

This register controls the system clock.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
SYSCLK	0x24	R/W	–	CLKDIV [2:0]			–	–	–	ENHSRC	0x01

Bits	Bits Name	Description
[7]	Reserved	–
[6:4]	CLKDIV [2:0]	The extra clock divider of SDADC is 000: 1 (Clock of SDADC is 250kHz) 001: 2 (Clock of SDADC is 125kHz) 010: 4 (Clock of SDADC is 62.5kHz) 011: 8 (Clock of SDADC is 31.25kHz) 100: 16 (Clock of SDADC is 15.625kHz) 101: 32 (Clock of SDADC is 7.8125kHz) 110, 111: Reserved
[3:1]	Reserved	–
[0]	ENHSRC	0: Disable internal high-speed oscillator 1: Enable internal high-speed oscillator

Interrupt Status Register

This register indicates the interrupt status.

Register	ADD	R/W	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Default
INSTA	0x25	R/W	INTF	SNSL	SNSH	–	–	–	–	INTEN	0x00

Bits	Bits Name	Description
[7]	INTF	0: An ADC conversion is in processing 1: An ADC conversion is done This flag is set by hardware and cleared by writing “1” through software.
[6]	SNSL	0: The shot-circuit test on external sensor is passed 1: The shot-circuit test on external sensor is failed. This flag is set and cleared by hardware.
[5]	SNSH	0: The open-circuit test on external sensor is passed 1: The open-circuit test on external sensor is failed. This flag is set and cleared by hardware.
[4:1]	Reserved	–
[0]	INTEN	0: Disable interrupt function (EOC, INTF) 1: Enable interrupt function (EOC, INTF)

ADC Threshold Register for Open-Circuit Test

These three registers are the 24-bit ADC threshold for open-circuit test.

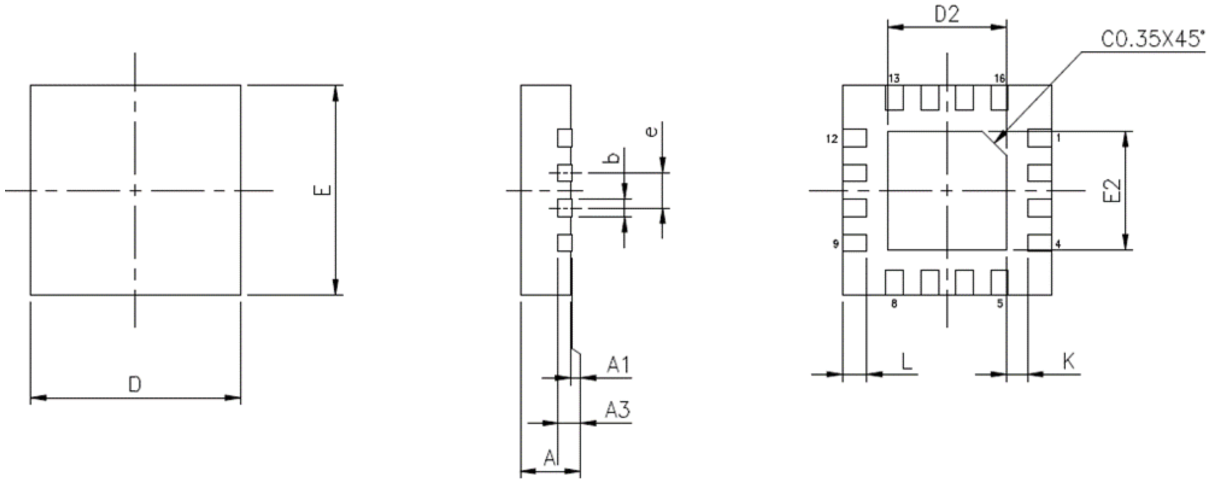
Register	ADD	R/W	Description	Default
SNSTH_HH	0x26	R/W	SNSTH_H [23:16]	0x00
SNSTH_HM	0x27	R/W	SNSTH_H [15:8]	0x00
SNSTH_HL	0x28	R/W	SNSTH_H [7:0]	0x00

ADC Threshold Register for Short-Circuit Test

These three registers are the 24-bit ADC threshold for short-circuit test.

Register	ADD	R/W	Description	Default
SNSTH_LH	0x26	R/W	SNSTH_H [23:16]	0x00
SNSTH_LM	0x27	R/W	SNSTH_H [15:8]	0x00
SNSTH_LL	0x28	R/W	SNSTH_H [7:0]	0x00

Package Outline Dimensions



UNIT: mm

SYMBOLs	Minimum	Normal	Maximum
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.02 REF.	
b	0.18	0.25	0.30
D	2.90	3.00	3.10
E	2.90	3.00	3.10
e		0.50 bsc.	
L	0.30	0.35	0.40
K	0.20	–	–
D2	1.60	1.70	1.80
E2	1.60	1.70	1.80

Reversion History

Version	Date	Description
1.0	2025.04.11	Initial Release
1.1	2025.08.30	➢ Add table of content (Page 4) ➢ Add content of input impedance (Page 25) ➢ Updated content descriptions ➢ Rearranged register MAP descriptions

Important Notice

The contents contained in this document are believed to be accurate at the time of publication. ESMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by ESMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of ESMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

ESMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.