AFEM-7780

UMTS2100 4x7 Front-end Module (FEM)



Data Sheet

Description

The AFEM-7780 is a fully matched WCDMA Band1 Frond-End Module (FEM) featuring the integration of Avago Technologies' power amplifier and FBAR.

The AFEM-7780 offers extended talk time and excellent linearity by using CoolPAM technology, which enhances efficiencies in low and medium power mode. Idle current is as low as 11mA.

The FBAR (Film Bulk Acoustic Resonator) based duplexer provides low insertion loss and outstanding isolation, which improves efficiency and RX sensitivity.

By using CoolPAM and FBAR technologies, AFEM-7780 shows best performance with smaller footprint.

Component Image



Feature

- Excellent linearity
- Operating Frequency:

Tx: 1920~1980 MHz Rx: 2110~2170 MHz

- 24.5 dBm Linear Output Power (HSDPA)
- Very low quiescence current in low power mode
- High isolation (Low Tx leakage at Rx port)
- HSDPA capable
- 50 ohm input and output matching
- 20-pin surface mounting package
- 4.0 x 7.0 x 1.1(typ) mm SMT Package

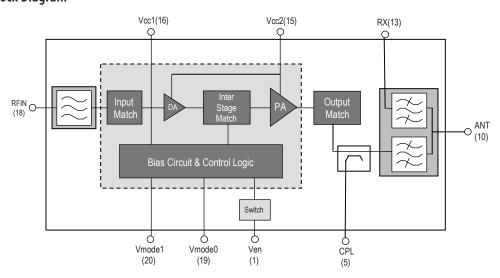
Applications

WCDMA handset (HSDPA)

Ordering Information

Part Number	Number of Devices	Container
AFEM-7780-TR1	1000	178mm (7") Tape/Reel
AFEM-7780-BLK	100	Bulk

Block Diagram



Absolute Maximum Rating

No damage assuming only one parameter is set at limit at a time with all other parameters set at or below typical value Operation of any single parameter outside these conditions with the remaining parameters set at or below typical values may result in permanent damage

Description	Min	Тур	Max	Unit	Associated Pins
Tx Input Power		0	10	dBm	RF _{IN}
DC Supply Voltage		3.4	5.0	V	Vcc
Enable Voltage		2.6	3.3	V	Ven
Control Voltages		2.6	3.3	V	Vmode0, Vmode1
Storage Temperature	-55	25	125	°C	

Recommended Operating Conditions

Description	Symbol	Min	Тур	Max	Unit
Tx Frequency		1920		1980	MHz
Rx Frequency		2110		2170	MHz
DC Supply Voltage (Vcc1, Vcc2)		3.2	3.4	4.2	V
Enable Voltage	LOW	0	0	0.5	V
(Ven)	HIGH	2.15	2.6	2.9	V
Mode Control Voltage	LOW	0	0	0.5	V
(Vmode0, Vmode1)	HIGH	2.15	2.6	2.9	V
Case Operating Temperature		-20	25	+90	°C

Operation Logic Table

Power Mode	Recommended Pout Range	Ven	Vmode0	Vmode1
High Power Mode	~ 24.5 dBm	HIGH	LOW	LOW
Mid Power Mode	~ 13.5 dBm	HIGH	HIGH	LOW
Low Power Mode	~ 4 dBm	HIGH	HIGH	HIGH
Shunt Down Mode		LOW	-	-

Electrical Characteristics

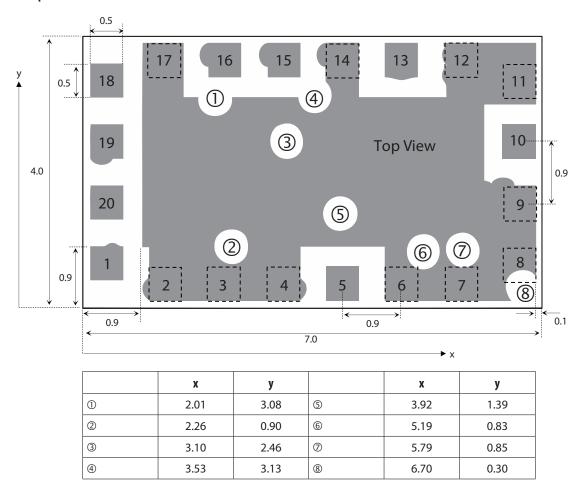
- Conditions: Vcc1=Vcc2=3.4, Ven=2.6V, Temp=25°C
- Signal configuration: HSDPA modulated uplink (DPCCH/DPDCH=12/15, HS-DPCCH/DPDCH=15/15)

Parameter	Condition	Min	Тур	Max	Unit
TX to Antenna Port					
Tx Operating Frequency Range	TX	1920		1980	MHz
Maximum Output Power	High Power Mode	24.5			dBm
Gain	High Power Mode, Po=24.5dBm	18	23.5		dB
	Mid Power Mode, Po=13.5dBm	8	13.5		dB
	Low Power Mode, Po=4dBm	5	11		dB
Power Added Efficiency	High Power Mode, Po=24.5dBm	20.6	23.9		%
	Mid Power Mode, Po=13.5dBm	7.9	9.5		%
	Low Power Mode, Po=4dBm	1.9	2.7		%
Current Consumption	High Power Mode, Po=24.5dBm		345	400	mA
	Mid Power Mode, Po=13.5dBm		66	80	mA
	Low Power Mode, Po=4dBm		25	35	mA
Quiescent Current	High Power mode		98	110	mA
	Mid Power mode		17	25	mA
	Low Power Mode		12	20	mA
Adjacent Channel Power	±5MHz offset, High Power Mode, Po=24.5dBm	-39	-36	dBc	
	±10MHz offset, High Power Mode, Po=24.5dBm	-52	-46	dBc	
	±5MHz offset, Mid Power Mode, Po=13.5dBm	-40	-36	dBc	
	±10MHz offset, Mid Power Mode, Po=13.5dBm			-46	dBc
	±5MHz offset, Low Power Mode, Po=4dBm		-43	-36	dBc
	±10MHz offset, Low Power Mode, Po=4dBm		-60	-46	dBc
Harmonics	2 nd Harmonics		-40	-33	dBm/MHz
	3 rd Harmonics		-55	-33	dBm/MHz
Input VSWR at Tx port			2.5:1		
Stability, spurious level	TX source VSWR < 5:1 FEM Antenna load VSWR < 5:1, all angles			-70	dBc
Leakage current at shut- down	Ven=0V, without RF			5	uA
Change in TX insertion	$MPM \leftrightarrow HPM$		20		degree
phase	$LMP \! \leftrightarrow \! MPM$		2		degree
Intermodulation	CW interface -40dBc @ 5MHz: Intermod products @10MHz: Intermod products		-43 -52	-35 -45	dBc dBc

Electrical Characteristics (continued)

Coupling port					3.84MHz
	1920-1980MHz		-27	-24	dBm/
Noise Power	2110-2170 MHz		-185	-181	dBm/Hz
Noise Power from TX to I					
	5940-6140 MHz	15	15.6		dB
	4220-4340 MHz	10	26.7		dB
	2500-4150 MHz	10	19.7		dB
	2400-2484 MHz	30	55.2		dB
	2255-2400 MHz	15	56.9		dB
	1980-2025 MHz	15	39.3		dB
	1920-1980 MHz	35	56.1		dB
	1805-1920 MHz	23	50.8		dB
	1730-1805 MHz	30	45.1		dB
	205-1730 MHz	23	38.4		dВ
Attenuation	175-205 MHz	30	65.4		dB dB
Input VSWR at RX port	0-175 MHz	23	2:1		dB
Rx Insertion Loss			1.5	2.5	dB
Range			1.5		
Rx Operating Frequency	RX	2110		2170	MHz
Antenna to Rx port	5. 55 55 15 <u>5</u>				
	5760-5940 MHz	27	57.9		dB
	3840-3960 MHz	27	63.9		dB dB
	2400-2500 MHz	35	47		dB
	2300-2400 MHz	32	47.5		dВ
	2110-2170 MHz	50	63.9		dB
	1580-1805 MHz 1805-1880 MHz	12	52.2 46.7		dB dB
	1570-1580 MHz	33	51.6		dB
	960-1570 MHz	25	50.2		dB
	925-960 MHz	42	60.4		dB
Attenuation	0-925 MHz	25	60.8		dB
A.,	Noise folding at DCS Band Tx port noise input power=-134dBm/Hz		-85	-78	dBm/ 100kHz
	ISM Band (2400-2480MHz)		-166	-164	dBm/Hz
	DCS Band (1805-1880Mhz)		-135	-132	dBm/Hz

Footprint

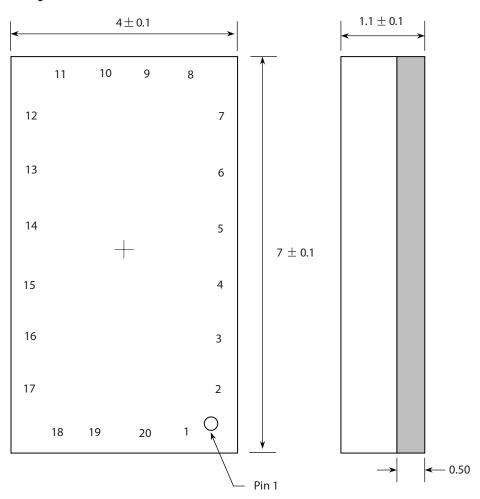


- 1. Dimensions in millimeters
- 2. All GND pins are merged into center ground3. Radius of non-ground circle is 0.52mm
- 4. Center position of non-ground circle

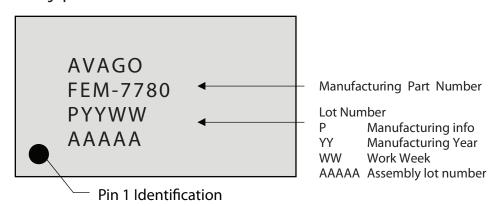
Pin Description

Pin#	Name	Description	Pin#	Name	Description
1	Ven	Module on/off control	11	GND	Ground
2	GND	Ground	12	GND	Ground
3	GND	Ground	13	RX	DPX RX output
4	GND	Ground	14	GND	Ground
5	CPL	TX Power Coupling Output	15	VCC2	DC Supply Voltage
6	GND	Ground	16	VCC1	DC Supply Voltage
7	GND	Ground	17	GND	Ground
8	GND	Ground	18	RFIN	TX RF Input
9	GND	Ground	19	Vmode0	Mode Control Voltage
10	ANT	Antenna	20	Vmode1	Mode Control Voltage

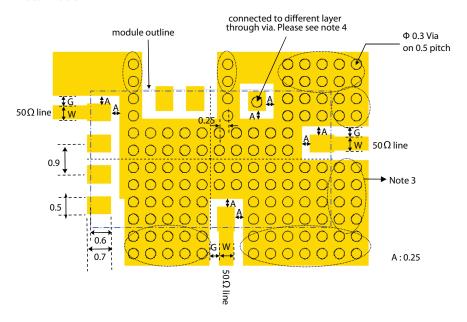
Package Dimensions (all dimensions are in millimeter)



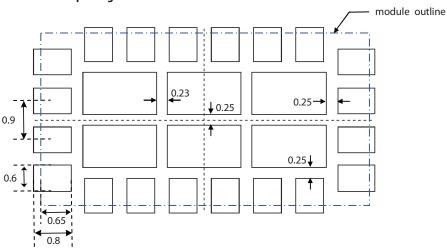
Marking Specification



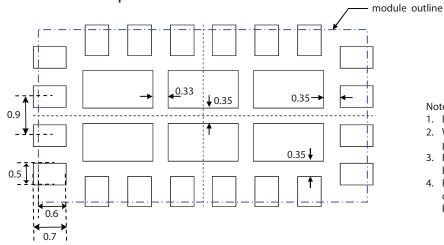
Metallization



Solder Mask Opening



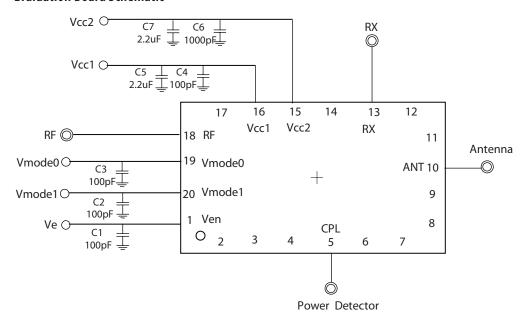
Solder Plate Stencil Aperture



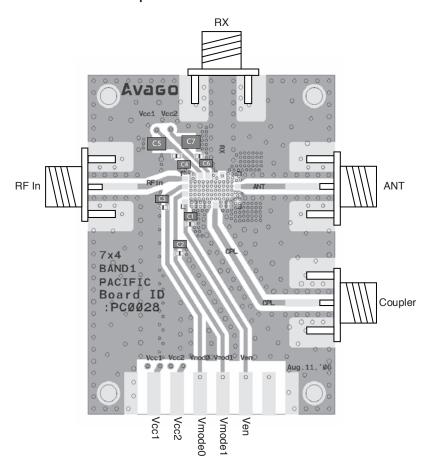
Notes:

- 1. Dimensions in millimeters
- 2. W and G adjusted for Zo=50 Ω (CPW type is preferable)
- 3. Extended Ground area and VIAs are required for better Tx/Rx isolation
- 4. Rx signal line and Ant signal line should be at the different layer with proper isolation by GND for better Tx/Rx isolation

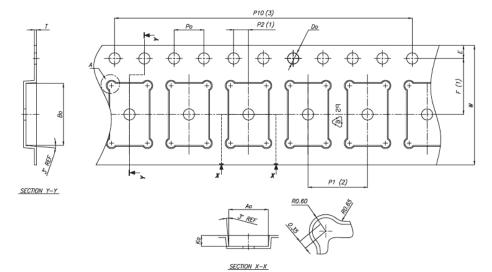
Evaluation Board Schematic



Evaluation Board Description

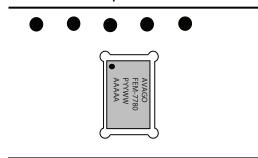


Tape Drawing

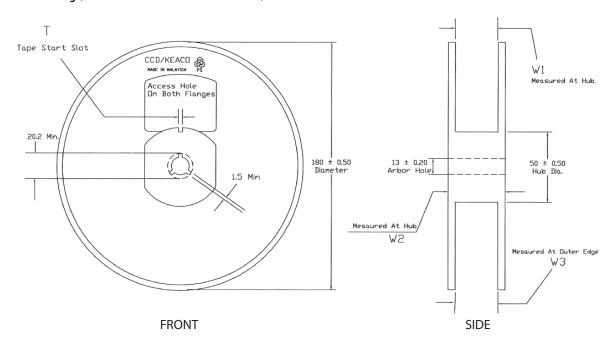


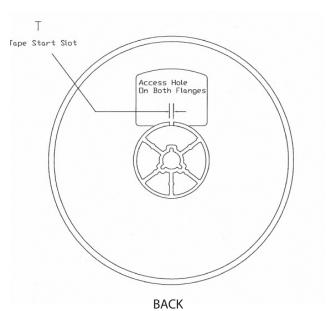
	Dimensi	on List	
Annote	Milimeter	Annote	Milimeter
Ao	4.30±0.10	Ε	1.75±0.10
Bo	7.30±0.10	F	7.50±0.10
Ko	1.55±0.10	W	16,00±0.30
Do	1.55±0.05	T	0.30±0.10
D1	1.50±0.10		
Po	4.00±0.10		
P1	8.00±0.10		
P2	2.00±0.10		
P10	40.00±0.20		

Part Orientation in Tape



Reel Drawing (all dimensions are in millimeters)





Notes:

1. Material:

2. Surface Resistivity Method

3. Static Decay

: Polystrene : < 10E12 OHMS/SQ : ASTM D-257 at 50% RH

: < 2 Secs at 50% RH

Tape Width	T	W1	W2	W3	
16 mm	4.4 ± 0.50	16.40 +1.5	22.0 MAX	16.40 +2.0	
		- 0.0		- 0.0	

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature.

Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. Af-

ter soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test describe below which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

AFEM-7780 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked. MSL classification reflow temperature for the AFEM-7780 is targeted at 260°C +0/-5°C. Figure and table on following page shows typical SMT profile for maximum temperature of 260 + 0/-5°C.

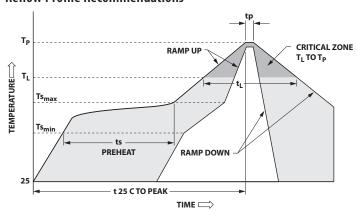
Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient $=$ < 30° C/ 60% RH or as stated
1	Unlimited at =< 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note

^{1.} The MSL Level is marked on the MSL Label on each shipping bag.

Reflow Profile Recommendations



Typical SMT Reflow Profile for Maximum Temperature = 260 + 0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (TL to TP)	3°C/sec max	3°C /sec max
Preheat		
- Temperature Min (Tsmin)	100°C	150°C
- Temperature Max (Tsmax)	150°C	200°C
- Time (min to max) (ts)	60-120 sec	60-180 sec
Tsmax to TL		
- Ramp-up Rate		3°C /sec max
Time maintained above:		
- Temperature (TL)	183°C	217°C
- Time (TL)	60-150 sec	60-150 sec
Peak temperature (Tp)	240 +0/-5°C	260 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10-30 sec	20-40 sec
Ramp-down Rate	6°C /sec max	6°C /sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.
·		

Storage Condition

Packages described in this document must be stored in sealed moisture barrier, antistatic bags. Shelf life in a sealed moisture barrier bag is 12 months at <40°C and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration

After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30°C and 60% RH.

Baking

It is not necessary to re-bake the part if both conditions (storage conditions and out-of bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125°C for 12 hours J-STD-033 p.8.

CAUTION

Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, detaped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount

If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per 4-2 prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis

Not following the above requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards

Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating due to Factory Environmental Conditions

Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in next table. This approach, however, does not work if the factory humidity or temperature is greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component package materials ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device.

Table on following page lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperature, 20°C, 25°C, and 30°C.

This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating this table:

- 1. Activation Energy for diffusion = 0.35eV (smallest known value).
- 2. For ≤60% RH, use Diffusivity = 0.121exp (-0.35eV/kT) mm2/s
 - (this used smallest known Diffusivity @ 30°C).
- 3. For >60% RH, use Diffusivity = 1.320exp (-0.35eV/kT) mm2/s

(this used largest known Diffusivity @ 30°C).

Recommended Equivalent Total Floor Life (days) @ 20° C, 25° C & 30° C

For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)

Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
•	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30
		∞	∞	∞	78	53	42	36	14	10	8	25
		∞	∞	∞	103	69	57	47	19	13	10	20
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30
D Th. : -		∞	∞	13	11	10	9	9	7	6	5	25
Body Thickness ≥3.1 mm Including		∞	∞	17	14	13	12	12	10	8	7	20
PQFPs >84 pin,	Level 4	∞	5	4	4	4	3	3	3	2	2	30
PLCCs (square)		∞	6	5	5	5	5	4	3	3	3	25
All MQFPs		∞	8	7	7	7	7	6	5	4	4	20
or	Level 5	∞	4	3	3	2	2	2	2	1	1	30
All BGAs ≥1 mm	2010.0	∞	5	5	4	4	3	3	2	2	2	25
		∞	7	7	6	5	5	4	3	2	3	20
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30
	Level Ju	∞	3	2	2	2	2	2	1	1	1	25
		∞	5	4	3	3	3	2	2	2	2	20
	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30
	LCVCI Zu	∞	∞	∞	∞	148	51	37	6	4	3	25
		∞	∞	∞	∞	∞	69	49	8	5	4	20
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30
Body 2.1 mm	Levers	∞	∞	25	15	12	10	9	5	3	3	25
≤ Thickness		∞	∞	32	19	15	13	12	7	5	4	20
<3.1 mm including	Level 4	∞	7	5	4	4	3	3	2	2	1	30
PLCCs (rectangular)	EC VCI 4	∞	9	7	5	5	4	4	3	2	2	25
18-32 pin		∞	11	9	7	6	6	5	4	3	3	20
SOICs (wide body) SOICs ≥20 pins,	Level 5	∞	4	3	3	2	2	2	1	1	1	30
PQFPs ≤80 pins	Level 5	∞	5	4	3	3	3	3	2	1	1	25
1 Q113 200 pins		∞	6	5	5	4	4	4	3	3	2	20
	Level 5a		2	1	1	1	1	1	1	0.5	0.5	30
	Level 3a	∞	2	2	2	2	2	2	1	0.5 1	0.5 1	25
		∞	3	2	2	2	2	2	2	2	1	20
	Lavel 2e							20			1	
	Level 2a	∞	∞	∞	∞ ∞	∞	∞	28 ∞	1 2	1 1	1 1	30 25
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20
	Lavel 2		-				11					30
	Level 3	∞	∞	∞	∞	∞	11 14	7 10	1 2	1 1	1 1	25
Body Thickness <2.1 mm including SOICs <18 pin All TQFPs, TSOPs or All BGAs <1 mm body		∞	∞	∞	∞	∞	20	13	2	2	1	20
	1 1 4											
	Level 4	∞	∞	∞	9 12	5 7	4	3 4	1	1 1	1 1	30 25
		∞	∞	∞	17	9	5 7	4 6	2 2	2	1 1	25
thickness	Level 5	∞	∞	13	5	3	2	2	1	1	1	30
		∞	∞	18 26	6 8	4 6	3 5	3 4	2 2	1 2	1 1	25 20
									-			
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30
		∞	13	5	3	2	2	2	1	1	1	25 20
		∞	18	6	4	3	2	2	2	2	1	20

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