International IƆR Rectifier

# HYBRID-HIGH RELIABILITY DC-DC CONVERTER

AFL2811R1S
(IR P/N 10209)
28V Input, Single Output

AFL

Description

The AFL Series of DC-DC converters feature high power density with no derating over the full military temperature range. This series is offered as part of a complete family of converters providing single and dual output voltages and operating from nominal +28V or +270V inputs with output power ranging from 80W to 120W. For applications requiring higher output power, individual converters can be operated in parallel. The internal current sharing circuits assure equal current distribution among the paralleled converters. This series incorporates International Rectifier's proprietary magnetic pulse feedback technology providing optimum dynamic line and load regulation response. This feedback system samples the output voltage at the pulse width modulator fixed clock frequency, nominally 550KHz. Multiple converters can be synchronized to a system clock in the 500KHz to 700KHz range or to the synchronization output of one converter. Undervoltage lockout, primary and secondary referenced inhibit, soft-start and load fault protection are provided on all models.

These converters are hermetically packaged in two enclosure variations, utilizing copper core pins to minimize resistive DC losses. Three lead styles are available, each fabricated with International Rectifier's rugged ceramic lead-to-package seal assuring long term hermeticity in the most harsh environments.

Manufactured in a facility fully qualified to MIL-PRF-38534, these converters are fabricated utilizing DSCC qualified processes. For available screening options, refer to device screening table in the data sheet. Variations in electrical, mechanical and screening can be accommodated. Contact IR San Jose for special requirements.
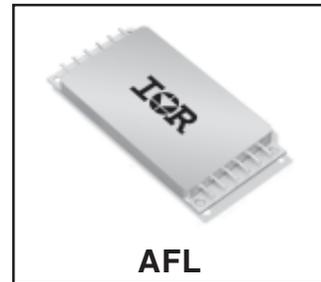
Features

- 16V To 40V Input Range
- High Power Density - up to 84W/in^3
- Up To 100W Output Power
- Parallel Operation with Power Sharing
- Low Profile (0.380") Seam Welded Package
- Ceramic Feedthru Copper Core Pins
- High Efficiency - to 84%
- Full Military Temperature Range
- Continuous Short Circuit and Overload Protection
- Primary and Secondary Referenced Inhibit Functions
- Line Rejection > 40dB - DC to 50KHz
- External Synchronization Port
- Fault Tolerant Design

Specifications

Absolute Maximum Ratings	
Input voltage	-0.5V to +50VDC (up to 1 second)
Soldering temperature	300°C for 10 seconds
Operating case temperature	-55°C to +125°C
Storage case temperature	-65°C to +135°C

Static Characteristics $-55°C \leq T_{CASE} \leq +125°C$, $16V \leq V_{IN} \leq 40V$ unless otherwise specified.

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
INPUT VOLTAGE		Note 6	16	28	40	V
OUTPUT VOLTAGE	1	V_{IN} = 28V, 100% Load	10.98	11.10	11.21	V
	2, 3		10.87		11.32	
OUTPUT CURRENT		V_{IN} = 16, 28, 40V - Notes 6, 10			7.2	A
MAXIMUM CAPACITIVE LOAD		Note 1	10,000			µF
OUTPUT VOLTAGE TEMPERATURE COEFFICIENT		V_{IN} = 28V, 100% Load – Notes 1, 6	-0.015		+0.015	%/°C
OUTPUT VOLTAGE REGULATION Line Load	 1, 2, 3 1, 2, 3	No Load, 50% Load, 100% Load V_{IN} = 16, 28, 40V	 -20 -1.0		 +20 +1.0	 mV %
OUTPUT RIPPLE VOLTAGE	1, 2, 3	V_{IN} = 16, 28, 40V, 100% Load, BW = 10MHz			45	mV$_{pp}$
INPUT CURRENT No Load Inhibit 1 Inhibit 2	 1 2, 3 1, 2, 3 1, 2, 3	V_{IN} = 28V I_{OUT} = 0 Pin 4 Shorted to Pin 2 Pin 12 Shorted to Pin 8			 80 100 5.0 50	mA
INPUT RIPPLE CURRENT	1, 2, 3	V_{IN} = 28V, 100% Load, BW = 10MHz			60	mA$_{pp}$
CURRENT LIMIT POINT	1, 2, 3	V_{OUT} = 90% V_{NOM}, V_{IN} = 16, 28, 40V Note 5	6.2		7.2	A
LOAD FAULT POWER DISSIPATION Overload or Short Circuit	1, 2, 3	V_{IN} = 28V			33	W
EFFICIENCY	1, 2, 3	V_{IN} = 28V, 100% Load	80	84		%

For Notes to Specifications, refer to page 3

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Static Characteristics (Continued)

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
ENABLE INPUTS (Inhibit Function)						
Converter Off	1, 2, 3	Logical Low on Pin 4 or Pin 12	-0.5		0.8	V
Sink Current		Note 1			100	µA
Converter On	1, 2, 3	Logical High on Pin 4 and Pin 12 - Note 9	2.0		50	V
Sink Current		Note 1			100	µA
SWITCHING FREQUENCY	1, 2, 3		500	550	600	KHz
SYNCHRONIZATION INPUT						
Frequency Range	1, 2, 3		500		700	KHz
Pulse Amplitude, Hi	1, 2, 3		2.0		10	V
Pulse Amplitude, Lo	1, 2, 3		-0.5		0.8	V
Pulse Rise Time		Note 1			100	ns
Pulse Duty Cycle		Note 1	20		80	%
ISOLATION	1	Input to Output or Any Pin to Case (except Pin 3). Test @ 500VDC	100			MΩ
DEVICE WEIGHT		Slight Variations with Case Style		85		g
MTBF		MIL-HDBK-217F, AIF @ T_C = 70°C	300			KHrs

Dynamic Characteristics -55°C $\leq$ T_{CASE} $\leq$ +125°C, V_{IN}=28V unless otherwise specified.

Parameter	Group A Subgroups	Test Conditions	Min	Nom	Max	Unit
LOAD TRANSIENT RESPONSE		Notes 2, 8				
Amplitude	4, 5, 6	Load Step 50% $\Leftrightarrow$ 100%	-750		750	mV
Recovery	4, 5, 6				200	µs
Amplitude	4, 5, 6	Load Step 10% $\Leftrightarrow$ 50%	-750		750	mV
Recovery	4, 5, 6				400	µs
LINE TRANSIENT RESPONSE		Note 1, 2, 3				
Amplitude		V_{IN} Step = 16 $\Leftrightarrow$ 40 Volts	-500		500	mV
Recovery					500	µs
TURN-ON CHARACTERISTICS		V_{IN} = 16, 28, 40 Volts. Note 4				
Overshoot	4, 5, 6	Enable 1, 2 on. (Pins 4, 12 high or			250	mV
Delay	4, 5, 6	open)	0	4.0	10	ms
LOAD FAULT RECOVERY		Same as Turn On Characteristics.				
LINE REJECTION		MIL-STD-461D, CS101, 30Hz to 50KHz Note 1	40	50		dB

Notes to Specifications:

1.   Parameters not 100% tested but are guaranteed to the limits specified in the table.
2.   Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1.0% of V_{OUT} at 50% load.
3.   Line transient transition time $\geq$ 100µs.
4.   Turn-on delay is measured with an input voltage rise time of between 100V and 500V per millisecond.
5.   Current limit point is that condition of excess load causing output voltage to drop to 90% of nominal.
6.   Parameter verified as part of another test.
7.   All electrical tests are performed with the remote sense leads connected to the output leads at the load.
8.   Load transient transition time $\geq$ 10µs.
9.   Enable inputs internally pulled high. Nominal open circuit voltage $\approx$ 4.0VDC.
10.   Set output current to 5.5A as test condition for regulation tests.

Block Diagram

Figure I. Single Output
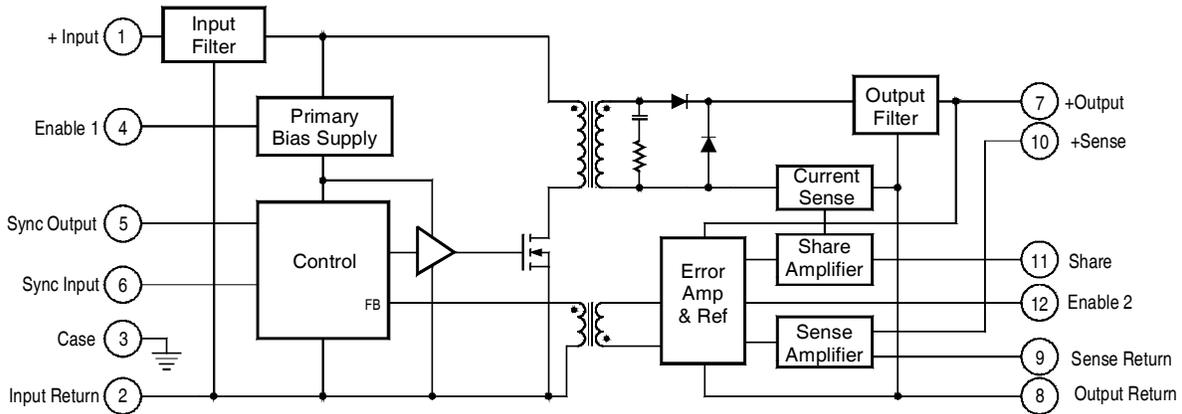
Circuit Operation and Application Information

The AFL series of converters employs a forward switched mode converter topology. (refer to Figure I) Operation of the device is initiated when a DC voltage whose magnitude is within the specified input limits is applied between pins 1 and 2. If pin 4 is enabled (at a logical 1 or open) the primary bias supply will begin generating a regulated housekeeping voltage bringing the circuitry on the primary side of the converter to life. A power MOSFET is used to chop the DC input voltage into a high frequency square wave, applying this chopped voltage to the power transformer at the nominal converter switching frequency. Maintaining a DC voltage within the specified operating range at the input assures continuous generation of the primary bias voltage.

The switched voltage impressed on the secondary output transformer winding is rectified and filtered to generate the converter DC output voltage. An error amplifier on the secondary side compares the output voltage to a precision reference and generates an error signal proportional to the difference. This error signal is magnetically coupled through the feedback transformer into the controller section of the converter varying the pulse width of the square wave signal driving the MOSFET, narrowing the width if the output voltage is too high and widening it if it is too low, thereby regulating the output voltage.

Remote Sensing

Connection of the **+** and **-** sense leads at a remotely located load permits compensation for excessive resistance between the converter output and the load when their physical separation could cause undesirable voltage drop. This connection allows regulation to the placard voltage at the point of application. When the remote sensing feature is not used, the sense leads should be connected to their respective output terminals at the converter. Figure III. llustrates a typical remotely sensed application.

Inhibiting Converter Output (Enable)

As an alternative to application and removal of the DC voltage to the input, the user can control the converter output by providing TTL compatible, positive logic signals to either of two Enable pins (pin 4 or 12). The distinction between these two signal ports is that Enable 1 (pin 4) is referenced to the Input Return (pin 2) while Enable 2 (pin 12) is referenced to the Output Return (pin 8). Thus, the user has access to an inhibit function on either side of the isolation barrier. Each port is internally pulled "high" so that when not used, an open connection on both enable pins permits normal converter operation. When their use is desired, a logical "low" on either port will shut the converter down.

Figure II. Enable Input Equivalent Circuit
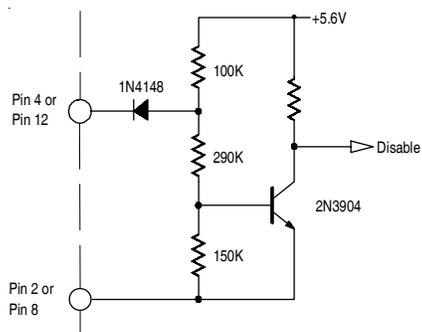
Internally, these ports differ slightly in their function. In use, a low on Enable 1 completely shuts down all circuits in the converter, while a low on Enable 2 shuts down the secondary side while altering the controller duty cycle to near zero. Externally, the use of either port is transparent to the user save for minor differences in standby current. (See specification table).

## Synchronization of Multiple Converters

When operating multiple converters, system requirements often dictate operation of the converters at a common frequency. To accommodate this requirement, the AFL series converters provide both a synchronization input and a synchronization output.

The Sync Input port permits synchronization of an AFL converter to any compatible external frequency source operating between 500KHz and 700KHz. This input signal should be referenced to the input return and have a 10% to 90% duty cycle. Compatibility requires transition times less

than 100ns, maximum low level of +0.8Vand a minimum highvel of +2.0V. The Sync Output of another converter which has been designated as the master oscillator provides a convenient frequency source for this mode of operation. When external synchronization is not required, the sync in pin should be left open (unconnected)thereby permitting the converter to operate at its own internally set frequency.

The Sync Output signal is a continuous pulse train set at 550 ± 50KHz, with a duty cycle of 15 ± 5%. This signal is referenced to the Input Return and has been tailored to be compatible with the AFL Sync Input port. Transition times are less than 100ns and the low level output impedance is less than 50Ω. This signal is active when the DC input voltage is within the specified operating range and the converter is not inhibited. This output has adequate drive reserve to synchronize at least five additional converters. A typical connection is illustrated in Figure III.

Figure III. Preferred Connection for Parallel Operation

(Other Converters)
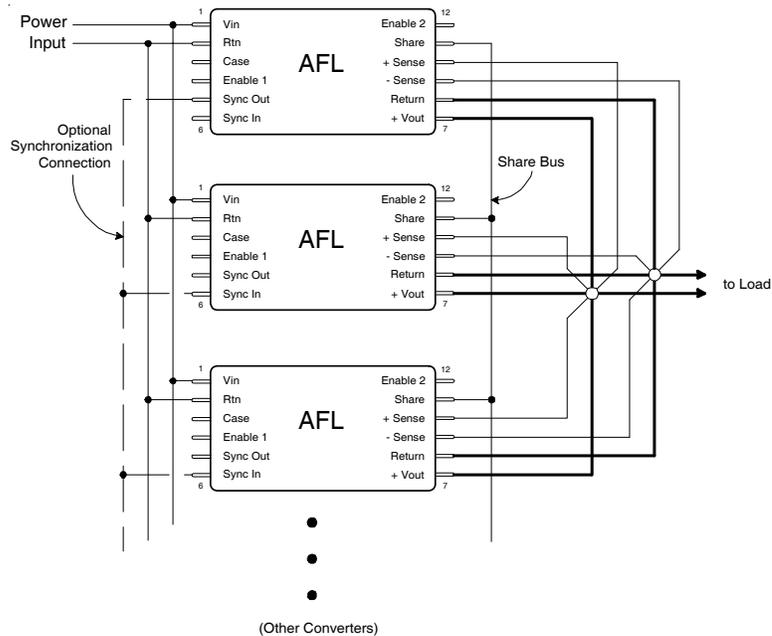
Parallel Operation-Current and Stress Sharing

Figure III. illustrates the preferred connection scheme for operation of a set of AFL converters with outputs operating in parallel. Use of this connection permits equal sharing among the members of a set whose load current exceeds the capacity of an individual AFL. An important feature of

the AFL series operating in the parallel mode is that in addition to sharing the current, the stress induced by temperature will also be shared. Thus if one member of a paralleled set is operating at a higher case temperature, the current it provides to the load will be reduced as compensation for the temperature induced stress on that device.

When operating in the shared mode, it is important that symmetry of connection be maintained as an assurance of optimum load sharing performance. Thus, converter outputs should be connected to the load with equal lengths of wire of the same gauge and should be connected to a common physical point, preferably at the load along with the converter output and return leads. All converters in a paralleled set must have their share pins connected together. This arrangement is diagrammatically illustrated in Figure III showing the Output and Return pins connected at a star point which is located close as possible to the load.

As a consequence of the topology utilized in the current sharing circuit, the share pin may be used for other functions. In applications requiring only a single converter, the voltage appearing on the share pin may be used as a "current monitor". The share pin open circuit voltage is nominally +1.00V at no load and increases linearly with increasing total output current to +2.20V at full load.

Thermal Considerations

Because of the incorporation of many innovative technological concepts, the AFL series of converters is capable of providing very high output power from a package of very small volume. These magnitudes of power density can only be obtained by combining high circuit efficiency with effective methods of heat removal from the die junctions. This requirement has been effectively addressed inside the device; but when operating at maximum loads, a significant amount of heat will be generated and this heat must be conducted away from the case. To maintain the case temperature at or below the specified maximum of 125°C, this heat must be transferred by conduction to an appropriate heat dissipater held in intimate contact with the converter base-plate.

Because the effectiveness of this heat transfer is dependent on the intimacy of the baseplate/heatsink interface, it is strongly recommended that a high thermal conductivity heat transferring medium is inserted between the baseplate and heatsink. The material most frequently utilized at the factory during all testing and burn-in processes is sold under the trade name of Sil-Pad® 400[1] . This particular product is an insulator but electrically conductive versions are also available. Use of these materials assures maximum surface contact with the heat dissipater thereby compensating for any minor surface variations. While other available types of heat conductive materials and thermal compounds provide similar effectiveness, these alternatives are often less convenient and can be somewhat messy to use.

[1]Sil-Pad is a registered Trade Mark of Bergquist, Minneapolis, MN

A conservative aid to estimating the total heat sink surface area ($A_{HEAT\ SINK}$) required to set the maximum case temperature rise (ΔT) above ambient temperature is given by the following expression:

$$A_{\text{HEAT SINK}} \approx \left\{ \frac{\Delta T}{80 P^{0.85}} \right\}^{-1.43} - 3.0$$

where

$\Delta T =$ Case temperature rise above ambient

$P =$ Device dissipation in Watts $= P_{OUT}\left\{ \dfrac{1}{Eff} - 1 \right\}$

As an example, it is desired to maintain the case temperature of an AFL2815S at ≤ +85°C while operating in an open area whose ambient temperature is held at a constant +25°C; then

$$\Delta T = 85 - 25 = 60°C$$

From the Specification Table, the worst case full load efficiency for this device is 83%; therefore the power dissipation at full load is given by

$$P = 120 \bullet \left\{ \frac{1}{.83} - 1 \right\} = 120 \bullet (0.205) = 24.6W$$

and the required heat sink area is

$$A_{\text{HEAT SINK}} = \left\{ \frac{60}{80 \bullet 24.6^{0.85}} \right\}^{-1.43} - 3.0 = 71\ \text{in}^2$$

Thus, a total heat sink surface area (including fins, if any) of 71 in^2 in this example, would limit case rise to 60°C above ambient. A flat aluminum plate, 0.25" thick and of approximate dimension 4" by 9" (36 in^2 per side) would suffice for this application in a still air environment. Note that to meet the criteria in this example, both sides of the plate require unrestricted exposure to the ambient air.

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Input Filter

The AFL28XXS series of converters incorporates a two stage LC input filter whose elements dominate the input load impedance characteristic during the turn-on. The input circuit is as shown in Figure IV.

Figure IV. Input Filter Circuit
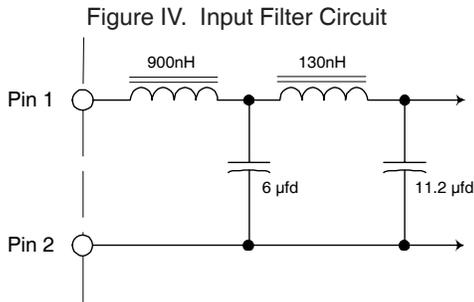
Undervoltage Lockout

A minimum voltage is required at the input of the converter to initiate operation. This voltage is set to 14V ± 0.5V. To preclude the possibility of noise or other variations at the input falsely initiating and halting converter operation, a hysteresis of approximately 1.0V is incorporated in this circuit. Thus if the input voltage droops to 13V ± 0.5V, the converter will shut down and remain inoperative until the input voltage returns to ≈14V.

Output Voltage Adjust

In addition to permitting close voltage regulation of remotely located loads, it is possible to utilize the converter sense pins to incrementally increase the output voltage up to 10% maximum above the nominal output voltage. The adjustments made possible by this method are intended as a means to "trim" the output to a voltage setting for some particular application, but are not intended to create an adjustable output converter. These output voltage setting variations are obtained by connecting an appropriate resistor value between the +sense and -sense pins while connecting the - sense pin to the output return pin as shown in Figure V. below. The range of adjustment and corresponding range of resistance values can be determined by use of the following equation.

$$R_{adj} \ = \ 100 \bullet \left\{ \frac{V_{NOM}}{V_{OUT} - V_{NOM} - .025} \right\}$$

Where, V_{NOM} = device nominal output voltage, and

V_{OUT} = desired output voltage, 110% of V_{NOM} maximum

Finding a resistor value for a particular output voltage, is simply a matter of substituting the desired output voltage and the nominal device voltage into the equation and solving for the corresponding resistor value.

Figure V. Connection for V_{OUT} Adjustment
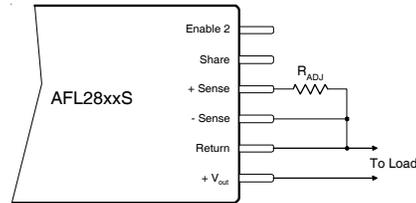
Note: R_{adj} must be set ≥ 500Ω

Attempts to adjust the output voltage to a value greater than 110% of nominal should be avoided because of the potential of exceeding internal component stress ratings and subsequent operation to failure. Under no circumstance should the external setting resistor be made less than 500Ω. By remaining within this specified range of values, completely safe operation fully within normal component derating limits is assured.

Examination of the equation relating output voltage and resistor value reveals a special benefit of the circuit topology utilized for remote sensing of output voltage in the AFL28XXS series of converters. It is apparent that as the resistance increases, the output voltage approaches the nominal set value of the device. In fact the calculated limiting value of output voltage as the adjusting resistor becomes very large is ≈ 25mV above nominal device voltage.

The consequence is that if the +sense connection is unintentionally broken, an AFL28XXS has a fail-safe output voltage of Vout + 25mV, where the 25mV is independent of the nominal output voltage. It can be further demonstrated that in the event of both the + and - sense connections being broken, the output will be limited to Vout + 440mV. This 440mV is also essentially constant independent of the nominal output voltage.

General Application Information

The AFL28XXS series of converters is capable of providing large transient currents to user loads on demand. Because the nominal input voltage range in this series is relatively low, the resulting input current demands will be correspondingly large. It is important therefore, that the line impedance be kept very low to prevent steady state and transient input currents from degrading the supply voltage between the voltage source and the converter input. In applications requiring high static currents and large transients, it is recommended that the input leads be made of adequate size to minimize resistive losses, and that a good quality capacitor of approximately 100µfd be connected directly across the input terminals to assure an adequately low impedance at the input terminals. Table I relates nominal resistance values and selected wire sizes.

Table 1. Nominal Resistance of Cu Wire

Wire Size, AWG	Resistance per ft
24 Ga	25.7 mΩ
22 Ga	16.2 mΩ
20 Ga	10.1 mΩ
18 Ga	6.4 mΩ
16 Ga	4.0 mΩ
14 Ga	2.5 mΩ
12 Ga	1.6 mΩ

As an example of the effects of parasitic resistance, consider an AFL2815S operating at full power of 120W. From the specification sheet, this device has a minimum efficiency of 83% which represents an input power of more than 145W. If we consider the case where line voltage is at its' minimum of 16V, the steady state input current necessary for this example will be slightly greater than 9 amperes. If this device were connected to a voltage source with 10 feet of 20 gauge wire, the round trip (input and return) would result in 0.2Ω of resistance and 1.8V of drop from the source to the converter. To assure 16V at the input, a source closer to 18V would be required. In applications using the paralleling option, this drop will be multiplied by the number of paralleled devices. By choosing 14 or 16 gauge wire in this example, the parasitic resistance and resulting voltage drop will be reduced to 25% or 31% of that with 20 gauge wire.

Another potential problem resulting from parasitically induced voltage drop on the input lines is with regard to the operation of the enable 1 port. The minimum and maximum operating levels required to operate this port are specified with respect to the input common return line at the converter. If a logic signal is generated with respect to a 'common' that is distant from the converter, the effects of the voltage drop over the return line must be considered when establishing the worst case TTL switching levels. These drops will effectively impart a shift to the logic levels. In Figure VI, it can be seen that referred to system ground, the voltage on the input return pin is given by

$$e_{Rtn} = I_{Rtn} \cdot R_P$$

Therefore, the logic signal level generated in the system must be capable of a TTL logic high plus sufficient additional amplitude to overcome e_{Rtn}. When the converter is inhibited, I_{Rtn} diminishes to near zero and e_{Rtn} will then be at system ground.

Incorporation of a 100μF capacitor at the input terminals is recommended as compensation for the dynamic effects of the parasitic resistance of the input cable reacting with the complex impedance of the converter input, and to provide an energy reservoir for transient input current requirements.

Figure VI. Problems of Parasitic Resistance in input Leads
(See text)

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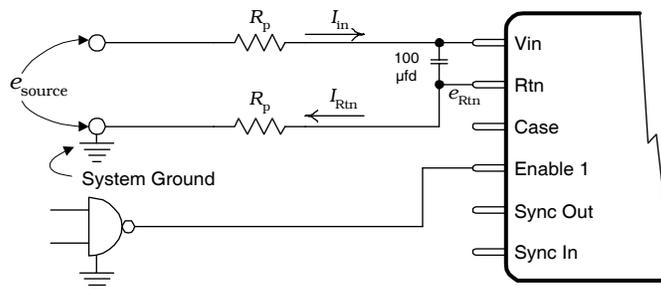
Mechanical Outlines

Case V

Case X
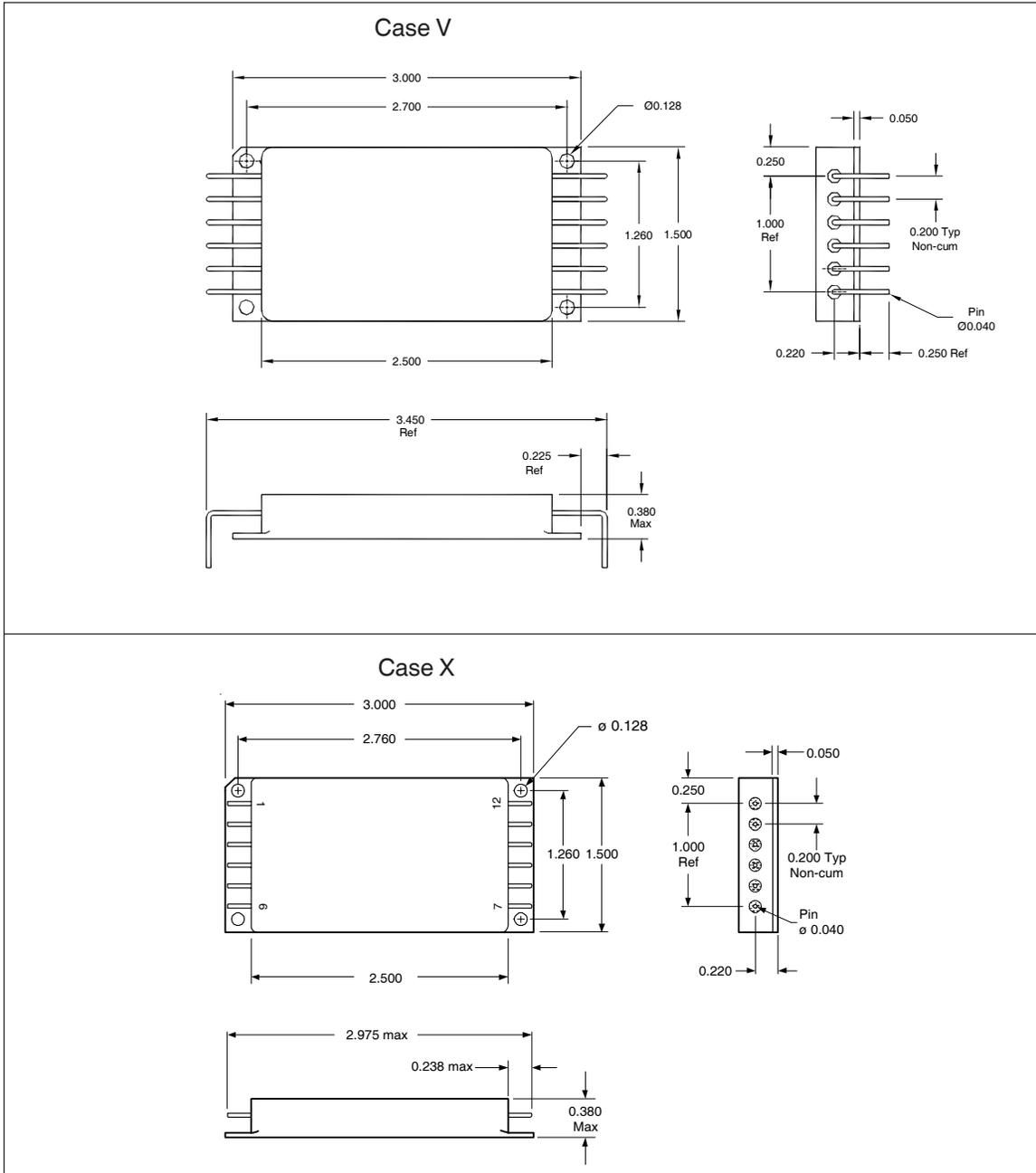
Tolerances, unless otherwise specified: .XX = ±0.010

.XXX = ±0.005

BERYLLIA WARNING: These converters are hermetically sealed; however they contain BeO substrates and should not be ground or subjected to any other operations including exposure to acids, which may produce Beryllium dust or fumes containing Beryllium

Device Screening

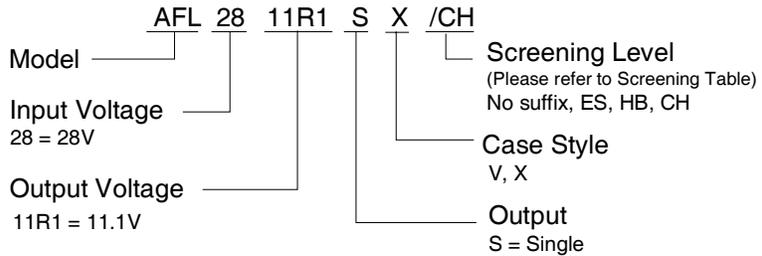| Requirement	MIL-STD-883 Method	No Suffix	ES ②	HB	CH
Temperature Range	—	-20°C to +85°C	-55°C to +125°C ③	-55°C to +125°C	-55°C to +125°C
Element Evaluation	MIL-PRF-38534	N/A	N/A	N/A	Class H
Non-Destructive Bond Pull	2023	N/A	N/A	N/A	N/A
Internal Visual	2017	①	Yes	Yes	Yes
Temperature Cycle	1010	N/A	Cond B	Cond C	Cond C
Constant Acceleration	2001, Y1 Axis	N/A	500 Gs	3000 Gs	3000 Gs
PIND	2020	N/A	N/A	N/A	N/A
Burn-In	1015	N/A	48 hrs @ hi temp	160 hrs @ 125°C	160 hrs @ 125°C
Final Electrical (Group A)	MIL-PRF-38534 & Specification	25°C	25°C ②	-55°C, +25°C, +125°C	-55°C, +25°C, +125°C
PDA	MIL-PRF-38534	N/A	N/A	N/A	10%
Seal, Fine and Gross	1014	Cond A	Cond A, C	Cond A, C	Cond A, C
Radiographic	2012	N/A	N/A	N/A	N/A
External Visual	2009	①	Yes	Yes	Yes

Notes:
① Best commercial practice
② Sample tests at low and high temperatures
③ -55°C to +105°C for AHE, ATO, ATW

Pin Designation

Pin #	Designation
1	+ Input
2	Input Return
3	Case Ground
4	Enable 1
5	Sync Output
6	Sync Input
7	+ Output
8	Output Return
9	Sense Return
10	+ Sense
11	Share
12	Enable 2

Part Numbering

AFL 28 11R1 S X /CH

Model

Input Voltage
28 = 28V

Output Voltage
11R1 = 11.1V

Output
S = Single

Case Style
V, X

Screening Level
(Please refer to Screening Table)
No suffix, ES, HB, CH

Part Definition

IR P/N 10209EM = AFL2811R1SX/ES
IR P/N 10209FM = AFL2811R1SV/HB

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