



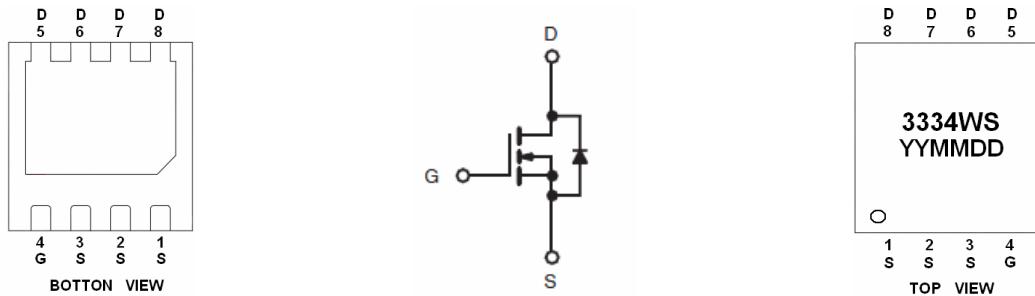
**Alfa-MOS
Technology**

**AFN3334WS
40V N-Channel
Enhancement Mode MOSFET**

General Description

AFN3334WS, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge. These devices are particularly suited for low voltage power management, such as smart phone and notebook computer and other battery powered circuits, and low in-line power loss are needed in commercial industrial surface mount applications.

Pin Description (DFN3X3-8L)



Application

- DC-DC Converter
- POL

Pin Define

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

Ordering Information

Part Ordering No.	Part Marking	Package	Unit	Quantity
AFN3334WSFN338RG	3334WS	DFN3X3-8L	Tape & Reel	5000 EA

※ YY year code

※ MM month code

※ DD date code

※ AFN3334WSFN338RG : 13" Tape & Reel ; Pb- Free ; Halogen -Free



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V_{DSS}	40	V
Gate –Source Voltage	V_{GSS}	± 20	V
Continuous Drain Current($T_J=150^\circ\text{C}$)	I_D	17	A
		14	
Pulsed Drain Current	I_{DM}	55	A
Continuous Source Current(Diode Conduction)	I_S	30	A
Power Dissipation	P_D	36	W
		18	
Operating Junction Temperature	T_J	150	$^\circ\text{C}$
Storage Temperature Range	T_{STG}	-55/150	$^\circ\text{C}$
Thermal Resistance-Junction to Ambient	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$

Electrical Characteristics

($T_A=25^\circ\text{C}$ Unless otherwise noted)

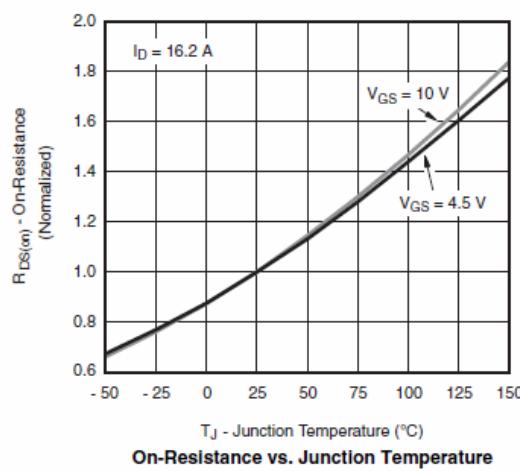
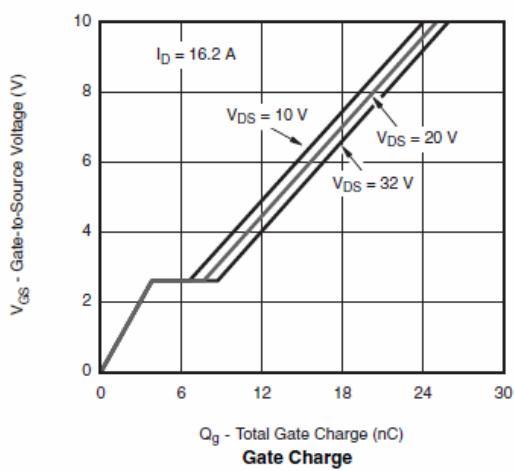
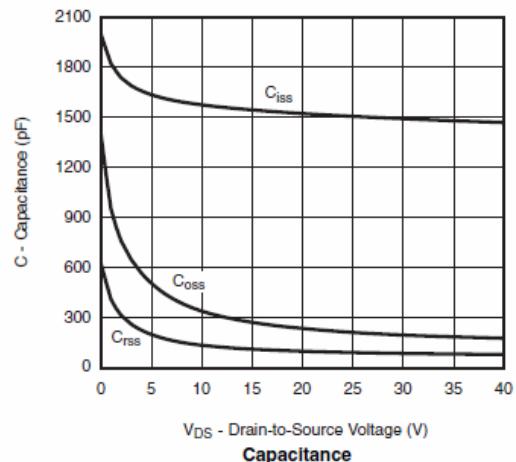
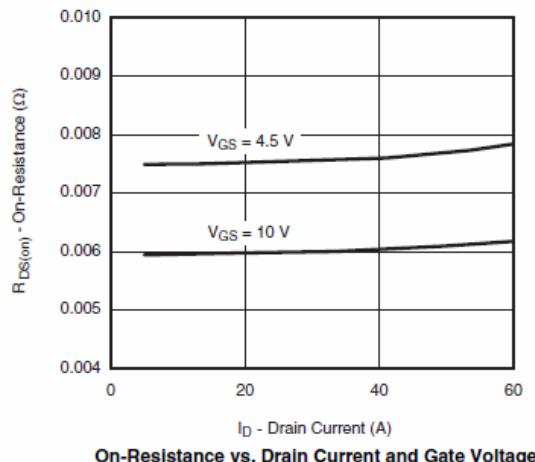
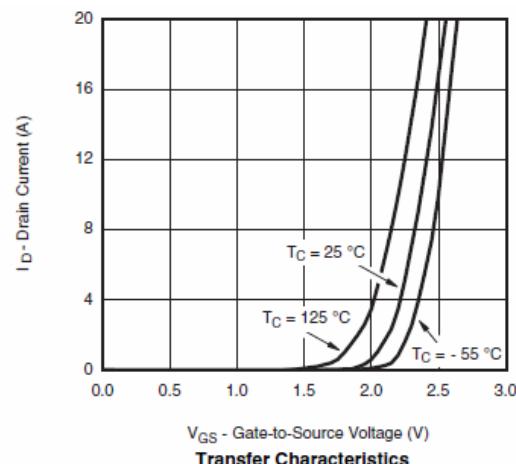
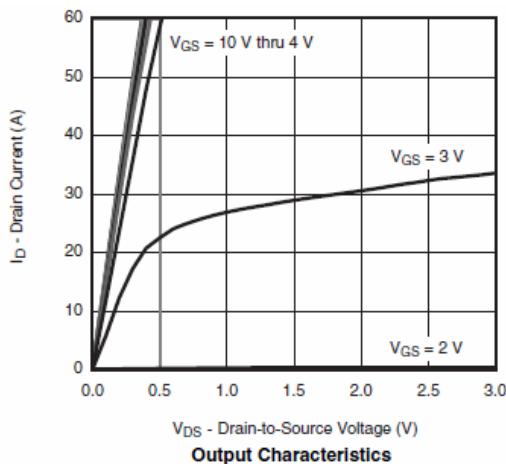
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	40			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0		2.5	
Gate Leakage Current	I_{GSS}	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=32\text{V}, V_{GS}=0\text{V}$			1	
		$V_{DS}=32\text{V}, V_{GS}=0\text{V}$ $T_J=85^\circ\text{C}$			10	uA
On-State Drain Current	$I_{D(\text{on})}$	$V_{DS}\geq 5\text{V}, V_{GS}=10\text{V}$	50			A
Drain-Source On-Resistance	$R_{DS(\text{on})}$	$V_{GS}=10\text{V}, I_D=20\text{A}$		5.2	6.4	$\text{m}\Omega$
		$V_{GS}=4.5\text{V}, I_D=15\text{A}$		6.5	7.8	
Forward Transconductance	g_{FS}	$V_{DS}=15\text{V}, I_D=16\text{ A}$		60		S
Diode Forward Voltage	V_{SD}	$I_S=10\text{A}, V_{GS}=0\text{V}$		0.8	1.3	V
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=20\text{V}, V_{GS}=4.5\text{V}$ $I_D\equiv 16\text{A}$		12	20	nC
Gate-Source Charge	Q_{gs}			4		
Gate-Drain Charge	Q_{gd}			4		
Input Capacitance	C_{iss}	$V_{DS}=20\text{V}, V_{GS}=0\text{V}$ $f=1\text{MHz}$		1540		pF
Output Capacitance	C_{oss}			240		
Reverse Transfer Capacitance	C_{rss}			100		
Turn-On Time	$t_{d(on)}$	$V_{DD}=20\text{V}, R_L=2.0\Omega$ $I_D\equiv 10\text{A}, V_{GEN}=10\text{V}$ $R_G=1.0\Omega$		10	20	ns
	t_r			10	20	
Turn-Off Time	$t_{d(off)}$			25	45	
	t_f			8	20	



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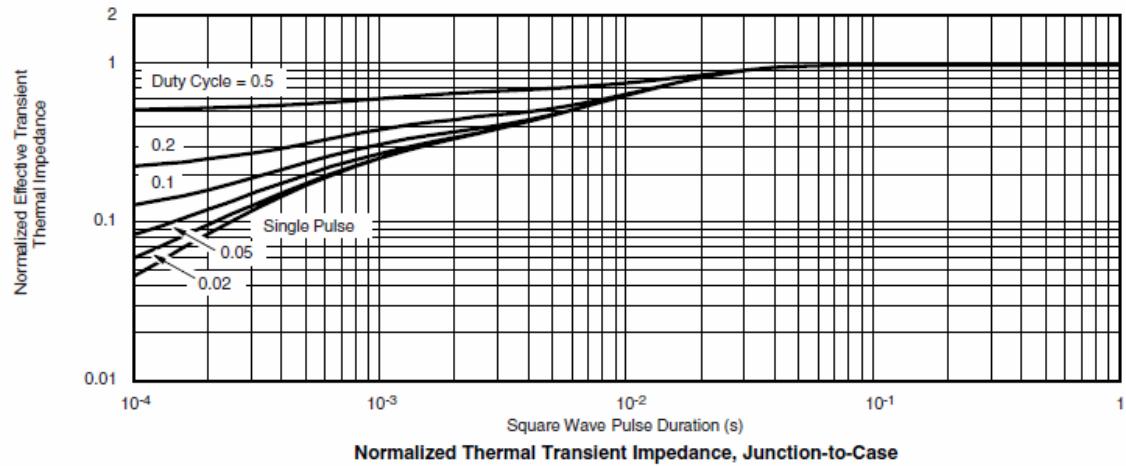
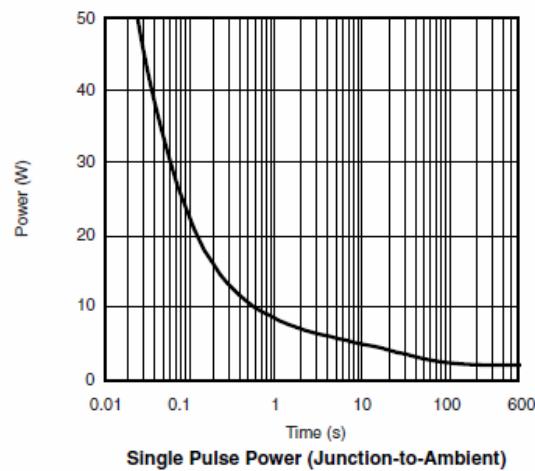
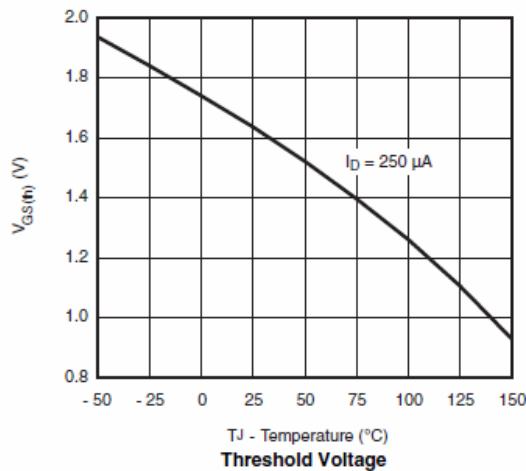
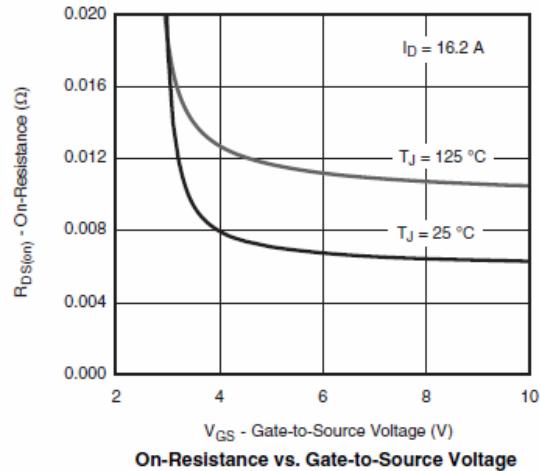
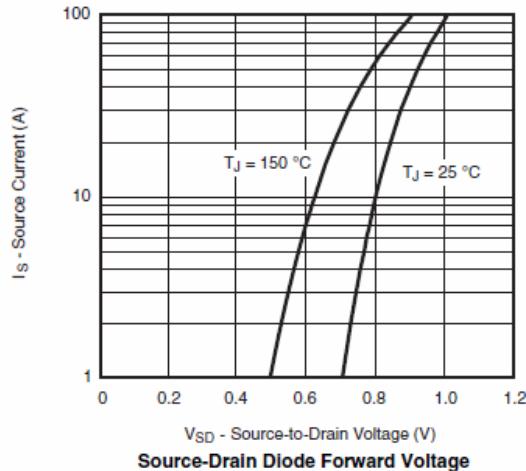




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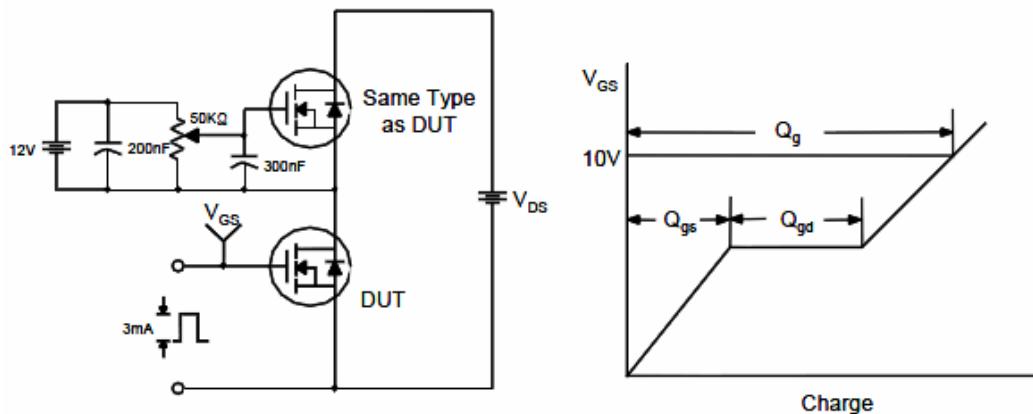


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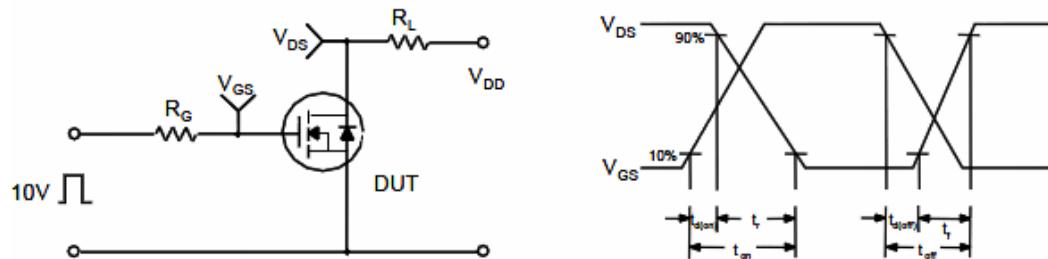
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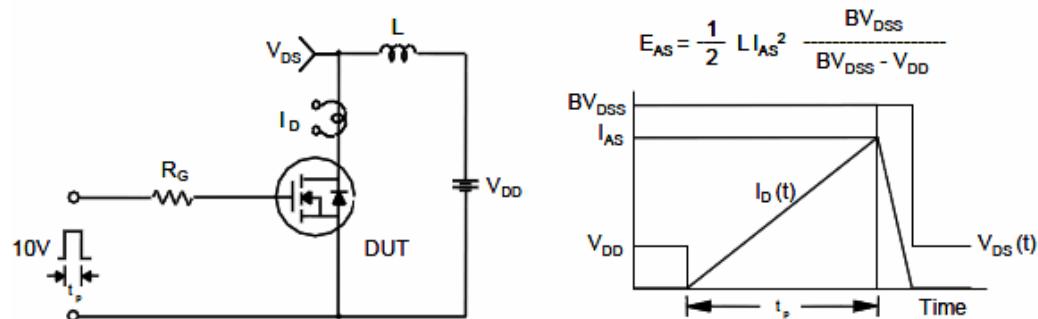
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

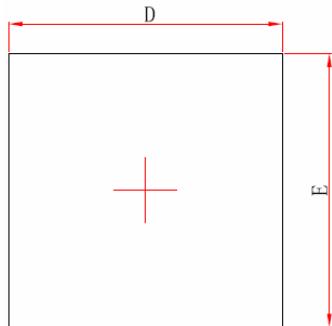


Unclamped Inductive Switching Test Circuit & Waveforms

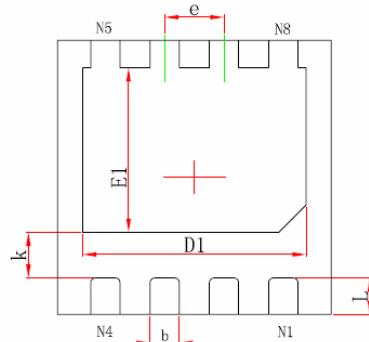




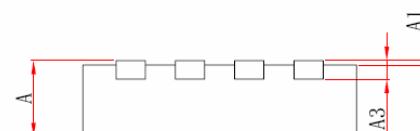
Package Information (DFN3X3-8L)



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.800	0.900	0.031	0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	2.924	3.076	0.115	0.121
E	2.924	3.076	0.115	0.121
D1	2.350	2.550	0.093	0.100
E1	1.700	1.900	0.067	0.075
k	0.450	0.550	0.018	0.022
b	0.270	0.370	0.011	0.015
e	0.650TYP.		0.026TYP.	
L	0.324	0.476	0.013	0.019

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